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G4A AEF

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GB 2231984 A

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(54) Abstract Title
Memory having a redundancy scheme

(57) A semiconductor memory device is provided with a plurality of global blocks (500), each of which includes a plurality of unit matrixes having a normal block (507) and a redundancy block (506), a normal division word line driver (504), a redundancy division word line driver (505), a main decoder (502) and an auxiliary decoder (503). In the main decoder (502), an output signal is selectively activated according to a row address signal regardless of using a redundancy cell. Also, in the auxiliary decoder (503), when a corresponding global block (500) is selected according to the row address signal for selecting a global block in a normal operation mode, or a redundancy scheme of the corresponding block is used in the redundancy operation mode, an output signal is selectively activated according to the row address signal.

FIG. 5

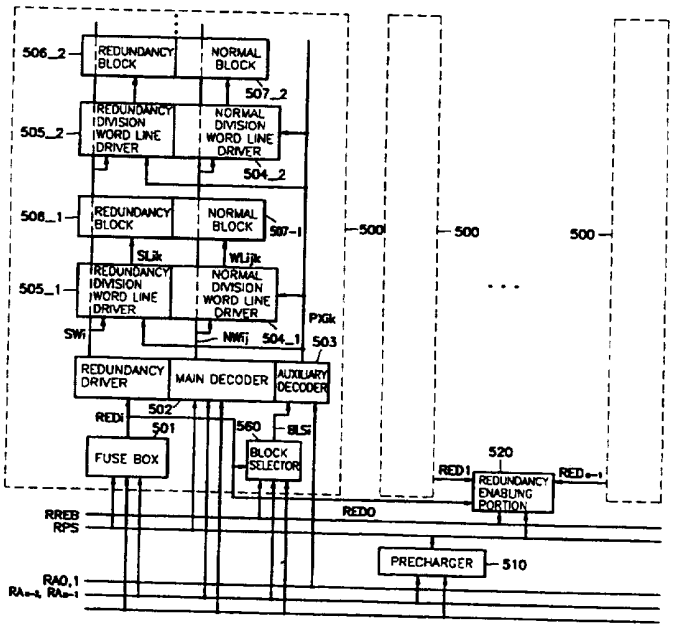

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FIG. 1 (PRIOR ART)

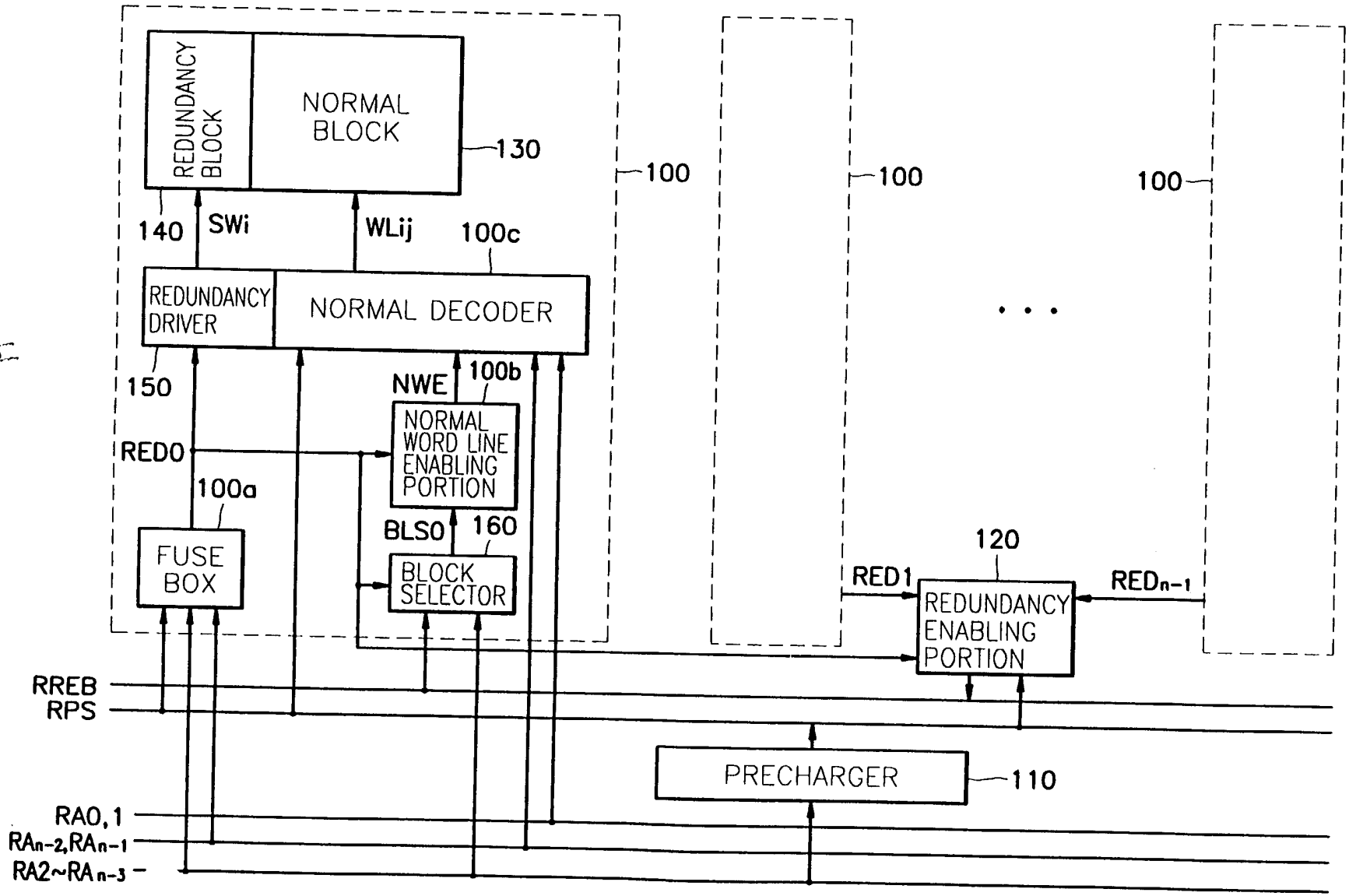


FIG. 2 (PRIOR ART)

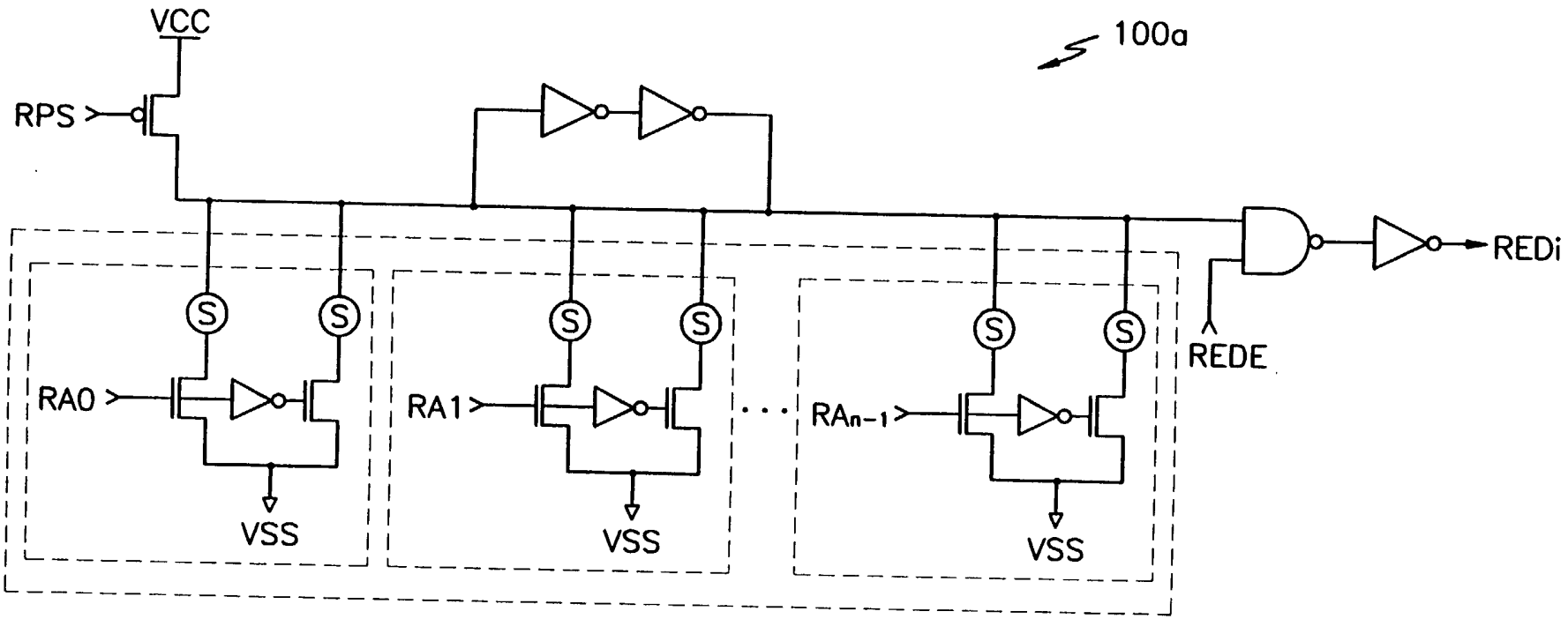


FIG. 3 (PRIOR ART)

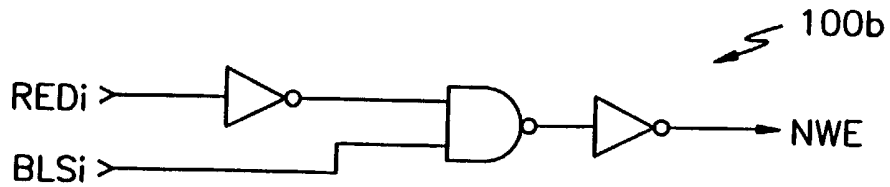


FIG. 4 (PRIOR ART)

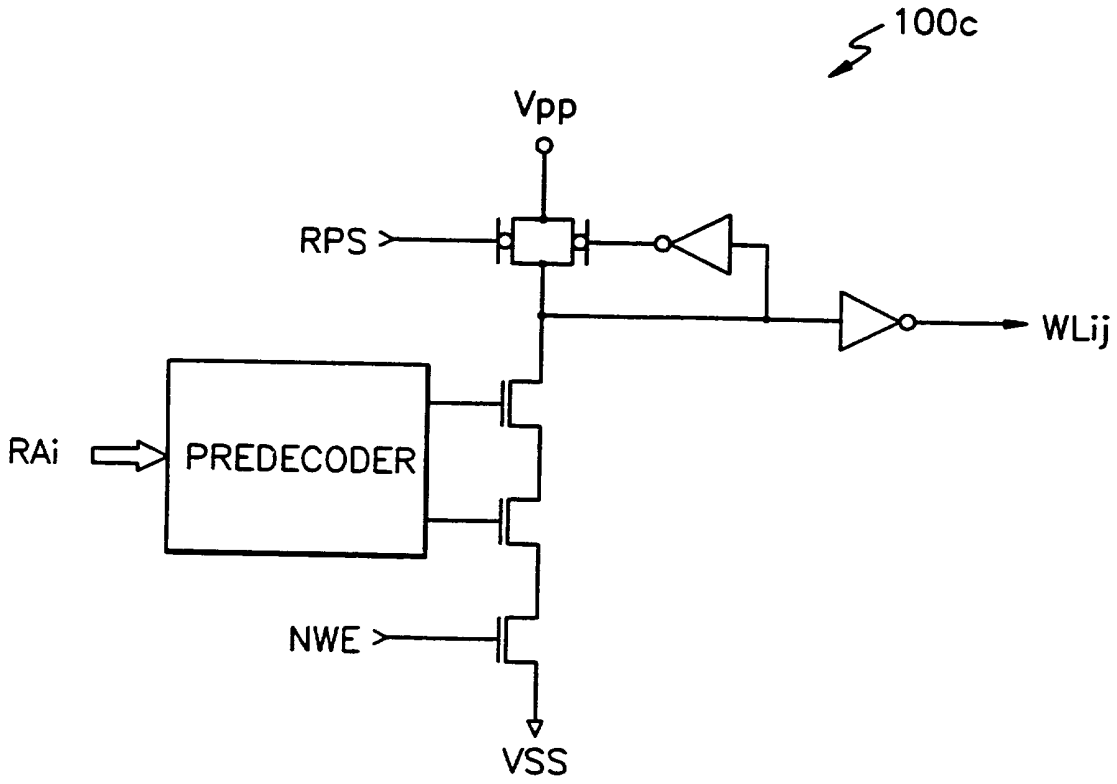


FIG. 5

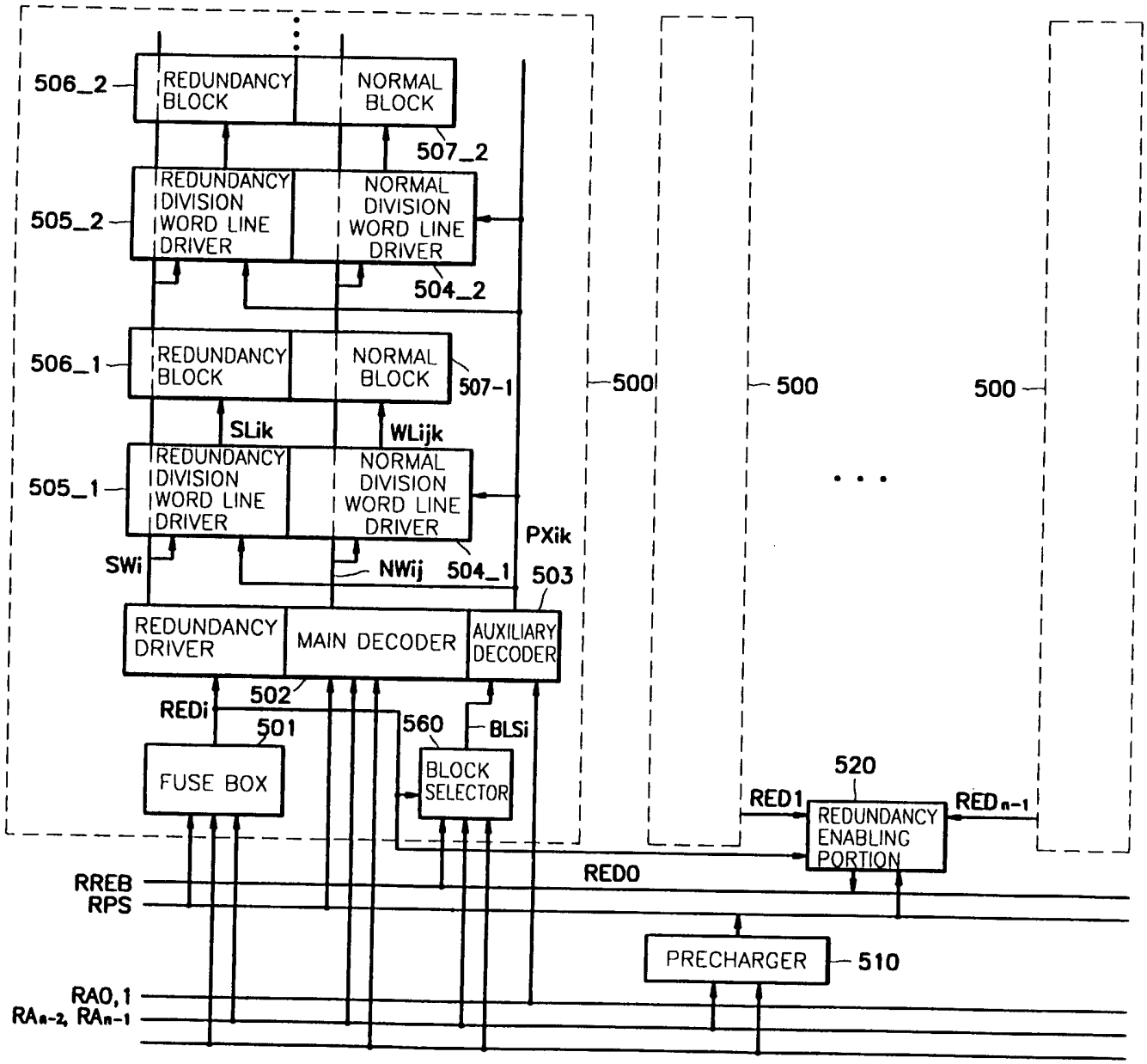

506_2
REDUNDANCY BLOCK
NORMAL BLOCK
507_2
505_2
REDUNDANCY DIVISION WORD LINE DRIVER
NORMAL DIVISION WORD LINE DRIVER
504_2
506_1
REDUNDANCY BLOCK
NORMAL BLOCK
507-1
500
500
500
SLik
WLijk
505_1
REDUNDANCY DIVISION WORD LINE DRIVER
NORMAL DIVISION WORD LINE DRIVER
PXik
SWi
NWij
504_1
503
REDUNDANCY DRIVER
MAIN DECODER
AUXILIARY DECODER
502
REDi
501
560
BLSi
FUSE BOX
BLOCK SELECTOR
520
RED1
REDn-1
REDUNDANCY ENABLING PORTION
RRED
RPS
RED0
PRECHARGER
510
RA0,1
RAn-2, RAn-1
RA2~RAn-3

FIG. 6

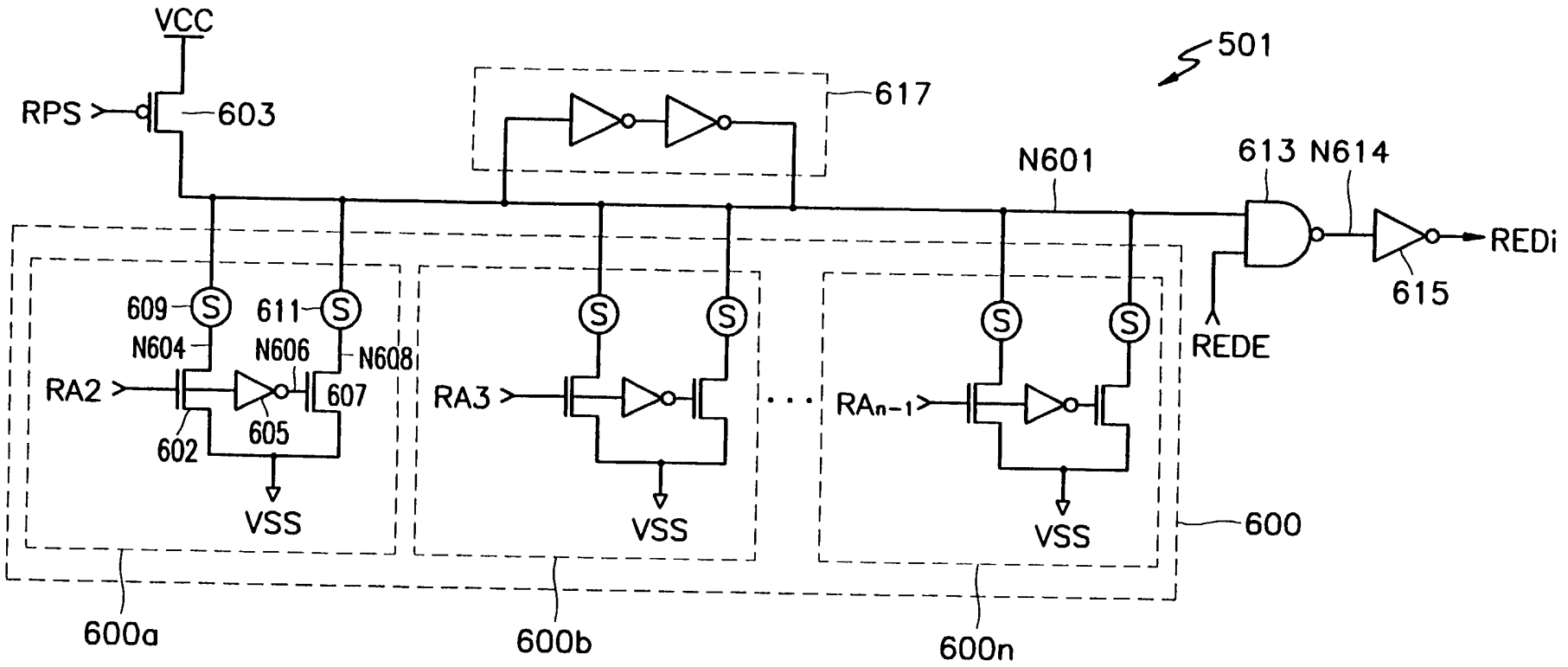

VCC
RPS
603
617
501
N601
613
N614
REDi
615
609
611
N604
N606
N608
RA2
607
605
602
VSS
RA3
RAn-1
REDE
600
600a
600b
600n

FIG. 7

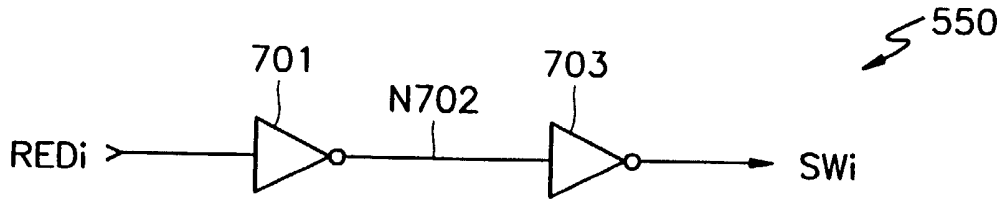

550
701
703
N702
REDi
SWi

FIG. 8

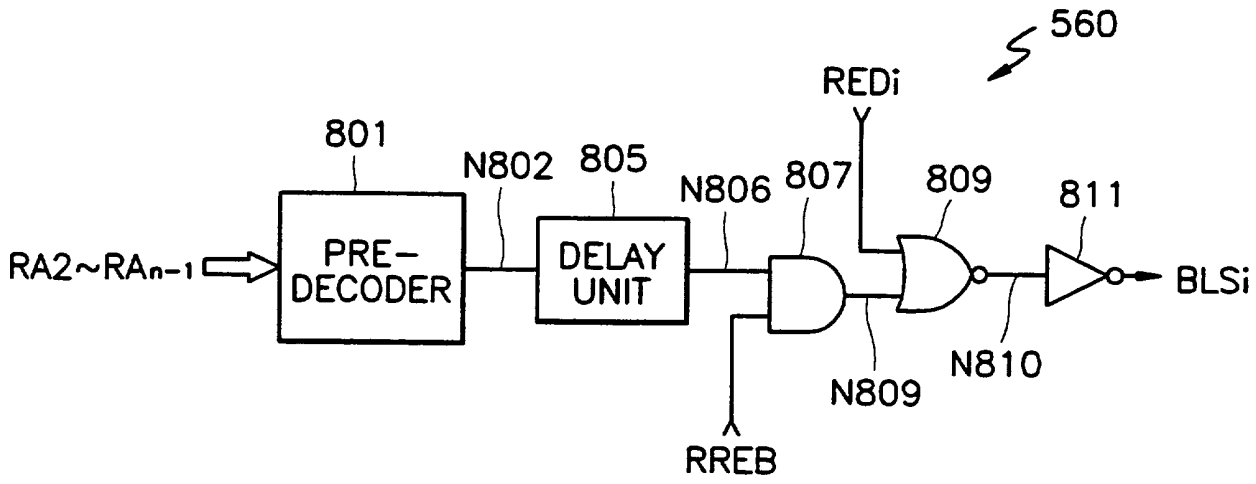

560
REDi
801
N802
805
N806
807
809
811
RA2~RAn-1
PRE-DECODER
DELAY UNIT
BLSi
N809
N810
RREB

FIG. 9

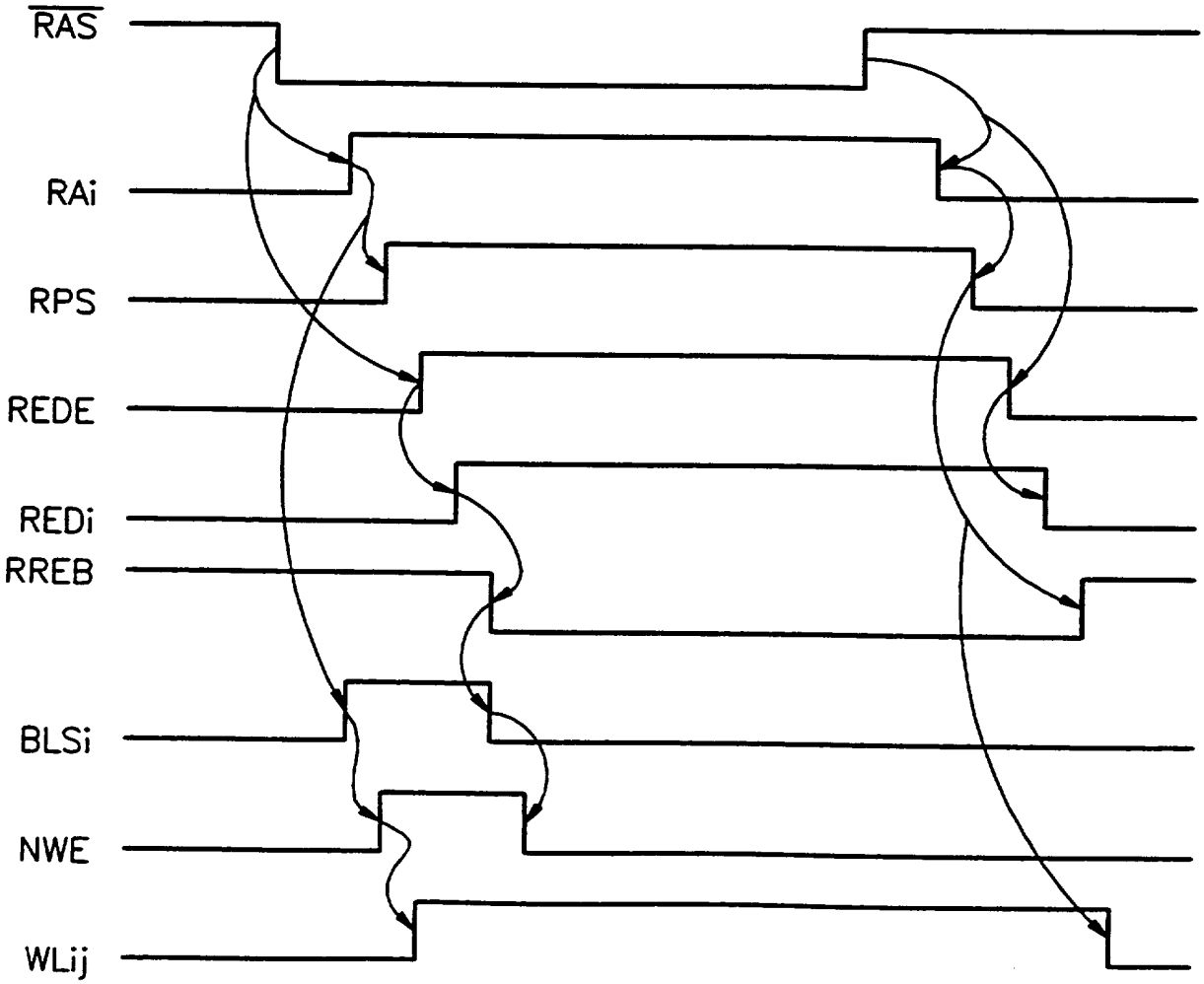

RAS
RAi
RPS
REDE
REDi
RREB
BLSi
NWE
WLij

FIG. 10

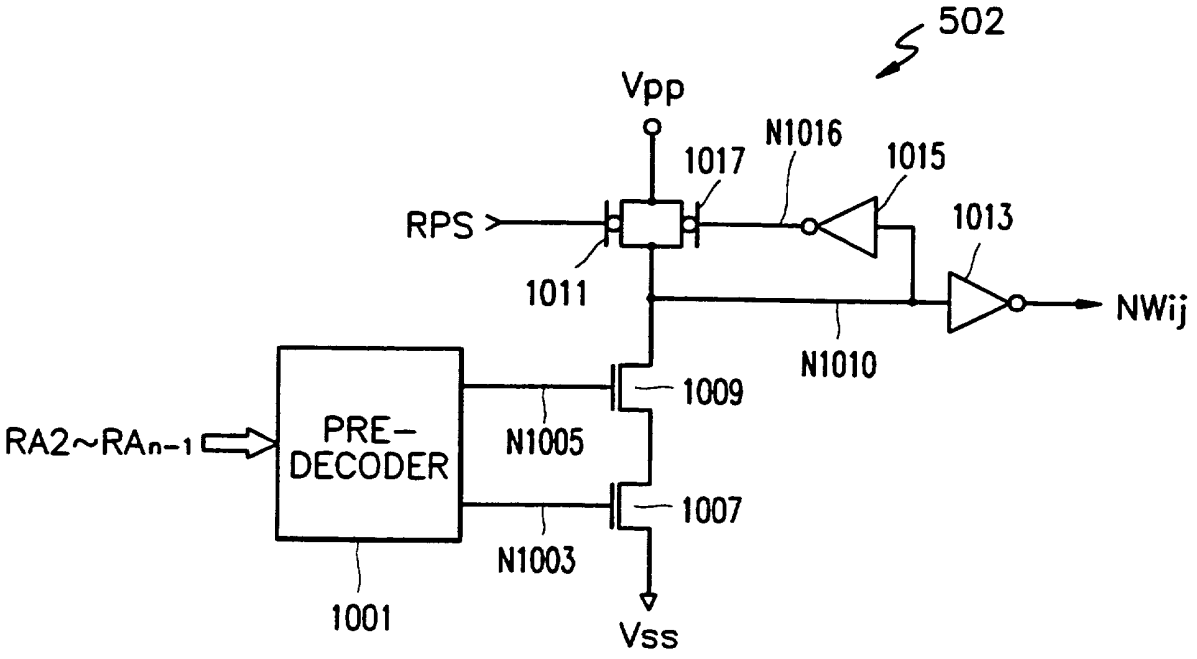

502
Vpp
N1016
1017
1015
RPS
1013
1011
NWij
N1010
1009
RA2~RAn-1
PRE-
DECODER
N1005
1007
N1003
1001
Vss

FIG. 11

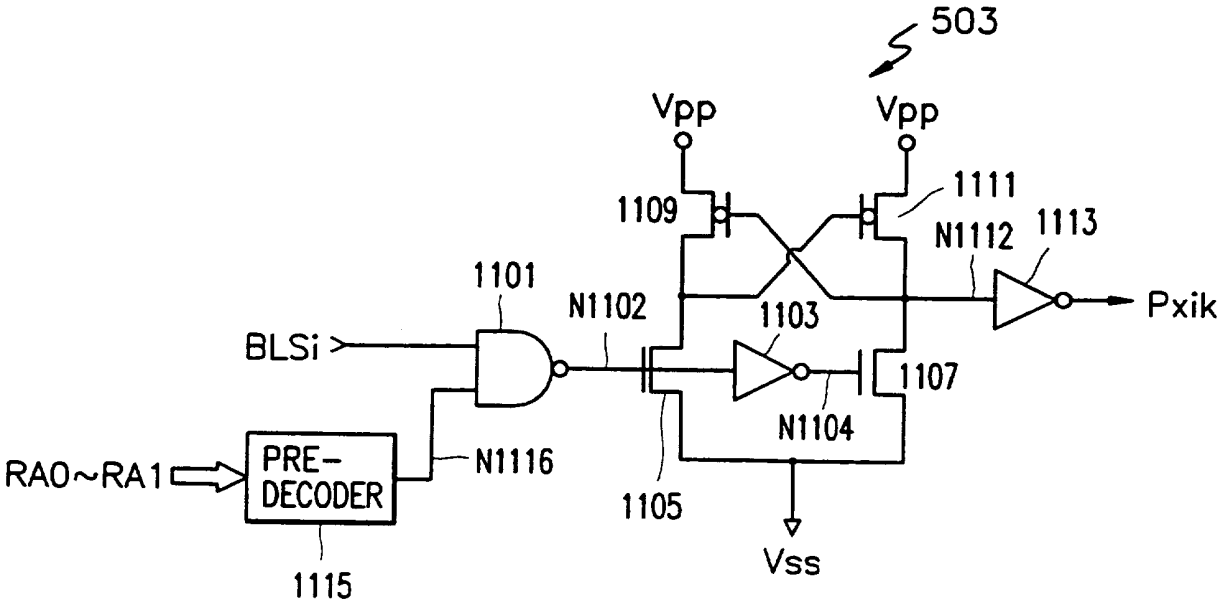

503
Vpp
Vpp
1111
1109
N1112
1113
1101
N1102
1103
Pxik
BLSi
1107
N1104
RA0~RA1
PRE-
DECODER
N1116
1105
Vss
1115

FIG. 12

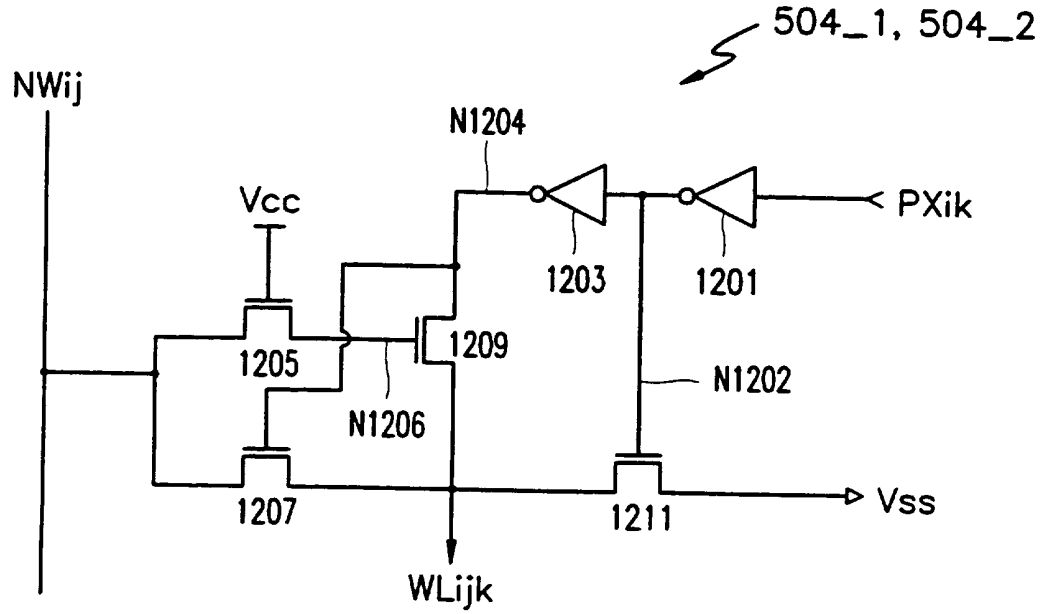

504_1, 504_2
NWij
N1204
Vcc
PXik
1203
1201
1205
1209
N1202
N1206
1207
1211
Vss
WLijk

FIG. 13

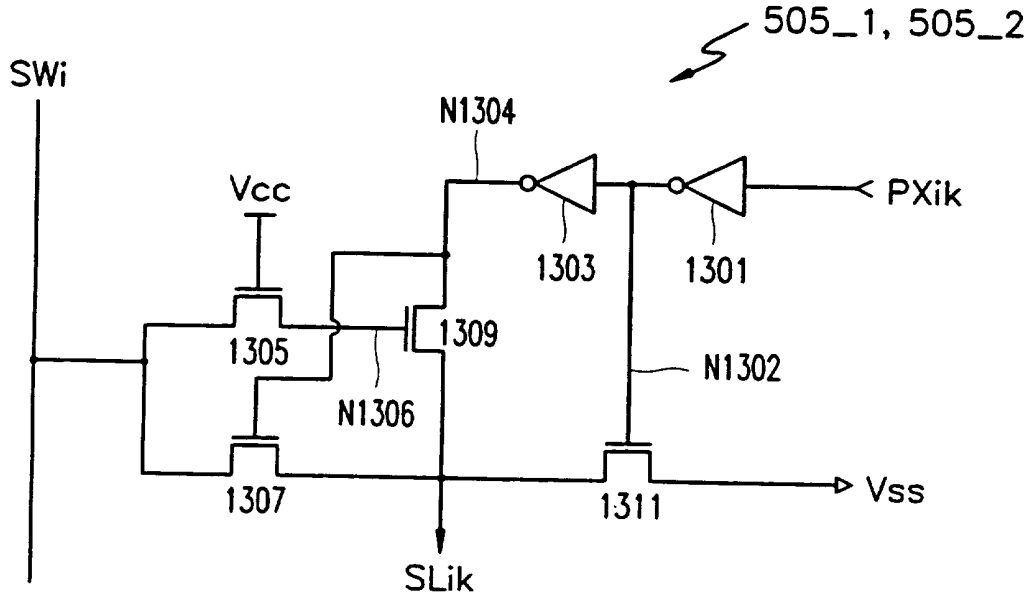

505_1, 505_2
SWi
N1304
Vcc
PXik
1303
1301
1305
1309
N1302
N1306
1307
1311
Vss
SLik

FIG. 14

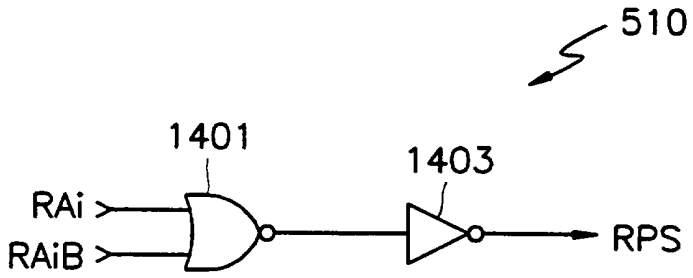
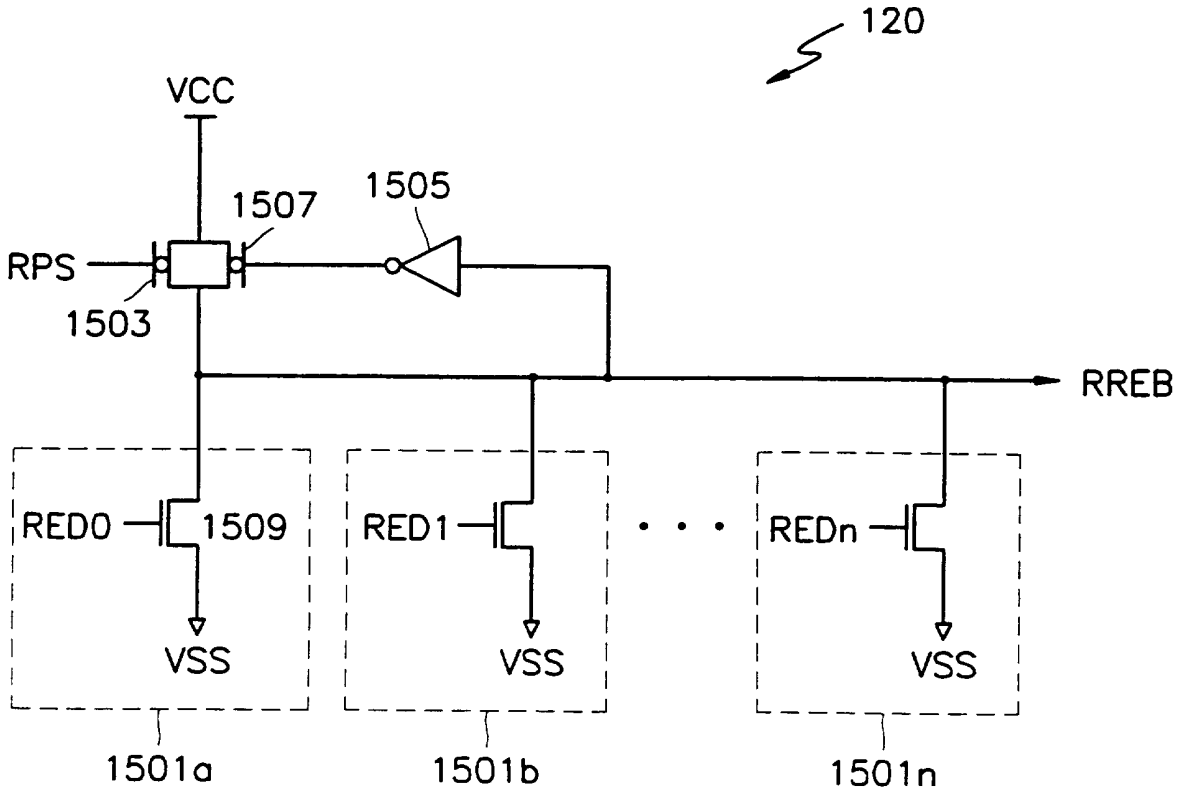

510
1401
1403
RAi
RAiB
RPS

FIG. 15


120
VCC
1507
1505
RPS
1503
RREB
RED0
1509
RED1
REDn
VSS
VSS
VSS
1501a
1501b
1501n

A SEMICONDUCTOR MEMORY DEVICE HAVING AN IMPROVED ROW REDUNDANCY SCHEME AND A METHOD FOR CURING A DEFECTIVE CELL

The present invention relates to a semiconductor memory device, and more particularly, to a semiconductor memory device having a row redundancy scheme and a method for curing a defective cell.

In a general semiconductor memory device with many memory cells, when a defective memory cell is generated, the memory device cannot be used. Also, as semiconductor memory device technology improves, a greater number of cells are being arranged on a signal chip and large integrated circuits are being fabricated. Accordingly, the chance of a defective memory cell in a chip is high, and curing of a defective cell in a highly integrated memory is very important for giving a higher yield of the chip.

To solve the above problems, in a conventional semiconductor memory device, a chip includes redundancy memory cells as well as basic memory cells. Redundancy memory cells are used to replace the defective normal memory cells. A circuit called a fuse box is used to make this replacement. For greater redundancy, the number of redundancy memory cells and fuse boxes are increased, or several memory cell blocks share a predetermined number of redundancy memory cells and fuse boxes.

FIG. 1 is a block diagram of a memory device having a

conventional row redundancy scheme. Here, several memory cell blocks share redundancy cells and fuse boxes. Referring to FIG. 1, the conventional memory device has a row redundancy scheme which includes a precharger 110, a plurality of global memory cell array blocks 100 and a redundancy enabling portion 120.

In the precharger 110, when a "low" or "high" signal is input into a predetermined row address, a low precharge signal RPS is activated.

The redundancy enable portion 120 is precharged by the RPS, and responds to a redundancy signal REDi (I= 0, 1, ..., n), which is an output signal of respective global memory cell array blocks 100. Accordingly, when a row redundancy scheme of a global memory cell array block is selected and operated, a row redundancy enable signal RREB becomes activated.

The global memory cell array block 100 is comprised of a normal block 130, a redundancy block 140, a fuse box 100a, a redundancy driver 150, a block selector 160, a normal word line enabling portion 100b and a normal decoder 100c. The normal block 130 includes many memory cells arranged in rows and column. The redundancy block 140 also includes many memory cells arranged in rows and column, and is selected and operated if a cell in the normal block 130 is defective.

FIG. 2 shows the fuse box 100a in greater detail. The fuse box 100a responds to the RPS signal to be precharged and generates the redundancy signals REDi (I=0,

1, ..., n) responding to all row address signals of RAi (I=0, 1, ... , n-1). When the address of a memory cell which normally operates in the normal block is selected, a logic state of the redundancy signal REDi (I=0, 1, ..., n) goes to "LOW". However, when the address of a defective cell of the normal block is selected, a fuse of a corresponding address shorts. Accordingly, in the second case, a logic state of the redundancy signal REDi (1=0, 1, ..., n-1) is kept "HIGH" and the redundancy scheme is used.

The normal word line enabling portion 100b is shown in FIG. 3. Here, the normal operation mode, the redundancy signal REDi is "LOW" and a block select signal BLSi of the selected global memory cell array block is "HIGH". Accordingly, a normal word line enable signal NWE output from the normal wordline enable portion 100b goes to "HIGH", to enable the normal word line.

The normal decoder 100c is shown in FIG. 4. During an initial operation, as shown in FIG. 4, the normal decoder 100c is precharged by the RPS. Also, when the NWE is "HIGH", the normal decoder responds to the row address signal RAi (I=0, 1, ..., n-1), to enable a word line WLij of a corresponding memory cell of the normal block 130.

However, the block selector 160 for generating the block select signal BLSi includes a delay unit. The delay unit prevents operation of the normal decoder in a redundancy operation mode, which would cause malfunction.

Accordingly, in the conventional memory device having

a row redundancy scheme, the NWE operates the normal decoder, through a delay path of REDi-RREB-BLSi-NWE, and further a delay unit is included in the block selector. As a result, the enabling of a word line is delayed even in a normal path. Also, since a defective cell is always replaced with a redundancy cell from the same global block, the efficiency is low.

According to a first aspect of the present invention, there is provided a semiconductor memory device having a plurality of global blocks, each of which comprises:

a semiconductor memory device having a plurality of global blocks, each global block comprising:

a plurality of unit matrixes including a normal block having an array by normal cells and a redundancy block having an array of redundancy cells;

a normal division word line driver for driving a word line of the normal cells;

a redundancy division word line driver for driving a word line of the redundancy cells;

a main decoder having an output signal supplied to the normal division word line driver; and

an auxiliary decoder having an output signal supplied to the normal division word line driver and the redundancy division word line driver,

wherein the main decoder includes an output signal selectively activated by a row address signal regardless of use of the redundancy cell, and the auxiliary decoder includes an output signal selectively activated by a row

address signal in the case that a corresponding global block is selected by a row address signal for selecting a global block in a normal operation mode or a redundancy scheme of a corresponding block in a redundancy operation mode is used.

According to a second aspect of the present invention, there is provided a method for curing a defective cell of a semiconductor memory device having a plurality of global blocks each comprising of two or more unit matrixes including a normal block and a redundancy block, a main decoder, and a fuse box, comprising the steps of selectively activating an output signal of the main decoder according to a row address signal regardless of using a redundancy cell of the redundancy block, and using the fuse box of other block to which the defective cell during curing is not included.

An example of the present invention will now be described in detail with reference to the accompanying drawings in which:

FIG. 1 is a block diagram of a memory device having a conventional row redundancy scheme;

FIG. 2 is a circuit diagram showing a fuse box of the memory device shown in FIG. 1;

FIG. 3 is a circuit diagram showing a normal word line enabling portion of the memory device shown in FIG. 1;

FIG. 4 is a diagram showing a normal decoder of the memory device shown in FIG. 1;

FIG. 5 is a block diagram showing an embodiment of a

memory device having a row redundancy scheme according to the present invention;

FIG. 6 is a circuit diagram showing a fuse box of the memory device shown in FIG. 5;

FIG. 7 is a circuit diagram showing a redundancy driver of the memory device shown in FIG. 5;

FIG. 8 is a diagram showing a block selector of the memory device shown in FIG. 5;

FIG. 9 is a timing diagram of signals of the block selector of FIG. 8 with no delay units;

FIG. 10 is a diagram showing a main decoder of the memory device shown in FIG. 5;

FIG. 11 is a diagram showing an auxiliary decoder of the memory device shown in FIG. 5;

FIG. 12 is a circuit diagram showing a normal division word line driver of a memory device shown in FIG. 5;

FIG. 13 is a circuit diagram showing a redundancy division word line driver of a memory device shown in FIG. 5;

FIG. 14 is a circuit diagram showing a precharger of the memory device shown in FIG. 5; and

FIG. 15 is a circuit diagram showing a redundancy enabling portion of the memory device shown in FIG. 5.

Referring to FIG. 5, a memory device according to the present invention includes a precharge portion 510, a redundancy enabling portion 520 and a plurality of global memory cell array blocks 500.

The global memory cell array block 500 includes normal

blocks 507_1, 507_2,..., redundancy blocks 506_1, 506_2,..., a fuse box 501, a redundancy driver 550, a block selector 560, a main decoder 502, an auxiliary decoder 503, normal division word line drivers 504_1, 504_2,..., and redundancy division word line drivers 505_1, 505_2, ...

The normal blocks 507_1, 507_2,... include a number of memory cells in rows and columns. The redundancy blocks 506_1, 506_2,... include a number of memory cells arranged in rows and columns and are selectively operated when there is damage in a memory cell array of the normal blocks 507_1, 507_2 ....

Referring to FIG. 6, the fuse box 501 responds to an output signal RPS of the precharges 510 to be precharged. The fuse box 501 responds to a row address signal $RA_2 \sim RA_{n-1}$ for decoding the main decoder 502, to generate a redundancy signal REDi.

The fuse box 501 includes an address sensing circuit 600, a PMOS transistor 603, a latch portion 617, a NAND gate 613, and an inverter 615. The RPS goes to "LOW" during an initial operation of a memory chip, causing PMOS transistor 603 to precharge an address sensing terminal N601 to logic "HIGH". The address sensing circuit 600 includes a plurality of address sensors 600a, 600b, ..., 600n. The address sensors 600a, 600b, ..., 600n each include a first NMOS transistor 602, an inversion unit 605, a second NMOS transistor 607, a first fuse 609 and a second fuse 611. In the case that the first and second fuses 609 and 611 do no short in a normal operation mode, i.e., in a fuse box of a

corresponding global box, the first and second NMOS transistors 602 and 607 are turned on according to a logic state of the predetermined address signal.

Accordingly, when the address signal is enabled, the voltage of the sensing terminal N601 is decreased, to keep the REDi in a "LOW" state. Also, the REDi is disactivated.

However, in the case that a memory cell of a normal block 507_1, 507_2, ... corresponding to a predetermined address is defective, a fuse corresponding to the predetermined address short. Accordingly, even though a predetermined address signal is input, the sensing terminal N601 is preserved as "HIGH" state. As a result, when the REDE signal goes to "HIGH", the output signal REDi of the fuse box goes to "HIGH", to activate the redundancy operation.

The fuse box further includes a latch portion 617 for latching the sensing terminal N601.

The redundancy driver 550, as shown in FIG. 7, includes first and second inversion units 701 and 703. The first inversion unit 701 inverts the redundancy signal REDi. The output N702 of the first inversion unit 701 is inverted, to enable a word line of a memory cell of a redundancy block 506_1, 506_2, ...

Accordingly, when the REDi signal goes to "HIGH", the output SWi thereof goes to "HIGH", to enable the word line of the memory cell of the redundancy block 506_1, 506_2, ...

FIG. 8, shows the block selector 560 which includes a

first predecoder 801, a delay unit 805, an AND unit 807, a NOR gate 809 and an inverter 811. The predecoder 801 decodes row address signals $RA_2 \sim RA_{n-1}$. The delay unit 805 delays output signals of the predecoder 801.

In the block selector, row address signals $RA_2 \sim RA_{n-1}$, the REDi(I=0, 1, ..., n-1) and a row redundancy enable signal RREB are input signals. Accordingly, in the case that the REDi is in enable state or the output N802 of the predecoder 801 goes to "HIGH" in "High" of the RREB signal, the BLSi is enabled by "HIGH". However, if the block selector had no delay unit 805, in the redundancy operation mode, a "glitch" would be generated. This is a phenomenon in which BLSi, which should be in a disable state, is momentarily enabled. This is because the time for enabling the RREB to "LOW" is later than that of the predecoded row address signal $RA_2 \sim RA_{n-1}$, as shown in FIG. 9. This causes the auxiliary decoder 700c of FIG. 5 to operate, which generate malfunction.

In the AND gate 807, the output N806 of the delay unit 805 and the row redundancy enable signal RREB are AND-operated. The NOR gate 809 NOR-operates the output N809 of the AND gate 807 and the redundancy signal REDi which is an output signal of the fuse box 500a. In the inverter 811, the output N810 of the NOR gate 809 is inverted, to generate the output BLSi.

Accordingly, in the block selector 560 of the memory device having the row redundancy scheme according to the present invention, when the redundancy signal REDi which is

an output signal of the fuse box 501 of a corresponding global memory cell array block is "HIGH", the BLSi goes to "HIGH". In the case that a row address is input which causes the output N806 of the delay unit 805 to be "HIGH", and the row redundancy enable signal RREB is disactivated by "HIGH", the BLSi goes to "HIGH".

In the case that the redundancy signal REDi is "LOW" and the output N806 of the delay unit 805 is "LOW", the BLSi goes to "LOW". In the case that the redundancy signal REDi is "LOW" and the row redundancy enable signal RREB becomes "LOW, the BLSi becomes "LOW".

Referring to FIG. 10, the main decoder 502 refuses the redundancy signal REDi and is decoded by row address signals $RA_2 \sim RA_{n-1}$, to activate an output signal NWij thereof. In detail, the main decoder 502 according to the present invention includes a predecoder 1001, a first NMOS transistor 1007, a second NMOS transistor 1009, a first PMOS transistor 1011 and a first inversion unit 1013.

The predecoder 1001 decodes row address signals $RA_2 \sim RA_{n-1}$ to generate first and second outputs N1003 and N1005, respectively. The first NMOS transistor 1007 includes a source connected to a ground voltage VSS, and a gate connected to the first output N1003 of the predecoder 1001. The second NMOS transistor 1009 includes a source connected to a drain of the first NMOS transistor 1007 and a gate connected to the second output N1005 of the predecoder 1001.

The first PMOS transistor 1011 includes a source connected to a predetermined boosted voltage VPP, a gate

connected to the row precharge signal RPS, and a drain connected to a drain of the second NMOS transistor 1009, to form a common connection line N1010. The first inversion unit 1013 inverts signals of the common connection line N1010 and outputs the main decoding signal NWij.

Accordingly, when the first and second outputs N1003 and N1005 of the predecoder 1001 go to "HIGH", the N1010 is enables to "HIGH". When the row precharge signal RPS is enabled by "LOW", the common connection line N1010 is precharged to "HIGH". Accordingly, the inversion output NWij is disabled to "LOW".

The main decoder of the memory device having a row redundancy scheme according to the present invention further includes a second inversion unit 1015 and a second PMOS transistor 1017. The second inversion unit 1015 inverts the logic state of the common connection line N1010. The second PMOS transistor 1017 includes a source connected to the boosted voltage VPP, a gate connected to the output N1016 of the second inversion unit N1015, and a drain connected to the common connection line.

Referring to FIG. 11, the auxiliary decoder 503 is enabled by a predetermined block select signal BLSi, and an output signal PXik thereof is selectively activated by row address signals RA0 and RA1.

When a corresponding global block is selected by row address signals $RA_2 \sim RA_{n-1}$ during a normal operation mode or a redundancy scheme of a corresponding global block is used during a redundancy mode, the block select signal BLSi is

activated.

The auxiliary decoder 503 according to the present invention includes a predecoder 1115, an AND gate 1101, a first inverter 1103, a first NMOS transistor 1105, a second NMOS transistor 1107, a first PMOS transistor 1109, a second PMOS transistor 1111 and a second inverter 1113. The predecoder 1115 decodes row address signals RA0 and RA1 to generate the output N1116. The NAND gate 1101 NAND-operates the block select signal BLSi and the output N116 of the predecoder 1115. The first inverter 1103 inverts the output N1102 of the NAND gate 1101.

The first NMOS transistor 1105 includes a source connected to a ground voltage VSS and a gate connected to the output N1104 of the first inversion unit 1103.

The first PMOS transistor 1109 includes a source connected to the boosted voltage VPP, a gate connected to a drain of the second NMOS transistor 1107, a drain commonly connected to a drain of the first NMOS transistor 1105.

The second PMOS transistor 1111 includes a source connected to the boosted voltage VPP, a gate connected to a drain of the first NMOS transistor 1105, and a drain commonly connected to the drain of the second NMOS transistor 1107, to be a common connection line N1112. The second inverter 1113 inverts a signal of the common connection line N1112 to output the auxiliary decoding signal PXik.

Accordingly, when the block select signal BLSi is logic "HIGH" and the output N1116 of the predecoder 1115 is logic

"HIGH", the second NMOS transistor 1107 is turned-on, to decrease the voltage of the common connection line N1112. Accordingly, the PXik is enabled to "HIGH".

Referring to FIG. 12, the normal division word line driver 504_1, 504_2 includes a first inversion unit 1201, a second inversion unit 1203, a first NMOS transistor 1205, a second NMOS transistor 1207, a third NMOS transistor 1209 and a fourth NMOS transistor 1211.

The first inverter 1201 inverts the auxiliary decoding signal PXik which is an output signal of the auxiliary decoder 700c. Also, the second inverter 1203 inverts the output N1202 of the first inverter 1201. At this time, the first and second inverters 1201 and 1203 drive the auxiliary decoding signal PXik which is an output signal of the auxiliary decoder 700c, and further a word line of a memory cell array of the normal block. The first NMOS transistor 1205 includes a gate connected to a power supply VCC and a first connection connected to a main decoding signal NWij which is the output of the main decoder 700b.

The second NMOS transistor 1207 includes a gate connected to the output N1204 of the second inverter 1203 and a first junction connected to the main decoding signal NWij. The third NMOS transistor 1209 includes a gate connected to a second junction N1206 of the first NMOS transistor 1205, a first junction connected to the output N1204 of the second inverter 1203, and a second junction commonly connected to the second junction of the second NMOS transistor 1207, to connect a word line WLijk of a memory

cell of the normal block 507_1, 507_2, ...

The fourth NMOS transistor 1211 includes a source connected to a ground voltage VSS, a gate connected to the output N1202 of the first inverter 1201, and a second junction commonly connected to the second junction of the second and third NMOS transistors 1207 and 1209, to connect to a word line WLijk of the memory cell of the normal block 507_1, 507_2, ...

Accordingly, in the normal division word line driver, the output NWij of the main decoder 502 is enabled to VPP, the second junction N1206 of the first NMOS transistor 1205 is precharged to VCC-Vtn. At this time, Vtn indicates a threshold voltage of the first NMOS transistor 1205. When the output PXik of the auxiliary decoder 503 is enabled by "HIGH", the second junction N1206 of the first NMOS transistor 1205 is precharged to VCC-Vtn. When the output PXik of the auxiliary decoder 503 is enabled by "HIGH", the second junction N1206 of the first NMOS transistor 1205 is increased to VCC-Vtn+VPP according to a principle of self boosting. Accordingly, the third NMOS transistor 1209 is turned-on, the word line WLijk of the memory cell of the normal block 507_1, 507_2, ... is enabled by a boosting voltage VPP. However, in the case that the output NWij of the main decoder 502 is disabled by "LOW", the word line WLijk of the memory cell of the normal block 507_1, 507_2, ... is decreased to a ground voltage VSS according to the second NMOS transistor 1207. Also, in the case that the output PXik of the auxiliary decoder 503 is in a state of

"LOW", the word line WLijk of the memory cell of the normal block 507_1, 507_2,... becomes a ground voltage VSS.

Referring to FIG. 13, the redundancy division wordline driver 505_1, 505_2,... includes a first inverter 1301, a second inverter 1303, a first NMOS transistor 1305, a second NMOS transistor 1307, a third NMOS transistor 1309 and a fourth NMOS transistor 1311.

The first inverter 1301 inverts the auxiliary decoding signal PXik which is an output signal of the auxiliary decoder 503. Also, the second inverter 1303 inverts the output N1302 of the first inverter 1301. At this time, the first and second inverters 1301 and 1303 drive the auxiliary decoding signal PXik to drive a word line of a memory cell array of a redundancy block. Also, the first NMOS transistor 1305 includes a gate connected to a power supply VCC and a first junction connected to the output SWi of the redundancy driver 550.

The second NMOS transistor 1207 includes a gate connected to the output N1304 of the second inverter 1303 and a first junction connected to the SWi. The third NMOS transistor 1309 includes a gate connected to a second junction N1306 of the first NMOS transistor 1305, a first junction connected to the output N1304 of the second inverter 1303 and a second junction commonly connected to the second junction of the second NMOS transistor 1307, and further connected to a word line SLik of a memory cell of the redundancy block 506_1, 506_2, ...

The fourth NMOS transistor 1311 includes a source

connected to a ground voltage VSS, a gate connected to the output N1302 of the first inverter 1301 and a second junction commonly connected to the second junction of the second and third NMOS transistors 1307 and 1309, and further connected to a word line SLik of a memory cell of the redundancy block 506_1, 506_2, ...

Accordingly, in the redundancy division word line driver, in the case that the SWi is enabled by VPP, a second junction N1306 of the first NMOS transistor 1305 is precharged to VCC-Vtn. At this time, Vtn indicates a threshold voltage of the first NMOS transistor 1305. Also, when the output PXik of the auxiliary decoder 700c is enabled by "HIGH", the second junction N1306 of the first NMOS transistor 1305 is increased to VCC-Vtn+VPP according to a principle of self boosting. Accordingly, the third NMOS transistor 1309 is turned-on, to enable the word line SLik of the memory cell of the redundancy block 506_1, 506_2, ... by a boosting voltage VPP. However, in the SWi is disabled to "LOW", the word line SLik of the memory cell of the redundancy block 50 is decreased to a ground voltage VSS. Also, in the case that the output Pxik of the auxiliary decoder 503 is "LOW", the word line Slik of the memory cell of the redundancy block 506_1, 506_2, ... goes to a ground voltage VSS.

Referring to FIG. 14, the precharger 510 includes an NOR gate 1401 and an inverter 1403.

The NOR gate 1401 receives a predetermined address signal RAi among row address signals RA_2 ~ RA_{n-1} and an

inversion signal RAiB of the predetermined address signal, to NOR-operate. Also, the inverter 1403 inverts the output N1402 of the NOR gate 1401.

When a memory chip is reset, the RAi and the RAiB go to "LOW". Accordingly, a row precharge signal RPS which is the output of the precharger is enabled by "LOW".

Referring to FIG. 15, the redundancy enabling portion 120 includes a plurality of redundancy sensing portion 1501a, 1501b, ..., 1501n and a first PMOS transistor 1503.

The redundancy sensing portion includes an NMOS transistor 1509 having a source connected to a ground voltage VSS, a gate connected to one of output signals RED0, RED1, ...,REDn-1 of a global memory cell array block and a drain connected to the row redundancy enable signal RREB.

Accordingly, a plurality of redundancy sensing portions 1501a, 1501b, ..., 1501n respond to each of output signals RED0, RED1,...,REDn-1 of the plurality of global memory cell array block, to generate the row redundancy enable signal RREB.

The first PMOS transistor 1503 includes a gate to which the row precharge signal RPS is applied, a source connected to a power supply VCC, and a drain connected to the row redundancy enable signal RREB.

Accordingly, when one fuse of the fuse boxes of the plurality of global memory cell array blocks is short, to make a redundancy signal REDi "HIGH", the RREB is enabled by "LOW".

The redundancy enable portion 120 further includes an

inversion unit 1505 for inverting the row redundancy enable signal RREB and a second PMOS transistor 1507. The second PMOS transistor 1507 includes a source connected to a power supply VCC, a gate connected to the output of the inverter 1505, and a drain connected to the row redundancy enable signal RREB.

Accordingly, when the row redundancy enable signal RREB is enabled by "LOW", the inversion unit 1505 and the second PMOS transistor 1507 latch the enabled row redundancy enable signal.

In the above memory device having a row redundancy scheme, in the case that a memory cell of the redundancy block is used, fuses of other blocks except a global block including a defective cell are short. Accordingly, in the main decoder 502 including the shorted fuse, the output signal NWij is not enabled by row address decoding. However, in the case of the redundancy driver 550, a redundancy signal REDi of a corresponding address to the short fuse is enabled. Also, the auxiliary decoder 503 is also enabled by the redundancy signal REDi, to selectively enable the output signal PKik of the auxiliary decoder according to the row address signal. Accordingly, in the global block where the fuse is short, the redundancy scheme is operated.

Also, in order to prevent the main decoder 502 and redundancy driver 550 from being simultaneously enabled, fuses of the other global memory cell array block should be cut off, during curing the memory cell having a defective

cell.

The main decoder 502 is decoded only by the row address signal, regardless of the logic state, i.e., enabling the block select signal BLSi.

Accordingly, a word line enable speed of the normal mode can be greatly enhanced. Also, the normal division word line drivers 504_1, 504_2,... can be driven by enabling the output NWij of the main decoder 502 much earlier than the output PXik of the auxiliary decoder 503. The enable time point of the wordline is determined according to the Nwij signal, so that as the NWij is enabled earlier, the wordline is enabled earlier.

In a memory device having a row redundancy scheme of the present invention, the time for enabling the word line of a normal path in a normal operation mode is earlier, to thereby increase an operation speed of a memory chip.

Also, the redundancy effect is enhanced by using a redundancy scheme of a global block which does not include a defective cell.

CLAIMS:

1. A semiconductor memory device having a plurality of global blocks, each global block comprising:

a plurality of unit matrixes including a normal block having an array by normal cells and a redundancy block having an array of redundancy cells;

a normal division word line driver for driving a word line of the normal cells;

a redundancy division word line driver for driving a word line of the redundancy cells;

a main decoder having an output signal supplied to the normal division word line driver; and

an auxiliary decoder having an output signal supplied to the normal division word line driver and the redundancy division word line driver,

wherein the main decoder includes an output signal selectively activated by a row address signal regardless of use of the redundancy cell, and the auxiliary decoder includes an output signal selectively activated by a row address signal in the case that a corresponding global block is selected by a row address signal for selecting a global block in a normal operation mode or a redundancy scheme of a corresponding block in a redundancy operation mode is used.

2. A semiconductor memory device according to claim 1, wherein the main decoder refuses a redundancy signal, and is precharged by a row address signal to activate an output

signal.

3. A semiconductor memory device according to claim 1 or 2, wherein the auxiliary decoder is enabled by a predetermined block select signal and has an output signal selectively activated by a row address signal, and in the case that a corresponding global block is selected by a row address signal of a normal operation mode or a redundancy scheme of a corresponding block of a redundancy mode is used, the block select signal is activated.

4. A semiconductor memory device according to any preceding claim, wherein in the case that a corresponding global block is selected by a row address signal for selecting a global block and a corresponding global block is selected, the global block further includes a block selector for generating a block select signal activated.

5. A semiconductor memory device according to claim 4, wherein the block selector comprises:

logic AND means of the row redundancy enable signal disabled during activating a predetermined row redundancy enable signal and a row address signal; and

logic OR means the redundancy signal activated during selecting a redundancy scheme of a corresponding block and the output of the logic AND means.

6. A semiconductor memory device according to any preceding claim, wherein the global block further comprises a fuse box which responds not to a row address signal for decoding the auxiliary decoder, but to a row address signal for decoding the main decoder.

7. A semiconductor memory device according to claim 6, wherein the fuse box comprises a plurality of address sensing portions for responding to each of the row address signals for decoding the main decoder during a normal operation mode to deactivate a redundancy signal which is an output signal of the fuse box.

8. A semiconductor memory device according to claim 6, further comprising a redundancy enabling portion for activating a row redundancy enable signal which is an output signal of one redundancy scheme of redundancy schemes of the global block which is selectively operated.

9. A semiconductor memory device according to claim 8, wherein the redundancy enabling portion comprises a plurality of redundancy sensing portions for responding to each of the redundancy signals which are output signals of a fuse box of the global block to activate a redundancy enable signal which is an output signal of the redundancy enabling portion.

10. A semiconductor memory device according to claim 9, wherein the redundancy sensing portion comprises an MOS transistor including a source connected to one selected from a group consisting of a ground voltage and a power supply, a gate connected to the redundancy signal, and a drain connected to the row redundancy enable signal.

11. A method for curing a defective cell of a semiconductor memory device: having a plurality of global blocks including two or more unit matrixes consisting of a normal block and a redundancy block and a fuse box, comprising the steps of:

selectively activating an output signal of a main decoder according to a row address signal regardless of the use of a redundancy cell of the redundancy block; and

curing the defective cell using a fuse box of another block where the defective cell is not included.

12. A semiconductor memory device substantially as shown in and/or described with reference to any of Figures 5 to 15 of the accompanying drawings.

13. A method for curing a defective cell in a semiconductor memory device substantially as shown in and/or described with reference to any of Figures 5 to 15 of the accompanying drawings.

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Claims searched:	All	**Date of search:**	24 October 1997

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): G4A AEF

Int Cl (Ed.6): G06F 11/20

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	GB 2231984 A (SAMSUNG).	-

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