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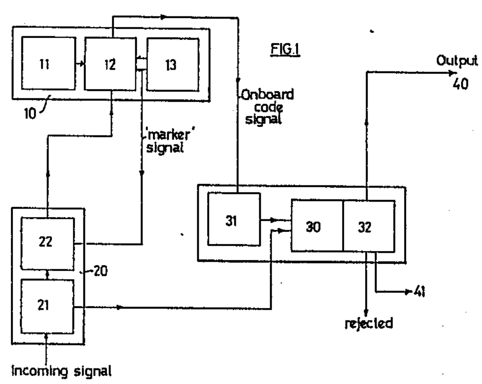
(54) **Electronic control unit.**

(57) An electronic control unit has means for receiving an external inhibit code signal (20), an internal code generator (10), means for comparing (30) the external inhibit code signal with a signal or signals produced from the internal code generator, and means for inhibiting (40) the operation of an alarm device which device will be activated if a correct external inhibit code signal is not received periodically by the control unit. A binary digital code word of 27 bits is described, of which the first 13 bits consist of a unique code, and the last 14 bits are synchronisation bits. This enables the external code signal to be synchronised with the internal code signal. The electronic control unit has been developed for use as a security switch, enabling the external code generator to be provided either in the form of a key or key-card which is placed in physical contact with a lock controlled by the electronic control unit, or in the form of a transmitter which transmits the appropriate code signal to a receiver which controls an alarm device, such that if the receiver does not receive the correct inhibit code signal at specified intervals, the alarm circuit will no longer be prevented from operating, and an alarm will be activated, or the alarm circuit can be used to disable the device, for example to disable the ignition of a motor vehicle.



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Description

ELECTRONIC CONTROL UNIT

FIELD

This invention relates to an electronic control unit for an electronic switch or similar apparatus, with particular application to systems utilising automatic recognition of a specific signal as a control means.

BACKGROUND

A large number of control systems have hitherto been available for the purpose of determining when a switch or piece of apparatus is turned on or off, operating by a wide variety of means, such as timers, meters, and control circuits. Many are operator controlled and require that a code signal is entered, or a key is presented in an appropriate orifice. In some circumstances however, none of these systems are particularly appropriate. There is often a need or place for a system or switch to be activated by the simple presence or absence of a key object or signal, particularly in the security field - Motor Vehicles in particular are often stolen without the aid of the appropriate key, and are not missed for long periods thereafter.

OBJECT

There is a need therefore for a control system which keeps a specific signal code in memory storage and which can compare this remembered signal with signals transmitted in its surroundings.

It is an object of this invention to provide an improved electronic control unit for an electronic switch, or to at least provide the public with a useful choice.

STATEMENT OF THE INVENTION

In one aspect the invention provides an electronic control unit including means for receiving an external inhibit code signal, an internal code generator, means for comparing the received external inhibit code signal with a signal or signals produced by the internal code generator, means for generating an alarm signal, and means for inhibiting the output of the alarm signal for a predetermined period following recognition of a correct received external inhibit code signal.

In another aspect the invention provides a location monitor including transmitter means capable of periodically transmitting a predetermined inhibit code signal, receiver means capable of detecting the predetermined code signal, connected to an alarm system, the receiver means including an electronic control unit as described above, such that if the transmitter means is disabled, or goes out of range of the receiver means, the inhibit code signals will no longer be received by the receiver means, and an alarm condition is signaled.

In a yet further aspect the invention provides a multiple inhibiting alarm system including a master control unit, a plurality of individual detectors each capable of detecting an alarm function, each individual detector having a receiver and a transmitter connected to an appropriate control bus, each detector being capable of transmitting an inhibit code signal, the master control unit being connected also to the control bus, alarm means associated with the master control unit such that if the master control unit fails to periodically receive an inhibit code signal from each of the individual detectors, then the alarm means will signal the presence of an alarm condition.

DRAWINGS

These and other aspects of this invention which should be considered in all its novel aspects, will become apparent from the following description which is given by way of example only, with reference to the accompanying drawings, in which:

Figure 1: is a block diagram of a first electronic control unit;

Figure 2: is a schematic diagram illustrating the operation of the electronic control unit of figure 1 both with a key (figure 2a) and in the absence of a key (figure 2b);

Figure 3: illustrates a 27 bit external inhibit code word;

Figure 4: is a prototype circuit for the recognition of a received external inhibit code word;

Figure 5: is a block diagram of a security alarm system using multiple inhibit code words;

Figure 6: is a master alarm control unit for figure 5;

Figure 7: is one of the detector units for figure 5;

Figure 8: is an audible alarm unit for figure 5;

Figure 9: is a receiver unit for a location monitor;

Figure 10: is a transmitter unit for use with the receiver of figure 9.

KEY OPERATED ELECTRONIC SWITCH - FIGURES 1 &; 2

The preferred system is an alarm control switch for use in a motor vehicle. It operates with the ignition system to prevent the vehicle being used without the use of the proper key. The system broadly consists of an input code generator 50, associated with a key device such as a "smart card" (a key card having its own microprocessor) or a mechanical key having an input code generator concealed within the body of the key, a control system 100 associated with the ignition, and a disabling system and/or alarm transmitter.

In Figure 2a the key device is represented a mechanical key but the operation is the same no matter how the input code generator is concealed (eg it may be built into a ring, watch, "smart card" or the like.) The word "key" in the context of this invention thus encompasses any item containing an input code generator.

If the correct key is used a sequence of operation is followed as shown in Figure 2a. The input code generator 50 is powered by the car battery and transmits a signal through to the control system 100. This control system recognises the signal from the key in a manner detailed below, and inhibits the alarm system while the ignition of the car proceeds. If no key or an incorrect key is used to start the car, the control system 100 is activated without receiving an incoming code signal and consequently does not inhibit the alarm system, which is duly activated. It may alternatively or additionally act to prevent ignition or otherwise disable the vehicle.

The alarm system may take the form of a simple siren or similar localised alarm, or alternatively may consist of a transmitter which switches on in the absence of the correct code signal, broadcasting a signal on a wavelength received by police or other monitoring services. The alarm signal may be unique to each individual alarm in the same way that the key code signal is unique (indeed, the same signal may be used for both purposes), allowing the police or monitoring service with the aid of a computer to identify which vehicle has been stolen.

The control system 100 in its preferred embodiment consists broadly of an Onboard Code Generator 10, an incoming signal receiver 20, a Comparator 30, and an output channel 40.

The Onboard code generator produces the code stored in the control system, with which incoming signals are compared. It consists of a master clock oscillator 11, a memory address counter 12 and a memory 13. The memory address counter 12 takes information out of the memory 13, in a sequential order, presenting each piece of information for examination by the Comparator. The master clock acts as a timer for use in sampling operations: it cycles 16 times faster than the memory addressing process, and thereby allows sampling operations to be carried out within the time interval of each unit presentation. In its preferred embodiment the memory 13 can hold 256 memory locations from which the address counter 12 can draw to make up the predefined code.

The Onboard Code Generator system 10 operates cyclically - repeating the code continually.

The incoming signal receiver 20 includes Translation apparatus 21 which converts a signal to a useful form, and a synchronising system 22 which matches the phase of the Onboard code with that of the incoming signal.

The incoming signal in normal use is generated by the Input Code Generator 50, associated with the key. The Input Code Generator preferably comprises a circuit similar to the Onboard Code Generator described above, consisting principally of a master clock, a memory address counter, and a memory. It is of course important that the same code is programmed into both generators, and also that the master clocks of both are set to the same frequency.

The Translation system 21 acts to invert the incoming data so as to restore logic levels. When a signal enters the system it is translated and then shunted to both the Comparator 30 (see below) and the Synchronising System 22. This activates the Synchronising System and causes it to monitor any demands the memory address counter 12 makes on a specific memory location in the memory 13, while it endlessly repeats the Onboard Code signal. At the end of each transmission of the code signal, the Onboard Code Generator produced a 'marker' signal, wherein the same specific memory location is called upon 64 times in a row. This is a signal which does not form a part of the Onboard Code, and thus when the Synchronising System monitors this 'marker' signal it recognises that one complete transmission of the Onboard Code has just been finished and another is about to begin. It then acts to release the Onboard Code as it is generated, such that it can be passed on to the Comparator 30 with the beginning of the code first and the end last.

The Comparator 30 simply acts like a switch - it compares the onboard signal with the incoming signal, and if they are the same the signal is passed on to produce an output, and activate or deactivate the switch which the system controls. If they are not the same then the incoming signal is rejected.

The Comparator system may also include some form of error reducing system. Because of interference and/or synchronisation errors, a particular transmission of the onboard code might not match an incoming code, even if the incoming code is correct. To reduce or avoid errors of this sort, a sampling system may be used.

In the time period over which each code bit is drawn from the memory 13 by the memory address counter 12 and transmitted, the master clock oscillator 11 marks 16 time intervals.

If the system is slightly out of synchronisation, the last segment of a transmission may occur where the first segment of the next code bit should be, or vice versa. Similarly, if there is interference with the signal, any part of the transmission may be different from all the rest. Thus if only the first 16th of the transmission, or only the last, is used in making up the onboard signal with which the incoming signal is compared, errors may easily occur. Similarly if the entire transmission is used for comparison, a single error caused by interference or mis-synchronisation may ruin the whole code.

Therefore the transmission of each information bit is examined three times, on the 4th, 8th, and 12th intervals of the 16 counted out by the master clock oscillator during each transmission, by a sample control system 31, and these three examples of the onboard signal are used for comparison with the incoming signal. If two or more out of the three match the appropriate unit of the incoming signal, the incoming signal is passed - if only one or none out of the three matches with the incoming signal, the incoming signal is assumed to be wrong and is rejected.

This rejection may not be final, if the system includes a 'word' error counter 32. This may be included to allow a specified number of incorrect units in each whole signal before rejection.

If the incoming signal is passed, i.e. if it matches the onboard signal to the required degree, it is passed on to the output channel, where it activates or deactivates the controlled switch.

In this first embodiment, the switch is used to cut off the ignition system, either until the correct signal is received, or for a set period of time after which the car may either start or the correct signal may be presented.

Preferably, the switch may also control a transmitter.

While a recognised incoming signal is being received the transmitter is inhibited by the signal output 40, and is prevented from broadcasting.

If however the wrong signal is received, or no incoming signal arrives at all, the transmitter 41 switches on, broadcasting the onboard code signal. Thus, the onboard code signal is used not only as a recognition code, but also as an alarm signal. It can be broadcast in a form suitable for being received and interpreted by a receiver station such as might be found with the police or other security services. By keeping a computer record of alarm systems in the district this could enable individual items such as cars or houses to be identified as broken into or stolen immediately after the crime occurs. Similarly, by broadcasting on a particular frequency, it can allow agents of the police or a security service to be immediately and automatically informed of a crime in the vicinity, without disturbance to the public at large.

The level of error acceptable will be dependent to some extent on the end use of the product.

If the control system is intended simply to provide a convenient and easy means for operating a switch e.g. to switch on a light when a person carrying an appropriate transmitter enters a room then a fairly lax control system allowing fairly low degree of occurrence in the signal matching may be acceptable.

However, if the control system is intended for fairly high security operations, such as in deactivating an alarm when opening a door or starting vehicle with the appropriate key, then a fairly high level of accuracy in the signal matching will be required.

The operation to which the output relates may, of course, be any one of a large number - almost any on-off switching operation might be controlled by this system, as well as a number of variable intensity operations : the output of the system might increase or decrease a level such as the speed of a vehicle, the intensity of a light, the volume of a speaker or the temperature of a heating or cooling element - every time an appropriate incoming signal or received. Similarly the incoming signal recognised might be of any of a number of types -radio, microwave, infra-red or electrical being the most convenient ways at present for delivering a digital binary code word to the control system.

INTERNAL CODE GENERATOR AND COMPARATOR - FIGURES 3 &; 4

Figure 3 represents a 27 bit external inhibit code word. The first thirteen bits consist of 'unique code'. The last fourteen bits are synchronisation bits. The code bits in the example could be any random combination of 1's or 0's except all 1's giving 2^{13}-1 combinations.

It will be noted that the horizontal scale is marked time. Bit 1 would, in practice occur first in time. Each of the 27 bits occurs for 1 time interval. The code word can be extended to as many bits as are required for security. We have tested word lengths of 105 bits of which 35 bits were used for the unique code giving 2^{35}-1 code combinations. The capacity of the prototype circuit of figure 4 is 2^{128}-1 with no modification to the circuit but with 1 wire change the circuit can handle up to 2^{1024}-1 with extra address gating.

The code generation circuitry for the binary code word is used, in both the external code generator (eg in a key) and in the electronic control unit. Figure 4 is the full circuit of the electronic control unit which recognises the received inhibit code and controls the output from the electronic control unit.

The code generator consists of a master clock oscillator IC 1, the memory address counter, and IC 2 the code memory.

The master clock clocks IC 1 pin 10. IC 1 is a 12 stage binary ripple counter and its outputs Q1 - Q12 are used to address IC 2 giving access to 256 memory locations. The contents of each location are presented sequentially at IC 2 pin 9 and each address is held for 16 counts of the master oscillator.

When address 256 is reached IC 1 resets itself to address zero and the process starts again.

The code generated thus is used in the prototype inhibitor.

The electronic control unit and external code generator come in matched pairs to inhibit the master clock. Frequencies in both need to be close. The code memories must contain the same information.

The electronic control unit functions as follows:

A radio frequency (R.F.) inhibit signal is received from an external code generator and is converted into binary logic. In the prototype the data is inverted hence IC 7 pins 12, 13, 11 inverts the input to restore logic levels. IC 8 pins 3, 2 reset IC 3. IC 3 is a 12 stage binary ripple counter pin 2 is count 64. When input data is zero IC 3 is held reset. When input data is one IC counts one count for each on board data bit via IC 1 pin 3 IC 6 pin 2, 3 IC 8 pins 5, 4. When IC 3 counts up to 64 the input data must be part of the synch bit as this is the only part of the code word that may have 64 consecutive ones. IC 3 stops counting via pin 2 going high and inhibiting the clock to IC 3 from IC 1 pin 3.

At the end of the incoming synch signal the input data goes low resetting IC 3 to zero, IC 3 pin 2 goes low resetting the on board memory address counter IC 1 to address zero the first code bit, via IC 8 pins 14, 15 and the differentiating circuit C_1 D_1 R_1.

The incoming data and electronic control unit data are now in synchronisation and will remain so.

Both the on board electronic control unit data and the incoming inhibit signals are fed to a comparator IC 5 pins 1 and 2. IC 5 pin 3 will go high only when its inputs pins 1 and 2 are different, that is when the on board data and inhibit data are different.

Because of the radio transmission and demodulation it was assumed that the received inhibit data would be of poor quality and that IC 5 pin 3 would be high during transitions and due to interference. The following method was used to allow some errors to occur and to minimise their occurrence.

The comparator output IC 5 pins 3 is fed to a NAND gate IC 7 pin 8. The signal is gated with examine pulses derived as follows. Remember each data bit exists for the time it takes the master clock to output 16 pulses.

During each data bit IC 1 pins 5, 6, 7 and 9 count from 0 to 15 inclusive a total of 16 intervals. The sample control circuit gates pulses 4, 8, 12 through to IC 7 pin 9. Enabling the comparator output to clock IC 4 pin 10 one pulse for each error or three pulses for one whole bit in error.

IC 4 is an optional 12 stage binary ripple counter. An output may be selected to allow a number of errors to be ignored. IC 4 is reset every synch bit and therefore only totalises errors every word.

When the requisite number of errors have been counted IC 7 pin 2 goes high gating the on board data out to the electronic control unit output stage (not shown).

MULTIPLE SECURITY ALARM SYSTEM AND BUS - FIGURE 5

The unit shown in figure 5 consists of five individual detectors each containing a transmitter-receiver unit, a master control unit and an audible alarm unit. The system operates as follows.

The master control unit is programmed for the total number of detector units operating in the system (only five are shown for ease of explanation). The master control unit initiates the sequence by transmitting the code for the receive portion of the first unit (in this case code 5) onto the code bus. The master control unit then waits for the transmit code from the first unit to appear on the inhibit bus. If this code (in this case code 1) is not received within a preset time an alarm is initiated via the code bus to the audible alarm unit.

Normally the first transmitter receiver unit will receive the start code and after a short delay transmit the correct code for the next unit. This second unit will receive the correct code via the code bus and the master control unit will also receive the inhibiting code via the inhibit bus. The master control unit will then wait for the inhibit code from the second unit, if any of the pre-programmed inhibit codes is not received an alarm will be initiated.

This process is repeated with thr second unit transmitting the correct code for the third unit whilst the master control unit waits for this code via the inhibit bus.

This process continues, each transmitter receiver initiates the next unit in sequence. The last unit in sequence transmits the code for the first unit in the sequence. The master control unit has to receive the correct codes in the sequence or an alarm will be initiated.

The master control unit can be programmed to allow for the loss of one or more of the inhibit codes from the sequence. This enables the overall system to operate with any individual detector heads isolated.

MASTER ALARM CONTROL UNIT - FIGURE 6

This unit is designed to operate in conjunction with several individual detectors each of which contains a code transmitter receiver unit and alarm/fault unit described below.

The master control unit consists of a micro-computer comprising a micro-processor, programme memory and operating keyboard. Also controlled by the micro-computer are a start code transmitter and a decoder receiver. The operation of the unit is as follows.

The micro-computer is programmed with the number and sequence of the code transmitter receivers in service on the system. This is achieved by programming each unit in the system to be active via the input keypad.

When all the active units have been programmed in and the system run initiated the micro-computer outputs the code compatible with the first transmitter receiver in the system. The micro-computer then waits for the output from that transmitter receiver to appear on the inhibit bus. Having received the correct code from the inhibit bus the computer then changes its input into the decode receiver to that of the next transmitter in the sequence. If at any time the next valid code is not received from the inhibit bus within a preset time interval the micro-computer alarm output goes high which prevents the operation of the system by imposing a permanent low level on the code bus. This low level being maintained on the code bus initiates an alarm in the audible alarm unit.

INDIVIDUAL CODE TRANSMITTER RECEIVER - FIGURE 7

These units are designed to operate in conjunction with a sensor (not shown) such as standard intruder alarm detector head which provides a closed contact which opens for an alarm condition.

In Figure 7, IC 1 is a serial code receiver which is programmed to respond to a specific serial code from the code bus. Upon receipt of the correct code, IC 1 output pin 17 goes low. This triggers IC 2A which provides a delay to allow the code bus to clear. At the end of this delay IC 2A triggers IC 2B which enables the code generally by IC 3 to be transmitted onto the code bus providing the alarm detector has not sensed an alarm.

The code from IC 3 is also transmitted to the inhibit bus.

IC 2B only allows IC 3 to transmit for a set time at the end of which the output from IC 4 is set to a high impedance to prevent more than one transmitter trying to use the code bus at one time.

If the alarm detector contact is open the code from IC 3 is not transmitted onto the inhibit bus.

AUDIBLE ALARM UNIT - FIGURE 8

The audible alarm unit consists of an audible alarm operated by a monostable IC.

Providing that the code is operating normally, the monostable IC is being continuously triggered and the audible alarm does not operate. If however the code bus is driven low by the master control unit, or the normal code transmission ceases for any reason the audible alarm is triggered. Other alarm monitors may be used in place of or in addition to this audible alarm unit.

LOCATION MONITOR - FIGURES 9 &; 10

Apparatus

1 Wrist radio transmitter - controlled by a pre-programmed micro processor.

2 Radio receiver coupled to a sending device eg either (a) an automatic dialing system on a phone in the locality or (b) a more powerful radio transmitter in the locality. This sending device is in turn coupled to a permanently manned monitoring agency.

3. The monitoring agency has a pre-programmed computer system designed to monitor all automatic sending devices in the system.

Method of Operation

The system is designed to work on a self monitoring principle, that is the computer is programmed to receive a set number of coded signals from the automatic dialing unit for it to remain in the non alarm state.

The radio receiver/automatic dialing unit is also programmed to receive coded signals at a prescribed rate from the wrist radio transmitter and if for any reason any of these signals are not received the system will go into alarm state at the computer terminal. The wrist radio transmitter is designed in such a way that if it is tampered with in any way or taken off the wrist the transmitter will be disabled thus causing the radio receiver to go into the alarm state. If the person wearing the wrist transmitter decides to go beyond the radio receiver range the system once again goes into alarm.

It is envisaged that this system, would be offered to each eligible individual as an alternative to being incarcerated in prison as such if they were to break the rules and bring the alarm up at the monitoring base then the person would be sent to prison for the remainder of this sentence. It functions as a probation system but similar apparatus could be used as any form of location monitor, eg to check that children or livestock remain in the vicinity of the receiver, or that equipment (such as televisions in a motel) are not taken away from the vicinity of the receiver.

Location Monitor Circuit Description

The transmitter sends pulses of short duration once a minute to the receiver. If the wristband is broken the transmitter is disabled and will not restart until the initialise button is pushed. The receiver uses these pulses to reset its internal timers and hence keep it in its inactive state. If no pulse is received over a two-minute period an alarm is sounded. This signals the wearer of the transmitter that they are out of range and must approach the receiver so that the signal can again be received, resetting the alarm. If, however, no further pulses are received, ie the transmitter is no longer in the vicinity, then after a further two minutes the receiver commands the autodialler to notify the monitoring station.

The system breaks into two parts, the transmitter and the receiver. For the purpose of this description they are covered separately.

THE RECEIVER - FIGURE 9

The receiver decodes the incoming signal and compare the code received with a preset code, set by the code switches. If identical a pulse is derived which activates a relay.

A CD4060 14 stage ripple carry binary counter provides a timer which gives outputs at 2 minutes and 4 minutes after reset. Another CD4060 gives 30 minutes on and 30 minutes off time periods.

Pulses from the decoder are used to reset the 2 minute/4 minute timer which prevents it from reaching its output states. If the transmission of pulses stops, the CD4060 will not be reset and after 2 minutes the output will go high. This results in the CD4013 D flip-flop latching its output high and hence allowing the BC547 to turn on pulling-in the (normally open contacts of the) warning output relay. If a decoded pulses arrives after this time the CD4060 and the latched output will return to the inactive state.

If a decoded pulse does not arrive within a further 2 minutes the 4-minute output will go high. The effect of this is that via the diode shown the clocking of the CD4060 will be inhibited, hence latching the device in that state. The receiver's original relay circuitry for the autodialler will be activated, pulling that relay in. Again the resumption of received transmissions will reset the system.

The BC557 transistor produces a reset when the power is turned on so that the counters and the latch come up in a controlled state.

THE TRANSMITTER - FIGURE 10

A transmitter is used to generate periodic signals, eg to produce a half second pulse every minute. The transmitter generated and transmitted an inhibit code (as previously described) set by links on its board.

The approach was again to use a CD4060 counter to give a one minute delay. This triggered a monostable, (U1c, U1d), to give a half second pulse. As the supply to the transmitter was derived from the output of the monostable, this allowed time for the code to be transmitted at least ten times, enough for the receiver to reliably recognise the code.

The R/S flip-flop formed by U1a and U1b is used to give the circuit a degree of protection against tampering.

After the wrist-strap is closed and the initialising button is pushed the output of the flip-flop is low, allowing the circuit to run.

If however the wrist-strap is opened the output of the flip-flop goes high holding the CD4060 reset and hence stopping the transmitter. Subsequent opening and closing of the wrist-strap will not change the flip-flop's state, hence latching the transmitter off. In the case of the prototype the only way to restart the transmitter is to close the wrist-strap and push the initialise button. This is acceptable for demonstration purposes but in the finished product the wrist-strap will be locked onto the wearer and activated by closing the wrist-strap, any interference with the device permanently disables it thus creating an alarm condition.

COMPUTER SYSTEM

The monitoring agency will have a receiver capable of detecting and monitoring signals from each locality transmitter/dialler and may be programmed to ignore signals at any given time, eg to allow a monitored person to leave home to go to work.

VARIATIONS

It will be appreciated that the above examples are only some of the security and control circuits that can be constructed using the inhibit code concept of this invention. Many other applications may be derived from the electronic control unit of this invention. Various alterations or modifications may also be made to the foregoing without departing from the scope of this invention as exemplified by the following claims.

Claims

1. An electronic control unit including means for receiving an external code signal (20), an internal code generator (10), means for comparing (30) the received external inhibit code signal with a signal or signals produced by the internal code generator, means for generating an alarm signal (41), CHARACTERISED IN THAT a correct external code signal functions as an inhibit code signal and the electronic control unit includes means (30) for inhibiting the output of the alarm signal (41) for a predetermined period following recognition of a correct received external inhibit code signal.

2. An electrical switch controlled by key means the switch controlling a first circuit (such as an ignition circuit of a vehicle), and a second circuit (such as an alarm circuit), CHARACTERISED IN THAT the key means includes an electronic code generator (50) capable of sending an inhibit code signal to inhibit the operation of the second circuit which without the presence of the inhibit code will operate an alarm and/or disable the operation of the vehicle.

3. A location monitor including transmitter means capable of periodically transmitting a predetermined inhibit code signal, receiver means connected to an alarm system, the receiver means including an electronic control unit as claimed in claim 1, CHARACTERISED IN THAT if the transmitter means is disabled, or goes out of range of the receiver means, the inhibit code signals will no longer be received by the receiver means, and an alarm condition is signaled.

4. A multiple inhibiting alarm system including a master control unit, a plurality of individual detectors each capable of detecting an alarm function, and alarm means associated with the master control unit, CHARACTERISED IN THAT each individual detector has a receiver and a transmitter connected to an appropriate control bus, each detector being capable of transmitting an inhibit code signal, the master control unit being connected also to the control bus, whereby in use if the master control unit fails to periodically receive an inhibit code signal from each of the individual detectors, then the alarm means will signal the presence of an alarm condition.

5. A multiple inhibiting alarm system as claimed in claim 4 CHARACTERISED IN THAT each detector is adapted to send its own unique inhibit code signal to the control bus in response to the receipt of a unique inhibit code signal from one of the other detectors so that in use a first individual detector transmits its own code signal to the main bus, which first signal is picked up by a second individual detector on the bus, which in turn transmits its own code signal to the bus, so that the code signals are sequentially detected and transmitted along the bus in a cyclic fashion whereby in the event of one of the individual detectors being unable to transmit its code signal (because it is disabled or because it has sensed a local alarm condition) the absence of its code signal will be detected by the master control unit and an alarm condition signaled.

FIG.1

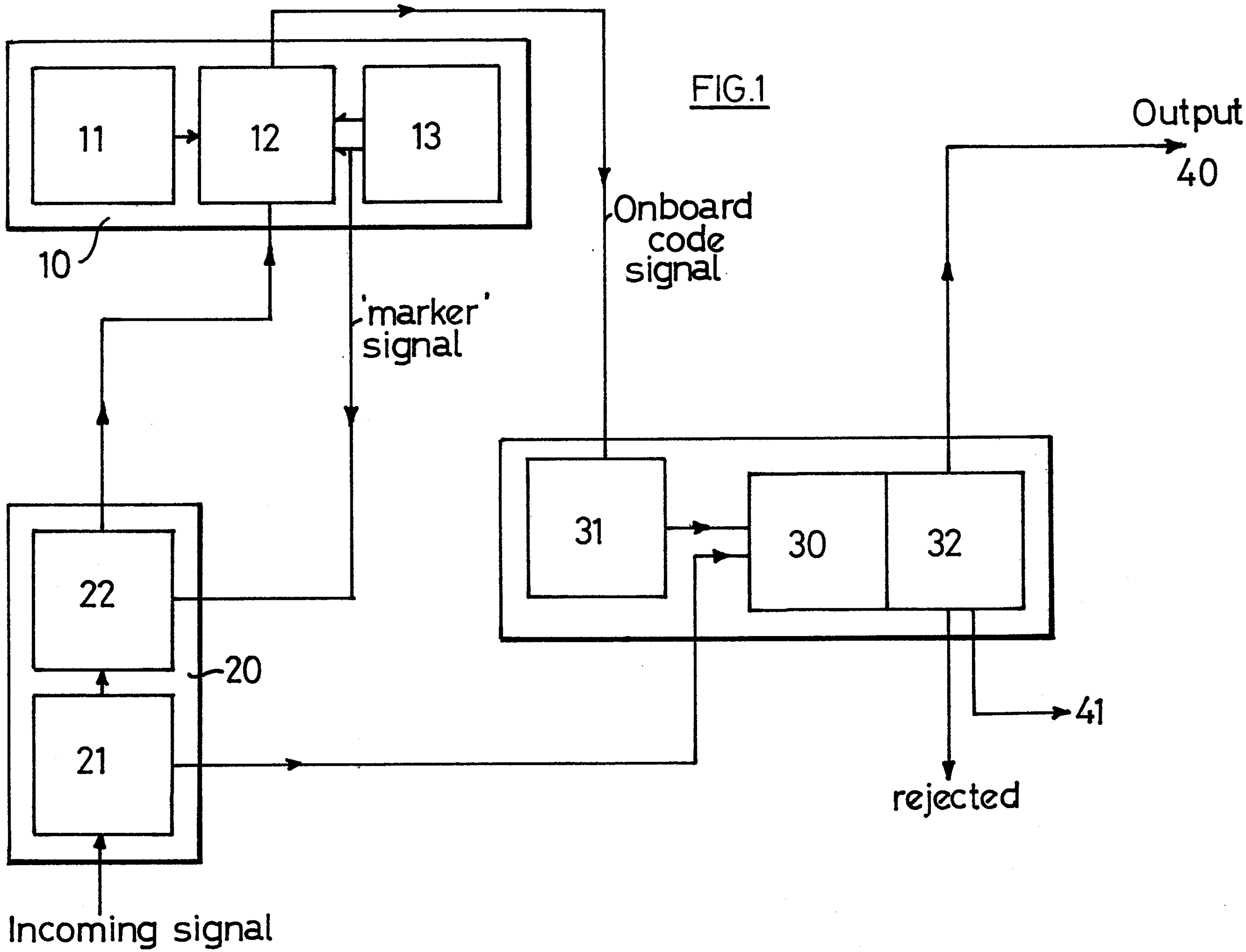
11
12
13
10
'marker' signal
Onboard code signal
Output
40
31
30
32
41
rejected
22
21
20
Incoming signal

FIG. 2

A

B

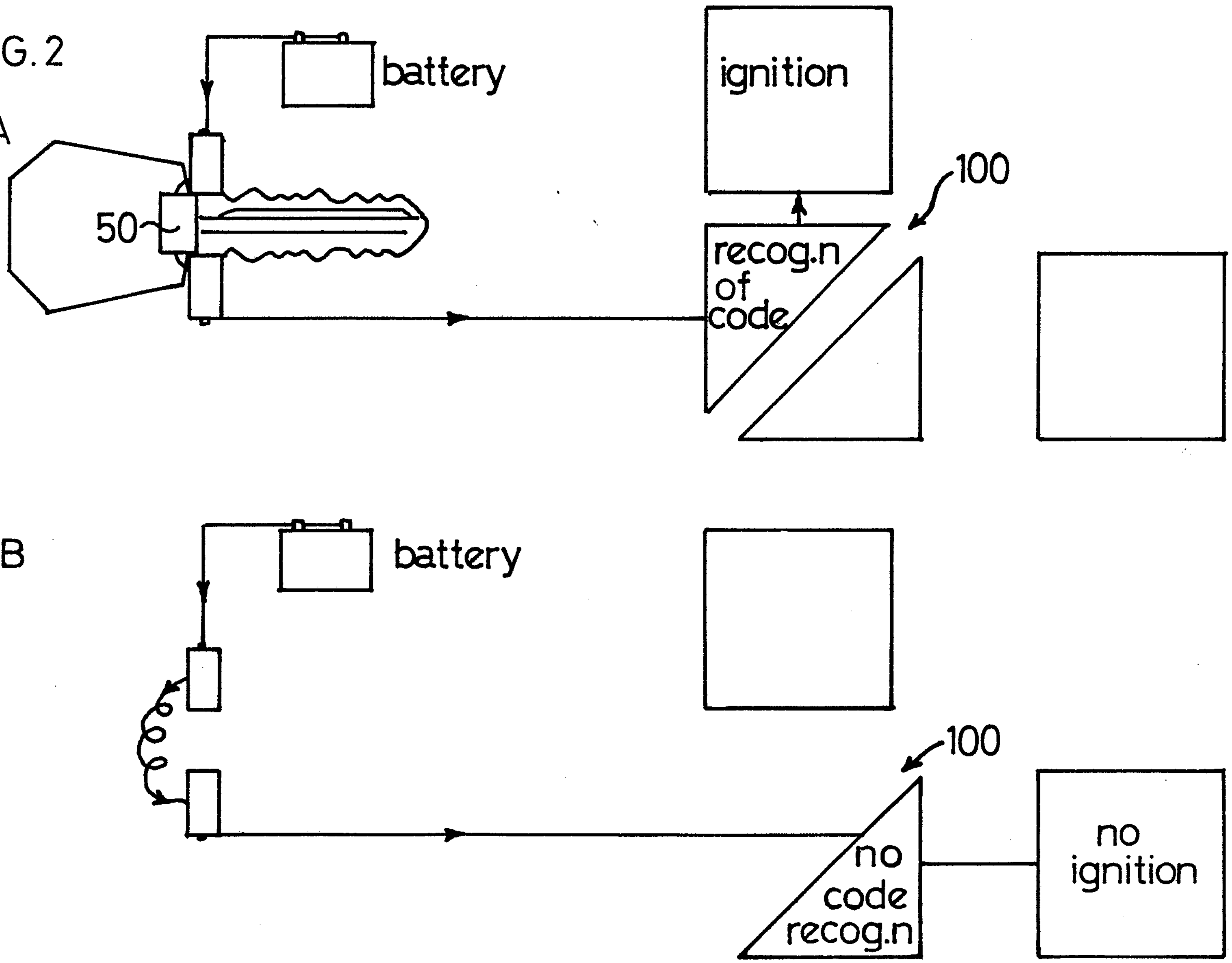
battery
50
ignition
recog.n
of
code
100
battery
100
no
code
recog.n
no
ignition

FIG. 3

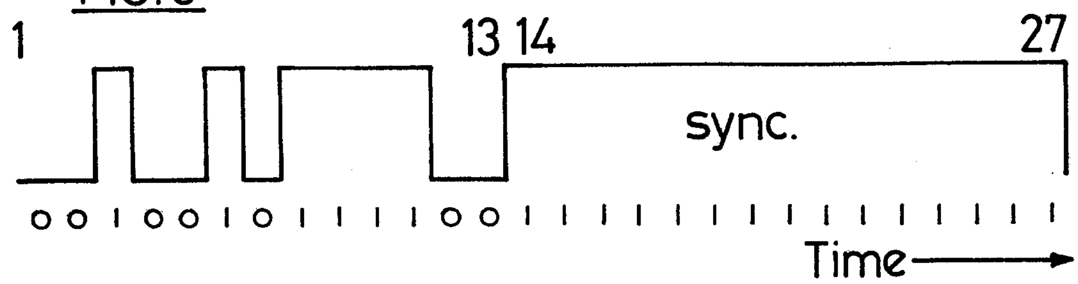
1
13 14
27
sync.
0 0 1 0 0 1 0 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Time

FIG.8

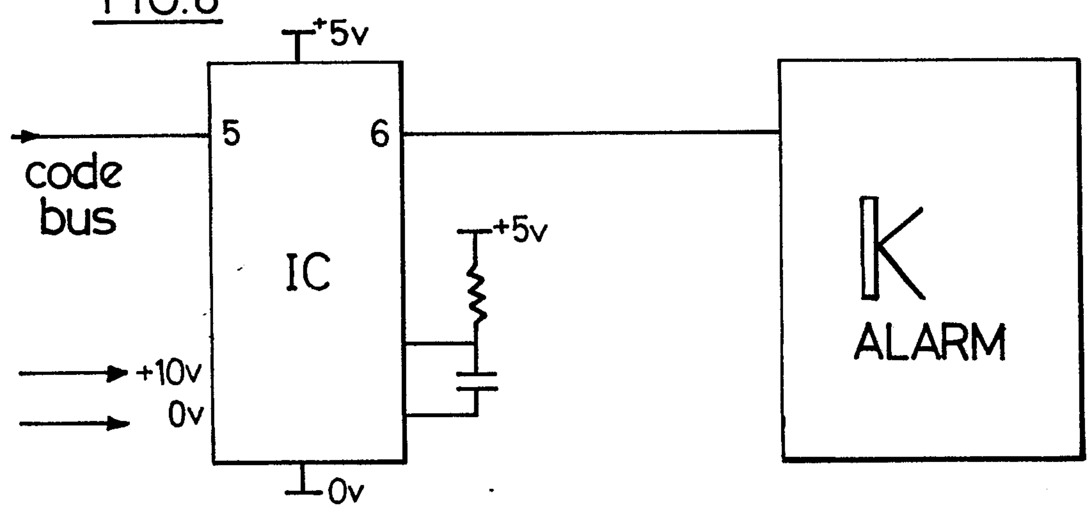
+5v
5
6
code
bus
IC
+5v
+10v
0v
0v
ALARM

FIG. 4

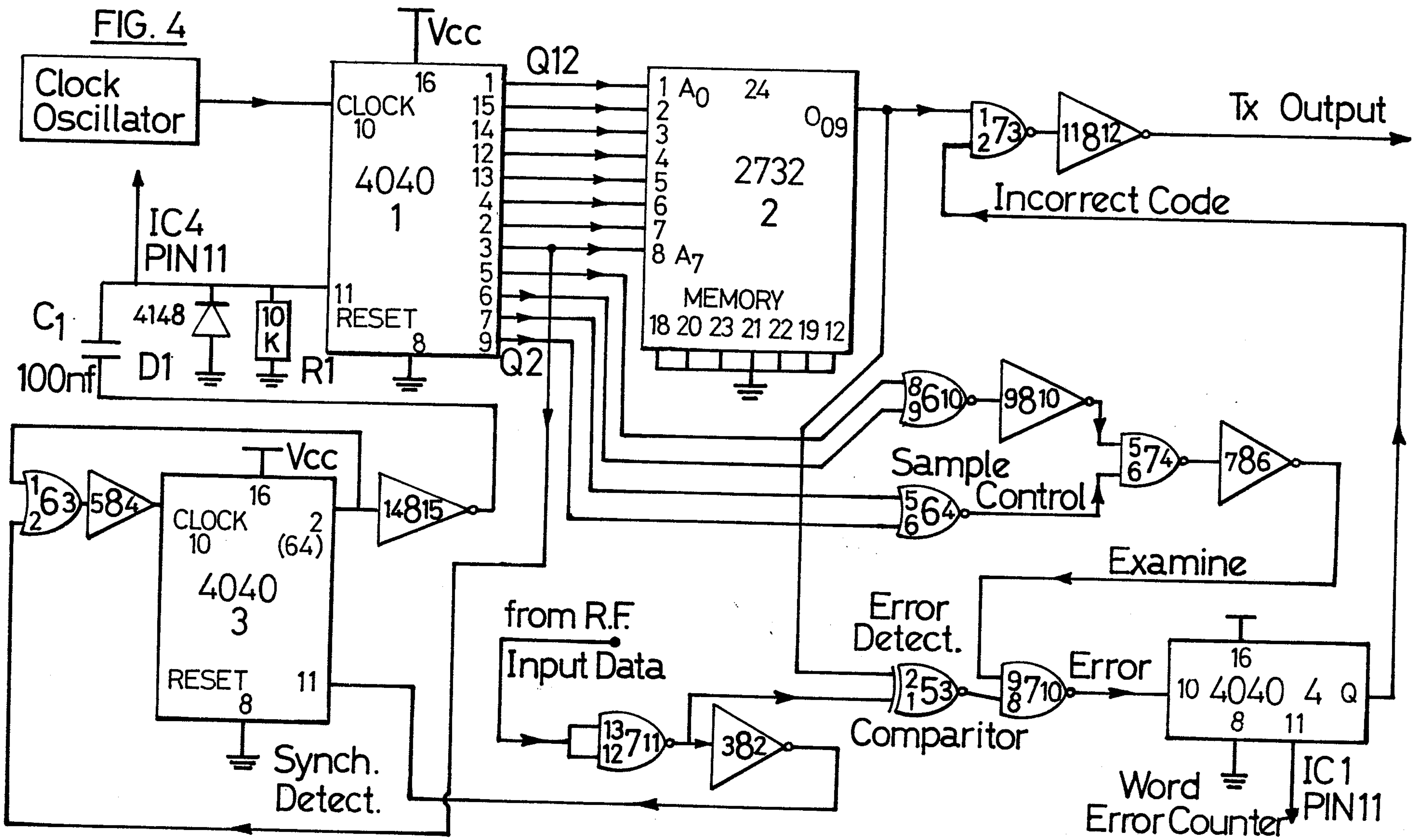
Clock Oscillator
Vcc
CLOCK 10
16
4040
1
RESET
11
8
Q12
Q2
IC4 PIN11
C1
100nf
4148
D1
10 K
R1
A0
A7
24
O09
2732
2
MEMORY
18 20 23 21 22 19 12
Tx Output
Incorrect Code
Sample Control
Examine
Error Detect.
Error
Comparitor
from R.F.
Input Data
4040
4
Q
IC1 PIN11
Word Error Counter
Vcc
CLOCK 10
(64)
4040
3
RESET
Synch. Detect.

FIG.5

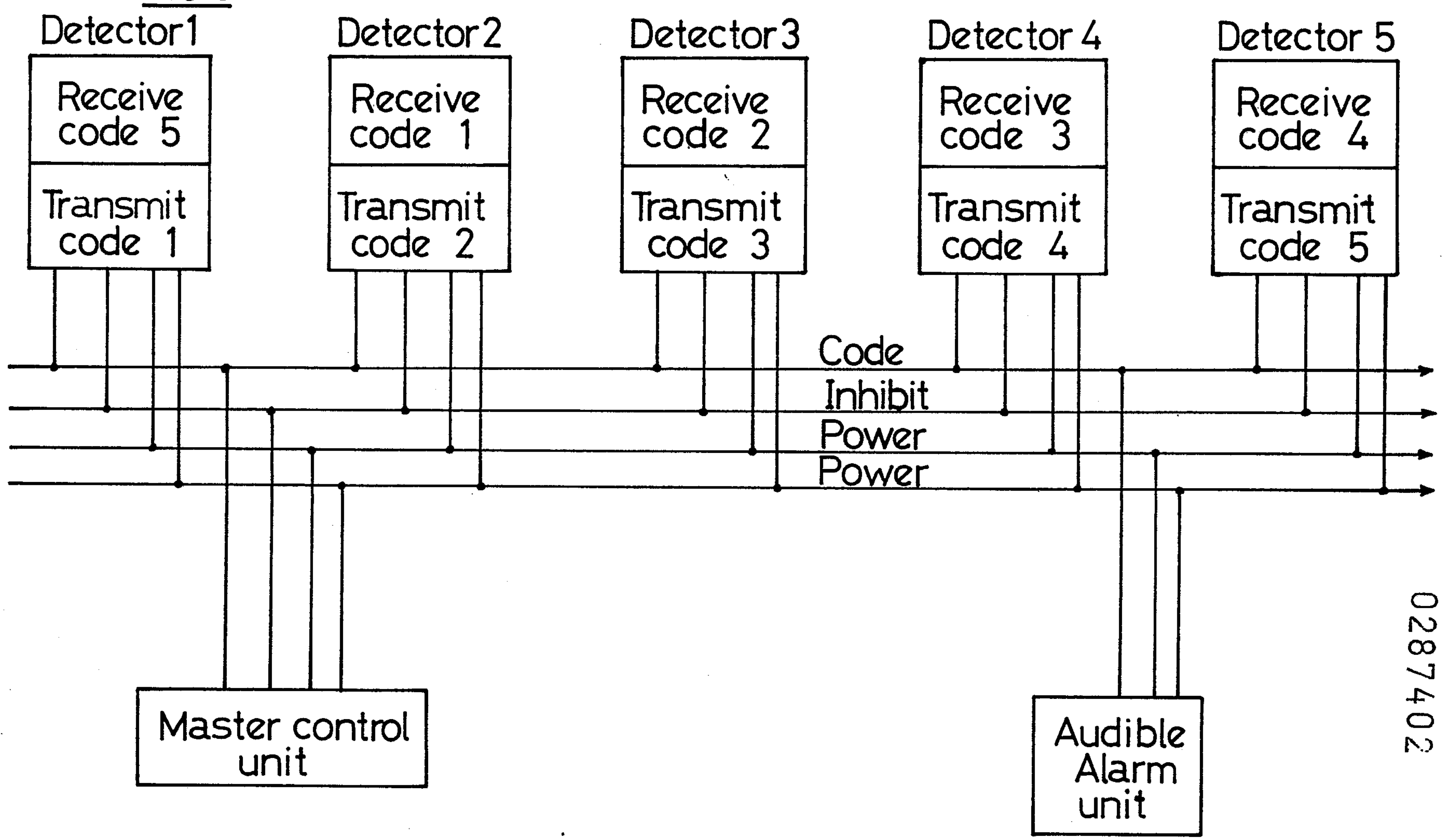

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FIG.6

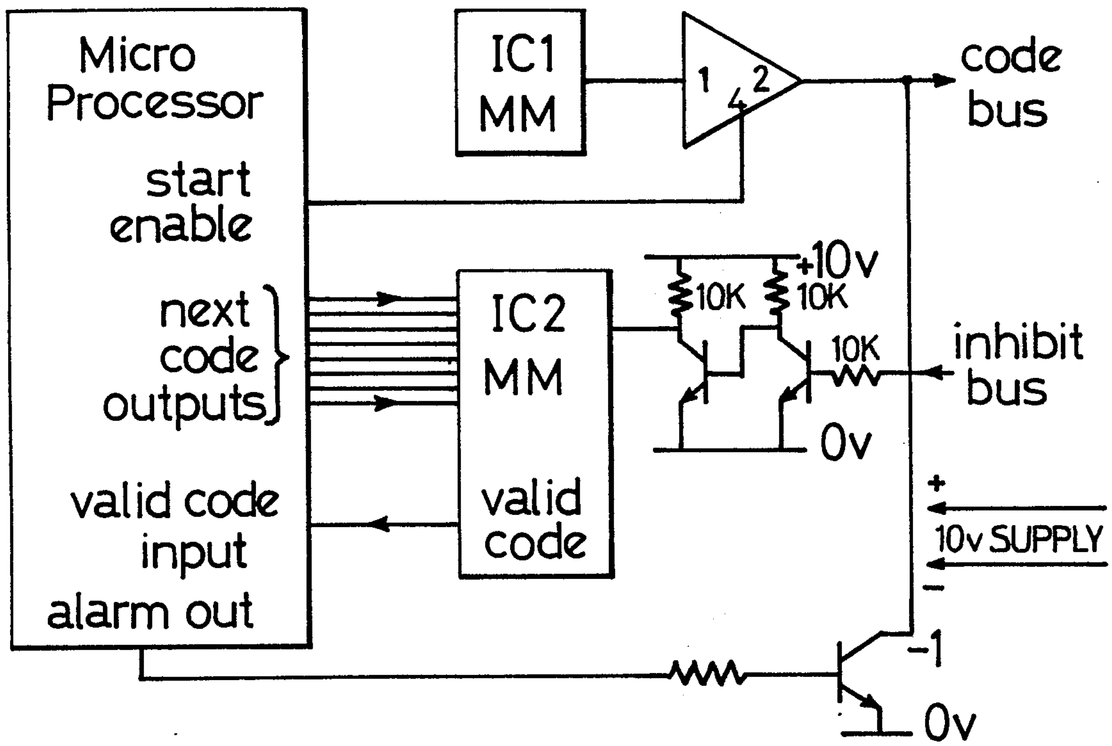
Micro Processor
start enable
next code outputs
valid code input
alarm out
IC1 MM
1
2
4
code bus
IC2 MM
valid code
+10v
10K
10K
10K
inhibit bus
0v
+
10v SUPPLY
−
−1
0v

FIG.7

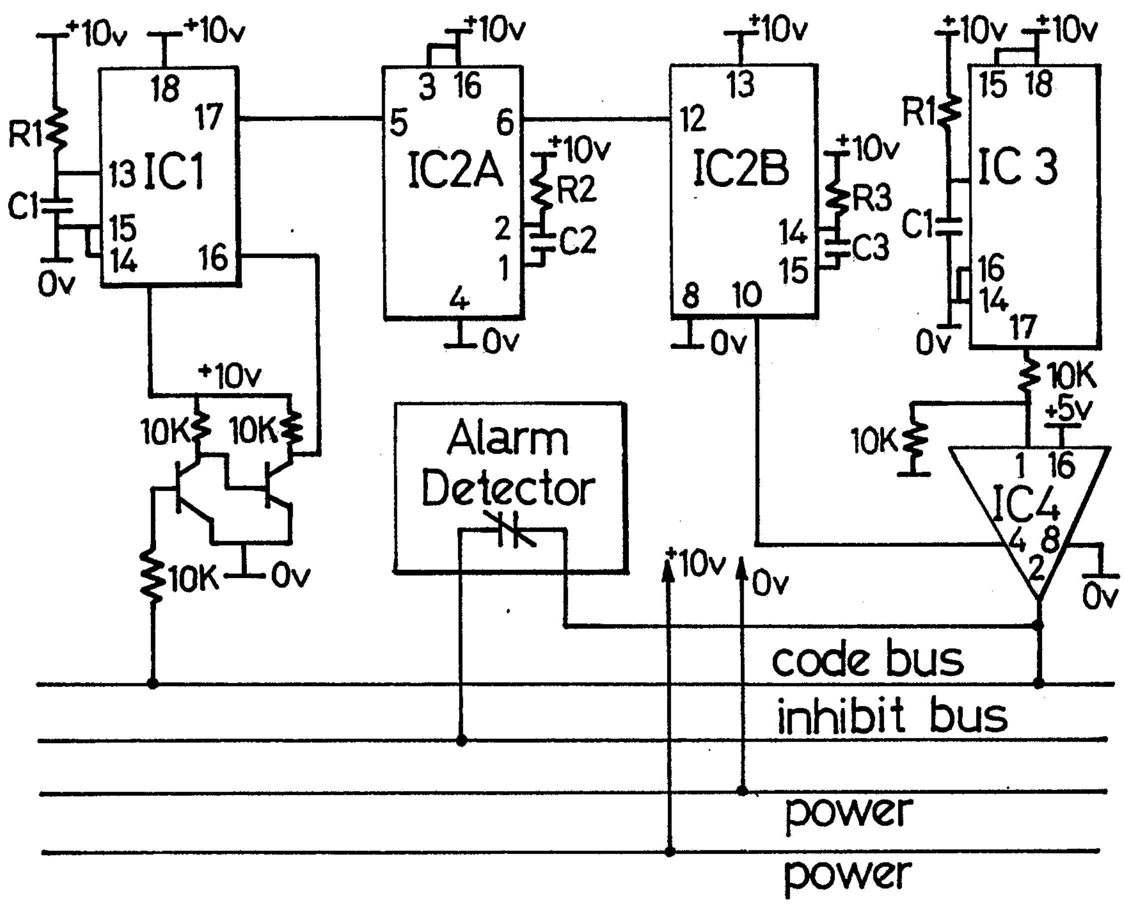
+10v
+10v
R1
C1
0v
18
17
13 IC1
15
14
16
IC2A
3 16
5
6
2
1
4
+10v
R2
C2
0v
IC2B
13
12
14
15
8 10
+10v
R3
C3
0v
IC 3
15 18
R1
C1
16
14
17
0v
10K
+5v
10K
IC4
1 16
4 8
2
0v
+10v
10K
10K
10K
0v
Alarm Detector
+10v
0v
code bus
inhibit bus
power
power

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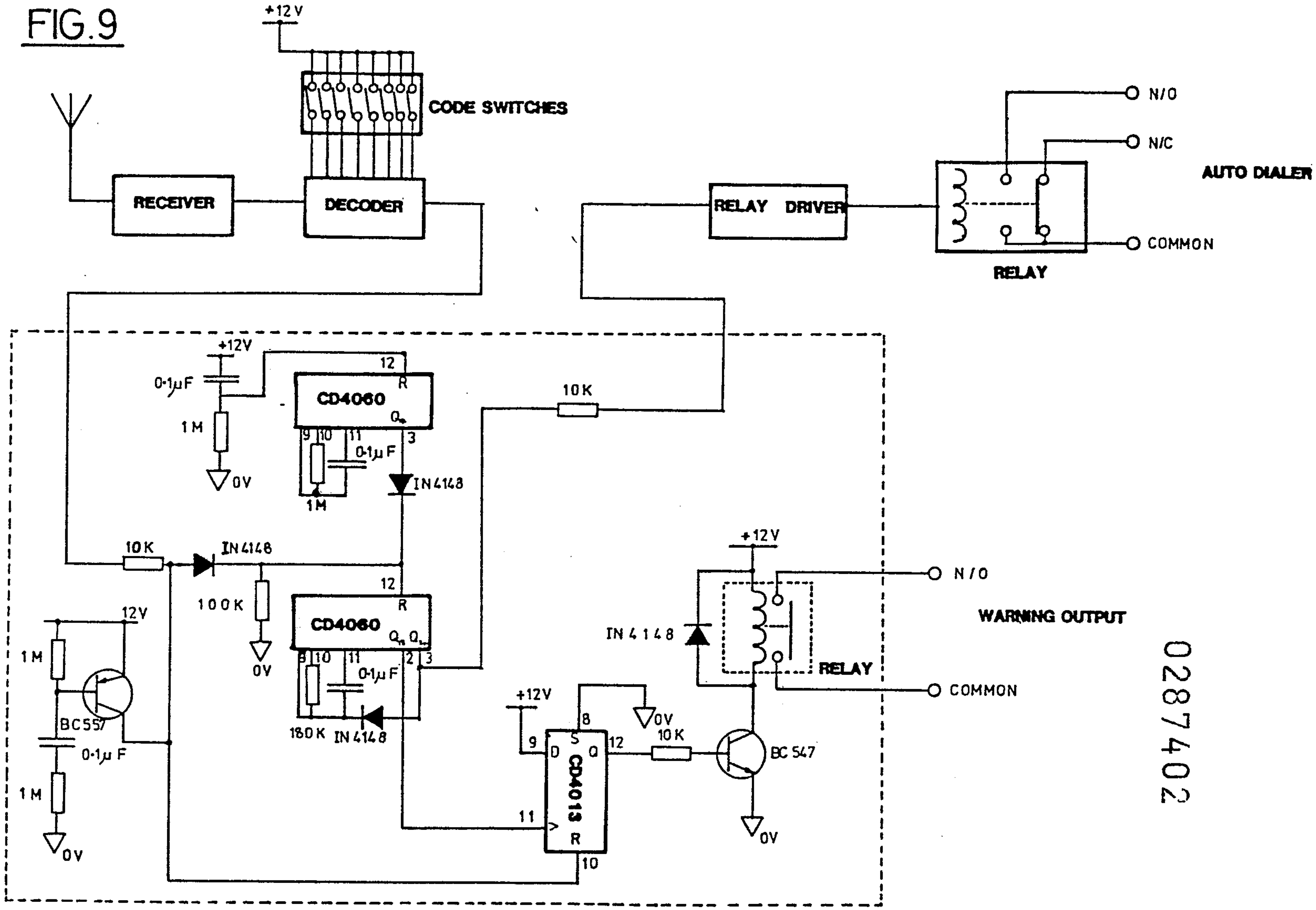
FIG.9



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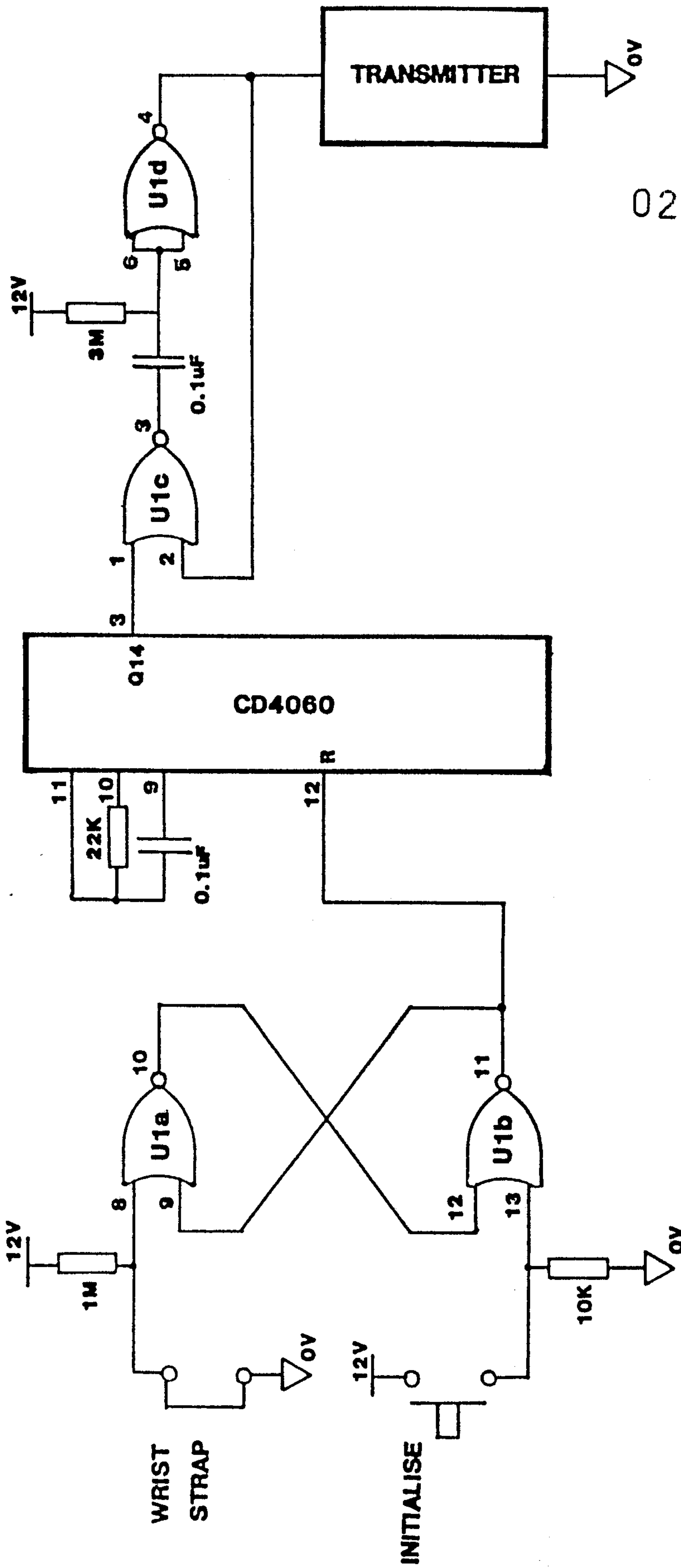

FIG.10