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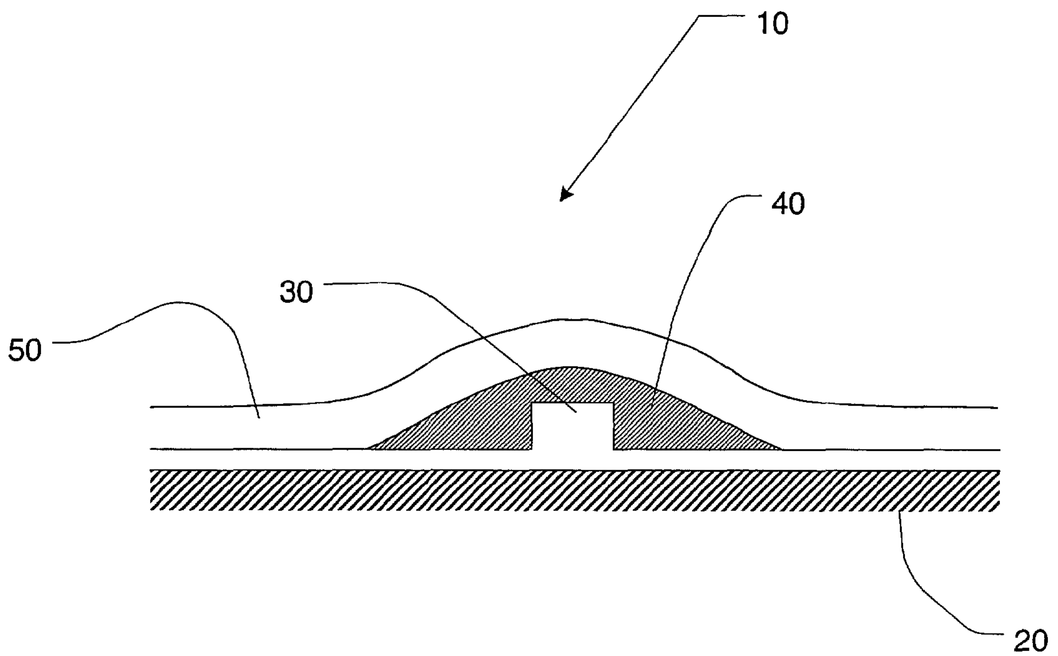
(54) **Title:** OPTICAL WAVEGUIDE CROSSING AND METHOD OF MAKING SAME



(57) **Abstract:** A photonic device (10) including: at least first and second optical waveguides (30, 50); and, a buffer (40) at least partially interposed between the first and second optical waveguides (30, 50) where they at least partially overlie one-another so as to at least partially mitigate interference between optical signals traversing the first and second optical waveguides (30, 50).

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OPTICAL WAVEGUIDE CROSSING AND METHOD OF MAKING SAME

Field of Invention

The present invention relates generally to photonic devices and interconnections, and more particularly to optical waveguides, waveguide crossings and methods for making the same.

Background of the Invention

Waveguide crossings are desirable for use in many photonic devices and Photonic Integrated Circuits (PICs) including III-V semiconductor photonic devices and waveguides, for example. Such circuits and devices may be monolithic in nature. One example of such a PIC or device may take the form of an optical crossconnect including a large number of channel counts wherein a large number of waveguide crossings may exist. Waveguide crossings in the same plane may cause significant loss and crosstalk, seriously limiting the performance of the devices and circuits, as is well understood by those possessing an ordinary skill in the pertinent arts.

Accordingly, it is highly desirable to provide for waveguide crossings that reduce the likelihood of losses and crosstalk resulting from them.

Summary of Invention

A photonic device including: at least first and second optical waveguides; and, a buffer at least partially interposed between the first and second optical waveguides where they at least partially overlie one-another so as to at least partially mitigate interference between optical signals traversing the first and second optical waveguides.

Brief Description of the Figures

Understanding of the present invention will be facilitated by consideration of the following detailed description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings, in which like numerals refer to like parts and in which:

Figure 1 illustrates a cross-section of an optical waveguide crossing structure according to an aspect of the present invention;

Figure 2 illustrates a method being suitable for forming the waveguide crossing structure of Figure 1; and,

Figure 3 illustrates a perspective view of a waveguide and buffer according to an aspect of the present invention.

Detailed Description of the Preferred Embodiments

It is to be understood that the figures and descriptions of the present invention have been simplified to illustrate elements that are relevant for a clear understanding of the present invention, while eliminating, for purposes of clarity, many other elements found in typical optical devices, photonic devices, Photonic Integrated Circuits (PICs) and manufacture methods. Those of ordinary skill in the art will recognize that other elements are desirable and/or required in order to implement the present invention.

However, because such elements are well known in the art, and because they do not facilitate a better understanding of the present invention, a discussion of such elements is not provided herein. The disclosure herein is directed to all such variations and modifications to such devices, PICs and methods known to those skilled in the art.

According to an aspect of the present invention, a three-dimensional (3-D) waveguide crossing may be achieved by forming a substantially smooth buffer layer over at least one waveguide, or set of waveguides, at one or more crossing points. The optical waveguides may include a core having a core refractive index. According to an aspect of the present invention, the buffer layer may include a material having a refractive index operatively lower than the core refractive index.

According to an aspect of the present invention, amorphous silicon (a-Si) materials, including a-Si:H and a-Si:F based alloys such as a-SiC_x where $0<x<1$, a-SiN_y where $0<y<1.33$, a-SiO_z where $0<z<2$ and a-$SiGe_w$ where $0<w<1$, may be utilized to form the waveguides. The waveguides may be deposited using plasma enhanced chemical vapor deposition at a relatively low processing temperature, such as below approximately 300°C or 250°C, as compared to epitaxial growth processes for type III-V semiconductor materials for example. Of course, other suitable materials and methods may also be used.

The buffer layer may be formed using a solution based material. The smooth shape of the buffer can be obtained by photolithography using a grey-scale mask, or actually through surface tension when the solution based material is deposited such as by ink-jet printing. Suitable materials for the buffer include, but are not limited to, standard planarization layer materials used in the IC industry, such as organosilane materials like polymethylsilsesquioxane and polyphenosilsesquioxane, and flowable oxides (FOX), to name a few. Further the buffer layer may take the form of a dielectric layer, using silicon oxide or silicon nitride for example. These materials may be deposited using a suitable technique, such as by plasma deposition, sputtering, spraying, inkjet printing or spin coating for example.

According to an aspect of the present invention, a first waveguide, or set of waveguides, may be formed using a plasma enhanced chemical vapor deposition process, for example. The buffer layer may then be formed over a portion of the first waveguide, or set of waveguides. A second waveguide, or second set of waveguides, may then be deposited over the buffer layer to form a waveguide crossing structure. This waveguide crossing structure may exhibit low loss, low crosstalk crossings of the waveguides.

Referring now to Figure 1, there is shown a non-limiting cross-sectional diagram of a waveguide crossing structure 10 according to an aspect of the present invention. Generally, the waveguide crossing structure 10 includes: substrate 20, waveguide 30, buffer layer 40 and waveguide 50. While waveguides 30, 50 are illustrated to cross one-another at approximately right-angles, such is not necessary. The present invention is equally applicable to any situation where at least one waveguide at least partially overlies another, in a PIC for example.

Substrate 20 may form a base plane for the structure 10. Substrate 20 may take the form of any suitable material, such as silicon (c-Si) or any suitable conventional semiconductor substrate, such as InP, GaAs or GaN, for example. The fabrication and operating characteristics of such substrates are well understood to those possessing an ordinary skill in the pertinent arts.

Waveguides 30, 50 may take any suitable form, such as a rib or ridge waveguide, and be formed of amorphous silicon (a-Si) material, including a-Si:H and a-Si:F based alloys thereof such as a-SiC_x where $0<x<1$, a-SiN_y where $0<y<1.33$, a-SiO_z where $0<z<2$ and a-$SiGe_w$ where $0<w<1$. The operational characteristics of such materials are well understood to include good compatibility with III-V semiconductor materials, low loss and good physical conformability. Further, methods for forming such waveguides are well understood in the pertinent arts, and may include for example RF or DC assisted plasma enhanced chemical vapor deposition, photolithography and etching, for example.

Of course, other materials or methods recognized by those possessing an ordinary skill in the pertinent arts as exhibiting similar characteristics could of course be used as well.

Waveguides 30, 50 may take any suitable shape and dimension. For example, the waveguides 30, 50 may include substantially straight and/or curved portions.

Buffer layer 40 is at least partially interposed between waveguides 30, 50 where they at least partially overlie one-another, such as by crossing, so as to at least partially mitigate losses due to the superposition of waveguides 30,50, including interference, such as crosstalk, between optical signals traversing waveguides 30, 50. Of course, crosstalk generally refers to a disturbance caused by interference.

Buffer layer 40 may form a sufficiently smooth surface profile elevating from the base plane sufficiently gradual such that waveguide 50 is elevated above waveguide 30 where they at least partially overlie, or cross for example, and to at least partially mitigate loss of optical signals traversing waveguide 50 by reason of the elevation. According to an aspect of the present invention, the rate at which the buffer layer 40 expands (in approximate diameter) as compared to its progress in elevation from the base plane (the "aspect ratio") may be approximately 5:1 to approximately 100:1, inclusive.

Referring now also to Figure 3, there is shown a magnified perspective view of a waveguide (such as waveguide 30, Fig. 1) and buffer (such as buffer 40, Fig. 1) according to an aspect of the present invention. The buffer of Figure 3 may be formed using spraying for example.

Referring again to Figure 1, as set forth buffer layer 40 may be formed of organosilane materials like polymethylsilsesquioxane and polyphenosilsesquioxane, flowable oxides (FOX) or dielectric materials such as Silicon oxide and Silicon nitride, for example. According to an aspect of the present invention, due to the inherent characteristics of such materials, buffer layer 40 provides desirable shielding effects for the waveguides 30, 50 where they at least partially overlie, e.g., cross, thereby mitigating otherwise potentially deleterious loss and cross-talk effects as will be readily understood by those possessing an ordinary skill in the pertinent arts. Of course, other materials exhibiting analogous characteristics to such materials may also be used, provided of course they are analogously compatible with suitable processing methodologies used to form the waveguides 30,50, for example.

According to an aspect of the present invention, one or more waveguides 50 may be elevated above one or more waveguides 30 by a single buffer layer 40. That is, a plurality of waveguides 50 may be elevated so as to cross-over a single waveguide 30, or plurality of waveguides 30, by buffer 40. Or, a single waveguide 50 may be elevated so as to cross-over a single waveguide 30, or plurality of waveguides 30, by buffer 40.

Referring now also to Figure 2, there is shown a method 100 being suitable forming the waveguide crossing structure 10 of Figure 1. Method 100 generally includes forming 110 waveguide 30 on substrate 20; forming 120 buffer 40 over waveguide 30; and forming 130 waveguide 50 over buffer 40.

Waveguide 30 may be formed 110 using any conventional method known to those possessing an ordinary skill in the pertinent arts. Suitable methods may include conventional plasma enhanced chemical vapor deposition of a-Si material, for example. For example, waveguide 30 may take the form of an a-Si alloy material layer having a refractive index of approximately 3.4 deposited upon an a-Si alloy material under-cladding layer having a refractive index of approximately 3.2 in turn deposited on a c-

Si wafer. The a-Si alloy undercladding layer may be approximately 1 μm thick, while the a-Si alloy core may be approximately 0.5 μm thick. An a-Si alloy material layer having a refractive index of approximately 3.2 may be provided as an overcladding layer, and have a thickness of approximately 1 μm for example. The a-Si alloy under- and overcladding may be formed using RF or DC plasma assisted decomposition of SiH_4 and N_2, for example. In the case of N_2, an N_2 to SiH_4 flow ratio of approximately 0.9 may be used while the substrate temperature is held at approximately 250°C. To form the a-Si alloy core layer, the N_2 to SiH_4 flow ratio may be approximately 0.45, while the substrate temperature is held at approximately 250°C. Processing pressure may be approximately 1.5 torr, while the 13.56-MHz RF power is held approximately at 50 W, for example.

Buffer layer 40 may be formed 120 over waveguide 30 prior to formation of waveguide 50, by inkjet printing of the buffer layer material, for example. Spraying of or spin coating of the buffer layer 40 material may also be used, optionally in conjunction with a subsequent patterning process to remove unwanted buffer layer 40 material, such as material not sufficiently adjacent to the crossing area to serve to elevate waveguide 50 where it at least partially overlaps waveguide 30, for example. Further, a layer of suitable buffer layer material, such as a dielectric material like Silicon oxide or Silicon nitride, may be deposited or spun over waveguide 30. This deposited layer of suitable material may be selectively removed, using a conventional graded index or grey-scale mask and etching for example, to form buffer 40 as will be readily understood by those possessing an ordinary skill in the pertinent arts.

Waveguide 50 may be formed 130 analogously to waveguide 30. Waveguides 30, 50 may be deposited at a relatively low processing temperature, such as below approximately 300 °C or 250 °C, as compared to epitaxial growth processes for III-V semiconductor materials.

It will be apparent to those skilled in the art that various modifications and variations may be made in the apparatus and process of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modification and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

What is claimed is:

1. A photonic device comprising:

at least first and second optical waveguides; and,

a buffer at least partially interposed between said first and second optical waveguides where they at least partially overlie one-another so as to at least partially mitigate interference between optical signals traversing said first and second optical waveguides.

2. The device of Claim 1, wherein said waveguides comprise at least one amorphous silicon material.

3. The device of Claim 2, wherein said amorphous silicon material comprises at least one material selected from the group consisting essentially of: a-Si:H and a-Si:F based alloys.

4. The device of Claim 2, wherein said amorphous silicon material comprises at least one material selected from the group consisting essentially of hydrogenated or fluorinated: a-SiC_x where $0<x<1$, a-SiN_y where $0<y<1.33$, a-SiO_z where $0<z<2$ and a-$SiGe_w$ where $0<w<1$.

5. The device of Claim 1, wherein:

each of said optical waveguides comprises a core having a core refractive index; and,

said buffer comprises a material having a refractive index operatively lower than said core refractive index.

6. The device of Claim 1, wherein said buffer comprises at least one material selected from the group consisting essentially of: at least one dielectric material, at least one organosilane material and at least one flowable oxide.

7. The device of Claim 1, wherein said buffer elevates said second of said optical waveguides with respect to said first of said optical waveguides, wherein said elevation is sufficiently gradual to at least partially mitigate loss of said optical signals traversing said second optical waveguide due to said elevation.

8 A method for making a photonic integrated circuit, said method comprising:

forming a first optical waveguide;

forming a buffer over at least a portion of said first optical waveguide; and,

forming a second optical waveguide over at least a portion of said buffer;

wherein, said buffer is adapted to at least partially mitigate interference between optical signals traversing said first and second optical waveguides.

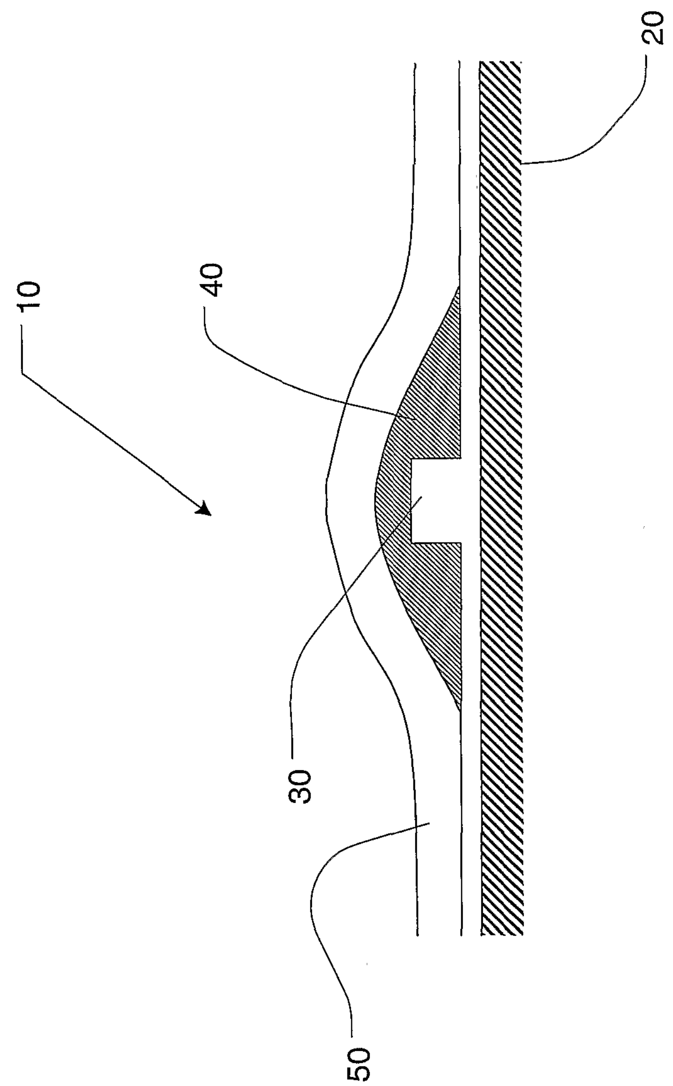
9. The method of Claim 8, wherein each of said optical waveguides comprises a core having a core refractive index, and forming said buffer comprises using a material having a refractive index lower than said core refractive index.

10. The method of Claim 9, wherein said forming said buffer comprises forming a layer using said material having a refractive index lower than said core refractive index and removing a portion of said formed layer using a grey scale mask.

11. The method of Claim 8, wherein said forming said buffer comprises inkjet printing said buffer.

12. The method of Claim 8, wherein said forming said buffer comprises spraying said buffer.

Figure 1



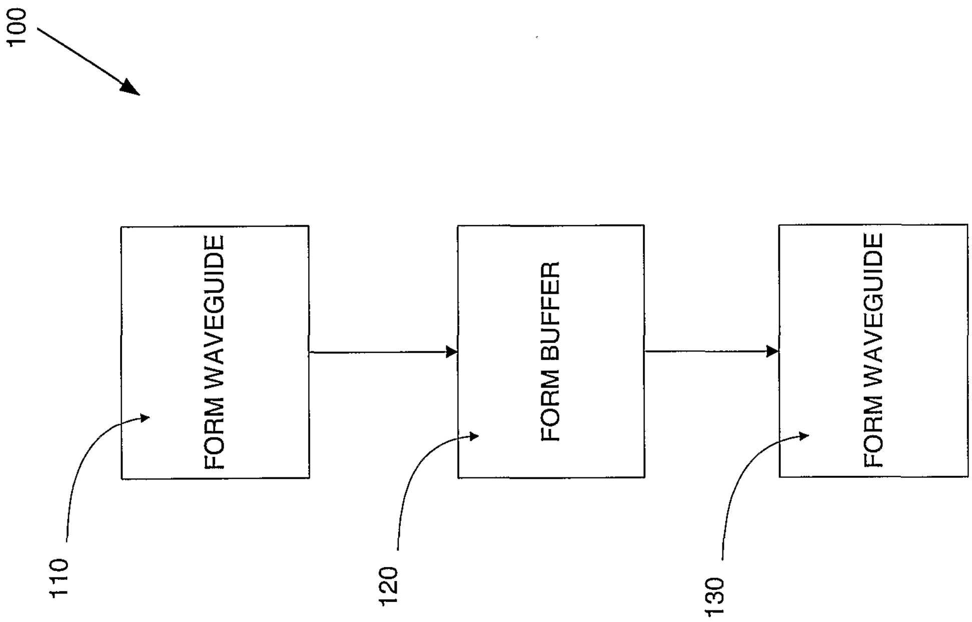


Figure 2

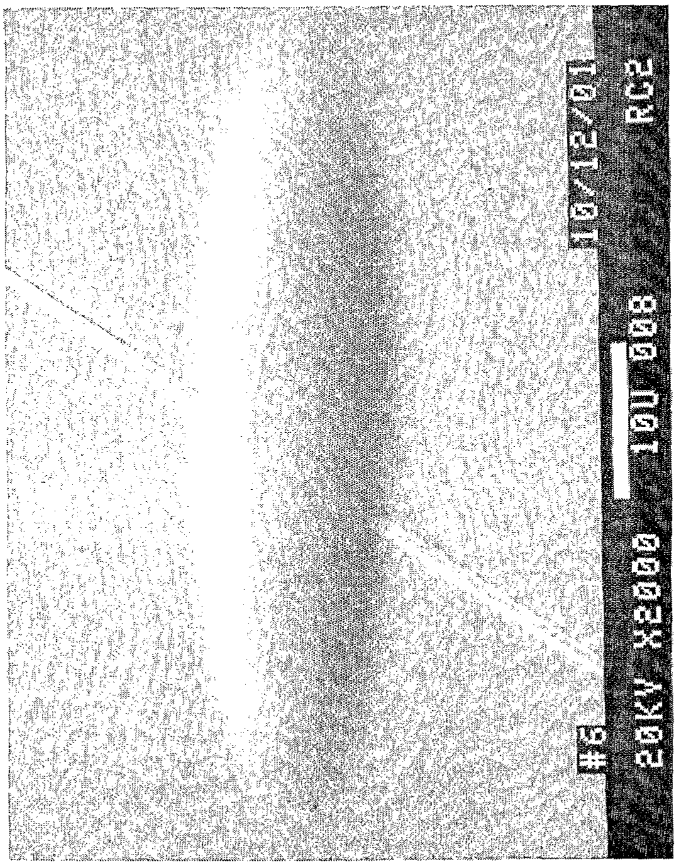


Figure 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/15035

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G02B 06/10,06/12
US CL : 385/14, 129
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 385/14,129,130,131,132

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3,663,194 A (GREENSTEIN et al) 16 May 1972 (16.05.1972), see entire document.	1 and 8
X --- Y	US 4,120,588 A (CHAUM) 17 October 1978 (17.10.1978), see entire document, especially Figures 4 and 5.	1 and 5-12 --- 2 and 3
A	US 4,521,443 A (NAIK et al) 04 June 1985 (04.06.1985), see entire document.	1-4
A	US 4,695,122 A (ISHIDA et al) 22 September 1987 (22.09.1987), see entire document.	1-4
X --- Y	US 5,636,298 A (JIANG et al) 03 June 1997 (03.06.1997), see entire document.	1, 5, 6, 8 and 9 --- 2 and 3
Y	US 6,108,464 A (FORESI et al) 22 August 2000 (22.08.2000), see entire document.	2 and 3
X, E	US 2002/0097942 A1 (HAMILTON) 25 July 2002 (25.07.2002), see entire document.	1 and 8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 July 2002 (26.07.2002)	23 SEP 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Akm Ullah Telephone No. 703-308-0956

Continuation of B. FIELDS SEARCHED Item 3:
USPTO EAST:
search terms: optical waveguide, amorphous silicon, remove, grey scale mask, dielectric, reduce, minimize, loss, cross-talk, buffer layer