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(54) Title: STRUCTURES AND DESIGNS FOR IMPROVED EFFICIENCY AND REDUCED STRAIN III-NITRIDE HETEROSTRUCTURE SEMICONDUCTOR DEVICES

(57) Abstract: The present invention provides semiconductor structures, and methods for making semiconductor structures, comprising an InAlN and/or InAlGaN strain relief layer that have a lattice constant larger than that of a substrate film upon which it is grown such that it allows the growth of strain-free or low-strain semiconductor devices.

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**STRUCTURES AND DESIGNS FOR IMPROVED EFFICIENCY AND REDUCED  
STRAIN III-NITRIDE HETEROSTRUCTURE SEMICONDUCTOR DEVICES**

5

CROSS REFERENCE

This application claims priority to U.S. Provisional patent application serial number 60,779,691 filed March 6, 2006, which is incorporated by reference herein in its entirety.

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FIELD OF THE INVENTION

This invention relates to wide-bandgap nitride materials, and more particularly, to design and growth of InGaN/InAlN/GaN heterostructures.

BACKGROUND OF THE INVENTION

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Wide bandgap nitride-based compound semiconductors, such as those formed from the group III elements Indium (In), Gallium (Ga) and Aluminum (Al) and the group V element Nitrogen (N) have applications in electronics such as high power transistors or the like and in optoelectronics, including devices such as lasers, light-emitting diodes (LEDs), photodetectors, modulators, waveguides, or other optoelectronic devices that can generate, absorb or manipulate a light signal. Of materials from the (In,Ga,Al)(N) (or III-N) family, the ternary compound InGaN is used as a light-processing region (such as an active region for an LED or a laser) for a wide variety of visible light emitting devices, including, but not limited to, LEDs and lasers. The bandgap of this material can be tuned to vary from approximately 0.7 eV to approximately 3.4 eV. Thus

InGaN based optoelectronic devices have the ability to generate, detect or manipulate light across the entire visible wavelength region of the optical spectrum. InGaN-based light emitting diodes have been demonstrated over the entire visible wavelength region. For examples of InGaN LEDs, see T. Mukai, M. Yamada, and S. Nakamura, in Jpn. J. Appl. Phys. Part 1, 38, 3976 (1999), incorporated herein by reference, Laser diodes have been demonstrated in the violet to blue region of the spectrum. For examples of nitride based laser diodes in the violet and blue wavelength ranges, see S. Nagahama, T. Yanamoto, M. Sano, and T. Mukai, Jpn. J. Appl. Phys. Part 1 40, 3075 (2001), incorporated herein by reference.

One important target application for these materials is in the fabrication of green laser diodes emitting light in the green wavelength range of the optical spectrum. In order to reach this wavelength range, it is necessary to grow  $\text{In}_x\text{Ga}_{1-x}\text{N}$  with an Indium fraction of  $x > 0.15$ . However, there are problems associated with the growth of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  with  $x > 0.15$  and these problems have made it difficult to achieve sufficiently high quality material required for laser diode applications in this wavelength range.

A problem with the growth of, for example, InGaN/GaN heterostructures is the large lattice mismatch (up to 11%) between InGaN and GaN, due to the different lattice constants of GaN and InN, and hence InGaN alloys. As the In content of an InGaN layer increases, the lattice mismatch between the layer and a GaN layer upon which it is deposited increases, and hence strain increase. For typical compositions required for green laser diodes, the lattice mismatch can be as high as 4%. Strain has two effects on the InGaN layer. Firstly, large biaxial strain limits the thickness of InGaN which can be grown pseudomorphically, or

defect-free, making it difficult to grow InGaN layers of a practical thickness and crystal quality to have sufficient gain for light emission. Lattice-mismatch induced strain defines a critical thickness of growth for an InGaN layer, 5 beyond which pseudomorphic growth of a smooth layer of material is not possible. Strain-accumulation in a layer can provide sufficient energy such that the layer grows non-pseudomorphically, and hence defects can be introduced into the layer. These defects act as non-radiative recombination 10 centers, reducing the luminescence of the material and hence reducing the optical quality of the InGaN material such that the material is not suitable for optoelectronic devices. Strain also impacts electronic properties of layers. Surface and interface roughness and defects introduced into a layer 15 can introduce carrier scattering and carrier traps that reduce the carrier mobility within a layer. Secondly, due to strong piezoelectric polarization in these materials, the strain introduces internal electric fields across the quantum well, resulting in reduced luminescence efficiency.

20 It is therefore desirable to grow InGaN, and other Group III-N-based semiconductor devices, under relaxed conditions in order to realize a laser diode with, for example, true green-wavelength-range emission. Until now, there have been no successful attempts at growing strain-free InGaN QWs. 25

It would be highly advantageous, therefore, to remedy the foregoing and other deficiencies inherent in the prior art.

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#### SUMMARY OF THE INVENTION

The present invention overcomes limitations of the prior art by providing an InAlN and/or InAlGaN strain relief layer that have a lattice constant larger than that of a

substrate film upon which it is grown such that it allows the growth of strain-free or low-strain Group III-N materials with a composition suitable for optoelectronic devices.

5 Thus, in one aspect, the present invention provides semiconductor structures comprising:

(a) a substrate;

(b) a substrate film overlaying the substrate;

(c) a strain relief layer overlaying the substrate  
10 film, wherein the strain relief layer comprises InAlN and/or InAlGaN; and

(d) a Group III-N layer overlaying the strain relief layer, wherein the Group III-N layer possesses a lattice constant greater than a lattice constant of the substrate  
15 film;

wherein the strain relief layer provides a transition from the smaller lattice constant of the substrate film to the larger lattice constant of the Group III-N layer.

In various further embodiments, the strain relief layer  
20 comprises  $\text{In}_y\text{Al}_{1-y}\text{N}$ , wherein  $y$  is at least 0.2; 0.3; 0.4; or wherein  $0.4 \leq y \leq 0.6$ ;  $0.50 \leq y \leq 0.60$ ; or wherein  $0.6 \leq y \leq 1.0$ .

In various further embodiments, the substrate is selected from the group consisting of substrates comprising sapphire, silicon carbide, silicon, bulk nitrides including  
25 gallium nitride and aluminum nitride, zirconium diboride, and binary III-V compounds including but not limited to indium phosphide, indium arsenide, gallium arsenide, aluminum nitride, and alloys thereof, including but not limited to AlGaN, AlInGaN.

30 In various further embodiments, the Group III-N layer comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}$ ; in further embodiments, the Group III-N layer comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}$  wherein  $0.28 \leq x \leq 0.60$ ;  $0.28 \leq x \leq 0.52$ ;  $0.4 < x < 0.5$ ; or wherein  $0.6 \leq x \leq 1.0$ .

In further embodiments, the strain relief layer comprises multiple layers with different InAlN and/or InAlGaN compositions. In these embodiments, the strain relief layer may be approximately lattice matched to the substrate film at a substrate film-strain relief layer interface, and is approximately lattice matched to the Group III-N layer at a Group III-N layer-strain relief layer interface.

In various further embodiments, the semiconductor structure comprises a plurality of strain relief layers and active layers. In these embodiments, the semiconductor structure may be suitable for use in an optoelectronic device that provides one or more of light emission, light absorption, light modulation, and waveguiding. The semiconductor structure may further comprise one or more of a digital alloy superlattice, an edge emitting laser, a band-edge alignment, a vertical-cavity surface-emitting laser, a quantum cascade laser, a light emitting diode, and a quantum well. In further embodiments where the semiconductor structure comprises a quantum well structure, the quantum well structure may be suitable optoelectronic devices including but not limited to green, yellow, red, infra-red, violet, blue, and UV optoelectronic devices.

In another aspect, the present invention provides methods for making the semiconductor structures of the invention. In one embodiment, the methods comprise

(a) depositing a substrate film on a substrate;

(b) depositing a strain relief layer over the substrate film, wherein the strain relief layer comprises InAlN and/or InAlGaN; and

(c) depositing a Group III-N layer over the strain relief layer, wherein the Group III-N layer possesses a

lattice constant greater than a lattice constant of the substrate film;

wherein the strain relief layer provides a transition from the smaller lattice constant of the substrate film to  
5 the larger lattice constant of the Group III-N layer.

It is an object of the present invention to provide strain-free or low-strain InGaN quantum wells that can be used in optoelectronic devices operating at, for example,  
10 the green-wavelength range.

It is another object of the present invention to provide a method for growing quantum well structures suitable, for example, for green-wavelength operation of optoelectronic devices.

15 It is a further object of the present invention to provide improved crystalline quality of strain relief layers and quantum well layers used for operation of optoelectronic devices.

It is yet another embodiment of the present invention  
20 to increase the internal quantum efficiency of InGaN quantum wells.

#### BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a graph showing direct bandgap energy versus  
25 the lattice constant for group III-nitride semiconductors formed using (In,Ga,Al) (N);

FIG. 2 is a schematic cross-section of a prior-art InGaN quantum well structure;

FIG. 3 is a schematic cross-section of a quantum well  
30 structure, in accordance with the present invention;

FIG. 4 is another schematic cross-section of a quantum well structure, in accordance with the present invention;

FIG. 5 is yet another schematic cross-section of a quantum well structure, in accordance with the present invention;

FIG. 6 is a schematic cross-section of a strain relief layer formed using a digital alloy superlattice, in accordance with the present invention;

FIG. 7 is a sectional view of an edge emitting laser, formed in accordance with the present invention;

FIG. 8 is a schematic band-edge alignment of a semiconductor device formed in accordance with the present invention;

FIG. 9 is a calculated phase diagram for an InAlN/GaN film for different film thicknesses;

#### 15 DETAILED DESCRIPTION OF THE INVENTION

In one aspect, the present invention provides semiconductor structures comprising:

- (a) a substrate;
- (b) a substrate film overlaying the substrate;
- 20 (c) a strain relief layer overlaying the substrate film, wherein the strain relief layer comprises InAlN and/or InAlGa<sub>N</sub>; and
- (d) a Group III-N layer overlaying the strain relief layer, wherein the Group III-N layer possesses a lattice constant greater than a lattice constant of the substrate film layer;

wherein the strain relief layer provides a transition from the smaller lattice constant of the substrate film to the larger lattice constant of the Group III-N layer.

30 The present invention provides semiconductor structures, and methods for making semiconductor structures, comprising an InAlN and/or InAlGa<sub>N</sub> strain relief layer that have a lattice constant larger than that of a substrate film



upon which it is grown such that it allows the growth of strain-free, low-strain, and reduced-strain devices with a composition suitable for use in, for example, optoelectronic devices.

5           As will be apparent to those of skill in the art, the semiconductor structures may contain any other layers and features, including but not limited to those embodiments disclosed herein, to provide the desired properties of a resulting semiconductor device.

10           Any suitable method for making the alloys of the invention, including InAlN and/or InAlGaN, can be used, including methods disclosed in Hums et al., Applied Physics Letters 90, 022105 (2007); and Terashima et al., Japanese Journal of Applied Physics, 45(21):L539-L542 (2006)).

15           Any substrate suitable for use in a semiconductor structure can be used in the present invention, including but not limited to sapphire, silicon carbide, silicon, gallium nitride, aluminum nitride, zirconium diboride, and binary III-V compounds including but not limited to indium  
20 phosphide, indium arsenide, gallium arsenide, aluminum nitride, and alloys thereof, including but not limited to AlGaN, AlInGaN. It is within the level of skill in the art to select an appropriate substrate for use in the present invention.

25           The substrate film comprises or consists of GaN. In various embodiments, the substrate film may consist of GaN, or may be alloyed to include 5%, 4%, 3%, 2%, 1%, or less of a suitable group III element, including but not limited to aluminum or indium. Furthermore, the substrate film can be  
30 doped (e.g., silicon, magnesium, etc.) to provide additional desired features. The substrate film can be grown on any orientation, including the c-axis, a-axis or any other practical axis, either polar or non-polar. In all of these

embodiments, the substrate film has a lattice constant that is less than the lattice constant of the Group III-N layer. The substrate film may be grown on the substrate with a buffer layer (ie: it is not required that the substrate film  
5 directly contact the substrate).

The strain relief layer comprises one or more layers between a substrate film and a Group III-N layer to provide a transition from a smaller lattice constant of the substrate film to the larger lattice constant of the Group  
10 III-N layer. While a single, uniform film of InAlN on GaN may not be lattice matched at an InAlN/GaN interface, the device will be lattice matched at the Group III-N layer/strain relief layer interface.

As discussed in more detail below, a strain relief  
15 layer may comprise multiple layers, wherein different layers have different or the same InAlN and/or InAlGaN compositions. Such layers may comprise a two or more graded layers; superlattices, etc. in which different layers have different InAlN or InAlGaN alloys (ie: different percentages  
20 of In, Al, Ga, and N in different layers); this does not require that each graded layer is different, although they can each be different. The semiconductor structures of the invention can comprise multiple such strain relief layers, as described in more detail below.

As is known to those of skill in the art, a lattice  
25 constant is a measure of the structural compatibility between different materials; when the lattice constants differ, strains are introduced into the layer, inhibiting epitaxial growth. Thus, the strain relief layer is chosen so  
30 that it is approximately lattice-matched to the active layer of interest

The Group III-N layer comprises or consists of any suitable combination of Group III atoms and nitrogen,

including but not limited to InN, GaN, AlN, InGaN, InAlN, GaAlN, and InGaAlN. The Group III-N layer is the interface with the strain relief layer, and is considered a portion of the semiconductor device, where "device" is defined as the active portion(s) of the semiconductor structure. Thus, the device may include additional layers that overlay the Group III-N layer, which can grow strain free, low strain, or reduced strain through use of the strain relief layer. The Group III-N layer may comprise any type of device layer, including but not limited to conductive layers, cladding layers, etc., as described in more detail below. Specific additional device layers for use in a given semiconductor structure will depend on the purpose for which the semiconductor structure is designed.

In one non-limiting example, the "device" for a laser structure may comprise or consist of the following layers:

- a. Conductive layers: n- and p-type III-nitride film, on either end of the device. These layers are responsible for carrying electrons and holes into the "active region". They may comprise or consist of doped InAlN or InAlGaN, and may be lattice matched to the strain relief layer.
- b. Cladding layers: This is a region of lower refractive index that is present on either side of the optical confinement layer. This may comprise or consist of InAlN or InAlGaN, and may be lattice matched to the strain relief layer. (InAlN or InAlGaN have a lower refractive index than InGaN)
- c. Optical confinement layers: this is a region of higher refractive index on either side of the carrier confinement region. This can comprise or consist of InGaN (or InAlGaN of a lower bandgap than the cladding layer) (The refractive index is smaller for a wider bandgap material. A smaller bandgap material has a higher refractive index). The thickness of this layer may, for example, be roughly equal to the wavelength of the light emitted, in the medium within which it is confined. For green lasers, where the light is confined in a group III-N medium, the wavelength

and therefore the width of the optical confinement layer may be approximately 150-200 nm.

5 d. Carrier confinement layers: This is a layer of intermediate bandgap between the conductive layer and the quantum wells. The bandgap may be the same as that of the optical confinement layer or it may be slightly lower. The width is typically 30 nm and its purpose is to localize carriers on either side of the quantum wells.

10 e. Quantum wells and barriers: A series of thin layers with alternately high and low bandgaps, where carriers are localized and light is emitted. In one embodiment, these comprise or consist of InGaN.

15 The carrier confinement layers and the quantum wells together can be called the "active region" of the device.

Further examples are provided below.

In various embodiments, the strain relief layer  
20 comprises  $\text{In}_y\text{Al}_{1-y}\text{N}$ , wherein  $y$  is at least 0.2; 0.3; or 0.4; or wherein  $0.4 \leq y \leq 0.6$ ;  $0.50 \leq y \leq 0.60$ ; or wherein  $0.6 \leq y \leq 1.0$ .

For example, where the goal is to develop a green or yellow wavelength-operation optoelectronic device, the strain relief layer may comprise  $\text{In}_y\text{Al}_{1-y}\text{N}$ , wherein  
25  $0.4 \leq y \leq 0.6$ ; and a Group III-N layer may comprise  $\text{In}_x\text{Ga}_{1-x}\text{N}$  wherein  $0.28 \leq x \leq 0.52$ . When the goal is to develop an infrared-operation optoelectronic device, the strain relief layer may comprise  $\text{In}_y\text{Al}_{1-y}\text{N}$ , wherein  $0.68 \leq y \leq 1.0$ , and a Group III-N layer may comprise  $\text{In}_x\text{Ga}_{1-x}\text{N}$  wherein  $0.6 \leq x \leq 1.0$ .

30 Based on the teachings herein, those of skill in the art will be able to design semiconductor structures with strain layers comprising or consisting of InAlGaN. For example, where the goal is to develop a green or yellow wavelength-operation optoelectronic device, and a Group III-  
35 N layer chosen is  $\text{In}_x\text{Ga}_{1-x}\text{N}$ , with  $x = 0.42$  (and where an  $\text{In}_y\text{Al}_{1-y}\text{N}$  strain relief layer could have a composition wherein  $y = 0.52$ ) then an exemplary composition for

In<sub>x</sub>Al<sub>y</sub>Ga<sub>1-x-y</sub>N strain relief layer is  $x = 0.46$ ,  $y = 0.22$ , which provides approximate lattice matching to the Group III-N layer. As will be apparent to those of skill in the art, other InAlGaN strain relief layer compositions can also be used to produce the desired semiconductor structures.

In further embodiments, the strain relief layer comprises multiple layers with different InAlN and/or InAlGaN compositions. In these embodiments, the strain relief layer may be approximately lattice matched to the substrate film at a substrate film-strain relief layer interface, and is approximately lattice matched to the Group III-N layer at an Group III-N layer-strain relief layer interface.

In various further embodiments, the Group III-N layer comprises In<sub>x</sub>Ga<sub>1-x</sub>N; in further embodiments, Group III-N layer comprises In<sub>x</sub>Ga<sub>1-x</sub>N wherein  $0.28 \leq x \leq 0.60$  (for example, for green, yellow, or red wavelength-operation optoelectronic devices);  $0.4 < x < 0.5$  (preferred for green wavelength devices); or wherein  $0.6 \leq x \leq 1.0$  for example, for infrared wavelength-operation optoelectronic devices. Based on the teachings herein, those of skill in the art can determine appropriate compositions for other Group III-N layers, depending on the desired optoelectronic device.

In various further embodiments, the semiconductor structure comprises a plurality (e.g., 2 or more) of strain relief layers and Group III-N layers. As will be understood by those of skill in the art, the further layers can be arranged as desired for a given purpose, and examples are provided in more detail below. In these embodiments, the semiconductor structure may be suitable for use in an optoelectronic device that provides one or more of light emission, light absorption, light modulation, and waveguiding. The semiconductor structure may further

comprise one or more of a digital alloy superlattice, an edge emitting laser, a band-edge alignment, a vertical-cavity surface-emitting laser, a quantum cascade laser, a light emitting diode, and a quantum well. In further embodiments  
5 where the semiconductor structure comprises a quantum well structure, the quantum well structure may be suitable for green, yellow, blue, red, violet, infrared, and UV-wavelength operation of optoelectronic devices

Furthermore, the strain relaxation structures disclosed  
10 herein may also be used in other electronic devices comprising Group III-N layers, including but not limited to heterostructure field effect transistors (HFET) and heterojunction bipolar transistors. An HFET is a field effect transistor with a heterojunction as the channel  
15 instead of an n-doped region. Thus, in this aspect, the heterojunction comprises the semiconductor structure as disclosed for any of the above embodiments (ie: substrate film, strain relief layer; Group III-N layer). The resulting HFETs can be discrete transistors, or may be part  
20 of an integrated circuit, such as a monolithic microwave integrated circuit. The HFETs can be used, for example, in cell phones and other communication devices, DBS receivers, electronic warfare systems (including but not limited to radar systems), and in radio astronomy. Heterojunction  
25 bipolar transistors can be used, for example, in ultra-fast circuits such as radio frequency systems.

In another aspect, the present invention provides methods for making the semiconductor substrates of the invention. In one embodiment, the methods comprise

- 30 (a) depositing a substrate film on a substrate;  
(b) depositing a strain relief layer over the substrate film, wherein the strain relief layer comprises InAlN and/or InAlGa<sub>1-x</sub>N; and

(c) depositing a Group III-N layer over the strain relief layer, wherein the active Group III-N layer possesses a lattice constant greater than a lattice constant of the substrate film;

5 wherein the strain relief layer provides a transition from the smaller lattice constant of the substrate film to the larger lattice constant of the Group III-N layer.

Various further embodiments of the methods are as disclosed above (in referring to specific embodiments of the  
10 substrate, layers, etc.) and below. Deposition of the semiconductor device layers can be by any suitable technique, including but not limited to molecular beam epitaxy (MBE) and metal-organo chemical vapor deposition (MOCVD), or any similar technique well known by those  
15 skilled in the art.

Turning to the exemplary embodiments as shown in the figures, FIG. 1 shows a plot of the bandgap energy versus the lattice constant for III-nitride semiconductors. These  
20 materials are used to realize electronic and optoelectronic devices. As can be appreciated by those skilled in the art, optoelectronic devices include devices that provide light emission, light absorption, light modulation, or other light manipulation, such as waveguiding and the like.

25 At typical compositions of InGaN required for green wavelength operation of optoelectronic devices such as laser diodes, the bandgap of the InGaN alloy is approximately 2.2 eV, with a lattice constant of approximately 3.34 Å. Therefore the lattice mismatch of a strained InGaN quantum  
30 well (QW) with respect to a GaN substrate film is approximately 4.6%. In order to grow an InGaN layer such as a QW, with the required Indium composition to realize a true green-wavelength-range emission laser diode, it is therefore

important to grow InGaN under relaxed or low-strain conditions. Until now, there have been no successful attempts at growing strain-free InGaN QWs.

To overcome the prior art limitations of design and growth of, for example, green-wavelength-range optoelectronic devices, an  $\text{In}_y\text{Al}_{1-y}\text{N}$  strain relief layer can be introduced between a GaN substrate film and an InGaN layer such as a QW layer. To the first order, at approximately  $y = 0.52$ , an  $\text{In}_y\text{Al}_{1-y}\text{N}$  strain relief is approximately lattice matched with an  $\text{In}_x\text{Ga}_{1-x}\text{N}$  active layer at  $x = 0.42$ . However, the  $\text{In}_y\text{Al}_{1-y}\text{N}$  strain relief has a bandgap energy approximately the same as the bandgap energy of GaN. Consequently, the active region of a laser diode or other optoelectronic device that includes an  $\text{In}_x\text{Ga}_{1-x}\text{N}$  active layer and a  $\text{In}_y\text{Al}_{1-y}\text{N}$  strain relief should have a good band offset with respect to the cladding layers. The band offset provides sufficient carrier confinement to allow the required radiative efficiency for optoelectronic devices. Furthermore, a sufficient refractive index contrast is provided for good optical confinement and waveguiding. A principal advantage of using this method is that a strain-free or low strain quantum well, approximately lattice matched to the cladding layers can be obtained without sacrificing carrier confinement and refractive index contrast. Also, lattice mismatch is transferred from the well-barrier interface to the InAlN/GaN interface. Any defects introduced due to the lattice mismatch are not within the well, but outside, enabling a higher quality InGaN quantum well.

Several researchers have developed  $\text{In}_y\text{Al}_{1-y}\text{N}$  layers, with In content of around  $y=0.17$ . See, for example J.-F. Carlin and M. Ilegems, in Appl. Phys. Lett. 83, 668 (2003) (the Carlin paper), incorporated by reference herein, grew



In<sub>y</sub>Al<sub>1-y</sub>N distributed Bragg reflectors (DBRs) lattice matched to a GaN barrier at  $y = 0.17$ , yielding a refractive index contrast of  $>7\%$ . However these compositions are unsuitable for providing lattice matching to InGaN with the required  
5 compositions for use in, for example, blue or longer wavelength light emitting devices. An example of higher In-content InAlN layers is described by Jmerik et al., in Phys. Stat. Sol, No. 7, 2846-2850 (2003), herein incorporated by reference. However, this reference discloses use of InAlN  
10 layers as a buffer layer to grow InN directly on sapphire, and thus significantly differs from the present invention.

FIG. 2 shows a simplified prior art QW structure 10'. A GaN substrate film 14' is deposited on a substrate 12' such as sapphire or the like. GaN substrate film 14' may also be  
15 grown on substrate 12' via a buffer layer (not shown), or on a patterned substrate such as an epitaxial lateral overgrowth (ELOG) substrate, or the like. An InGaN QW 16' is then deposited on layer 14' and a second GaN layer 18' is deposited on InGaN QW layer 16' to form a QW  
20 heterostructure. FIG. 2 shows one QW only, and it will be understood that more than one QW structure can also be used. Additional layers such as conductive layers, metallization and the like, used in real devices are not shown.

FIG. 3 shows a simplified QW heterostructure 10 in  
25 accordance with the present invention. Substrate 12 is a material including, but not limited to sapphire, silicon carbide, silicon, gallium nitride, aluminum nitride, zirconium diboride or the like. Substrate 12 can include a strain relief layer 16 deposited upon a substrate film 14 to  
30 provide a strain relief layer having a lattice constant approximately lattice matched to the lattice constant of GaN. Substrate 12 can also be a patterned substrate such as an ELOG substrate, or the like. Substrate film 14 is

deposited onto substrate 12. Strain relief layer 16 is then deposited on substrate film 14. Strain relief layer 16 has a thickness  $t_{16}$ . In an exemplary embodiment, strain relief layer 16 is an  $\text{In}_y\text{Al}_{1-y}\text{N}$  layer with  $0.50 \leq y \leq 0.60$ . However, it will be understood that other compositions of strain relief layer 16 can also be used. Increasing In content can provide a larger relaxed lattice constant for strain relief layer 16, and decreasing In content can provide a smaller relaxed lattice constant for strain relief layer 16. In an exemplary embodiment thickness  $t_{16}$  of strain relief layer 16 has a value of approximately 100 nm. However, it will be understood that other thicknesses of strain relief layer 16 can also be used. In another exemplary embodiment, thickness of strain relief layer 16 is chosen to be greater than a critical thickness for relaxation of the layer such that the layer thickness is sufficient to allow strain relaxation of strain relief layer 16. Group III-N layer (in this example, a QW layer) 18 is deposited on strain relief layer 16. In an exemplary embodiment, QW layer 18 is  $\text{In}_x\text{Ga}_{1-x}\text{N}$  with  $0.4 < x < 0.5$ . However it will be understood other compositions of QW layer 18 can also be used. Second strain relief layer 20 is then deposited on QW layer 18. Second strain relief layer 20 has composition  $\text{In}_z\text{Al}_{1-z}\text{N}$  and thickness  $t_{20}$ . In an exemplary embodiment,  $0.50 \leq z \leq 0.60$ , and  $z = y$ . However, it will be understood other compositions for strain relief layer 20 can also be used. Furthermore, the composition of strain relief layer 20 can be different from the composition of strain relief layer 16. In an exemplary embodiment, the thickness of strain relief layer 20  $t_{20}$  is equal to the thickness of strain relief layer 16  $t_{16}$ . However, it will be understood that strain relief layer 16 and strain relief layer 20 can have different thicknesses. GaN layer 22 is deposited on second strain relief layer 20.

In FIG. 3, only one QW structure is shown, by way of example, and to aid in clarity of description. However, it will be understood that multiple QWs can also be grown, and an active region of an optoelectronic device includes at least one QW. FIG. 4 shows an embodiment of the present invention with an optoelectronic active region consisting of 2 QWs, with a layer structure of GaN/InAlN/InGaN/InAlN/InGaN/InAlN/GaN. Other layers used in semiconductor devices, including but not limited to substrates, contacting layers, and the like are not shown, for sake of clarity of the QW structure. FIG. 5 shows another embodiment of a 2 QW structure with a layer structure of GaN/InAlN/InGaN/InAlN/GaN/InAlN/InGaN/InAlN/GaN. Other layers used in semiconductor devices, including but not limited to substrates, contacting layers, and the like are not shown, for sake of clarity of the QW structure.

Strain relief layer 16 and strain relief layer 20 can be grown as a bulk alloy. However, it will also be understood that a strain relief layer can be grown as a digital alloy superlattice, formed using thin layers (which are each thin, typically of the order 10-100 Angstroms thick) of at least two layer types that have different compositions. By way of example, a digital alloy can be formed using two different layer types, as shown in FIG. 6. In this case, a strain relief layer structure can be formed using layers 30 and 32, with thicknesses  $t_{30}$  and  $t_{32}$ , respectively. Layers 30 and 32 have compositions  $\text{In}_{y_1}\text{Al}_{1-y_1}\text{N}$  and  $\text{In}_{y_2}\text{Al}_{1-y_2}\text{N}$ , respectively, where  $y_1$  and  $y_2$  are chosen to be different). The average composition of a strain relief layer is determined by the compositions ( $y_1$ , and  $y_2$ ) and the thicknesses ( $t_{30}$  and  $t_{32}$ ) of the digital alloy layers.  $N$  pairs of superlattice layers can be used to form a strain

relief layer with a desired thickness. Digital alloy superlattices are able to provide a relaxed lattice constant. Strain at the interface between individual digital alloy layers can be used to prevent misfit dislocations propagating in the direction of growth of the layer, thereby forming a layer with a relaxed lattice constant of InAlN with a desired composition. For examples of III-Nitride superlattice structures, see J.P. Zhang et al., in Appl. Phys. Lett. 80, 3542 (2002), herein incorporated by reference. In this work, superlattices were used for strain management in the growth of AlGa<sub>N</sub> layers for UV light emitters.

Turning now to **FIG. 7**, a sectional view of an edge emitting laser (EEL) 100 is illustrated. EEL 100 is illustrated in an exemplary embodiment for simplicity and ease of discussion. However, it will be understood that other optoelectronic devices could be used and the illustration of EEL 100 is not meant to limit the scope of the invention. For example, a vertical-cavity surface-emitting laser, a quantum cascade laser, light emitting diode, or the like may also be used.

In one embodiment, EEL 100 includes a substrate (not shown) wherein substrate may comprise or consist of sapphire, silicon carbide, indium phosphide (InP), indium arsenide (InAs), gallium arsenide (GaAs), silicon (Si), zirconium diboride (ZrB<sub>2</sub>), an epitaxially grown material (such as a ternary or quaternary semiconductor), an ELOG substrate, or the like. It will also be understood that substrate 102 typically includes a lattice constant chosen to minimize defects in materials subsequently grown thereon.

A substrate film 102 is deposited upon the substrate. Substrate 102 can also be a patterned substrate such as, or the like. In one embodiment, a strain relief layer 104 is

positioned on substrate film 102. It will be understood that strain relief layer 104 may comprise more than one material layer, but is illustrated as including a single layer in this embodiment for simplicity and ease of discussion. In one embodiment, strain relief layer 104 is an InAlN layer grown as a bulk (or random) alloy. A thickness of strain relief layer 104 is chosen such that strain relief layer 104 provides a relaxed lattice constant of InAlN, which may be different from the lattice constant of the substrate film 102, and is chosen to minimize defects in materials subsequently grown thereon. In another embodiment, strain relief layer 104 consists of a DA semiconductor superlattice of InAlN layers, designed to provide a low defect density. As understood by those skilled in the art, a digital alloy is an alloy with an average composition that is grown using two or more different semiconductor components. The average composition of the digital alloy depends on the thickness and composition of each of the constituent layer types used to form the superlattice. The superlattice layers are typically thin, of the order of 10-100 Angstrom, so that the resulting material has the properties of the average composition and not of the individual layers constituting the alloy. Further, strain relief region 104 provides a lattice constant, which may be different from the lattice constant of substrate film 102, and is chosen to minimize defects in materials subsequently grown thereon.

In yet another embodiment, strain relief layer 104 includes a plurality of layers, wherein the different layers with the same or different average InAlN composition. This allows a transition of lattice constant from that of substrate film 102 to that of a Group III-N layer 106 subsequently grown on strain relief layer 104. In one embodiment, the transition in lattice constant is achieved

by altering the composition of the metamorphic strain relief layers. For example, the strain relief layers may be  $\text{In}_y\text{Al}_{1-y}\text{N}$  layers, where  $y$  varies from one value at the substrate film interface to another value at the interface to the  
5 Group III-N layer. The lattice constant may vary in a continuous fashion, in a step-graded fashion, or otherwise. In an exemplary embodiment, the lattice constant varies monotonically. In one approach, this can be achieved by monotonically varying  $y$  in a corresponding fashion; each  
10 value of  $y$  is chosen to produce the corresponding desired lattice constant. In another approach, metamorphic strain relief layers are based on DA layers. Material with an average composition of  $\text{In}_y\text{Al}_{1-y}\text{N}$  can be formed using at least two materials (sublayers) of the form  $\text{In}_{y1}\text{Al}_{1-y1}\text{N}$  and  $\text{In}_{y2}\text{Al}_{1-y2}\text{N}$  (where  $y1$  and  $y2$  are chosen to be different (as shown in  
15 FIG. 6), wherein the composition and thickness of each sublayer is chosen to provide an average composition of bulk  $\text{In}_y\text{Al}_{1-y}\text{N}$ . One advantage of digital alloys is that the effective lattice constant can be changed by varying the  
20 relative thicknesses of the sublayers, rather than by changing the material composition.

In one embodiment, (FIGURE 7) the Group III-N layer comprises a conductive  $\text{InAlN}$  layer 106 positioned on strain relief layer 104, which is positioned on the substrate film  
25 102. In this embodiment, the Group III-N layer 106 is a conductive layer which may comprise, for example, doped  $\text{InAlN}$  of the same composition as the strain relief layer

It will be understood that Group III-N conductive layer 106 may include more than one material layer, but is  
30 illustrated as including a single layer in an embodiment for simplicity and ease of discussion. Also in an embodiment, Group III-N conductive layer 106 includes highly doped semiconductor material with a conductivity type (i.e. n-type

or p-type) to provide a lateral contact and current spreading.

In one embodiment, the device further comprises a cladding layer 108 positioned on Group III-N conductive layer 106. In this embodiment, the structure may further comprise waveguiding layer 110 positioned on cladding layer 108. Cladding layer 108 and waveguiding layer 110 are part of a laser structure; p and n cladding layers may be made of InAlN of the same composition as undoped strain relief layer 104, while waveguide may be made of InGaN of a slightly lower composition than the quantum well (in which case some strain is likely to be present in the well or the barrier). The device further comprises active layer 112 positioned on waveguiding layer 110 wherein active layer 112 comprises a material capable of emitting a substantial amount of light at a desired wavelength of operation. As can be appreciated by those skilled in the art, an active layer capable of emitting light is a light processing region. Other light processing regions include regions to absorb light and regions to modulate light. In one embodiment, the desired wavelength of operation is in the green wavelength range, approximately from 500 nm to 590 nm. However, it will be understood that other wavelength ranges may be desired and will depend on the active region and the intended application.

Further, it will be understood that active layer 112 may include various light emitting structures, such as quantum dots, quantum wells, or the like, which improve a light emitting efficiency of EEL 100. Also, it will be understood that active layer 112 may include more than one material layer, but is illustrated as including a single layer in an embodiment for simplicity and ease of discussion.

In one embodiment, the device further comprises a waveguiding layer 114 positioned on active layer 112 and a cladding layer 116 positioned on waveguiding layer 114. In a further device embodiment, a conductive layer 118 is  
5 positioned on cladding layer 116. It will be understood that conductive semiconductor layer 118 may include more than one material layer, but is illustrated as including a single material layer in an embodiment for simplicity and ease of discussion. Conductive layer 118 may include highly doped  
10 semiconductor material with a conductivity type opposite to that of conductive layer 106 (i.e. p-type or n-type). However, conductive layer 118 can also be formed using a structure such as a tunnel junction or the like.

In one embodiment, blanket regions of material (i.e. layers 102, 104, 106, 108, etc.) are typically positioned on  
15 the substrate sequentially so that a plurality of EELs may be formed in an array. However, only one such device (i.e. EEL 100) is illustrated for simplicity and ease of discussion. Also, in an embodiment, layers 102, 104, 106,  
20 108, etc. may be deposited using molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), or a similar technique well known by those skilled in the art.

In one embodiment, a ridge 101 is formed by etching through to Group III-N conductive layer 106 as shown. It  
25 will be understood that ridge 101 may be formed using techniques well known to those skilled in the art such as wet-etching, or dry-etching using inductance-coupled plasma (ICP) etching, or the like. In this embodiment, a lower ohmic contact 120 may be formed on the etched, exposed Group  
30 III-N conductive layer 106 of EEL 100. An upper ohmic contact 122 may be formed on the conductive layer 118 of EEL 100. It will be understood that ohmic contact regions 120 and 122 may include gold (Au), titanium (Ti), platinum (Pt),



palladium (Pd), gold-germanium (Au--Ge), nickel, (Ni), metal alloys, or the like.

Lower ohmic contact 120 can also be formed on other layers, such as the substrate, on an etched upper surface of the substrate, or on a lower side of substrate in the case of a conductive substrate, and illustration of ohmic contact 120 formed on the etched, exposed Group III-N conductive layer 106 of EEL 100 is shown by way of example only.

FIG.8 shows a schematic band-edge alignment of a semiconductor device 130 formed in accordance with the present invention. Thicknesses of layers are not shown. Thicknesses for layers illustrated are known in the art. The conduction band ( $E_c$ ) alignment and the valence band alignment ( $E_v$ ) are schematically shown. Substrate film 132 is a deposited on a substrate, including, but not limited to silicon carbide, sapphire, zirconium diboride and the like. Strain relief layer 134 is deposited on substrate film 132. In an exemplary embodiment, strain relief layer 134 is an  $\text{In}_y\text{Al}_{1-y}\text{N}$  layer with  $0.50 \leq y \leq 0.60$ . However, it will be understood that other compositions of strain relief layer 134 can also be used. In an exemplary embodiment, the band alignment of strain relief layer 134 matches the band alignment of substrate film 132. However, strain relief layer 134 can have different band alignment to substrate film 132. Strain relief layer has a minimum thickness to provide a relaxed lattice constant of, for example,  $\text{InAlN}$ , chosen to minimize defects in materials subsequently grown thereon. The Group III-N layer (not shown) can comprise, for example, an  $\text{InAlN}$  conductive layer, an  $\text{InAlN}$  cladding layer and the like, wherein the layers may have the same or different compositions of  $\text{InAlN}$ , as the strain relief layer. A Group III-N conductive region may comprise highly doped semiconductor material with a conductivity type (i.e. n-type

or p-type) to provide a lateral and/or a vertical conductivity. The device further comprises a light processing region, comprising waveguiding layers 136, quantum wells 138 and barriers 140. In an exemplary  
5 embodiment, waveguiding layers 136 comprise  $\text{In}_p\text{Ga}_q\text{Al}_{1-p-q}\text{N}$ . A composition of waveguiding layers 136 is chosen to provide electrical and optical confinement for the quantum wells in semiconductor device 130. In an exemplary embodiment, QWs 138 are  $\text{In}_x\text{Ga}_{1-x}\text{N}$  with  $0.4 < x < 0.5$ . However, it will be  
10 understood other compositions of QW layers 138 can also be used. In an exemplary embodiment, barrier layers 140 are  $\text{In}_r\text{Ga}_s\text{Al}_{1-r-s}\text{N}$ . Composition of barrier layers 140 is chosen to provide electrical confinement for the quantum wells in semiconductor device 130.

15 A further InAlN layer 142 can include a cladding region, a contacting region and the like. In an exemplary embodiment, a conductive region of InAlN layer 142 includes highly doped semiconductor material with a conductivity type opposite to that of a conductive region of InAlN layer 134  
20 (i.e. p-type or n-type) to provide a lateral and/or a vertical conductivity. However, a conductive region InAlN layer 142 can also be formed using a structure such as a tunnel junction or the like.

In an exemplary embodiment, contacting layer 144 is a  
25 GaN layer and an electrical contact may be formed on contacting layer 142.

The active region of III-N based devices can also be improved, by optimizing the internal quantum efficiency of InGaN QWs.

30  $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$  is lattice matched with GaN. MOCVD growth of nitride semiconductors is typically carried out using ammonia as a source for nitrogen. However, the presence of hydrogen is not favorable for growth because of the weak

nature of the bond. We propose to grow (by MOCVD) using a nitrogen carrier gas with a low ammonia partial pressure and a low reactor pressure (approximately 70 mbar), as outlined by A. Dadgar et al. in Appl. Phys. Lett., Vol. 85, pp5400-,  
5 2004, and herein incorporated by reference (the Dadgar paper). Other pressures can also be used. The growth temperatures for a film with  $y = 0.17$  is approximately in the range of 800-850°C. To achieve higher concentrations of Indium, lower growth temperatures are used. The Dadgar paper  
10 describes the growth of InAlN with  $y \sim 0.25$ , and these layers are shown to be partially relaxed. The growth conditions described in the Carlin paper are similar (a pressure of 50-75 mbar; N<sub>2</sub> carrier gas; 800-850°C growth temperatures). In the Carlin paper, alternate layers of AlInN and GaN were  
15 grown for distributed Bragg reflectors (DBRs). While the InAlN was grown at 800-850°C, subsequent GaN growth was performed at 1050°C. They report that the quality of the InAlN did not deteriorate from this thermal cycling. This is beneficial for post-growth thermal annealing procedures,  
20 which can be used improving the crystalline quality of the films disclosed herein.

In order to grow In<sub>y</sub>Al<sub>1-y</sub>N layers with  $0.4 < y$ , MOCVD growth temperatures lower than 750°C are used. The main problems with increasing indium composition are:

- 25 (a) large lattice mismatch.
- (b) phase separation.
- (c) poor crystalline quality due to low growth temperatures.

30 The lattice mismatch between In<sub>0.50</sub>Al<sub>0.50</sub>N and GaN is ~4%. We have observed in our studies on the InGaN-GaN system that the heterostructures are partially relaxed for an indium composition above 10%, when the threading dislocation

density in the GaN layer is reduced ( $\sim 10^7 \text{ cm}^{-2}$ ). We studied the microstructure of InGaN epilayers grown on two GaN layers having different threading dislocation densities. We observed that the strain relaxation mechanisms in the two sets of samples are fundamentally different. At high dislocation densities, the film remains pseudomorphic and partial relaxation occurs via formation of pyramidal defects. When the dislocation density is reduced ( $\sim 10^7 \text{ cm}^{-2}$ ) systematic plastic relaxation by slip is observed. This relaxation occurs by the activation of a secondary slip system, when the threading dislocation density in the underlying GaN layer has been reduced to  $\sim 10^7 \text{ cm}^{-2}$ . The basal plane slip is inactive in this conventional c-plane epitaxy. This form of relaxation is preferable for the growth of high quality films and for the incorporation of high indium content. For information, see S. Srinivasan et al., Appl. Phys. Lett 83, 5187 (2003), herein incorporated by reference. The relaxation allows the growth of a better structural quality InGaN film. A similar relaxation mechanism may be triggered by growing InAlN on GaN, using a low dislocation density GaN substrate such as an ELOG substrate or bulk GaN. Another method to overcome these problems is to grow in a semi-polar direction, on a plane that is inclined to the basal plane. This will trigger the basal plane slip. High quality semi-polar wafers are now available. This will allow the relaxation of the InAlN film and improve its crystalline quality. Moreover, misfit dislocations are now generated at the InAlN/GaN interface, leaving the InGaN/InAlN interface relatively clean. This interface is beneficial for lasing to occur and it is preferred to keep it as defect-free as possible.

Phase separation and material quality are related to the temperature of growth. Phase separation is expected to

occur for higher indium compositions due to a large miscibility gap in the InN-AlN system temperatures. For example, at  $T = 1000$  K, the spinodal decomposition of relaxed films typically occurs if the In content varies approximately from 16 to 70%. This has been experimentally observed in relaxed  $\text{In}_y\text{Al}_{1-y}\text{N}/\text{GaN}$  films for  $y > 0.17$ . For information on spinodal decomposition, see V.G. Deibuk and A.V. Voznyi, *Semiconductors* 39, 1063 (2005), incorporated herein by reference. However, spinodal decomposition is strongly affected by the strain. A calculated phase diagram of the InN-AlN system is shown in **FIG. 9**. Different film thicknesses correspond to different stress states. At a growth temperature of approximately  $750^\circ\text{C}$  (1023K, represented by the dotted line in **Fig. 7**), for a 100 nm thick film, phase separation would occur for  $y > 0.30$ . We propose the use of a post-growth annealing procedure to improve the structural quality and compositional homogeneity of the InAlN layers. The InAlN alloy is stable at all temperatures for  $T > 1400\text{K}$  ( $1130^\circ\text{C}$ ). Annealing at this temperature for sufficient time will reverse the phase separation and remove structural defects. A significant problem during annealing may be the out-diffusion of indium from the film. This can be prevented by growing a thin layer of GaN or AlN on the surface of the InAlN layers. Indium being a bigger atom will not diffuse easily through the GaN or AlN layer.

Another growth method that can be used for the growth of III-Nitrides is molecular beam epitaxy (MBE). This method uses lower growth temperatures and is favorable for the growth of InAlN films with high Indium composition. For examples, D. S. Katzer et al. in *J. Vac. Sci. Technol.* B23, 1204 (2005), herein incorporated by reference, have grown  $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$  at temperatures as low as  $460^\circ\text{C}$  using MBE.

Using an MBE growth approach, with a suitable growth temperature for higher-In content layers, and appropriate flux conditions for the group III and the group V sources used in MBE growth, a stoichiometric InAlN layer can be  
5 incorporated, either as a bulk layer or as a digital alloy superlattice with an average composition approximately equal to that of a desired bulk InAlN layer. Subsequent post-growth annealing can then be used to improve the crystalline quality.

10 In summary of one example of the present invention, the use of InAlN strain relief layers between a substrate film and Group III-N layer can be used to grow, for example, InGaN quantum well layers with compositions required for green-wavelength-range emission from laser diodes. The InAlN  
15 can be chosen to be approximately lattice matched to an InGaN QW, or with a lattice constant that allows pseudomorphic growth of an InGaN QW. At typical compositions required for green laser diodes, the approximately lattice matched InAlN has a bandgap similar to that of GaN. InAlN  
20 can also be used as a strain free template to allow the growth of complete electronic and optoelectronic devices pseudomorphically grown on the InAlN strain relief.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of  
25 ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of  
embodiments of the present invention. It is to be understood  
30 that the above description is intended to be illustrative, and not restrictive, and that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Combinations of the above embodiments and other

embodiments will be apparent to those of skill in the art upon studying the above description. The scope of the present invention includes any other applications in which embodiment of the above structures and fabrication methods are used. The scope of the embodiments of the present invention should be determined with reference to claims associated with these embodiments, along with the full scope of equivalents to which such claims are entitled.

We claim:

1. A semiconductor structure comprising:
  - (a) a substrate;
  - 5 (b) a substrate film overlaying the substrate;
  - (c) a strain relief layer overlaying the substrate film, wherein the strain relief layer comprises InAlN and/or InAlGaN; and
  - 10 (d) a Group III-N layer overlaying the strain relief layer, wherein the Group III-N layer possesses a lattice constant greater than a lattice constant of the substrate film; andwherein the strain relief layer provides a transition from the smaller lattice constant of the substrate film to  
15 the larger lattice constant of the Group III-N layer.
2. The semiconductor structure of claim 1, wherein the strain relief layer comprises  $\text{In}_y\text{Al}_{1-y}\text{N}$ , wherein  $y$  is at least 0.2.
3. The semiconductor structure of claim 1, wherein the  
20 strain relief layer comprises  $\text{In}_y\text{Al}_{1-y}\text{N}$ , wherein  $y$  is at least 0.4.
4. The semiconductor structure of claim 1, wherein the strain relief layer comprises  $\text{In}_y\text{Al}_{1-y}\text{N}$ , and wherein  $0.4 \leq y \leq 0.6$ .
- 25 5. The semiconductor structure of claim 1, wherein the strain relief layer comprises  $\text{In}_y\text{Al}_{1-y}\text{N}$ , and wherein  $0.68 \leq y \leq 1.0$ .
6. The semiconductor structure of claim 1, wherein the substrate is selected from the group consisting of  
30 substrates comprising sapphire, silicon carbide, silicon, bulk nitrides, zirconium diboride, and binary III-V compounds and alloys thereof.



7. The semiconductor structure of any one of claims 1-6, wherein the Group III-N layer comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}$ .

8. The semiconductor structure of claim 4 wherein the Group III-N layer comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}$ , and wherein  $0.28 \leq x \leq 0.60$ .

9. The semiconductor structure of claim 5 wherein the Group III-N layer comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}$ , and wherein  $0.6 \leq x \leq 1.0$ .

10. The semiconductor structure of any one of claims 1-9, wherein the strain relief layer comprises multiple layers with different InAlN and/or InAlGaN compositions.

11. The semiconductor structure of claim 10, wherein the strain relief layer is approximately lattice matched to the substrate film at a substrate film-strain relief layer interface, and is approximately lattice matched to the Group III-N layer at a Group III-N layer-strain relief layer interface.

12. The semiconductor substrate of any one of claims 1-11, comprising a plurality of strain relief layers and Group III-N layers.

13. The semiconductor structure of any one of claims 1-12, wherein the semiconductor structure is suitable for use in an optoelectronic device that provides one or more of light emission, light absorption, light modulation, and waveguiding.

14. The semiconductor structure of any one of claims 1-13, wherein the semiconductor structure comprises one or more of a digital alloy superlattice, an edge emitting laser, a band-edge alignment, a vertical-cavity surface-emitting laser, a quantum cascade laser, a light emitting diode, and a quantum well.

15. The semiconductor structure of claim 14, wherein the semiconductor structure comprises a quantum well structure.

16. The semiconductor structure of claim 15, wherein the quantum well structure is suitable for optoelectronic devices.

17. A method for making a semiconductor substrate,  
5 comprising:

(a) depositing a substrate film on a substrate;

(b) depositing a strain relief layer over the substrate film, wherein the strain relief layer comprises InAlN and/or InAlGa<sub>N</sub>; and

10 (c) depositing a Group III-N layer over the strain relief layer, wherein the Group III-N layer possesses a lattice constant greater than a lattice constant of the substrate film;

wherein the strain relief layer provides a transition  
15 from the smaller lattice constant of the substrate film to the larger lattice constant of the Group III-N layer.

18. The method of claim 17, wherein the strain relief layer comprises In<sub>y</sub>Al<sub>1-y</sub>N, wherein y is at least 0.2.

19. The method of claim 17, wherein the strain relief layer  
20 comprises In<sub>y</sub>Al<sub>1-y</sub>N, wherein y is at least 0.4.

20. The method of claim 17, wherein the strain relief layer comprises In<sub>y</sub>Al<sub>1-y</sub>N, and wherein  $0.4 \leq y \leq 0.6$ .

21. The method of claim 17, wherein the strain relief layer comprises In<sub>y</sub>Al<sub>1-y</sub>N, and wherein  $0.68 \leq y \leq 1.0$ .

25 22. The method of claim 17, wherein the substrate is selected from the group consisting of substrates comprising sapphire, silicon carbide, silicon, bulk nitrides, zirconium diboride, and binary III-V compounds and alloys thereof.

23. The method of any one of claims 17-22, wherein the  
30 Group III-N layer comprises In<sub>x</sub>Ga<sub>1-x</sub>N.

24. The method of claim 20 wherein the Group III-N layer comprises In<sub>x</sub>Ga<sub>1-x</sub>N, and wherein  $0.28 \leq x \leq 0.60$ .

25. The method of claim 21 wherein the Group III-N layer comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}$ , and wherein  $0.6 \leq x \leq 1.0$ .

26. The method of any one of claims 17-25, wherein the strain relief layer comprises layers with different InAlN  
5 and/or InAlGaN compositions.

27. The method of claim 26, wherein the strain relief layer is approximately lattice matched to the substrate film at a substrate film-strain relief layer interface, and is approximately lattice matched to the Group III-N layer at an  
10 Group III-N layer-strain relief layer interface.

28. The method of any one of claims 17-27, comprising a plurality of strain relief layers and Group III-N layers.

29. The semiconductor structure of any one of claims 1-16, wherein the semiconductor structure is suitable for use in  
15 heterojunction field effect transistors or heterjunction bipolar transistors.

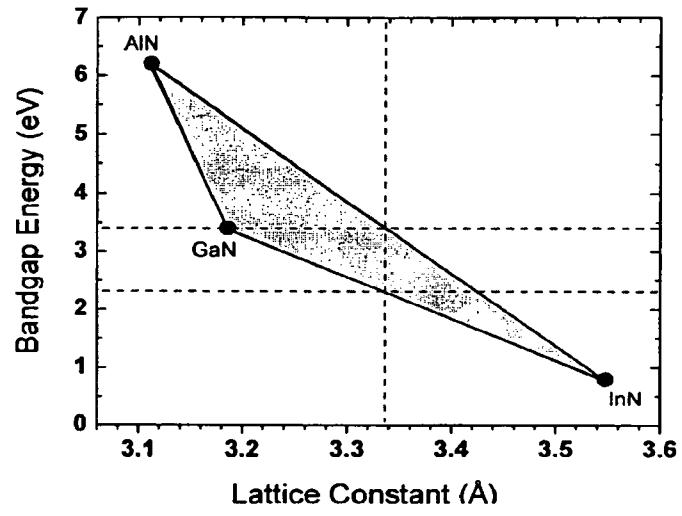


FIG. 1

10'

18'
16'
14'
12'

FIG. 2

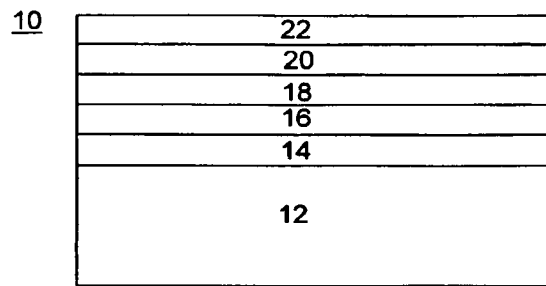


FIG. 3

GaN
InAlN
InGaN
InAlN
InGaN
InAlN
GaN

FIG. 4

GaN
InAlN
InGaN
InAlN
GaN
InAlN
InGaN
InAlN
GaN

FIG. 5



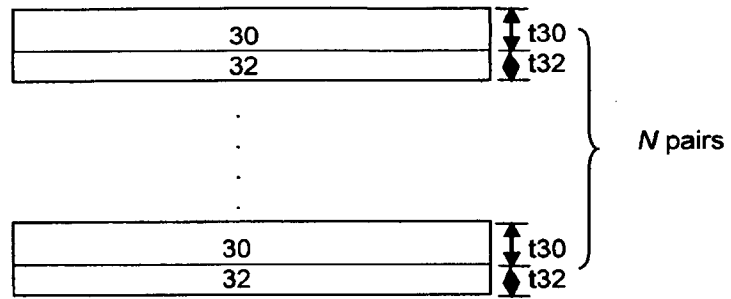


FIG. 6

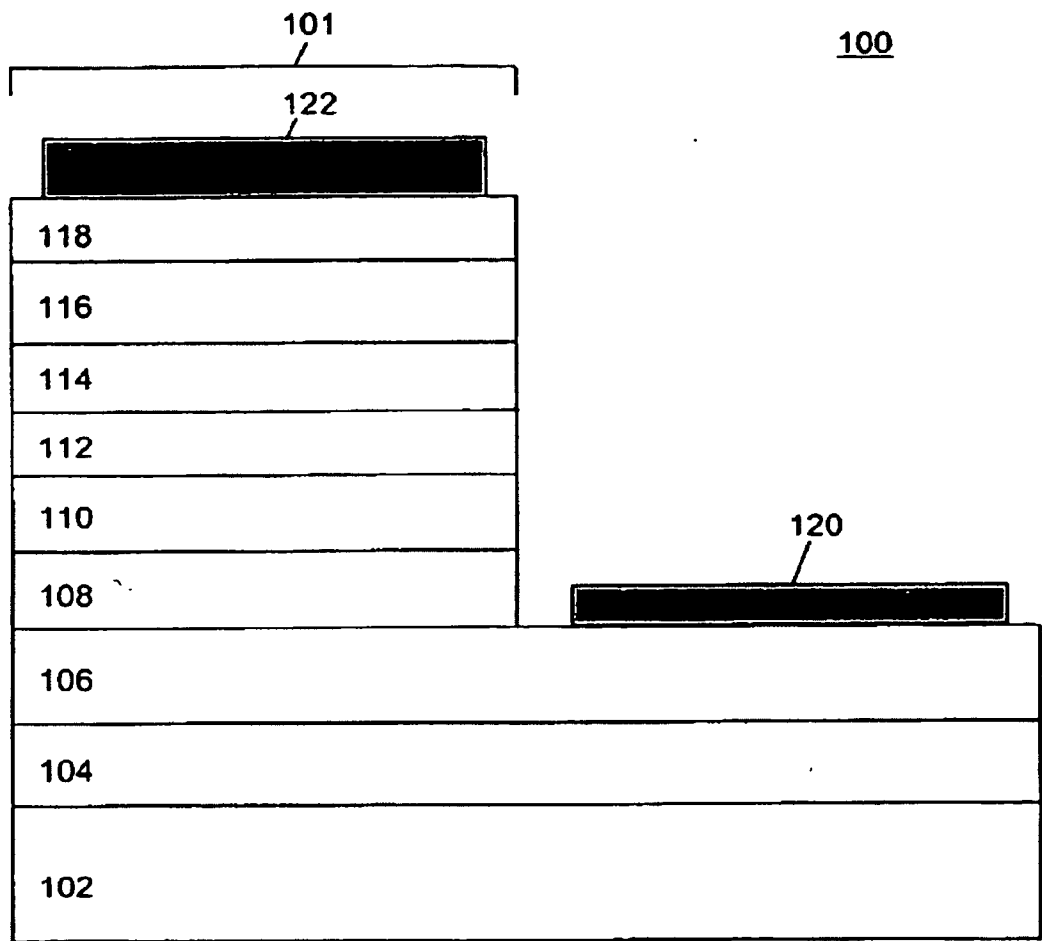
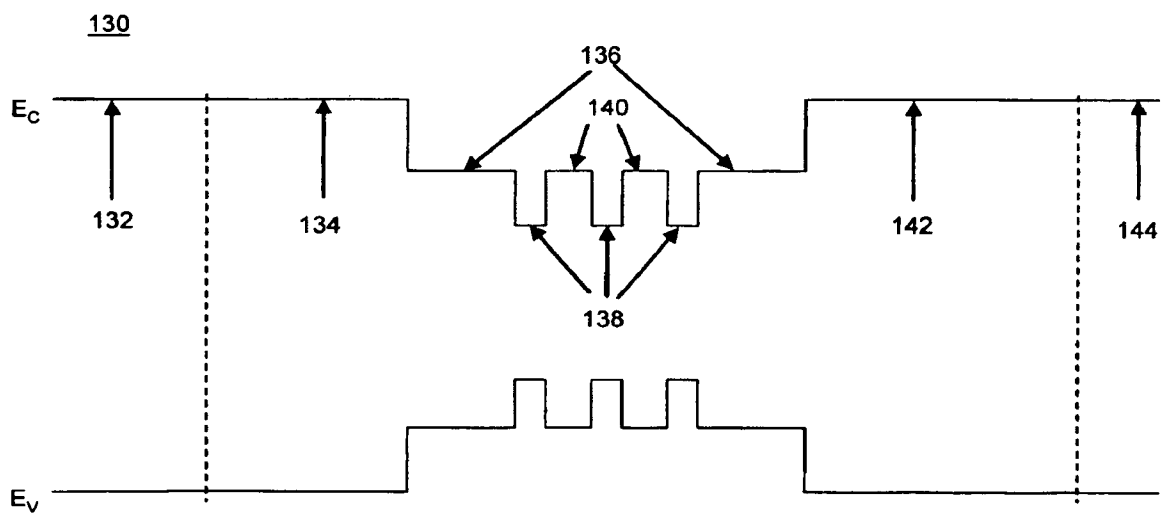


FIG. 7



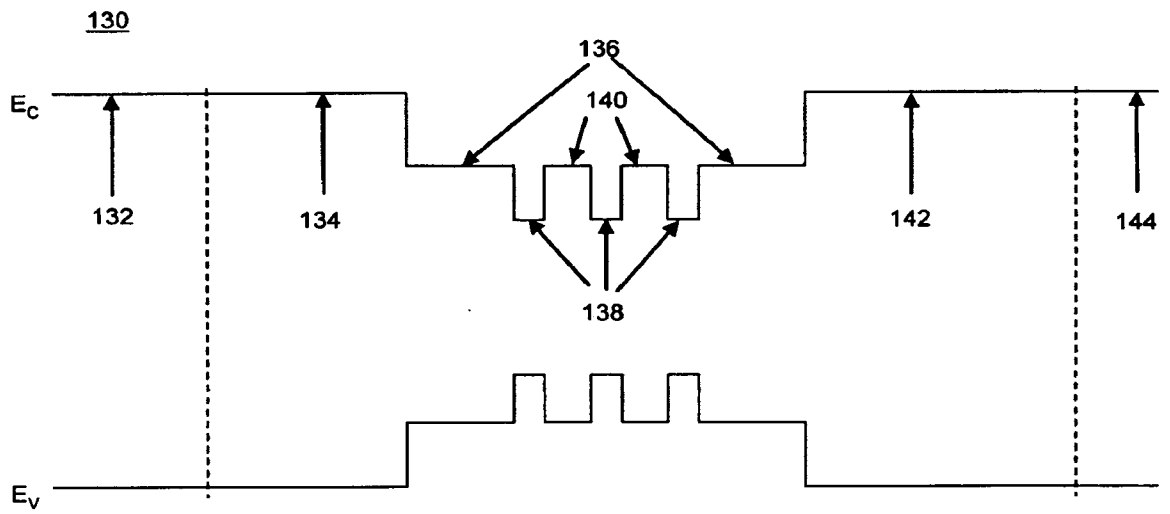


FIG. 8

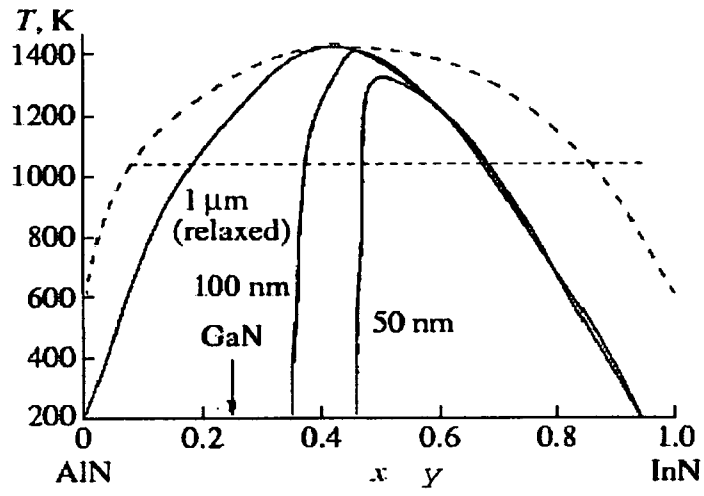


FIG. 9