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(54) **ADC WITH ENHANCED AND/OR ADJUSTABLE ACCURACY**

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(57) **ABSTRACT**

An analog-to-digital-converter includes an input signal connector, an output signal port, two or more sub-ADCs, and a digital signal processing block. The result from each sub-ADC is used by the digital signal processing block to output data with increased performance.
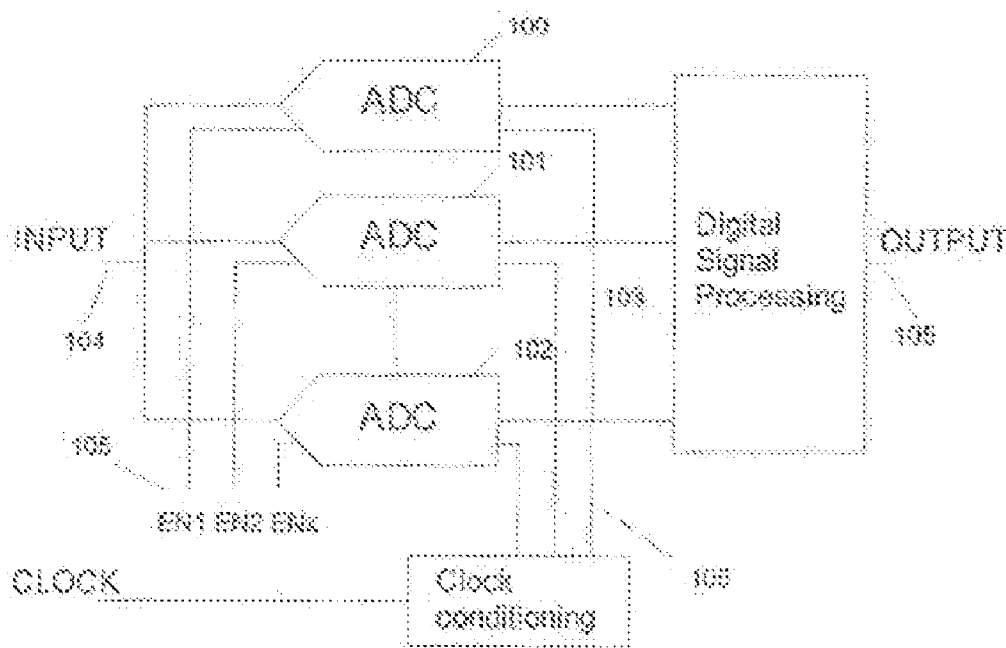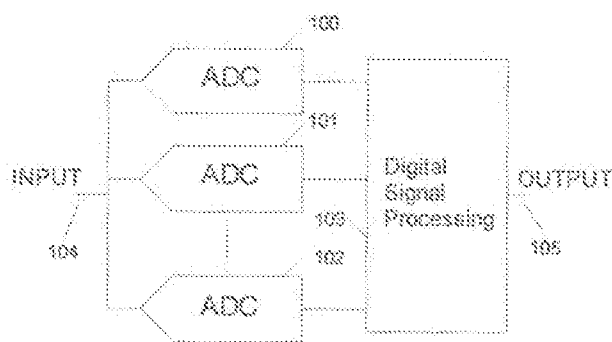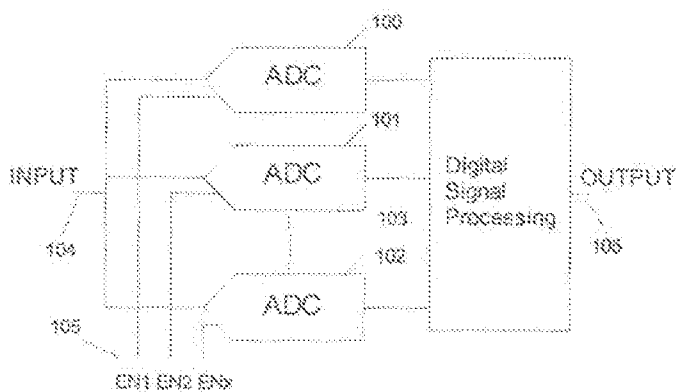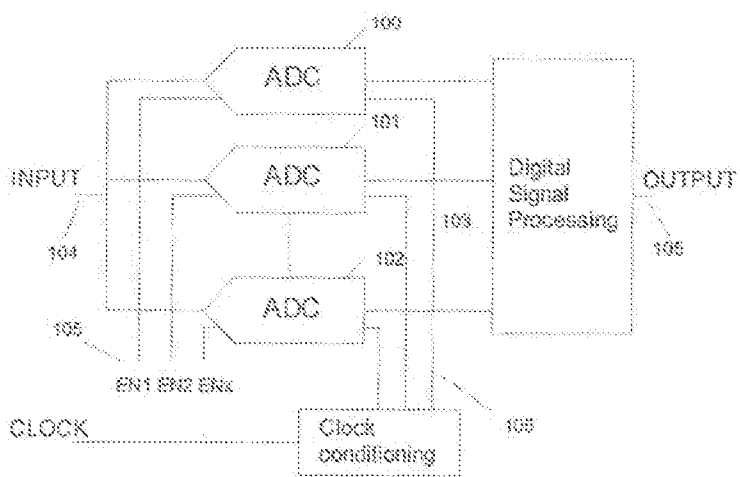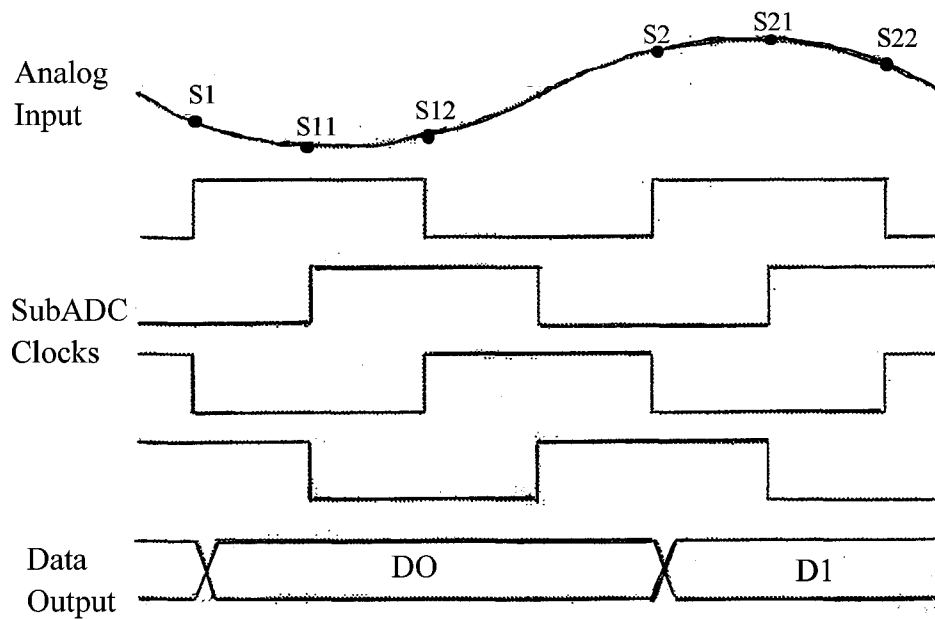
FIG. 1

FIG. 2

FIG. 3

FIG. 4

ADC WITH ENHANCED AND/OR ADJUSTABLE ACCURACY

BACKGROUND

[0001] This application claims priority to U.S. Provisional Application Ser. No. 61/232,978 filed on Aug. 11, 2009.

TECHNICAL FIELD

[0002] This disclosure generally relates to analog-to-digital conversion and in particular to analog-to-digital converters (ADCS) with enhanced and/or adjustable accuracy.

[0003] Several electronic systems require analog-to-digital converters (ADCs) for their function. Depending on the characteristics of the system, there are specific requirements to the ADC and the performance parameters of the ADC. Increased performance as accuracy, resolution and linearity comes at a cost of increased power dissipation due to the laws of physics. The electronics industries therefore strive to obtain the best possible performance at the lowest possible power dissipation.

[0004] For many systems, the requirement to the ADC is very dependent on external conditions. For example, in a mobile communication system, the requirements vary according to distance to the base station and the presence of interfering signals. The system is therefore designed to work under worst scenarios resulting in higher requirements for the ADC and other circuitry. This results in an average power dissipation that is much higher than required since the requirements are set for worst case scenarios while the system very seldom operates under these conditions.

[0005] System designers therefore need ADCs where the accuracy and performance can be modified during operation. Previously, the solutions have bees able to scale power dissipation with only a few percent by switching on and off auxiliary blocks and adjusting supply currents in the ADC. These solutions suffer from unpredictable performance in the low performance mode since each block work under unintended condition. The range of power dissipation variation is also very small.

[0006] SUMMARY OF THE DISCLOSURE

[0007] An analog-to-digital converter disclosed herein, comprises several sub-ADCs, a signal input, a digital signal processing block and a digital output. Each sub-ADC converts the input signal with a given accuracy and transfers the output to the digital signal processing block. The average of the results from each sub-ADC is calculated to output a single digital output word with higher Signal-Noise Ratio.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Features and advantages of the disclosed ADCs will be apparent to those of ordinary skill in the art in view of the detailed description of exemplary embodiments which is made with reference to the drawings.

[0009] FIG. 1 shows a block diagram of the embodiment of a disclosed ADC with enhanced performance.

[0010] FIG. 2 shows a block diagram of the a disclosed ADC with enhanced and adjustable performance.

[0011] FIG. 3 shows a block diagram of an alternative embodiment ADC where the sampling clock to each channel is skewed in order to obtain possibilities for frequency domain filtering in addition to the improved performance.

[0012] FIG. 4 shows a timing diagram of the embodiment of FIG. 3 with four sub-ADCs.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

[0013] The principle of operation of the disclosed ADCs is based on averaging of multiple ADC channels in order to increase accuracy.

[0014] FIG. 1 shows an embodiment where accuracy is improved but fixed. FIG. 2 shows an embodiment where accuracy is improved and adjustable. The basic operation of these two embodiments is the same, but flexibility is better for the embodiment in FIG. 2.

[0015] The operation of the circuit as follows. The input signal 104 is applied to an arbitrary number of sub-ADCs 100-102 in parallel. These sub-ADCs can be completely separate ADCs or any combination of multi channel ADCs. This signal can be passed through separate buffers or analog signal conditioning circuitry without altering the principal operation of the disclosed ADCs. Each ADC samples the input signal and converts it to a digital word with a given accuracy. The digital output data ate collected by a digital signal processing block and output in a suitable format for further processing.

[0016] The digital signal processing can be performed in different ways depending on desired properties of the output signal. However, the most obvious operation is to calculate the average of the data from each sub-ADC. Calculating the average is equivalent to summing all sub-ADC outputs and if desired truncate the output to a suitable number of bits.

[0017] Assuming that the noise is uncorrelated in each of the sub-ADCs, the equivalent output noise is reduced by a factor of 3 dB each time the number of sub-ADCs is doubled. Denoting the signal-to-noise-ratio (SNR) of a single sub-ADC as $SNR_{sub\text{-}ADC}$, the total SNR at the output (SNR_{total}) can be shown by Equation (1) below, if $N_{sub\text{-}ADC}$ equals the number of sub-ADCs are used.

$$SNR_{total} = SNR_{sub\text{-}ADC} + 10 \, \log_{10}(N_{sub\text{-}ADC}) \qquad (1)$$

[0018] This noise acts like ordinary thermal noise can be explained the following way: When adding two sub-ADC outputs, the output signal will double as the input signals are equal. The noise however is uncorrelated and must be added as root mean square (RMS) values resulting in a square root of two increase. Hence the SNR increases by the square root of two.

[0019] Adjustable performance can be obtained by the embodiment shown in FIG. 2. Specifically, in addition to the embodiments shown in FIG. 1, each sub-ADC in FIG. 2 comprises an enable input 105 allowing the user to enable or disable a given sub-ADC. In the disabled mode, the sub-ADC is in Power Down mode consuming an insignificant amount power. The digital signal processing block must be designed to properly scale the digital output depending on the number of active sub-ADCs.

[0020] With all channels enabled, the total ADC has full performance according to Equation (1). With only one channel enabled, the performance of the ADC is equal to the performance of the sob-ADC. Performance points between can be selected by having other numbers of sub-ADCs enabled.

[0021] As an example, with four sub-ADCs the total power dissipation can be adjusted with a factor of four, and total SNR can be adjusted in a 6 dB range

[0022] A significant advantage with the disclosed ADCs over traditional approaches is that the performance in the low power modes is predictable. Each sub-ADC will work under

optimum conditions, and performance is given by the characteristics of the sub-ADC. Compared to a solution where bias currents are manipulated to non-optimum values, the disclosed ADCs is superior.

[0023] Further improvements can be obtained by the embodiments in FIG. **3**. The additional feature of the embodiment of FIG. **3** is the clock conditioning circuitry. This circuitry ensures that the sampling limes of the sub-ADCs are distributed over the entire ADC clock cycle.

[0024] The timing diagram in FIG. **4** shows the timing in case of an ADC with four sub-ADCs. The main sampling points are S1 and S2 and consecutive points at the same frequency. Denote this frequency FS. Instead of having all sub-ADCs sampling at the same point, it Is possible to make each sub-ABC sample at S11, S12 and S13 respectively, each one at frequency FS. Since the sub-ABC samples are distributed over the entire clock period, the effective sampling rate Is increased by a factor of four. This moves the input frequency where signal components will be aliased into the signal band up with a factor of four to 4×FS/2 instead of FS/2. This will reduce the requirements to the Anti Aliasing filter required in front of any ADC. The Digital Signal processing block can filter out particular frequency bands outside the signal band, and a custom frequency mask can easily be made by modifying the digital signal processing block. Compared with the embodiment of FIG. **1** and FIG. **2** this gives an additional freedom to shape the signal in the frequency band, suppress particular aliased tones and simplify analog circuitry in front of the ADC.

[0025] If the signal band is set equal to FS/2, it is possible to get the same improvement in SNR as predicted by Equation 1. However, the digital signal processing block will be more complex than the averaging function required for the embodiments in FIGS. **1** and **2**.

[0026] The detailed description is to be construed as exemplary only and does not describe every possible embodiment because describing every possible embodiment would be impractical, if not impossible. Numerous alternative embodiments could be implemented, using either current technology or technology developed after the filing date of this patent, which would still fall within the scope of this disclosure.

1. An analog-to-digital-converter comprising
an input signal connector
an output signal port
two or more sub-ADCs
and a digital signal processing block, whereas the result from each sub-ADC is used by the digital signal processing block to output data with increased performance.

2. An analog-to-digital-converter according to claim **1** where the analog input signal is passed through separate blocks prior to being applied at the input of each sub-ADC.

3. An analog-to-digital-converter comprising
an input signal connector
an output signal port
two or more sub-ADCs
means to enable and disable the functionality of each sub-ADC individually
and a digital signal processing block, whereas the result from each sub-ADC is used by the digital signal processing block to output data with increased performance, and ability to select the number of sub-ADCs used to generate the output data thereby adjusting the total performance

4. An analog-to-digital-converter according to claim **3** where the analog input signal is passed through separate blocks prior to being applied at the input of each sub-ADC.

5. An analog-to-digital-converter comprising
an input signal connector
an output signal port
two or more sub-ADCs
means to enable and disable the functionality of each sub-ADC individually
and a digital signal processing block, whereas the sampling time of each sub-ADC is skewed such that their sampling times are distributed across the ADC sampling period, whereas the result from each sub-ADC is used by the digital signal processing block to output data with increased performance.

6. An analog-to-digital-converter according to claim **5** where the analog input signal is passed through separate blocks prior to being applied at the input of each sub-ADC.

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