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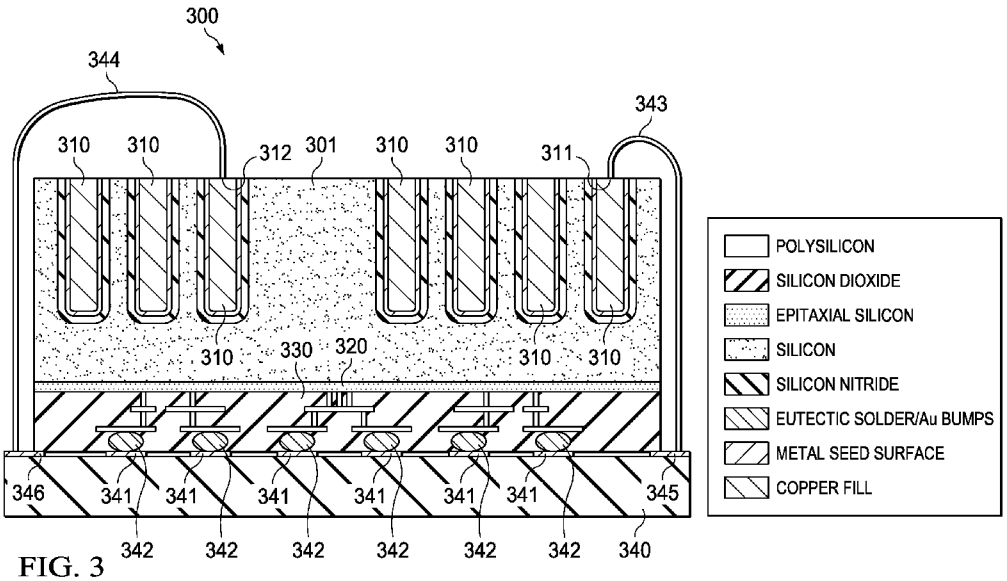

FIG. 3

(57) Abstract: In described examples, an integrated circuit (IC) (300) includes a circuit substrate (301) having a front side surface (320) and an opposite backside surface. Active circuitry is located on the front side surface (320). An inductive structure (310) is located within a deep trench formed in the circuit substrate (301) below the backside surface. The inductive structure (310) is coupled (343, 344) to the active circuitry.

[Continued on next page]

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SEMICONDUCTOR DIE WITH BACKSIDE INTEGRATED INDUCTIVE COMPONENT

[0001] This relates to fabrication of integrated circuits, and more particularly to the fabrication of an inductive component on the backside of a semiconductor die.

BACKGROUND

[0002] Occasionally, a circuit that is implemented within an integrated circuit (IC) requires an inductive component. An inductive component may be fabricated by forming a coil on one or more of the metal layers of the IC; however, the inductance of such a component is limited to a relatively low value. However, the quality factor of in inductor formed in the metal layers of the IC may be limited given the very high resistance per square of a typical metal layer. Typically, such an inductor may only be useful for ultra high frequency (UHF) circuits, such as 300MHz–3 GHz frequency range. Furthermore, they may contribute to significant switching losses.

[0003] Currently, silicon IC's such as switch-mode DC-DC converters use co-packaged discrete inductors which are large and bulky, contribute to package complexity, and may be a large percentage of the package cost.

SUMMARY

[0004] In described examples, an integrated circuit (IC) includes a circuit substrate having a front side surface and an opposite backside surface. Active circuitry is located on the front side surface. An inductive structure is located within a deep trench formed in the circuit substrate below the backside surface. The inductive structure is coupled to the active circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 is an illustration of an example inductor fabricated on the backside of an IC.

[0006] FIG. 2 is an illustration of example coupled inductors fabricated on the backside of an IC.

[0007] FIGS. 3-5 illustrate various ways of connecting a backside inductor to active circuitry of the IC.

[0008] FIGS. 6A-6G illustrate a method for forming an inductive component on the backside of an IC.

[0009] FIGS. 7A-7B illustrate an alternative embodiment in which a seed layer is deposited using a printer.

[0010] FIGS. 8A-8B illustrate simulation results for an example backside inductor.

[0011] FIG. 9 illustrates another embodiment with inductors formed in multiple substrate layers.

[0012] FIG. 10 is a block diagram of an example system that includes an IC with a backside inductor.

[0013] FIG. 11 is a block diagram of an example system that includes an IC with a backside inductor created using multiple metallization layers.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0014] Like elements in the drawings are denoted by like reference numerals for consistency.

[0015] A wide portfolio of silicon IC's require inductors which cannot be integrated within the metal stack due to the limited size, current capability, and efficiency obtainable within metal layer integrated inductors. Functions that may require inductors that cannot be implemented within the metal layers of the IC may include: filter output voltage and current; store energy that is delivered cycle by cycle; provide an efficient way to move energy from two or more voltage domains; perform auxiliary functions such as providing adiabatic gate drivers and zero voltage transitions; etc.

[0016] A majority of ICs are fabricated on a silicon substrate in which a large portion of the silicon substrate is typically needed only to mechanically support the active devices that are created on the surface of the silicon substrate. In a method described herein, an inductor, or two or more coupled inductors, may be formed within the unused bulk silicon substrate. Example embodiments may be used to implement various functions, such as those described hereinabove.

[0017] FIG. 1 is an illustration of an example spiral inductor 110 fabricated on the backside of a circuit substrate 101. In this example, inductor 110 has on outside endpoint 111 and in inside endpoint 112. In this example, substrate 101 is a silicon die that forms an integrated circuit and includes active circuitry that is formed on the other side of substrate 101. Example embodiments may incorporate an inductor into the unused die silicon by etching a trench into the backside of the silicon, and using the etched trench area to implement a high density, high quality factor (Q) inductor. Quality factor Q is a measure of the efficiency of an inductor; a high Q inductor indicates the inductor will be an efficient, low loss inductor.

[0018] Example embodiments intrinsically integrate inductor 110 into silicon substrate 101. This means that by three dimensional (3D) post processing on the silicon wafer, it will be possible to have a co-packaged solution without the need for complex and expensive packaging technology, such as chip-on-die, SIP, etc.

[0019] Example embodiments may be smaller in size than other known solutions. Instead of having the silicon IC and an inductor placed side by side, it will enable "vertical" integration which saves total solution silicon area.

[0020] Previous solutions may have included a laminate air core inductor or a fiberglass printed circuit board (PCB), such as grade FR4 PCB material. Another previous solution may have included a closed core chip inductor. Unfortunately, closed core inductors suffer from core saturation. Therefore, an application in which very large peak current are needed may not be viable with a closed core inductor.

[0021] Example embodiments may benefit by having much taller copper traces to provide lower DCR (direct current resistance) for the same inductance, and thereby high Q. The tall copper traces may allow very large peak currents for applications that require large peak currents. Tall copper traces may also improve ACR (alternating current resistance) by providing a better configuration for proximity effects.

[0022] As described hereinbelow, a process for forming an inductor in trenches in the bulk silicon substrate may be an inexpensive process.

[0023] FIG. 2 is an illustration of example coupled inductors fabricated on the backside of an IC substrate 201. In this example, a first spiral coil 210 surrounds a second spiral coil 212. This configuration allows a magnetic field produced by one of the coils to couple with and produce a current in the other coil. Coil 210 has endpoints 213, 214 and coil 212 has endpoints 215, 216. Various ways of coupling contact points at the coil endpoints to active circuitry on the other side of the circuit substrate are described hereinbelow.

[0024] In another embodiment, the two coils may be interleaved for improved coupling.

[0025] In another embodiment, a first coil may be formed in a first layer of the substrate, and then a second substrate layer may be formed on the first substrate layer and a second coil may then be formed in trenches in the second layer of the substrate, as described hereinbelow.

[0026] While circular spiral coils are illustrated in FIGS. 1 and 2, other embodiments may use other shapes, such as oval, rectangular, etc.

[0027] FIG. 3 is a cross-section view of example IC 300 illustrating a way of connecting a backside inductor 310 to active circuitry of IC 300. IC 300 includes a bulk silicon substrate 301 in which inductor 310 is formed in trenches, as described hereinbelow.

[0028] An epitaxial (epi) silicon layer 320 may be formed on one side of substrate 301. A thick epi layer may be beneficial for power semiconductors and MEMS-based sensors and actuators. "Thick" is a relative term. Today, epi films of more than 20μm are regarded as thick, although developmental targets for films can be as much as ~150μm in thickness. The electrical isolating qualities of the undoped thick epi films may provide a benefit for power semiconductors. They enable higher voltages with larger R(off) values, and contribute to higher switching speeds and reduced device footprints. Various transistors may be formed in epi layer 320 using known fabrication techniques.

[0029] Multiple layers of metal, such as copper, may then be formed between insulating layers such as silicon dioxide using known or later developed processes to form a multilayer interconnect 330 that connects with the various transistors to form an active circuit.

[0030] In this example, IC 300 is fabricated as a "flip chip". Flip chip is a method for interconnecting semiconductor devices, such as IC chips and micro-electromechanical systems (MEMS), to external circuitry with solder bumps 342 that have been deposited onto the chip pads. The solder bumps may be deposited on the chip pads on the top side of the wafer during the final wafer processing step. To mount the chip to package substrate 340 (e.g., a lead frame, a circuit board or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads 341 on the external circuit or leadframe 340, and then the solder is reflowed to complete the interconnect. This is in contrast to wire bonding, in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry or lead frame.

[0031] Processing a flip chip is similar to conventional IC fabrication, with a few additional steps. Near the end of the manufacturing process, the attachment pads are metalized to make them more receptive to solder. This typically consists of several treatments. More recently, a process is used in which metal posts are formed on each metalized attachment pat to extend the height of the contact. A small dot of solder may then deposited on each metalized pad. Alternatively, the solder dots may be placed on the leadframe. The chips are then cut out of the wafer as normal.

[0032] To attach the flip chip into a circuit, the chip is inverted to bring the solder dots down onto connectors on the underlying leadframe or circuit board. The solder is then re-melted to produce an electrical connection, typically using a Thermosonic bonding or alternatively a reflow solder process.

[0033] In this embodiment, a wire bonding process may be used to couple inductive coil 310 to the active circuitry in the epi layer 320 of IC 300. In this example, wire bond 343 couples an outside end point 311 of coil 310 to contact pad 345 on package substrate 340. Similarly, wire bond 344 couples an inside end point 312 of coil 310 to contact pad 346 on package substrate 340. Copper or other types of metal, traces may then couple contact pads 345, 346 to other contact pads 341 and thereby to active circuitry within epi layer 320.

[0034] In another example, bonding clips may be used to couple inductive coil 310 to the active circuitry in the epi layer 320 of IC 300. Bonding clips are larger than bond wires and provide much larger current carrying capacity.

[0035] FIG. 4 is a cross-section view of example IC 400 illustrating another way of connecting a backside inductor 410 to active circuitry of IC 400. IC 400 includes a bulk silicon substrate 401 in which inductor 410 is formed in trenches, as described hereinbelow.

[0036] As described hereinabove, epi layer 420 may be formed on one surface of bulk substrate 401. Various transistors may be fabricated in epi layer 420 to form active circuitry that is interconnected by a multilayer interconnect 430.

[0037] In this example, the silicon die is mounted upright on a package substrate 440 that may be a lead frame or other type of substrate such as a circuit board. Solder bump 443 may be used to couple an outside end of coil 410 to a pad on substrate 440. Similarly, solder bump 444 may be used to couple an inside end of coil 410 to a pad on substrate 440.

[0038] Wire bonds 441, 441 may then couple from leads on substrate 440 to pads 446 on interconnect layer 430 and thereby to transistors with epi layer 420. Similarly, additional wire bonds (not shown) may couple from other pads in interconnect layer 530 to substrate 440 in order to route other signals to/from the active circuitry in epi layer 420.

[0039] FIG. 5 is a cross-section view of example IC 500 illustrating another way of connecting a backside inductor 510 to active circuitry of IC 500. IC 500 includes a bulk silicon substrate 501 in which inductor 510 is formed in trenches, as described hereinbelow.

[0040] As described hereinabove, epi layer 520 may be formed on one surface of bulk

substrate 501. Various transistors may be fabricated in epi layer 520 to form active circuitry that is interconnected by a multilayer interconnect 530.

[0041] In this example, "through silicon vias" (TSV) are used to interconnect the backside inductor 510 with active circuitry in epi layer 520. For example, TSV 541 may be used to couple an outside end of coil 510 to a pad in interconnect layer 530 and thereby to active circuitry in epi layer 530. Similarly, TSV 542 may be used to couple an inside end of coil 510 to a pad in interconnect layer 530 and thereby to active circuitry in epi layer 530.

[0042] In some embodiments, additional TSVs, such as any of TSVs 543 may be used to connect additional contact points on the various loops of inductor 510 to active circuitry in epi layer 530. For example, this may allow configuring the coil for various needs using switch transistors. Various implementations may include: tuning of the coil by enabling fewer or more turns, configuring turns in parallel, etc.

[0043] In some embodiments, IC 500 may be packaged using flip chip technology to complete the remaining connections between the active circuitry in epi layer 520 and the lead frame or substrate, similar to FIG. 3. In other embodiments, IC 500 may be mounted on a leadframe or substrate in a conventional top up configuration in which bond wires may be used to complete the remaining connections between the active circuitry in epi layer 520 and the leadframe or substrate, similar to FIG. 4. Other embodiments may use other known or later developed packaging and interconnect technology to interconnect to IC 500, while TSVs are used to connect one or more backside coils to active circuitry on the front surface of the substrate.

[0044] FIGS. 6A-6G are cross-sectional views of a portion of a silicon wafer 601 illustrating a method for forming an inductive component on the backside of an IC, as described hereinabove. The method may be performed to the backside of a silicon wafer after the front side has been processed to fabricate an array of integrated circuits. Alternatively, the backside inductive components may be formed first and then the active circuitry may be fabricated on the front surface of the silicon wafer.

[0045] Conventional processes exist for fabricating semiconductor circuitry on a silicon wafer. Typically, hundreds of IC dies are fabricated on a single silicon wafer. The completed circuits may then be tested using test probes to activate on monitor the individual circuit die. The wafer may then be cut into individual dies, attached to a leadframe or other substrate, packaged and final tested using known or later developed processes.

[0046] FIGS. 6A-6F illustrate only the backside of a silicon wafer 601. Circuitry on the front side is not shown for simplicity, or may not be there yet. FIG. 6A illustrates a portion of a silicon wafer 601 that forms a substrate. A layer 650 of silicon dioxide is deposited on the back surface of substrate 601. A resist layer 652 is applied over silicon dioxide layer 650 and may be patterned using known or later developed photolithography process to form a mask for the next step of deep silicon etch. The mask may be patterned to form a spiral or other shape trench, or multiple spirals for one or more backside inductors, such as shown in FIGS. 1 and 2.

[0047] FIG. 6B illustrates an example trench that may be formed in the bulk silicon of substrate 601 using one of several process, such as a deep reactive ion etch or a Bosch silicon etch. Initially, a chemical etch of the hard mask layer 650 may be performed using photo mask layer 652. The Bosch process, named after the German company Robert Bosch GmbH, is also known as pulsed or time-multiplexed etching. The Bosch process alternates repeatedly between two modes to achieve nearly vertical structures. The first mode is a standard nearly isotropic plasma etch. The plasma contains ions which attack the wafer from a nearly vertical direction. Sulfur hexafluoride [SF6] is often used for silicon. The second mode is deposition of a chemically inert passivation layer. For example, C4F8 (Octafluorocyclobutane) gas yields a substance similar to Teflon.

[0048] Each phase lasts for several seconds. The hard mask 650 on the surface and the passivation layer on the sides of the trench protects the entire substrate from further chemical attack and prevents further etching. However, during the etching phase, the directional ions that bombard the substrate attack the passivation layer at the bottom of the trench, while leaving the sides generally unaffected. The ions collide with the passivation layer at the bottom of the trench and sputter it off, exposing the substrate at the bottom of the trench to the chemical etchant. These etch/deposit steps are repeated many times resulting in a large number of very small isotropic etch steps taking place only at the bottom of the etched pits. For example, to etch a 500 um deep trench in a silicon wafer, 100–1000 etch/deposit steps may be needed. The two-phase process may cause the sidewalls to undulate, such as with an amplitude of about 100–500 nm. The cycle time may be adjusted: short cycles yield smoother walls, and long cycles yield a higher etch rate.

[0049] For example, trenches 654 for embodiments of a backside inductor may be etched to a depth of 25-500 um for a silicon substrate that is approximately 750 um thick. A tradeoff may

exist in depth of the trench versus diameter of the coil and thickness of the substrate, in order to maintain adequate bulk material for mechanical strength of the substrate.

[0050] FIG. 6C illustrates substrate 601 after cleaning the wafer, stripping off photolithographic resist layer 652 and removing the passivation layer polymers used during formation of trenches 654.

[0051] FIG. 6D illustrates substrate 601 after forming a dielectric surface isolation 655 on the inside of trench 654. Various compounds may be used to form dielectric surface isolation 655, such as: an atomic layer deposition (ALD) of Al2O3, silicon nitride, silicon dioxide, or other non-conductive dielectric materials.

[0052] FIG. 6E illustrates substrate 601 after forming a metal seed layer 656 over the surface of the substrate 601 and trench 654. Metal seed layer 656 may be selected from various metallic compounds, such as: titanium nitride (TiN), titanium tungsten (TiW), etc. using a known or later developed process, such as atomic layer deposition.

[0053] FIG. 6F illustrates substrate 601 after forming a copper fill layer 657 using a plating process in which the copper plating adheres to the metallic seed layer 656.

[0054] FIG. 6G illustrates a nearly complete IC 600 after a backside grind process is used to remove the surface portion of metal plate 657, along with mask layer 650 to form a smooth surface 658 on the backside of substrate 601.

[0055] An epi layer 620 that includes various transistors and interconnect layer 630 are also illustrated in FIG. 6G on the front side of substrate 601. As described hereinabove, the active circuitry in epi layer 620 and interconnect layer 630 may be fabricated either before or after the backside inductor 654 is formed.

[0056] Connections between backside inductor and active circuitry in epi layer 620 may be completed in various manners, such as those illustrated in FIG. 3, 4 or 5.

[0057] FIG. 7A illustrates an alternative embodiment in which a seed layer 756 is deposited using a printer in place of metallic seed layer 656 illustrated in FIG. 6E. FIG. 7A illustrates an inkjet printer 760 depositing a series of droplets 761 that contain metal nanoparticles into trench 654. Ink jet printers or similar printers can "print" various polymer materials to fabricate three dimensional structures. For example, see "3D printing," Wikipedia, Sept 4, 2014. Printing allows for the rapid and low-cost deposition of thick dielectric and metallic layers, such as 100 um – 1000 um thick, while also allowing for fine feature sizes, such as 20um feature sizes.

[0058] The ink may include a solvent or several solvents to match rheology and surface tension, and metallic nanoparticles. For example, the size of the nanoparticle may be in a range of 2-100nm. The ink may also include a dispersant such as polyvinylpyrrolidone (PVP) or be charge dispersed to prevent agglomeration of the particles. The ink may also include binders such as polymer epoxies, and other known or later developed ink additives.

[0059] The film residue that is left from the ink may then be cured in the case of solvent or dispersant based ink where solvent or dispersant is evaporated. Curing may be thermal (50-250C or higher), UV, Infrared, Flash Lamp, or of another form that is compatible with the ink being used.

[0060] In this example, the metal nanoparticles that form seed layer 756 may be copper, TiN, or TiW.

[0061] FIG. 7B illustrates substrate 701 after forming a copper fill layer 757 using a plating process in which the copper plating adheres to the metallic seed layer 756. In this example, because the plating process adheres only to the seed layer in the bottom of the trenches 654, no copper plating is deposited on the surface of substrate 601. Therefore, a backside grind process as illustrated in FIG. 6G is not required in this embodiment.

[0062] In another embodiment, the entire trench 654 may be filled with copper using an inkjet process.

[0063] FIGS. 8A-8B illustrate simulation results for an example backside inductor similar to those described hereinabove. In this simulation, the inductor has a diameter of 5mm and has a spiral coil with two turns. The simulated trenches are 150um deep and 70um wide, with 150um trench spacing. As illustrated in FIG. 8A, at 10 MHz the inductance is approximately 18nH. As illustrated in FIG. 8B, at 10 MHz the Q is approximately 16. The DC resistance is approximately 36mOhm.

[0064] FIGS. 8A-8B illustrate that the performance of the backside inductor is reasonably stable over a frequency range of 1-100 MHz.

[0065] FIG. 9 illustrates another embodiment of an IC 900 with inductors formed in multiple substrate layers. In this example, an inductor 910 may be fabricated in a first substrate layer 901 as described hereinabove and interconnected to active circuitry in epi layer 920 and interconnect layer 930 using TSVs, such as TSVs 941, 942. For example, additional connections may be made using one or more TSV 943.

[0066] In this embodiment, a second wafer with substrate layer 961 may be bonded to the first substrate layer 901. For example, an insulative layer 960 (such as silicon dioxide) may be formed on both wafers, and then the two wafers may be stacked with the insulative layers together and bonded in a furnace to create a single wafer.

[0067] A second inductor 911 may then be formed in the second substrate layer 961 as described hereinabove. The second inductor 911 may be coupled to lead frame or other substrate 940 via bumps 944, 945 and thereby to active circuitry in epi layer 920 using wire bonds 946 to pads 947, such as described hereinabove in connection with FIG. 4.

[0068] In another embodiment, IC 900 may be package as a flip chip, such as described in connection with FIG. 3.

System Example

[0069] FIG. 10 is a block diagram of an example system 1000 that includes an IC 1001 with a backside inductor. In this example, active circuitry 1020 is coupled to inductor 1010 which is formed on the backside of IC 1001. For example, inductor 1010 may be coupled to active circuitry 1020 using any of the techniques described hereinabove in connection with FIGS. 3-5.

[0070] System 1000 may use inductor 1010 for various functions, such as: filter output voltage and current; store energy that is delivered cycle by cycle; provide an efficient way to move energy from two or more voltage domains; perform auxiliary functions such as providing adiabatic gate drivers and zero voltage transitions; etc.

[0071] In some embodiments, a second inductor 1012 may be included that is coupled to active circuitry 1022. Inductor 1012 may also be formed on the backside of IC 1001 as described in more detail hereinabove. For example, inductor 1012 may be coupled to active circuitry 1022 using any of the techniques described hereinabove in connection with FIGS. 3-5.

[0072] In this example, inductor 1010 is configured to inductively couple to inductor 1012. In another example, only one of the inductors may be present.

[0073] Also, for example, system 1000 may use both inductors 1010 and 1012 to provide transformer isolation.

[0074] System 1000 may include additional ICs and other components mounted on a system substrate 1002 to provide a particular function using known or later developed techniques. For example, system substrate 1002 may be a printed circuit board.

[0075] FIG. 11 is a block diagram of an example system that includes an IC 1100 with a

backside inductor created in substrate 1101 using 3D printing that may produce multiple metallization layers 1170, 1172. Active circuitry may be fabricated on the front side of substrate 1101 in an active layer 1120, as described hereinabove. In this example, a spiral trench 1110 may be fabricated as described hereinabove. A copper seed layer may then be 3D printed, as described in more detail with reference to FIG. 7A, seed layer 756. A copper fill layer 1170 may then be fabricated using a plating process, as described in more detail with reference to FIG. 7B, fill layer 757. In this example, fill layer 1170 may be stopped when trench 1110 is only partially filled.

[0076] An insulator layer 1171 may then be 3D printed within trench 1110 to cover and insulate copper fill layer 1170. Then, a second seed layer and fill layer 1172 may be fabricated in a similar manner. In this example, another insulator layer 1173 may be 3D printed within trench 1110 to cover and insulate copper fill layer 1172. Contact pads (such as pad 1174, 1175) may be provided by 3D printing a conductive column. Alternatively, copper fill layer 1172 may extend to the surface of substrate 1101, similar to copper fill layer 757 in FIG. 7B.

[0077] Depending on a chosen thickness for each copper fill layer 1170, 1172 and the depth of trench 1110 in substrate 1101, two or more layers of inductive coils may be fabricated in this manner. In this example, two separate coils 1170 and 1172 are illustrated. For example, silicon substrate 1101 may be approximately 300um thick, while each copper fill layer 1170, 1172 is approximately 100 um thick. TSV 1176, 1177 may be provided to connect a lower coil 1170 to active circuitry in layer 1120 as described in more detail with reference to FIG. 5, while bond wires, bond clips, etc may be used to couple coil 1172 to active circuitry in layer 1120 as described in more detail with reference to FIGS. 3, 4. In this example, the inductive structure 1170, 1172 has a radius of approximately 1mm and is coupled to switching circuitry in active layer 1120 that switches at a frequency of approximately 5 MHz.

[0078] In another example, a coil formed by copper fill layer 1170 may be connected in series with a coil formed in copper fill layer 1172 to form a single coil by 3D printing a contact between the two coils.

Other Embodiments

[0079] Embodiments of backside inductors formed in a silicon substrate have been described herein, but other embodiments of one or more inductors formed on the backside of a semiconductor substrate and interconnected with active circuitry on a front side of the

semiconductor substrate may be implemented using other types of semiconductor substrates, such as Germanium, Carbon, Antimony, Gallium Arsenide, Gallium Nitride, etc. In another embodiment, a non-semiconductor substrate such as glass or sapphire may be used.

[0080] In another embodiment, the IC may be based on a "silicon on insulator" technology, and the backside inductor may be formed in the insulator layer if a bulk insulator is used. For example, the insulator may be sapphire in a "silicon on sapphire" technology. In this case, one or more backside inductors may be formed in the sapphire substrate. For a silicon-insulator-silicon technology, one or more backside inductors may be formed in the bulk silicon portion of the substrate.

[0081] Copper is described herein for forming the conductive coils of a backside inductor, but other conductive metals, compounds, or polymers may be used to form the coils, such as: silver, gold, tin, carbon, graphite, polysilicon, etc.

[0082] A plating process for forming the coils is described herein, but other embodiments may form the coils using a spun on slurry to fill the trenches. Other known or later developed techniques for metal deposition may be used to fill the trenches.

[0083] A thick epi layer in which the circuit transistors are formed is described herein, but other embodiments may use a thin epi layer, or no epi layer, depending on the semiconductor process being used to form the active circuitry. In any case, as use herein, the term "active circuitry located on the front side surface" refers to circuitry that may (or may not) be formed in an epi layer. Also, for example, it refers to circuitry that may be covered by one or more interconnect layers and by one or more additional protective layers.

[0084] A circular spiral trench is described herein, but other embodiments may use other configurations for the backside coils, such as oval, square/rectangular, etc.

[0085] Components in digital systems may be referred to by different names and/or may be combined in ways not shown herein without departing from the described functionality. In this description, the term "couple" and derivatives thereof mean an indirect, direct, optical and/or wireless electrical connection. Thus, if a first device couples to a second device, that connection may be through a direct electrical connection, through an indirect electrical connection via other devices and connections, through an optical electrical connection, and/or through a wireless electrical connection. Also, where the term "couple" is used in reference to coupling two coils, that usage refers to electromagnetic coupling.

[0086] Although method steps may be presented and described herein in a sequential fashion, one or more of the steps shown and described may be omitted, repeated, performed concurrently, and/or performed in a different order than the order shown in the drawings and/or described herein. Accordingly, example embodiments are not limited to the specific ordering of steps shown in the drawings and/or described herein.

[0087] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:

a circuit substrate having a front side and an opposite backside;

active circuitry located on the front side; and

an inductive structure embedded within a deep trench formed in the circuit substrate on the backside.

2. The IC of claim 1, further including multiple inductive structures embedded in the circuit substrate on the backside configured to inductively couple to each other.

3. The IC of claim 1, wherein the inductive structure is connected to the active circuitry by through silicon vias in the circuit substrate.

4. The IC of claim 1, further including a package substrate, wherein the circuit substrate is mounted on the package substrate such that contact pads of the active circuitry are bump bonded to leads on the package substrate, and wherein the inductive structure is connected to the active circuitry via wire bonds from the leads to contact points on the inductive structure.

5. The IC of claim 1, further including a package substrate, wherein the circuit substrate is mounted on the package substrate such that contact points on the inductive structure are bump bonded to leads on the package substrate, and wherein wire bonds couple the active circuitry to the leads and thereby to the inductive structure.

6. The IC of claim 1, wherein the deep trench has a depth in the range of approximately 25-500um.

7. The IC of claim 1, wherein the deep trench is at least four times as deep as it is wide.

8. The IC of claim 2, wherein the circuit substrate includes a first substrate layer and a second substrate layer separated by an insulating layer, wherein a first one of the multiple inductive structures is formed in the first substrate layer, and wherein a second one of the multiple inductive structures is formed in the second substrate layer.

9. The IC of claim 1, wherein the circuit substrate is a silicon-on-insulator substrate, and wherein the trench is formed in an insulator portion of the circuit substrate.

10. The IC of claim 4, wherein the package substrate is a lead frame.

11. A system comprising:

a system substrate; and

an integrated circuit (IC) mounted on the system substrate, wherein the IC includes:

a circuit substrate having a front side surface and an opposite backside surface;

active circuitry located on the front side surface; and

an inductive structure located within a deep trench formed in the circuit substrate below the backside surface, wherein the inductive structure is coupled to the active circuitry.

12. The system of claim 11, further including a package substrate, wherein the inductive structure is coupled to the active circuitry via the package substrate.

13. A method for making an integrated circuit having an integrated inductive component, the method comprising:

fabricating active circuitry on a front side of a circuit substrate of the integrated circuit (IC);

etching a deep trench into a backside of the circuit substrate;

filling the trench with an electrically conductive material to form a coil; and

coupling the coil to the active circuitry.

14. The method of claim 13, wherein etching a deep trench forms multiple deep trenches for multiple coils configured to inductively couple to each other.

15. The method of claim 13, further including forming through silicon vias (TSV) to couple the coil to the active circuitry.

16. The method of claim 13, further including:

mounting the circuit substrate on a package substrate such that contact pads of the active circuitry are bump bonded to leads on the package substrate; and

connecting the inductive structure to the active circuitry via wire bonds from the leads to contact points on the inductive structure.

17. The method of claim 13, further including:

mounting the circuit substrate on a package substrate such that contact points on the inductive structure are bump bonded to leads on the package substrate; and

coupling the active circuitry to the leads with wire bonds and thereby to the inductive structure.

18. The method of claim 13, wherein the deep trench is etched to a depth within a range of approximately 25-500um.

19. The method of claim 14, wherein the circuit substrate includes a first substrate layer and a second substrate layer separated by an insulating layer, and wherein a first one of the multiple coils is formed in the first substrate layer; and further including:

etching a second deep trench into the second substrate layer;

filling the second trench with an electrically conductive material to form a second coil; and

coupling the second coil to the active circuitry.

20. The method of claim 13, wherein the circuit substrate is a silicon-on-insulator substrate, and wherein the trench is etched in an insulator portion of the circuit substrate.

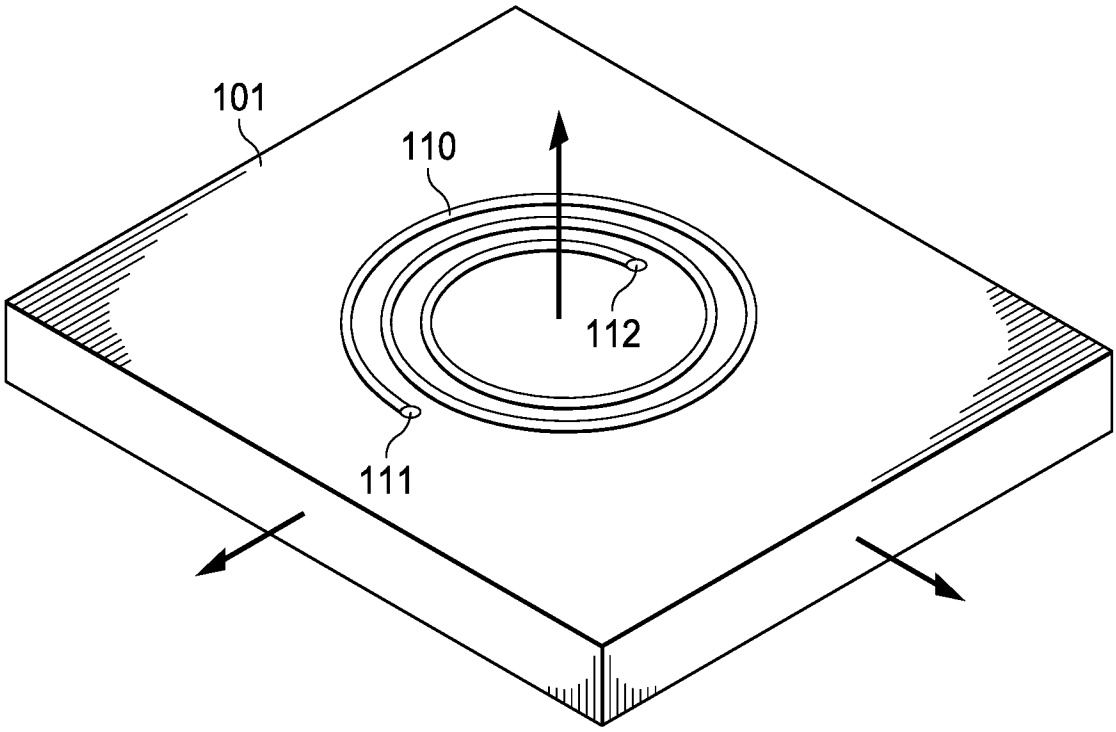

FIG. 1

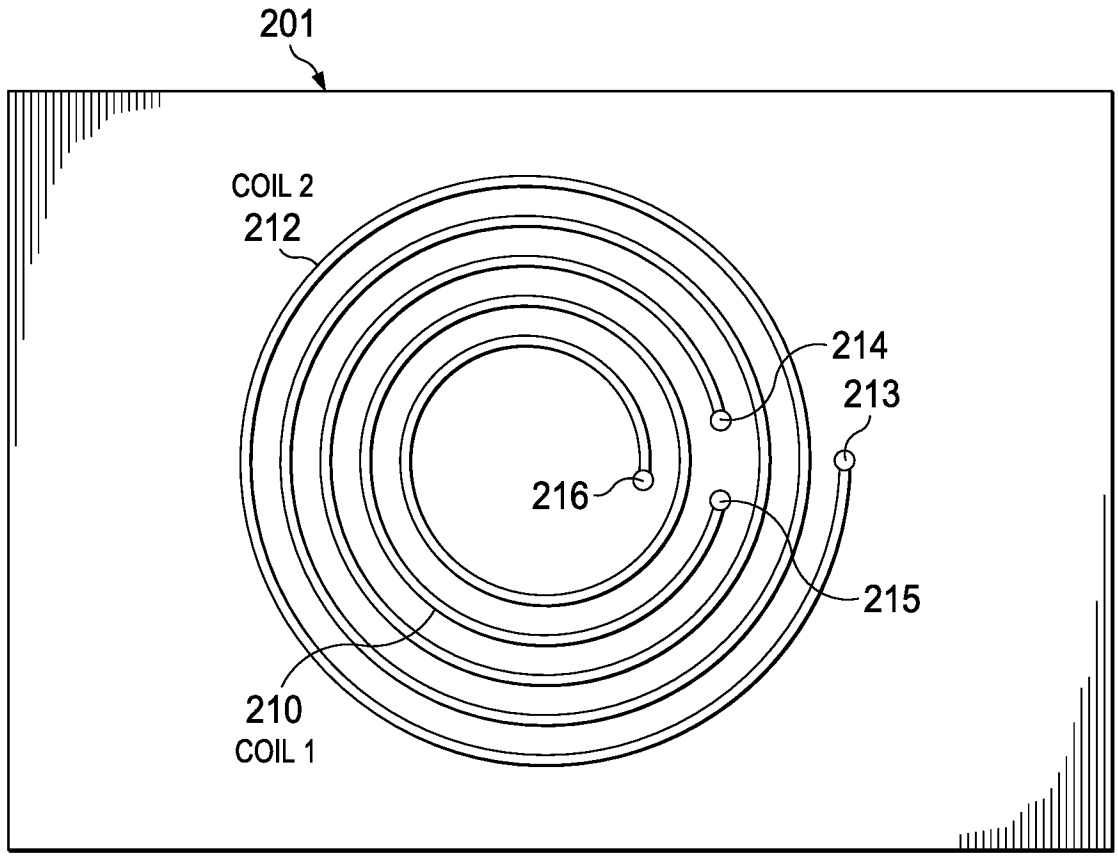

FIG. 2

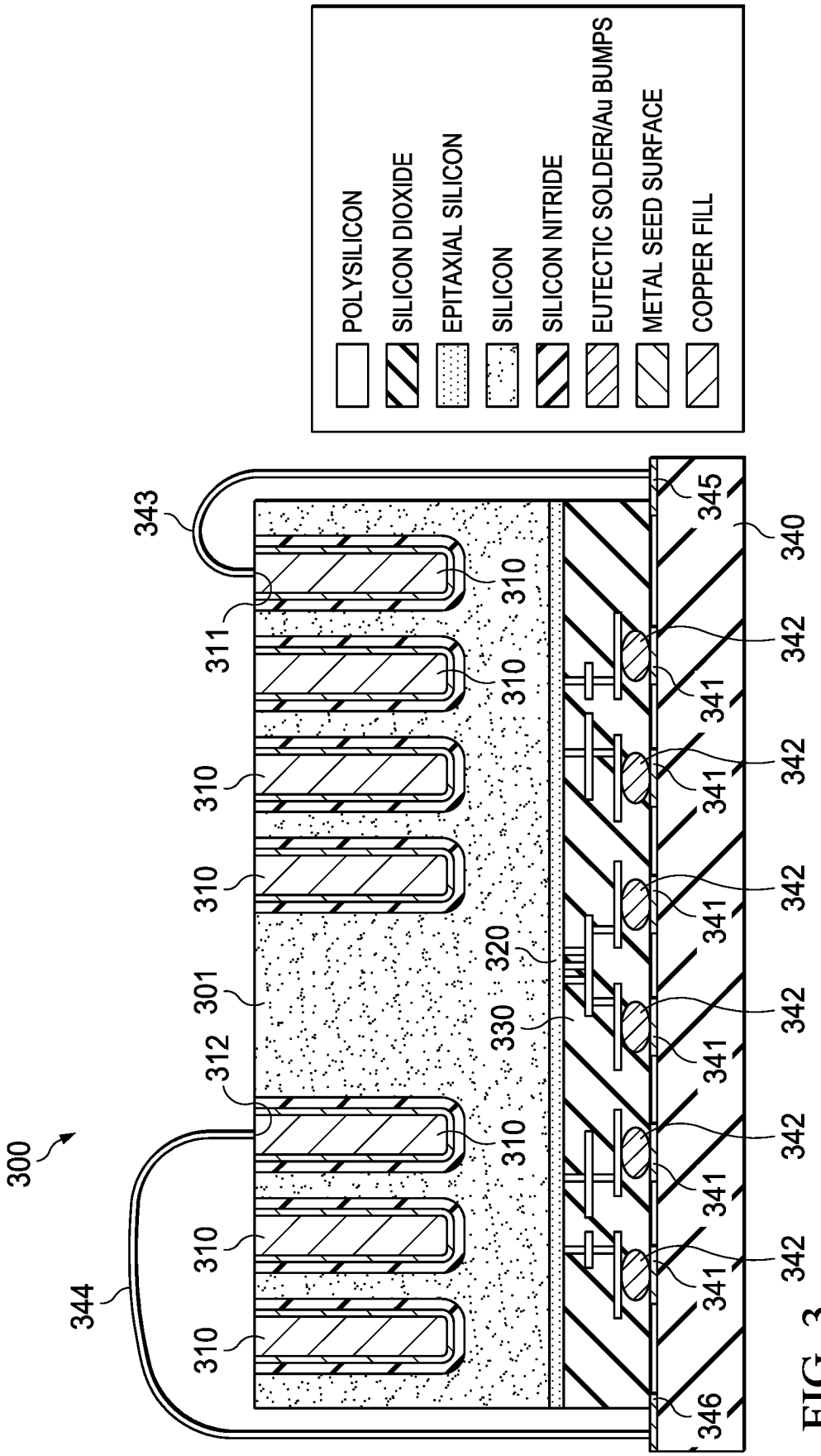
POLYSILICON
SILICON DIOXIDE
EPITAXIAL SILICON
SILICON
SILICON NITRIDE
EUTECTIC SOLDER/Au BUMPS
METAL SEED SURFACE
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FIG. 3

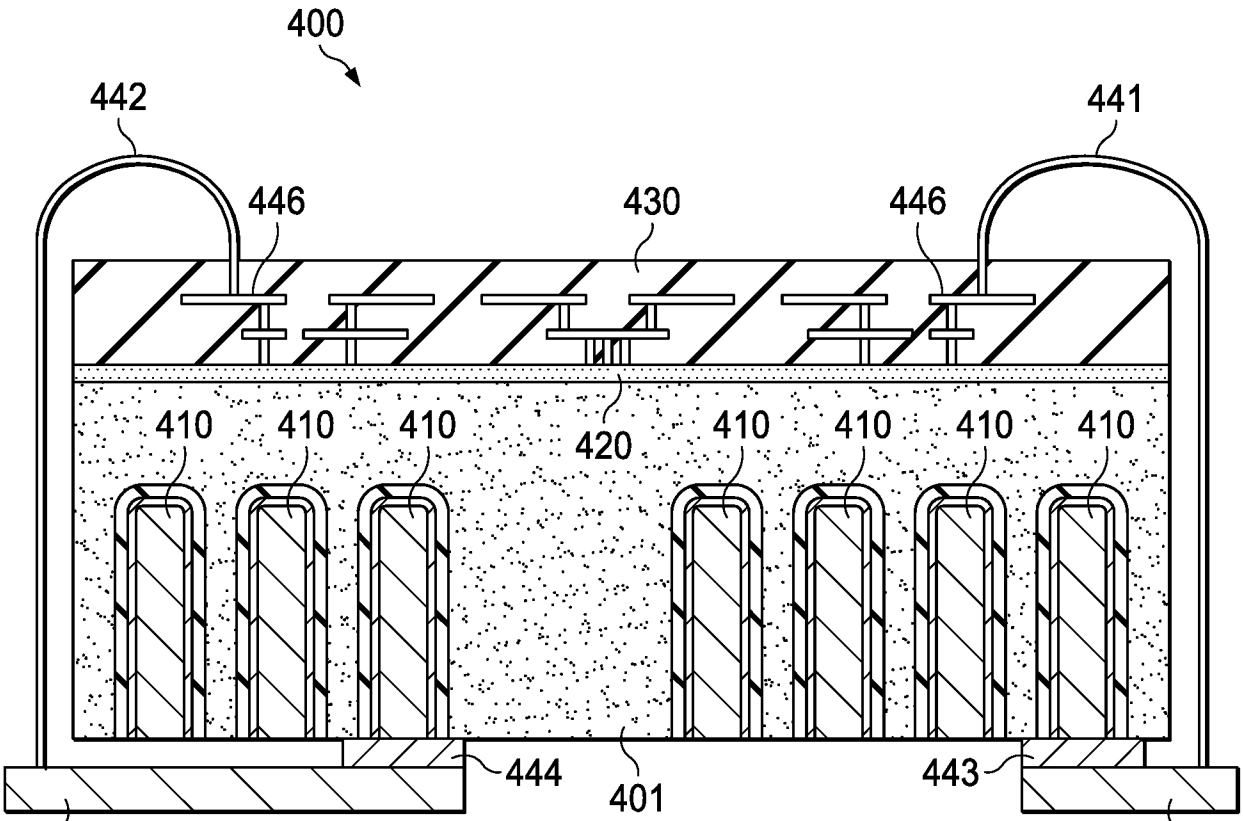
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FIG. 4

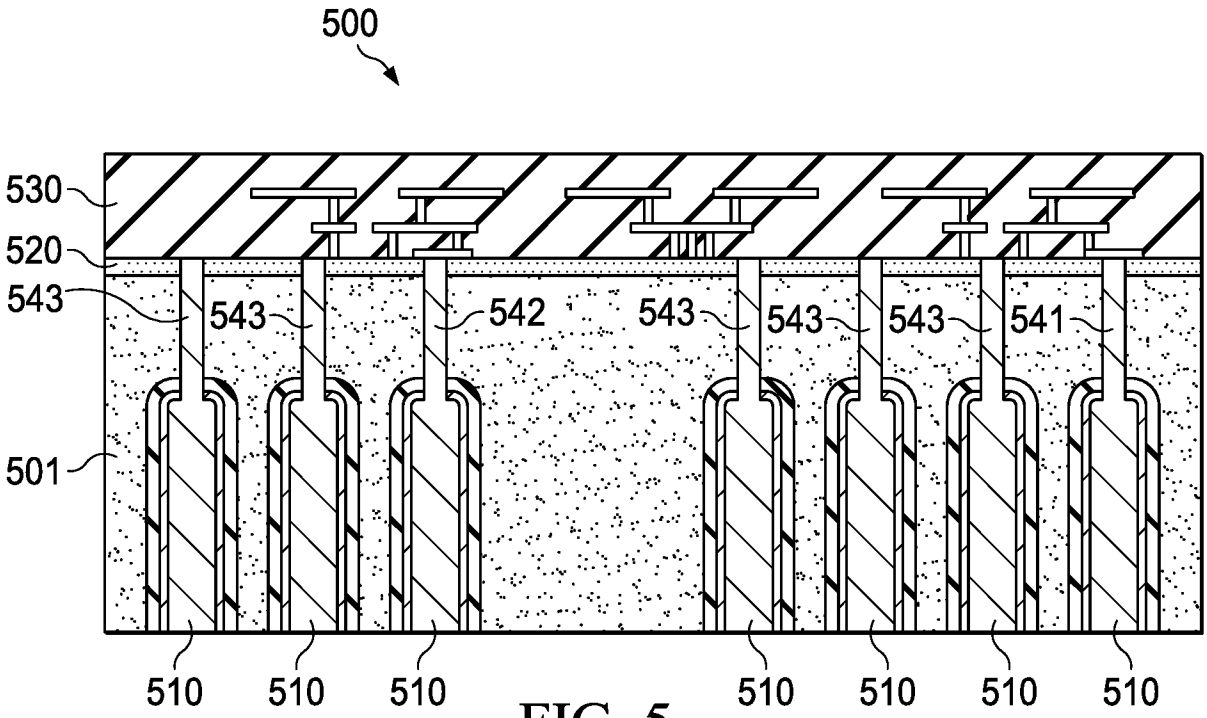
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FIG. 5

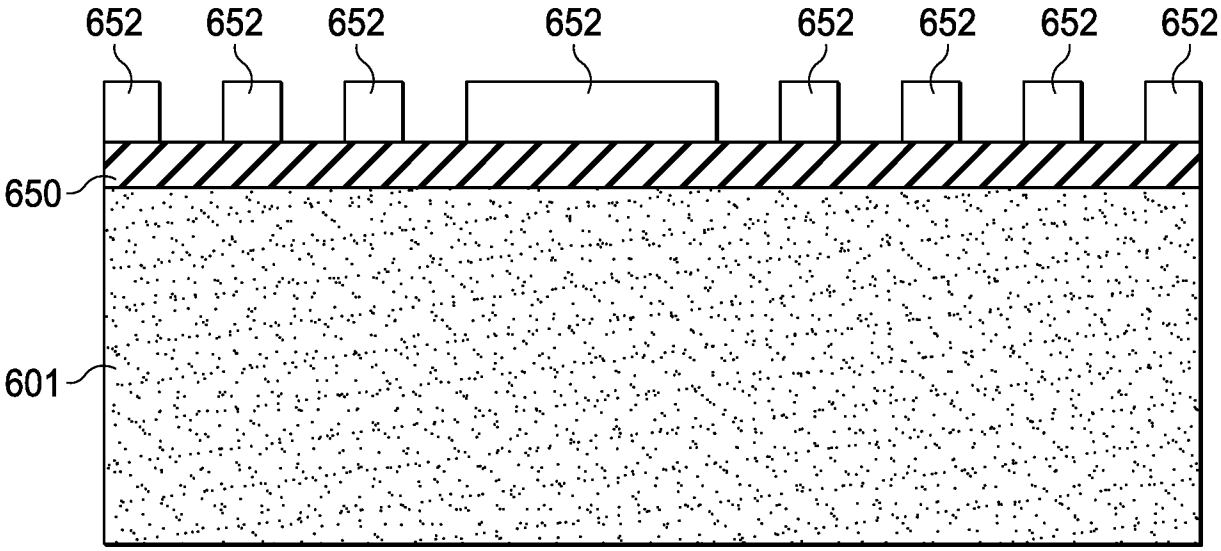
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FIG. 6A

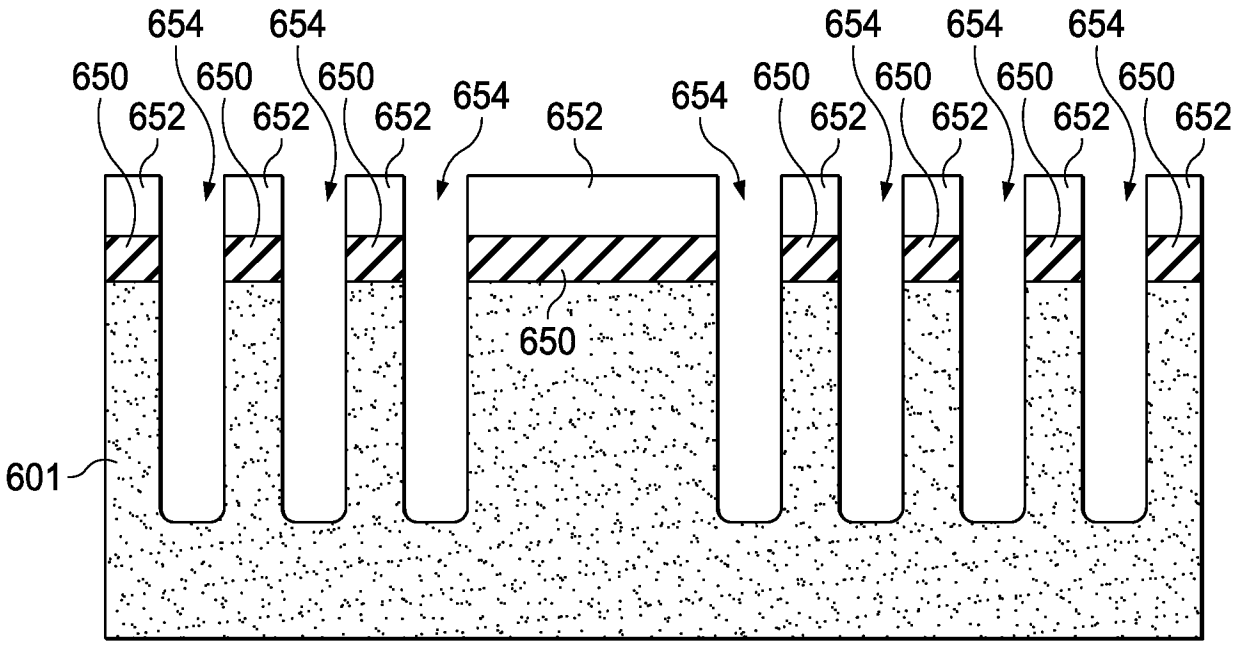
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FIG. 6B

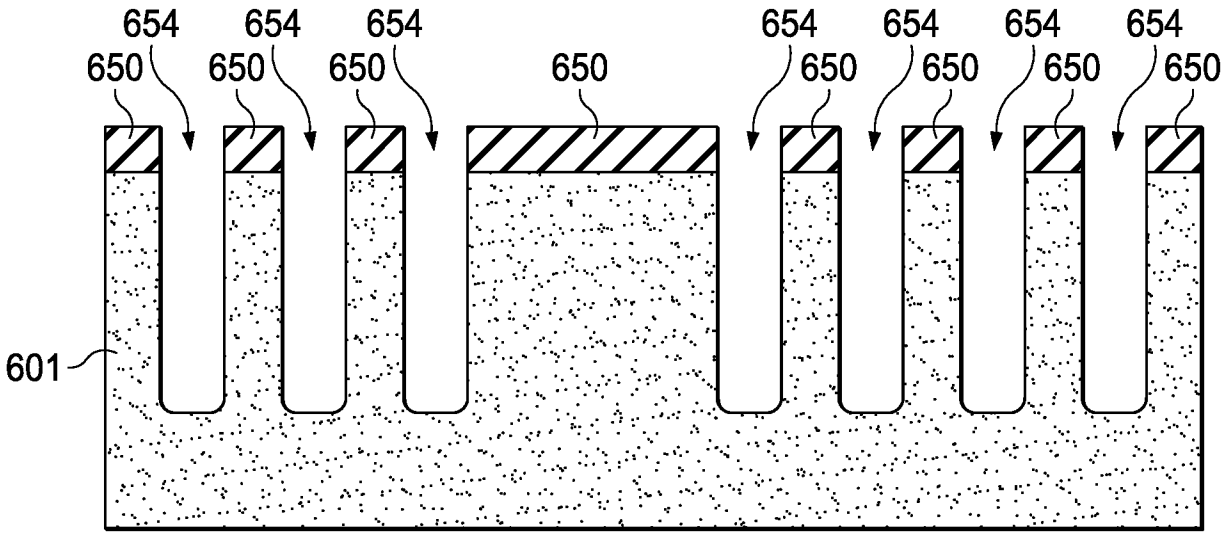
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FIG. 6C

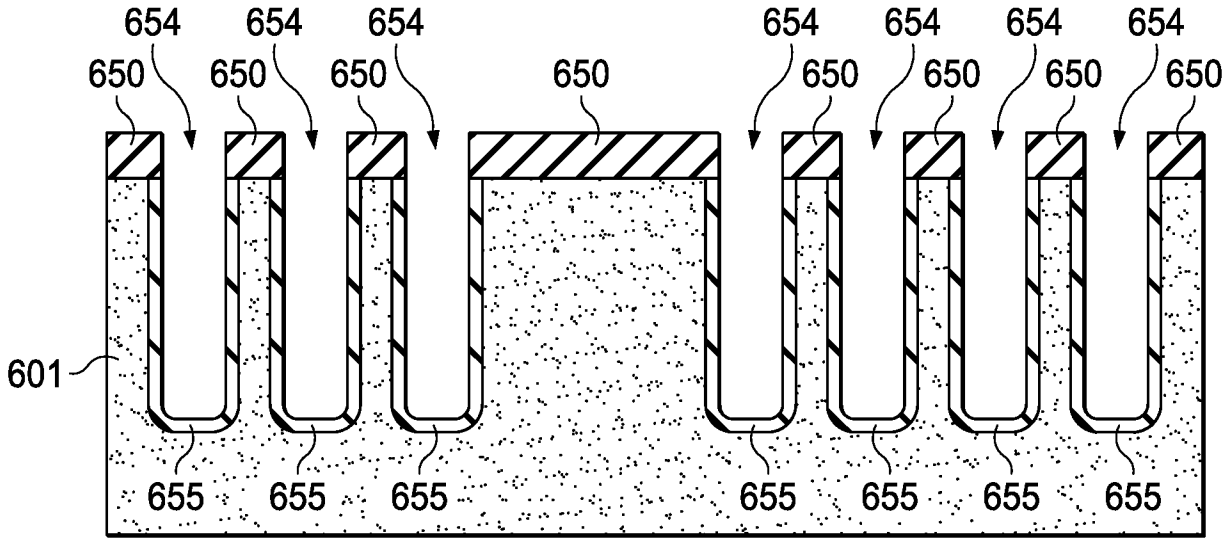
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FIG. 6D

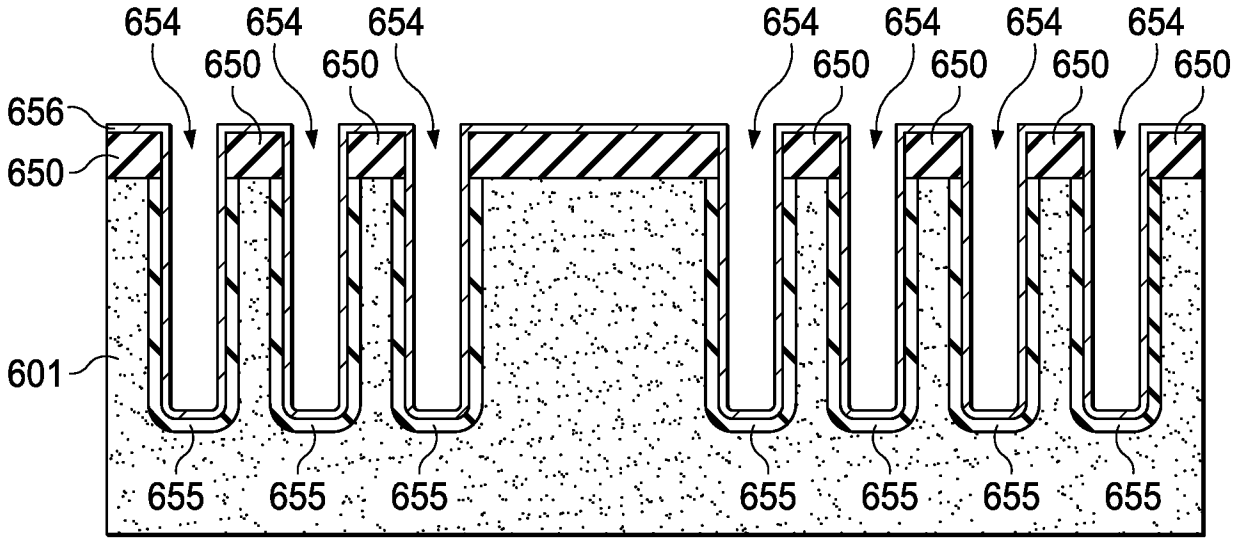
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FIG. 6E

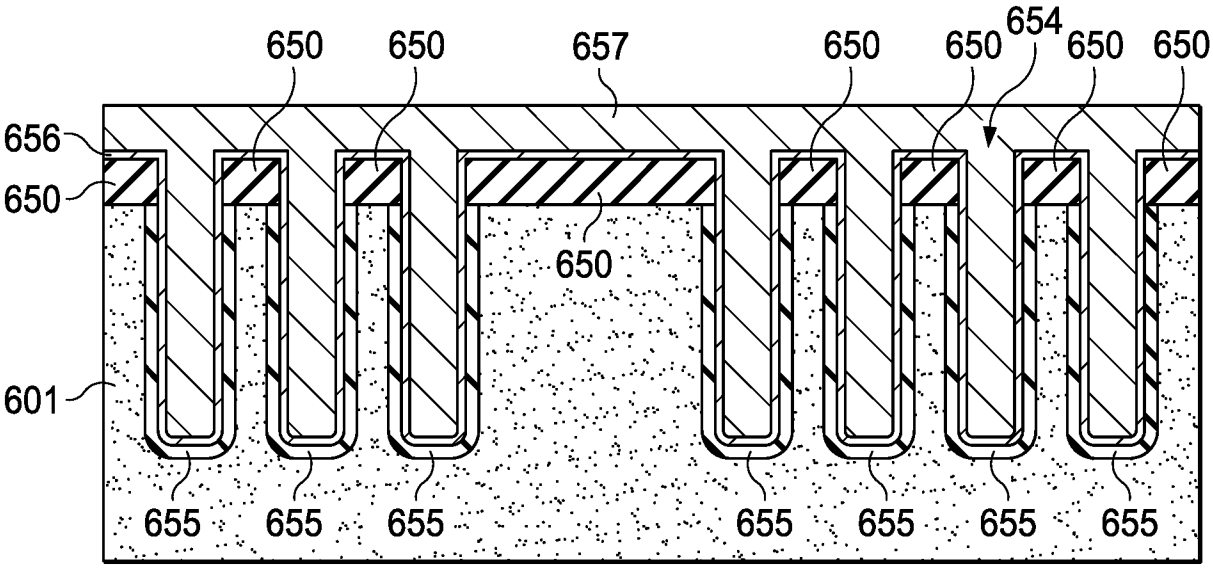
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FIG. 6F

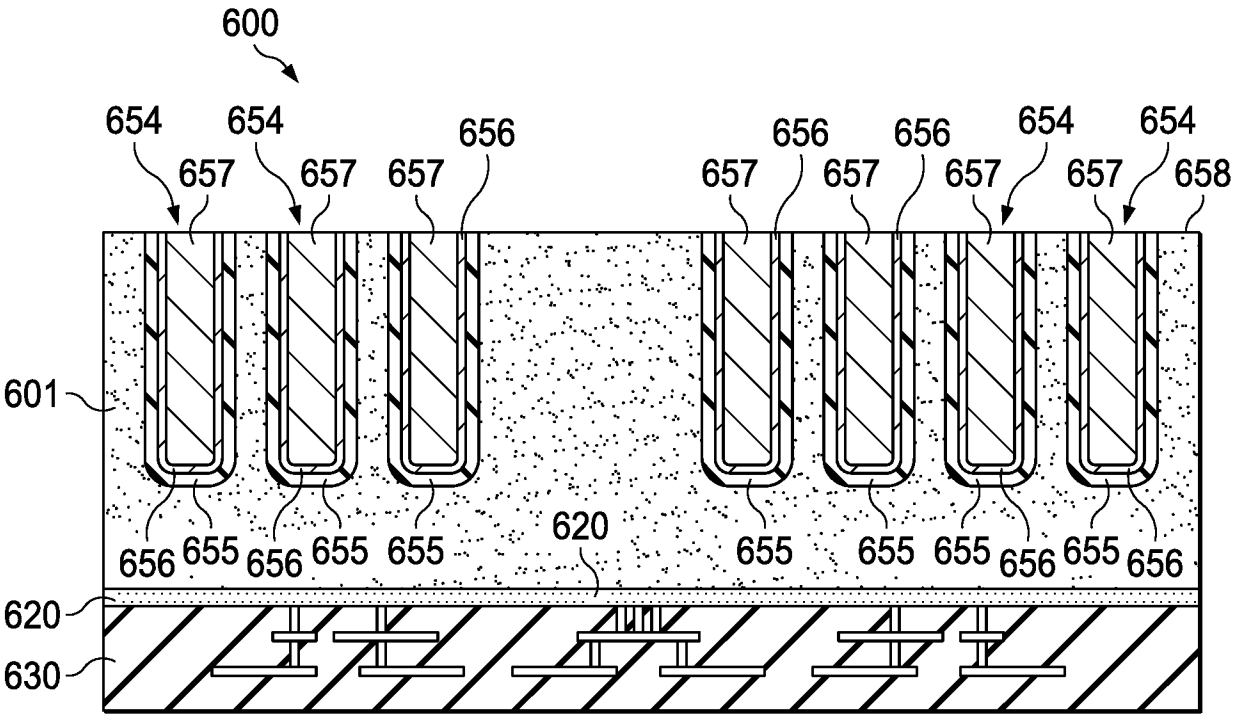
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FIG. 6G

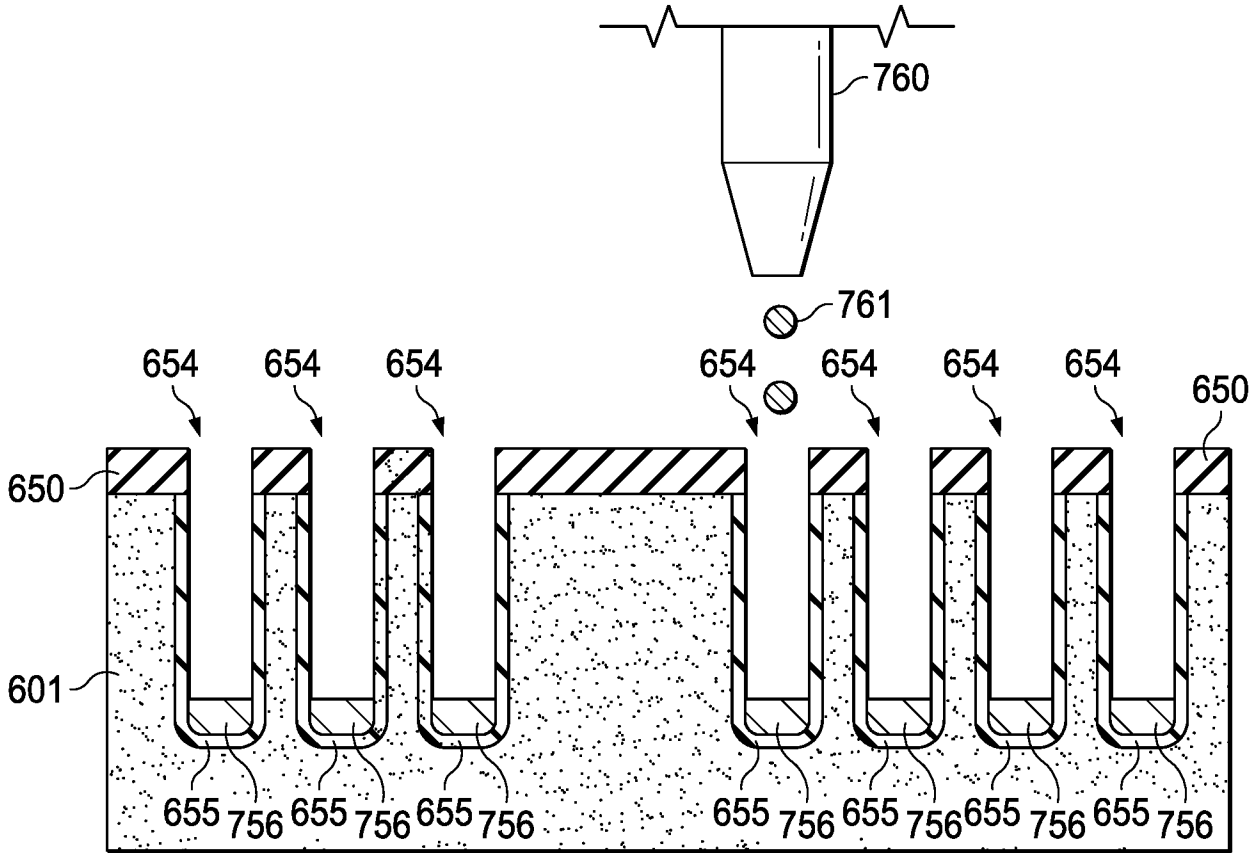
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FIG. 7A

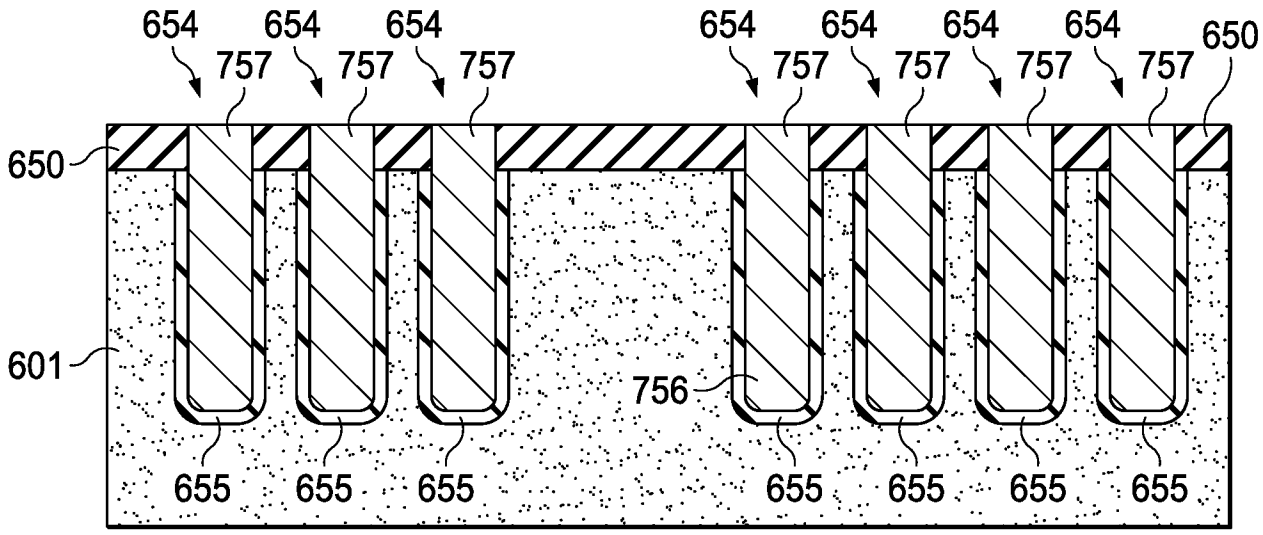
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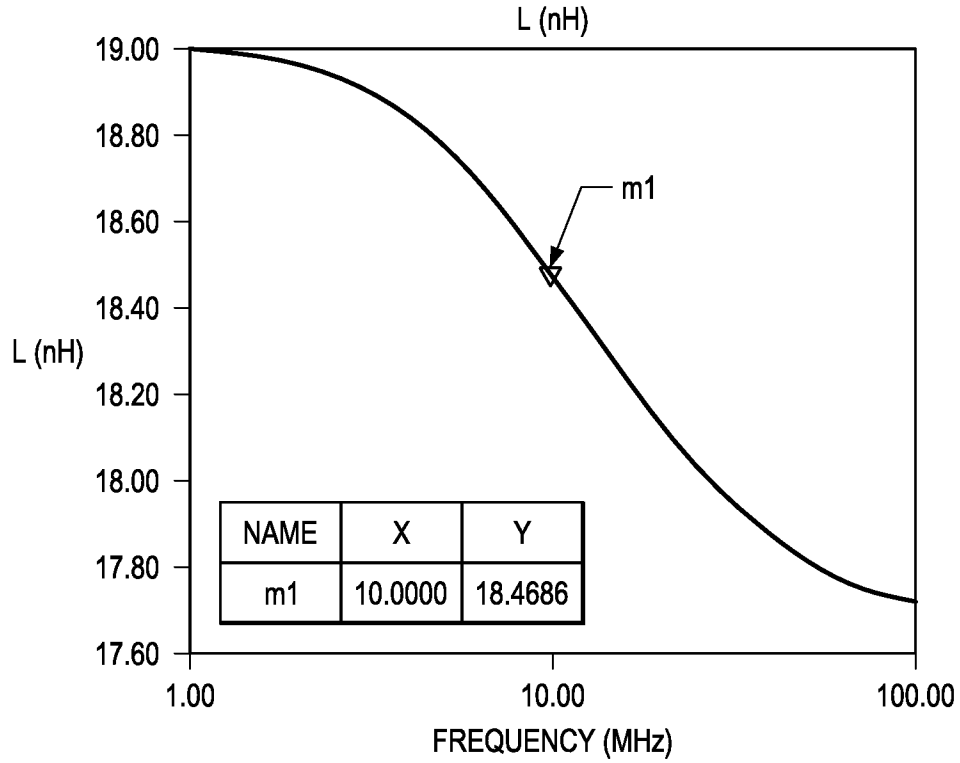
FIG. 7B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18.60
18.40
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18.00
17.80
17.60
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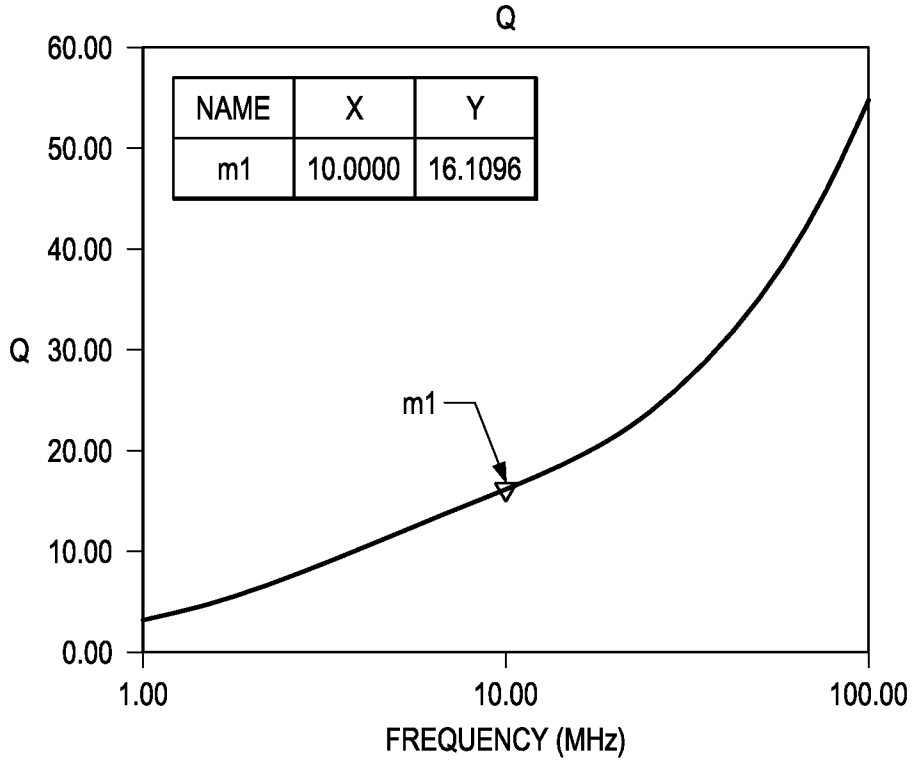
1.00
10.00
100.00
FREQUENCY (MHz)

FIG. 8A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Q
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m1 10.0000 16.1096
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10.00
100.00
FREQUENCY (MHz)

FIG. 8B

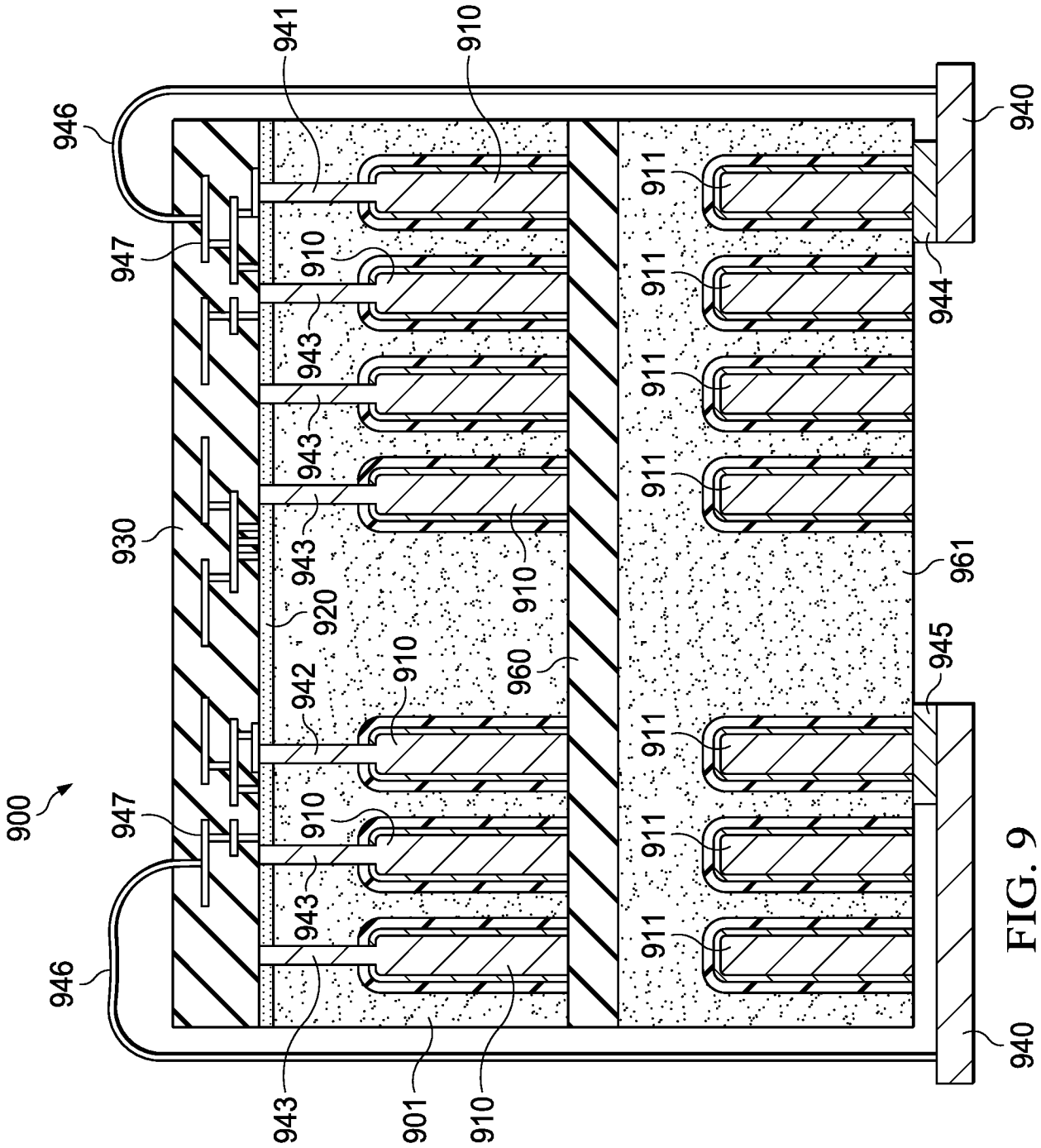
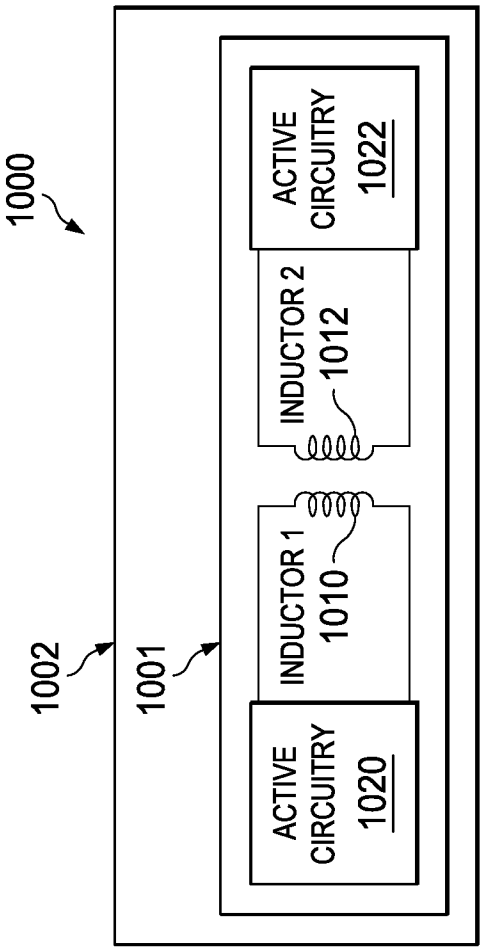


FIG. 9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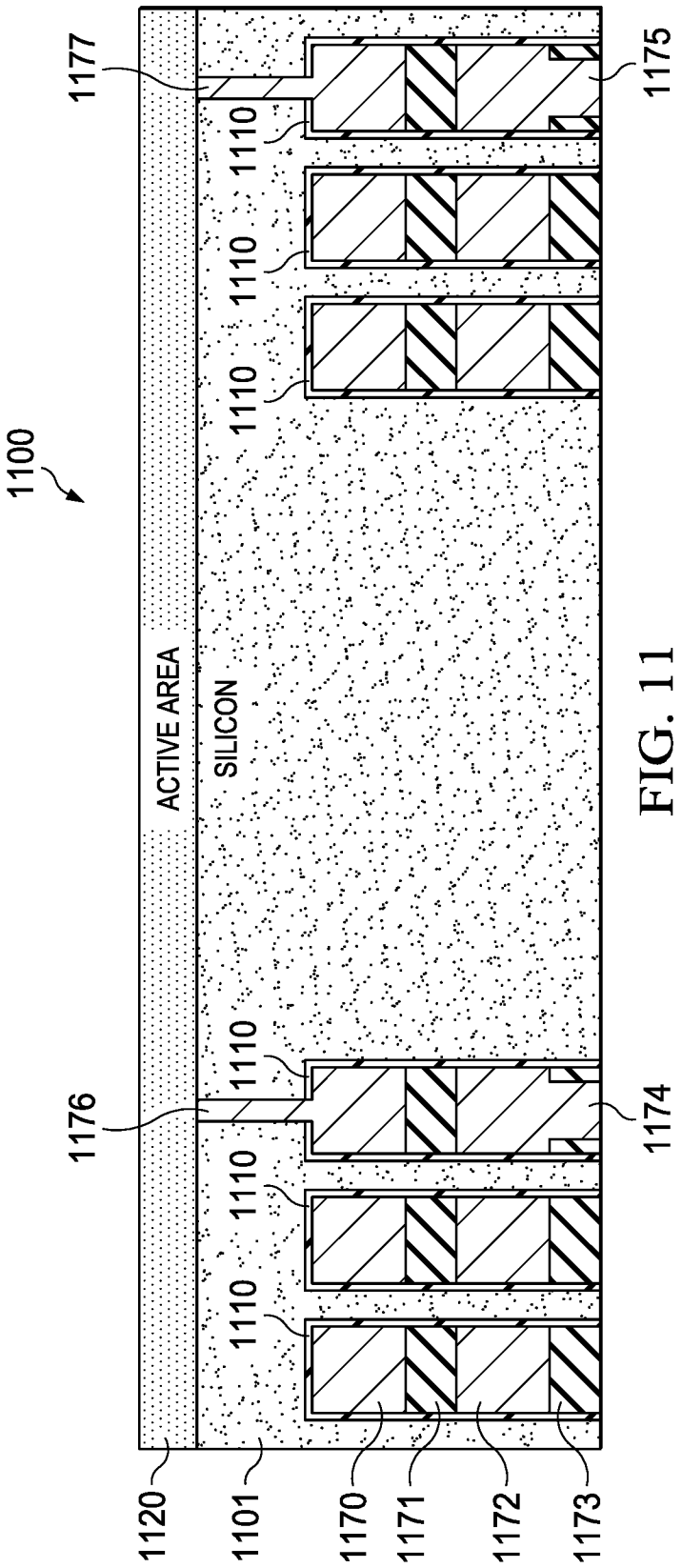
ACTIVE CIRCUITRY 1022

FIG. 10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1173

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/032247

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/04 *(2006.01)*
H01L 25/10 *(2006.01)*
H01L 21/82 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/04, 21/82, 25/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/0020488 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 24.01.2008, abstract, fig. 1-2, par. [0001]-[0014], [0021]-[0028], [0049]-[0051]	1-3, 6-7, 9, 11-15, 18, 20
Y		4-5, 10, 16-17
A		8, 19
Y	US 2003/0057539 A1 (MICHEL KOOPMANS) 27.03.2003, abstract	4-5, 16-17
Y	US 8664752 B2 (FAIRCHILD SEMICONDUCTOR CORPORATION) 04.03.2014	10
A	US 2012/0068301 A1 (THE HONG KONG UNIVERSITY OF SCIENCE AND TEHNOLOGY) 22.03.2012	1-20

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 July 2017 (21.07.2017)	17 August 2017 (17.08.2017)

Name and mailing address of the ISA/RU:
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Authorized officer

I. Baginskaya

Telephone No. 8-499-240-25-91

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/032247

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/0023639 A1 (TZU-JIN YEH et al.) 03.02.2005	1-20
A	US 8299572 B2 (SKYWORKS SOLUTIONS, INC.) 30.10.2012	1-20