(12) UK Patent Application (19) GB (11) 2 260 839 (13) A

(43) Date of A publication 28.04.1993

(21) Application No 9222496.3

(22) Date of filing 26.10.1992

(30) Priority data
(31) 9118833 (32) 25.10.1991 (33) KR

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(51) INT CL[5]
**G11C 7/00**

(52) UK CL (Edition L)
**G4C C700B**

(56) Documents cited
**EP 0481084 A1** **US 4984202 A**

(58) Field of search
UK CL (Edition L) **G4C C700B**
INT CL[5] **G11C 7/00**

# (54) Data transmission circuit for a semiconductor memory

(57) The data transmission circuit processes data input/output at high speed by suppressing the generation of a DC current through output transistors 61, 62 when performing a data write operation after a data read operation. The data transmission circuit 100 has common input/output lines 65, 66, a sensing transistor circuit 59, 60 for sensing a potential difference of bit lines 53, 54, an input transistor circuit 63, 64 for writing data, and an output transistor circuit 61, 62 for reading data. The common input/output lines 65, 66 are electrically insulated from the output transistor circuit 61, 62 and the sensing transistor circuit 59, 60 during a data write operation. Memory cells 51, 52 exist in two different memory array blocks commonly controlled by the circuit 100.

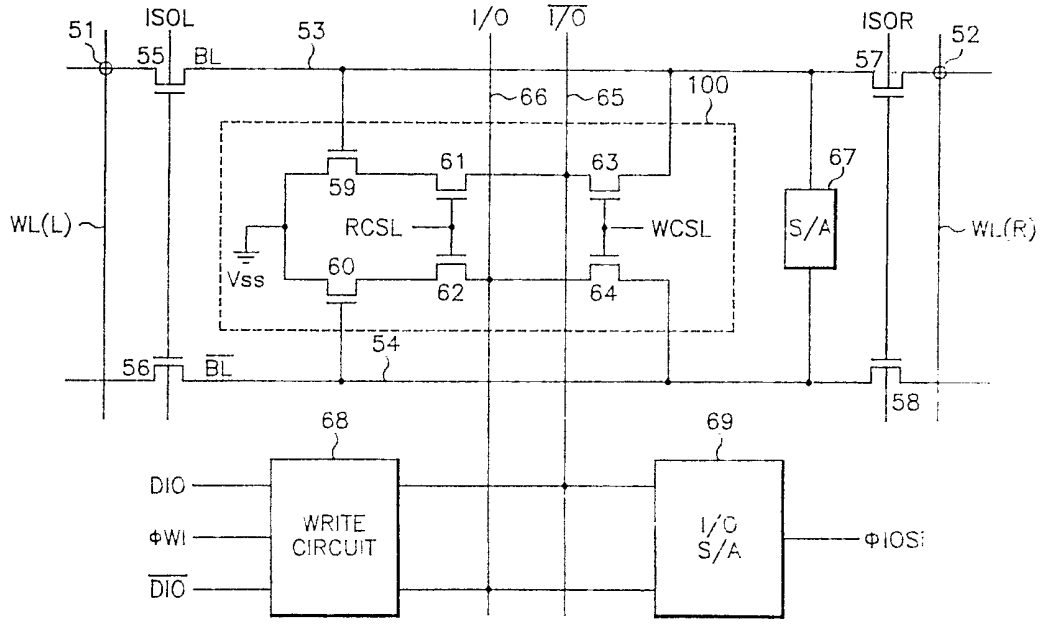


FIG. 5

GB 2 260 839 A

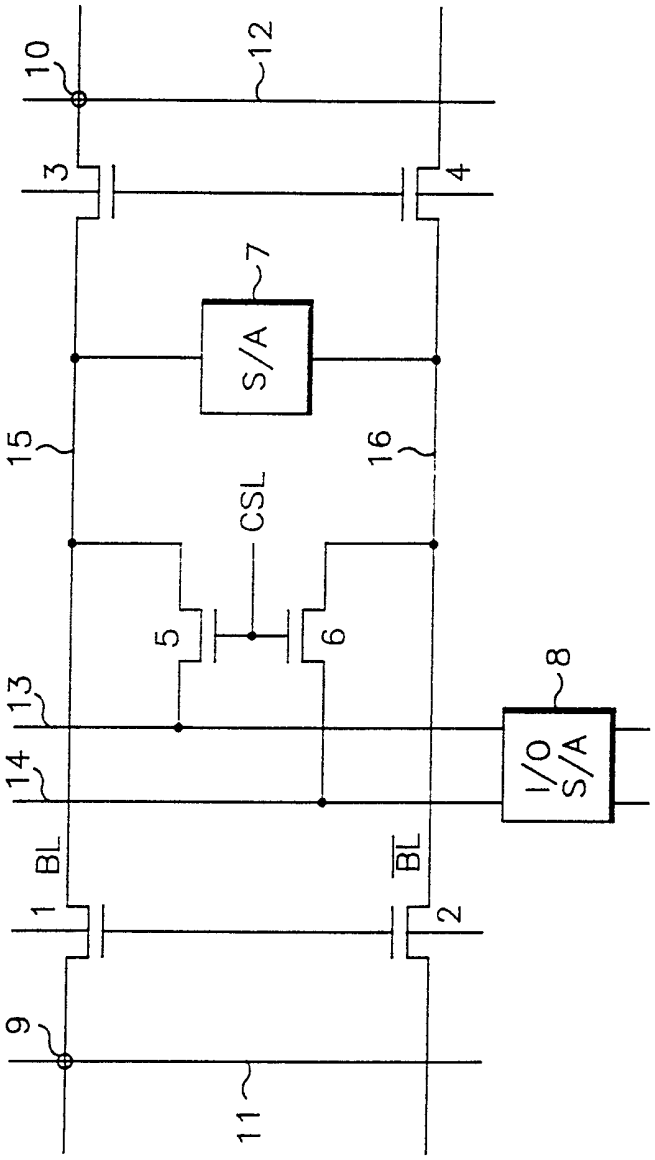


FIG. 1

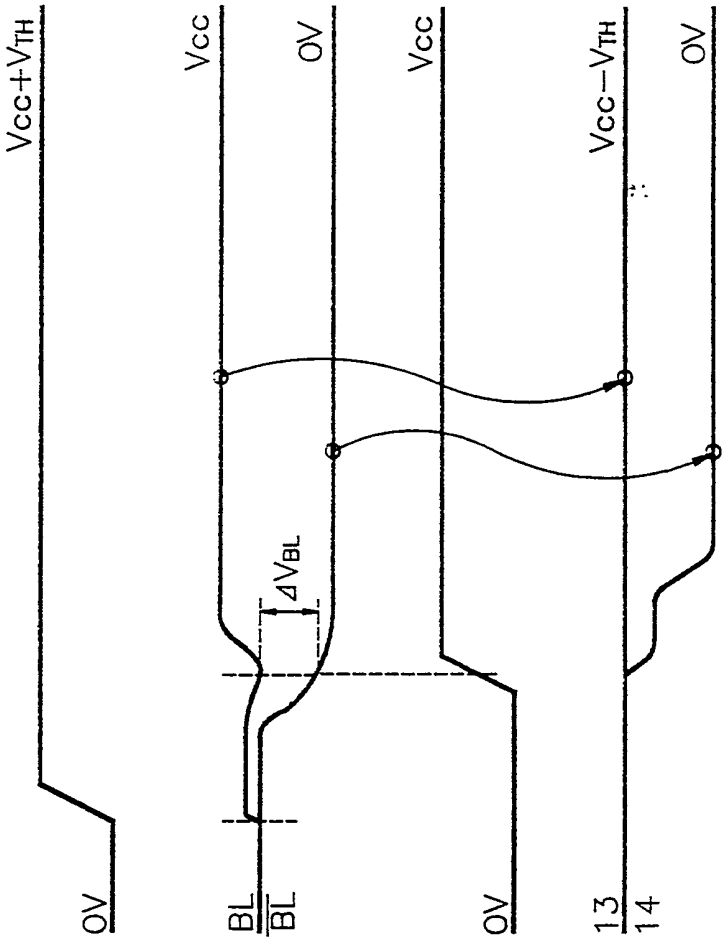


FIG. 2A WORD-LINE

FIG. 2B BIT-LINE

FIG. 2C CSL

FIG. 2D I/O-LINE

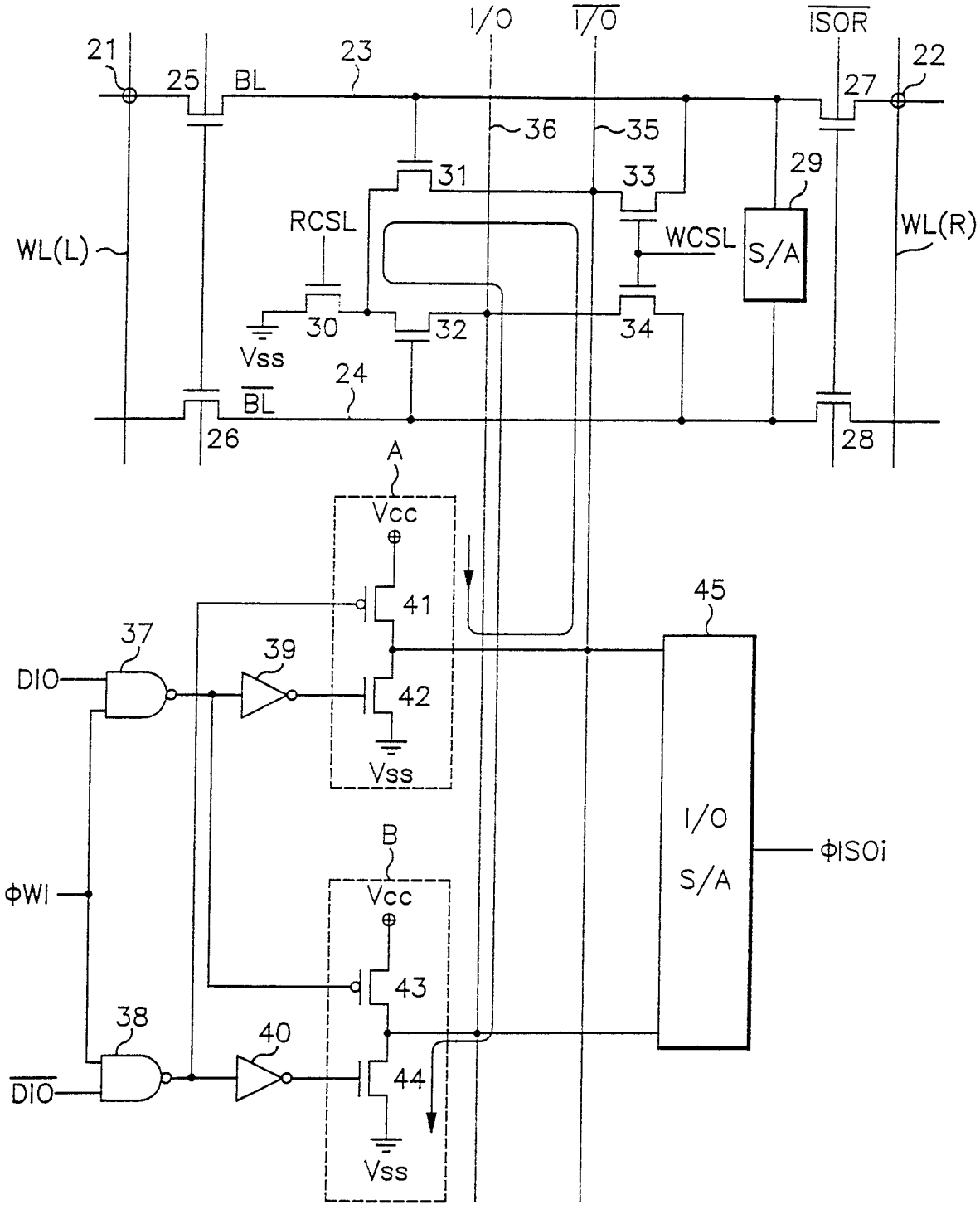
I/O
$\overline{I/O}$
$\overline{ISOR}$
21
25
BL
23
22
27
36
35
31
33
29
RCSL
WCSL
S/A
WL(L)
WL(R)
30
32
34
Vss
24
$\overline{BL}$
26
28
A
Vcc
41
45
37
39
DIO
42
Vss
B
I/O
S/A
ϕISOi
ϕWI
Vcc
43
38
40
$\overline{DIO}$
44
Vss

*FIG. 3*

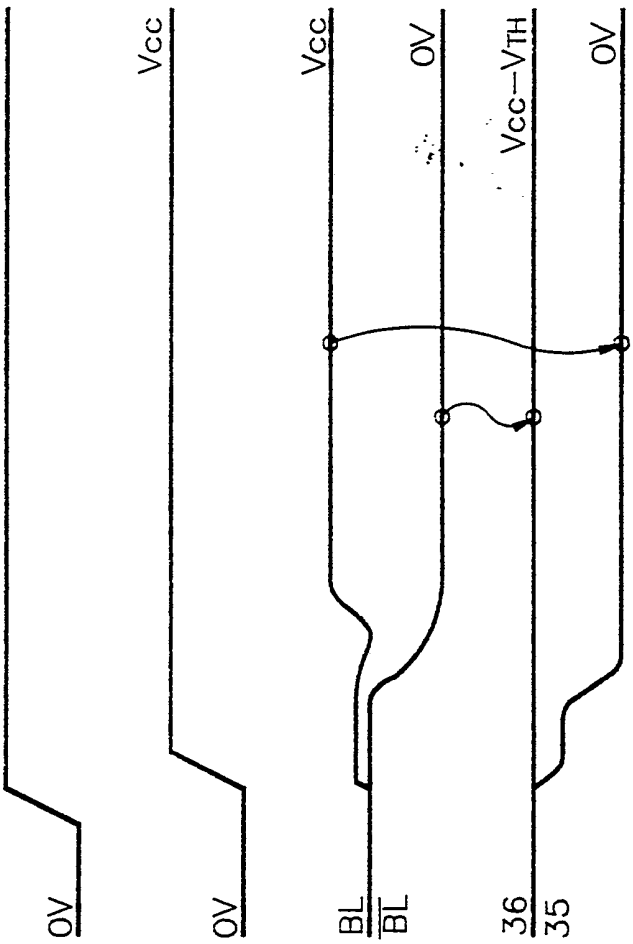


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D

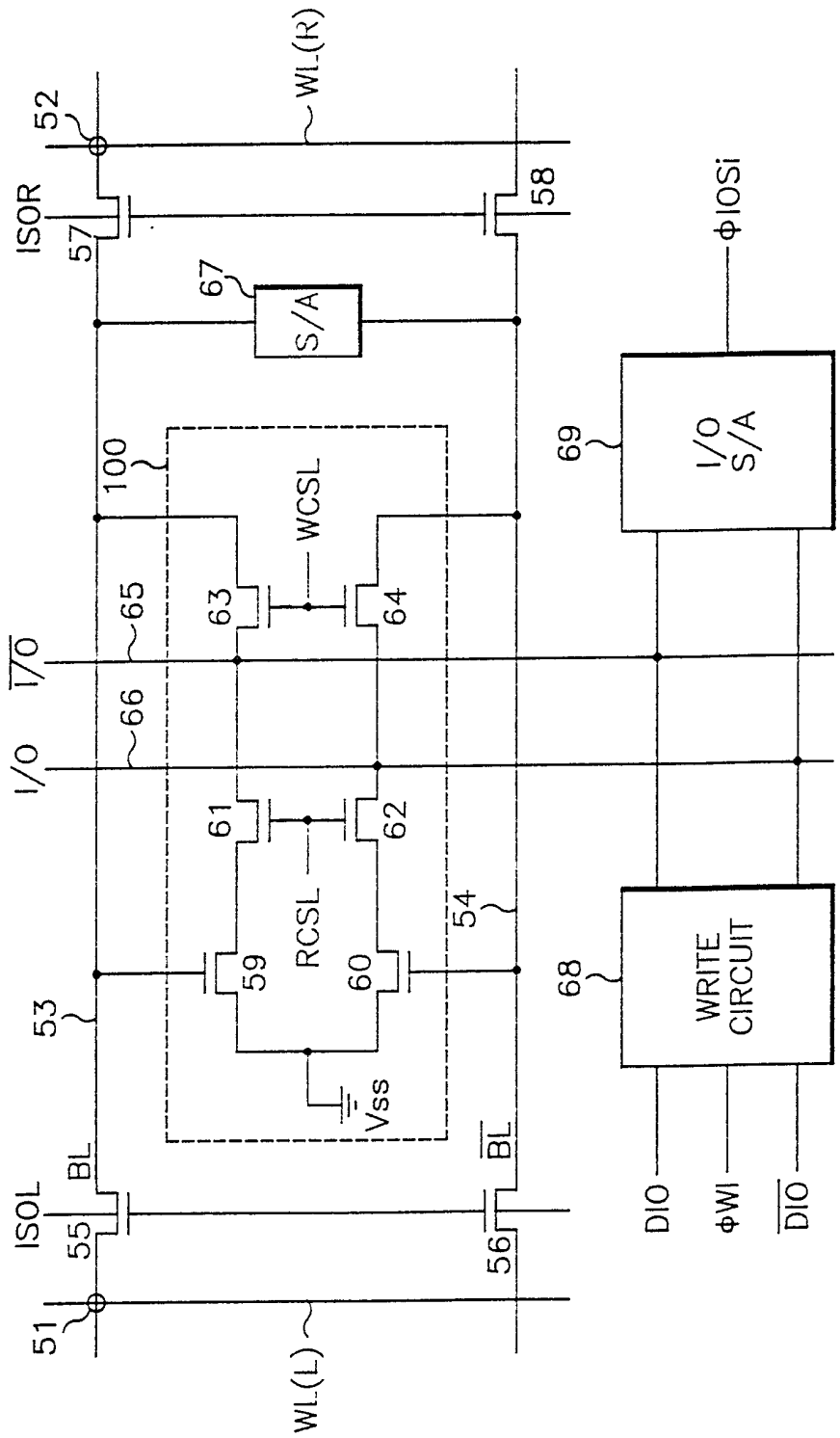
WL(R)
52
ISOR
57
58
67
S/A
φIOSi
100
WCSL
63
64
69
I/O
S/A
65
I/O
66
61
62
RCSL
54
59
60
53
68
WRITE
CIRCUIT
Vss
ISOL
BL
55
56
DIO
φWI
DIO
51
WL(L)

FIG. 5

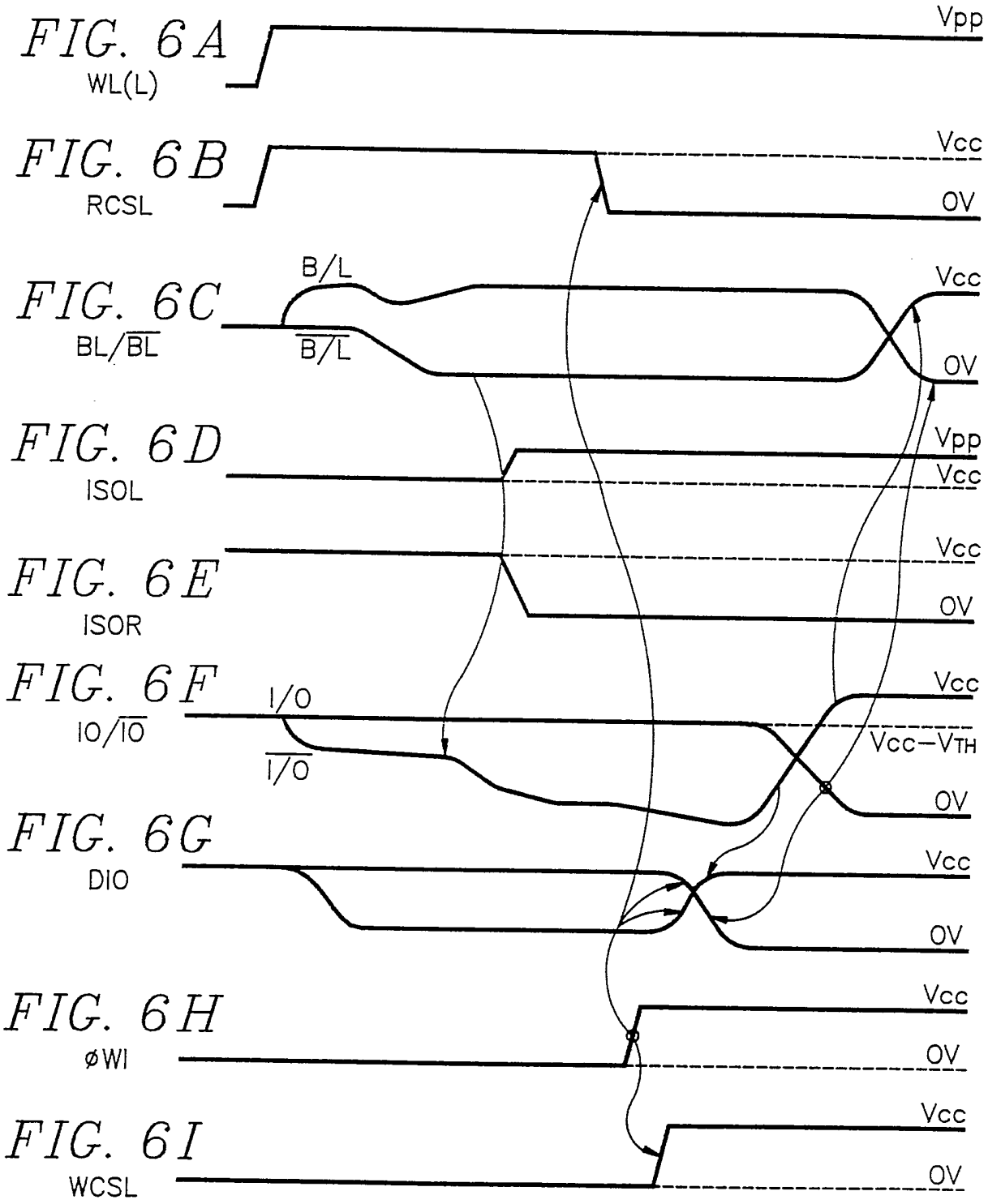
FIG. 6A
WL(L)
Vpp
FIG. 6B
RCSL
Vcc
0V
FIG. 6C
BL/$\overline{BL}$
B/L
$\overline{B/L}$
Vcc
0V
FIG. 6D
ISOL
Vpp
Vcc
FIG. 6E
ISOR
Vcc
0V
FIG. 6F
IO/$\overline{IO}$
I/O
$\overline{I/O}$
Vcc
Vcc−VTH
0V
FIG. 6G
DIO
Vcc
0V
FIG. 6H
øWl
Vcc
0V
FIG. 6I
WCSL
Vcc
0V

# DATA TRANSMISSION CIRCUIT

The present invention relates to data transmission circuits for semiconductor memory devices, and is concerned particularly, although not exclusively, with dynamic random access memories (DRAM) and particularly highly integrated data transmission circuits for processing data at high speed.

Recently, semiconductor integrated circuits have developed with a high degree of integration of the circuit and high speed operation. However, if high integration of the circuit is achieved, the operating speed is generally reduced. On the contrary, if high speed operation is achieved, it is difficult to realize high integration of the circuit. Therefore, the simultaneous achievement of high-speed operation and high integration of the circuit is one of the problems to be solved in the field of semiconductor integrated circuits. In particular, because a data transmission circuit for use in a semiconductor integrated circuit has an influence on the high-speed operation and high integration of the circuit, the configuration of the data transmission circuit and the proper selection of components thereof are essential for the realization of the high-speed operation and high integration of the semiconductor integrated circuit.

Referring to Figure 1 of the accompanying diagrammatic drawings, a conventional data transmission circuit is shown which includes memory cells 9 and 10, word lines 11 and 12, bit lines 15 and 16, a sense amplifier 7 connected between the bit lines 15 and 16, isolation transistors 1, 2, 3 and 4 for isolating the memory cells 9 and 10 from the bit lines 15 and 16, input/output transistors 5 and 6 having source-drain channels, terminals of the respective source-drain channels being connected to the bit lines 15 and 16,

common input/output lines 13 and 14 connected to the other terminals of the respective source-drain channels of the input/output transistors 5 and 6, and an input/output sense amplifier 8 connected to the common input/output lines 13 and 14.

Operation of the circuit of Figure 1 will now be described in conjunction with Figures 2A to 2D of the accompanying diagrammatic drawings. When data is read out from the memory cell 9, the isolation transistors 1 and 2 connected to the memory cell 9 are turned on, while the isolation transistors 3 and 4 are turned off. Moreover, the word line 11 connected to the memory cell 9 is selected so that the data of the memory cell 9 is transferred to the bit line 15. Thus, the sense amplifier 7 amplifies the potential difference between the bit lines 15 and 16. If a column select line signal CSL is enabled, data on the bit lines 15 and 16 is transferred to the input/output lines 13 and 14 through the input/output transistors 5 and 6. The potential difference of the data on the input/output lines 13 and 14, which is pulled down by the parasitic capacitance of the input/output lines 13 and 14, is again amplified by the input/output sense amplifier 8. The main feature of this data transmission circuit lies in that the source-drain channels of the input/output transistors 5 and 6 are respectively connected between the bit lines 15 and 16 and the input/output lines 13 and 14. As shown in Figures 2B and 2C, when the potential difference $\Delta V_{BL}$ of the bit lines 15 and 16 is approximately 1V, the column select line signal CSL is enabled as logic "high" level. Moreover, since the column select line signal CSL must be enabled after the potential difference of the bit lines 15 and 16 is sufficiently amplified, there occurs a decrease of the operating speed caused by the delay time of the column select line signal CSL. Furthermore, since the data transferred to the input/output lines 13 and 14 passes through the input/output

transistors 5 and 6, a voltage drop as much as the threshold voltage of the input/output transistors 5 and 6 is generated. In addition, when the input/output transistors 5 and 6 are turned on, since the input/output lines 13 and 14 and the bit lines 15 and 16 are connected to the input/output transistors 5 and 6, the parasitic capacitance is increased, and the potential difference of the data transferred to the input/output lines 13 and 14 is further decreased. As a result, the sensing capability of the input/output line sense amplifier 8 deteriorates.

In Figure 3 of the accompanying diagrammatic drawings, there is provided another conventional data transmission circuit in which certain problems of the circuit of Figure 1 are solved. This data transmission circuit is disclosed in Korean Patent publication No. 91-13283, filed on July 31, 1991. In order to allow the data input/output to operate at high speed, the gates of first and second output transistors 31 and 32 are directly connected to bit lines 23 and 24, respectively, and the source-drain channels of first and second input transistors 33 and 34 are respectively connected between data input/output lines 35 and 36 and the bit lines 23 and 24. Further, in order to achieve high integration of the circuit, the input/output lines 35 and 36 are used as a pair of common input/output lines, thereby reducing the number of transistors. Reference numerals 37 to 44 constitute a write circuit and blocks A and B shown in dashed lines indicate write drivers, respectively.

Operation of the circuit of Figure 3 will now be described with reference to Figures 4A to 4D of the accompanying diagrammatic drawings.

When data is read out from the memory cell 21, a word line WL(L) is selected, and the data stored in the memory cell 21 is transferred to the bit

line 23. Then the potentials of the bit lines 23 and 24 transit respectively to a power voltage level Vcc and a ground voltage level Vss by a sense amplifier 29. Thereafter, if a read column select line signal RCSL is enabled, a discharge transistor 30 is turned on, and the first and second output transistors 31 and 32 are operated as a current sense amplifier. It can be understood that the potential of the input/output line 35 maintains its level, when the first output transistor 31 is turned off. Meanwhile, the potential of the input/output line 36 is discharged to a ground voltage terminal through the discharge transistor 30, because the second output transistor 32 is turned on at this moment. Then, the potential difference between the first and second input/output lines 35 and 36 is more greatly amplified by an input/output line sense amplifier 45, and the output of the sense amplifier 45 is transferred externally of the memory device. The above read operation is performed at higher speed in comparison with the case that the data of the bit lines is transferred to the input/output lines through the source-drain channels of the input/output transistors, as is shown in Figure 1.

Next, a data write operation is described. If data input is supplied to NAND gates 37 and 38 and a write enable signal $\phi$WI is set to the logic "high", the write drivers A and B respectively transfer the data input to the input/output lines 35 and 36. In this case, the input/output line sense amplifier 45 is in a disabled state. Thereafter, if a write column select line signal WCSL is enabled, the data is transferred to the bit lines 23 and 24 through the first and second input transistors 33 and 34 and stored in the memory cell 21 or 22.

Generally, since the parasitic capacitance of the data input/output lines is higher than that of the bit lines by about 10 times, the source-drain channels

of the first and second input transistors 33 and 34 should be small in size in order to implement proper charge sharing. Hence, the potentials of the bit lines 23 and 24 are not so quickly changed to a desired state and accordingly, there occurs a period for which the potentials are maintained at an intermediate state. Consequently, a DC current flows in an arrow direction of Figure 3, so that the current consumption increases. Further, since the potentials of the bit lines are maintained at an intermediate state for a period, an enable time of a write operation after a read operation is delayed when a read-modify-write operation is performed, whereby the characteristic of the memory device deteriorates. For reference, the read-modify-write operation is one operating mode of a dynamic RAM, in which data input applied to a data input terminal is modified into data output to a data output terminal.

Preferred embodiments of the present invention aim to provide a data transmission circuit for suppressing the generation of a DC current and improving the characteristic of a read-modify-write operation.

According to one aspect of the present invention, there is provided a data transmission circuit for use in a semiconductor memory device having first and second memory array blocks with a plurality of memory cells each for storing input data, a pair of bit lines each commonly connected to said first and second memory array blocks, first and second isolation transistor circuits for isolating/connecting said bit lines from/to said first or second memory array block, and a bit line sense amplifier for amplifying a potential difference between said bit lines, said circuit comprising:

a pair of common input/output lines for commonly transferring data of said first and second memory array blocks;

sensing means connected between a ground voltage terminal and said common input/output lines, for sensing a potential difference between said bit lines;

input means connected between said bit lines and said common input/output lines, for connecting said common input/output lines to said bit lines in response to a first control signal so as to transfer data of said common input/output lines to said bit lines; and

output means connected between said sensing means and said common input/output lines, for transferring data stored in a memory cell to said common input/output lines in response to a second control signal.

Preferably, said first and second control signals are a write column select line signal and a read column select line signal, respectively.

Preferably, said sensing means comprises first and second sensing transistors having gates respectively connected to said bit lines and having source-drain channels, first terminals of said source-drain channels being commonly connected to said ground voltage terminal and second terminals of said source-drain channels being respectively connected to said common input/output lines.

Preferably, said output means comprises first and second output transistors having gates commonly connected to receive said second control signal and having source-drain channels respectively connected between terminals of said source-drain channels of said first and second sensing transistors and said common input/output lines.

Preferably, said input means comprises first and second input transistors having gates commonly connected to said first control signal and having source-drain channels respectively connected between said bit lines and said common input/output lines.

Preferably, the data of said common input/output lines is electrically insulated from said sensing means and said output means during a write operation.

According to another aspect of the present invention, there is provided a data transmission circuit for use in a semiconductor memory device having first and second memory array blocks with a plurality of memory cells each for storing input data, a pair of bit lines each commonly connected to said first and second memory array blocks, first and second isolation transistor circuits for isolating/connecting said bit lines from/to said first or second memory array block, and a bit line sense amplifier for amplifying a potential difference between said bit lines, said circuit comprising:

a pair of common input/output lines for commonly transferring data of said first and second memory array blocks;

first and second sensing transistors having gates respectively connected to said bit lines and having source-drain channels, first terminals of said source-drain channels being commonly connected to a ground voltage terminal and second terminals of said source-drain channels being respectively connected to said common input/output lines;

first and second input transistors having gates commonly connected to a first control signal and having source-drain channels respectively connected between said bit lines and said common input/output lines; and

first and second output transistors having gates commonly connected to a second control signal and having source-drain channels respectively connected between terminals of said source-drain channels of said first and second sensing transistors and said common input/output lines.

Preferably, said first and second control signals are a write column select line signal and a read column select line signal respectively,

Preferably, the data of said common input/output lines is electrically insulated from said first and second sensing transistors and said first and second output transistors during a write operation.

According to a further aspect of the present invention, there is provided a data transmission circuit for a semiconductor memory device having a plurality of memory cells for storing data, said circuit comprising input/output lines, bit lines, sensing means, input means and output means, so arranged that generation of DC current is suppressed when performing a memory write operation after a memory read operation.

A circuit as above may further comprise any one or more of the features disclosed in the accompanying specification, claims, abstract and/or drawings, in any combination.

The invention also extends to a semiconductor memory device provided with a data transmission circuit according to any of the preceding claims.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to Figures 5 and 6 of the accompanying diagrammatic drawings, in which:

Figure 5 is a circuit diagram of one example of a data transmission circuit embodying of the present invention; and

Figures 6A to 6I are operational timing charts during the read-modify-write operation of Figure 5.

Referring to Figure 5, a block 100 shown in a dashed line represents improved parts in comparison with a conventional circuit, and therefore, a detailed description of the general configuration except the block 100 is not given.

The block 100 includes first and second sensing transistors 59 and 60 with gates respectively connected to a pair of bit lines 53 and 54 and a terminal of each source-drain channel connected to a ground voltage terminal Vss. There are also provided first and second output transistors 61 and 62 with gates commonly connected to receive a read column select line signal RCSL and source-drain channels respectively connected between the other terminals of the source-drain channels of the first and second sensing transistors 59 and 60 and a pair of data input/output lines 65 and 66. First and second input transistors 63 and 64 are also provided with gates commonly connected to receive a write column select line signal WCSL and source-drain channels respectively connected between the input/output lines 65 and 66 and the bit lines 53 and 54. It is to be noted that, in this embodiment, memory

cells 51 and 52 exist in different memory array blocks (not shown), and one data transmission circuit commonly controls two memory array blocks.

Operation of the circuit of Figure 5 will now be described in detail with reference to Figures 6A to 6I.

First, a read operation in which data is read out from, for example, the memory cell 51 will be described. As a preliminary step, it is to be assumed that when neither the memory cell 51 nor the memory cell 52 is selected, that is, for a precharge state, an isolation signal ISOL applied to the gates of isolation transistors 55 and 56 and an isolation signal ISOR supplied to the gates of isolation transistors 57 and 58 are maintained at a power supply voltage Vcc; and if the memory cell 51 is selected, the potential of the isolation signal ISOL becomes Vpp=Vcc+Vt and that of the isolation signal ISOR becomes Vss=0V. Therefore, if the memory cell 51 is selected, since the isolation signals ISOL and ISOR have the potentials of Vpp and 0V respectively, a word line WL(L) is enabled and the data stored in the memory cell 51 charge-shares with the potential of the bit line 53. Then a bit line sense amplifier 67 senses an increased potential difference of the bit lines 53 and 54 and respectively changes the potentials of the bit lines 53 and 54 into a power voltage level Vcc and a ground voltage level Vss. Hence, the first sensing transistor 59 is turned on.

If the read column select line signal RCSL is enabled in a little while, a given potential difference between the input/output lines 65 and 66 is generated. At this time, the enabled time of the read column select line signal RCSL can be enabled quickly relative to the time shown in Figure 6B. That is, if the data stored in the memory cell 51 is at logic "high" state, the first

sensing transistor 59 is turned on and thus, the potential of the input/output line 65 is lowered to a ground voltage level. In this case, a waveform illustrating the potential difference of the input/output lines 65 and 66 is shown in Figure 6F, and the potential difference between the input/output lines 65 and 66 is further increased by the input/output sense amplifier 69. Thus, the data read from the memory cell 51 is output externally of the circuit.

Next, a data write operation is described. If a write enable signal $\phi$WI is applied to a write circuit 68, complementary data inputs DIO and $\overline{\text{DIO}}$ are supplied to the write circuit 68 and respectively transferred to the input/output lines 65 and 66. Moreover, if the write column select line signal WCSL is selected, the data of the input/output lines 65 and 66 is transferred to the bit lines 53 and 54 through the first and second input transistors 63 and 64, respectively. In this case, since the potential of the isolation signal ISOL is Vpp, the isolation transistors 55 and 56 are turned on. Then, the data of the bit line 53 is stored in the memory cell 51 through the isolation transistor 55. During the write operation, since the first and second output transistors 61 and 62 are turned off, the generation of a DC current is suppressed. Therefore, the enabled time of the write operation after the read operation is not delayed, thereby improving the characteristic of the memory device.

As described above, when performing a write operation after a read operation, such as in a read-modify-write mode, the illustrated data transmission circuit suppresses the generation of the DC current and thus, high-speed operation of data input/output is performed. Furthermore, a stable operation of an integrated circuit is obtained and high integration of a circuit is easily achieved.

Although an example of the present invention has been described above in terms of a specific structure, it will be apparent to those skilled in the art, in light of this disclosure, that many modification and alteration may be made thereto. Accordingly, it is intended that all modifications and alterations may be included within the spirit and scope of the invention as defined by the appended claims.

The term "ground potential" (or like terms such as "ground voltage" or "earth" potential or voltage) is used conveniently in this specification to denote a reference potential. As will be understood by those skilled in the art, although such reference potential may typically be zero potential, it is not essential that it is so, and may be a reference potential other than zero.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly

stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

## CLAIMS

1. A data transmission circuit for use in a semiconductor memory device having first and second memory array blocks with a plurality of memory cells each for storing input data, a pair of bit lines each commonly connected to said first and second memory array blocks, first and second isolation transistor circuits for isolating/connecting said bit lines from/to said first or second memory array block, and a bit line sense amplifier for amplifying a potential difference between said bit lines, said circuit comprising:

a pair of common input/output lines for commonly transferring data of said first and second memory array blocks;

sensing means connected between a ground voltage terminal and said common input/output lines, for sensing a potential difference between said bit lines;

input means connected between said bit lines and said common input/output lines, for connecting said common input/output lines to said bit lines in response to a first control signal so as to transfer data of said common input/output lines to said bit lines; and

output means connected between said sensing means and said common input/output lines, for transferring data stored in a memory cell to said common input/output lines in response to a second control signal.

2. A data transmission circuit as claimed in claim 1, wherein said first and second control signals are a write column select line signal and a read column select line signal, respectively.

3. A data transmission circuit as claimed in claim 1 or 2, wherein said sensing means comprises first and second sensing transistors having gates

respectively connected to said bit lines and having source-drain channels, first terminals of said source-drain channels being commonly connected to said ground voltage terminal and second terminals of said source-drain channels being respectively connected to said common input/output lines.

4. A data transmission circuit as claimed in claim 3, wherein said output means comprises first and second output transistors having gates commonly connected to receive said second control signal and having source-drain channels respectively connected between terminals of said source-drain channels of said first and second sensing transistors and said common input/output lines.

5. A data transmission circuit as claimed in any of the preceding claims, wherein said input means comprises first and second input transistors having gates commonly connected to said first control signal and having source-drain channels respectively connected between said bit lines and said common input/output lines.

6. A data transmission circuit as claimed in any of the preceding claims, wherein the data of said common input/output lines is electrically insulated from said sensing means and said output means during a write operation.

7. A data transmission circuit for use in a semiconductor memory device having first and second memory array blocks with a plurality of memory cells each for storing input data, a pair of bit lines each commonly connected to said first and second memory array blocks, first and second isolation transistor circuits for isolating/connecting said bit lines from/to said first or second

memory array block, and a bit line sense amplifier for amplifying a potential difference between said bit lines, said circuit comprising:

a pair of common input/output lines for commonly transferring data of said first and second memory array blocks;

first and second sensing transistors having gates respectively connected to said bit lines and having source-drain channels, first terminals of said source-drain channels being commonly connected to a ground voltage terminal and second terminals of said source-drain channels being respectively connected to said common input/output lines;

first and second input transistors having gates commonly connected to a first control signal and having source-drain channels respectively connected between said bit lines and said common input/output lines; and

first and second output transistors having gates commonly connected to a second control signal and having source-drain channels respectively connected between terminals of said source-drain channels of said first and second sensing transistors and said common input/output lines.

8. A data transmission circuit as claimed in claim 7, wherein said first and second control signals are a write column select line signal and a read column select line signal respectively,

9. A data transmission circuit as claimed in claim 7 or 8, wherein the data of said common input/output lines is electrically insulated from said first and second sensing transistors and said first and second output transistors during a write operation.

10. A data transmission circuit for a semiconductor memory device having a plurality of memory cells for storing data, said circuit comprising

input/output lines, bit lines, sensing means, input means and output means, so arranged that generation of DC current is suppressed when performing a memory write operation after a memory read operation.

11. A circuit according to claim 10, further comprising any one or more of the features disclosed in the accompanying specification, claims, abstract and/or drawings, in any combination.

12. A data transmission circuit substantially as hereinbefore described with reference to Figures 5 and 6 of the accompanying drawings.

13. A semiconductor memory device provided with a data transmission circuit according to any of the preceding claims.

**Patents Act 1977**
**Examiner's report to the Comptroller under Section 17 (The Search Report)**

Application number

GB 9222496.3

**Relevant Technical fields**

(i) UK Cl (Edition L ) G4C C700B

(ii) Int Cl (Edition 5 ) G11C 7/00

Search Examiner

M J BILLING

**Databases** (see over)

(i) UK Patent Office

(ii)

Date of Search

8 JANUARY 1993

**Documents considered relevant following a search in respect of claims** 1 TO 10

| Category (see over) | Identity of document and relevant passages | Relevant to claim(s) |
|---|---|---|
| X,P | EP 0481084 A1 (FUJITSU) eg see circuit elements Q1, Q2, Q6, Q7, Q8, Q9 in Figure 2, published 22 April 1992 | 1 to 10 |
| X | US 4984202 A (HITACHI) eg see circuit elements MR1, MR2, MR3, MR4, MW1, MW2 in Figure 52 | 1 to 10 |

| Category | Identity of document and relevant passages | Relevant to claim(s. |
|---|---|---|
| | | |

## Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

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