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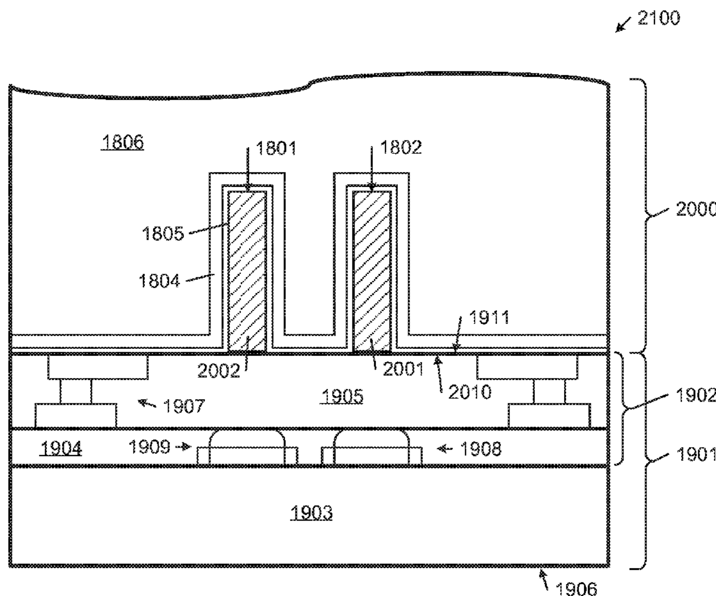

FIG. 21

(57) Abstract: A method is disclosed. The method comprises fabricating a device layer on a top portion of a semiconductor wafer that comprises a substrate. The device layer comprises an active device. The method also comprises forming a trap rich layer at a top portion of a handle wafer. The forming comprises etching the top portion of the handle wafer to form a structure in the top portion of the handle wafer that configures the trap rich layer. The method also comprises bonding a top surface of the handle wafer to a top surface of the semiconductor wafer. The method also comprises removing a bottom substrate portion of the semiconductor wafer.

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SEMICONDUCTOR STRUCTURE WITH TRL AND HANDLE WAFER CAVITIES

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is an international application of U.S. patent application No. 14/633,024, filed February 26, 2015, which is a continuation-in-part of U.S. patent application Ser. No. 14/454,370 filed Aug. 7, 2014, which is a continuation-in-part of U.S. patent application Ser. No. 14/043,764 filed Oct. 1, 2013, which is a continuation of U.S. patent application Ser. No. 13/762,257 filed Feb. 7, 2013, now U.S. Pat. No. 8,581,398, which is a continuation of U.S. patent application Ser. No. 13/652,240 filed Oct. 15, 2012, now U.S. Pat. No. 8,481,405, which is a continuation-in-part of U.S. patent application Ser. No. 13/313,231 filed Dec. 7, 2011, now U.S. Pat. No. 8,466,036, which claims priority to U.S. Provisional Patent Application No. 61/427,167 filed Dec. 24, 2010, under 35 U.S.C. .sctn.119(e), all of which are incorporated herein by reference in their entirety.

[0002] This application is also a continuation-in-part of U.S. patent application Ser. No. 14/013,000, filed Aug. 28, 2013, which is a continuation of U.S. patent application Ser. No. 13/684,623 filed on Nov. 26, 2012, now U.S. Pat. No. 8,536,021, which is a continuation-in-part of U.S. patent application Ser. No. 13/313,231 filed Dec. 7, 2011, now U.S. Pat. No. 8,466,036, which claims priority to U.S. Provisional Patent Application No. 61/427,167 filed Dec. 24, 2010, under 35 U.S.C. .sctn.119(e), all of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

[0003] Semiconductor-on-insulator (SOI) technology, which represents an advance over traditional bulk silicon processes, was first commercialized in the late 1990s. The defining characteristic of SOI technology is that the semiconductor region in which circuitry is formed is isolated from the bulk substrate by an electrically insulating layer. One advantage of isolating circuitry from the bulk substrate is a dramatic decrease in parasitic capacitance which allows access to a more desirable power-speed performance horizon. Therefore, SOI structures are particularly appealing for high frequency applications such as radio frequency (RF) communication circuits.

As consumer demand continues to tighten the power constraints faced by RF communication circuits, SOI technology continues to grow in importance.

[0004] A typical SOI structure 100 is shown in FIG. 1. The SOI structure 100 includes a substrate layer 101, an insulator layer 102, and an active layer 103. The substrate layer 101 is typically a semiconductor material such as silicon. The insulator layer 102 is a dielectric which is often silicon dioxide formed through the oxidation of the substrate layer 101 in situations where the substrate layer 101 is silicon. The active layer 103 includes an active device layer 104 and a metallization or metal interconnect layer 105, which further include a combination of dopants, dielectrics, polysilicon, metal wiring, passivation, and other layers, materials or components that are present after circuitry has been formed therein. The circuitry may include metal wiring 106 (e.g. in the metal interconnect layer 105); passive devices such as resistors, capacitors, and inductors; and active devices such as a transistor 107 (e.g. in the active device layer 104).

[0005] As used herein and in the appended claims, the region in which signal processing circuitry is formed on an SOI structure is referred to as the "active layer" of the SOI structure. For example, in FIG. 1 the active layer is the active layer 103 which includes devices or components such as the transistor 107 and the metal wiring 106. When reference is made particularly to the layer of active semiconductor material that forms the active devices themselves the term "active device layer" (e.g. 104) is used instead. For example, in FIG. 1 the active device layer 104 is the portion of the active layer 103 that contains the transistor 107 and does not include the metal wiring 106 of the metal interconnect layer 105.

[0006] Also as used herein and in the appended claims, the "top" of the SOI structure 100 references a top surface 108 while the "bottom" of the SOI structure 100 references a bottom surface 109. This orientation scheme persists regardless of the relative orientation of the SOI structure 100 to other frames of reference, and the removal of layers from, or the addition of layers to the SOI structure 100. Therefore, the active layer 103 is always "above" the insulator layer 102. In addition, a vector originating in the center of the active layer 103 and extending towards the bottom surface 109 will always point in the direction of the "back side" of the SOI structure 100 regardless of the relative orientation of the SOI structure 100 to other frames of references, and the removal of layers from, or the addition of layers to the SOI structure 100.

[0007] Consumer demand continues to tighten the constraints on the quality and performance of RF devices. These constraints directly affect the required linearity and precision of the signals that are produced and decoded by RF circuits. Among other requirements, signals in one portion of a circuit must be kept from affecting and degrading signals in another portion of the circuit. This effect is called cross talk. The mitigation of cross talk is of critical importance for RF communication circuits because the impedance of certain parasitic pathways within a circuit tend to reach a minimum at frequencies that are used to carry signals in RF circuits. Since these same parasitic pathways connect nodes within a circuit that carry differing signals, the problem of cross talk is especially problematic for RF applications. In addition, it is critically important for the parasitic capacitances to which the signals within a circuit may be exposed not to be signal dependent. This requirement is critical because it is difficult to calibrate out an error that is signal dependent, and such errors are inherently nonlinear.

[0008] One solution to the problem of cross talk in electronic circuits is the use of a high resistivity substrate. With reference to FIG. 1, increasing the resistance of the substrate layer 101 reduces cross talk by maintaining the impedance of the parasitic paths through the substrate higher than the impedance would be without an increased substrate resistance. Materials used for the substrate layer 101 typically include very lightly doped silicon such that the substrate layer 101 takes on some of the characteristics of an insulator. The use of high resistivity substrates has proven capable of extending the benefit of SOI structures for RF communication circuits by roughly two orders of frequency magnitude.

[0009] Although high resistivity substrates are capable of reducing substrate loss when they are used in SOI processes, they are highly susceptible to another phenomenon called parasitic surface conduction. The problem of parasitic surface conduction and a potential solution can be explained with reference again to FIG. 1. As mentioned previously, the typical high resistivity substrate device insulator layer 102 is silicon dioxide, and the substrate layer 101 is high resistivity silicon. The problem of parasitic surface conduction comes from the fact that the lightly doped silicon that forms the substrate layer 101 can form an inversion or accumulation region as charge carriers are affected by signal voltages in the active layer 103. The degree to which charge carriers in the region 110 are displaced is directly altered by the signals in the active layer 103. As a result, the capacitance of the junction between the substrate layer 101 and the active layer 103, as seen by the active layer, depends on the electric field

emanating from the active layer. This capacitance results in nonlinearity and a concomitant loss of signal purity. In addition, an electric field can invert this interface on the side of the substrate layer 101 and create a channel-like layer within the region 110 where charge can move very easily in a lateral direction despite the fact that the substrate layer 101 is highly resistive. Therefore, this effect can also lead to signal-degrading cross talk in RF communication circuits.

[0010] A solution to the problem of the undesirable creation of the channel-like layer 110 has commonly been to form a trap rich layer along the top of the substrate layer 101 within the region 110. The presence of this trap rich layer effectively combats parasitic surface conduction because the trap rich layer significantly degrades the carrier lifetimes of the free charge carriers in the region 110. Since the carriers cannot travel far before being trapped, therefore, the effective resistance of the substrate layer 101 is preserved and the capacitance as seen by the active layer 103 is not as dependent upon the signals in the active layer 103.

[0011] A problem with the trap rich layer in region 110, however, is that when the trap rich layer is formed prior to the subsequent processing for the formation of the structures in the active layer 103, those later processing steps can degrade the trap rich layer. Processing of semiconductor devices and in particular the production of active devices in the active layer 103 generally involves high temperature processes conducted at temperatures from 1000.degree. C. to 1100.degree. C. High temperature processing of semiconductor structures acts to anneal defects in a semiconductor crystal lattice. This effect is commonly utilized to enhance the electrical properties of electrical circuits. However, contrary to usual applications, the performance of trap rich layers formed from amorphous or polycrystalline silicon crystal patterns is actually decreased when imperfections are annealed out since the number of traps is decreased.

BRIEF SUMMARY OF INVENTION

[0012] Some embodiments of the invention comprise a method. The method comprises fabricating a device layer on a top portion of a semiconductor wafer that comprises a substrate. The device layer comprises an active device. The method also comprises forming a trap rich layer at a top portion of a handle wafer. The forming comprises etching the top portion of the handle wafer to form a structure in the top portion of the handle wafer that configures the trap rich layer. The method also comprises bonding a top surface of the handle wafer to a top surface of the

semiconductor wafer. The method also comprises removing a bottom substrate portion of the semiconductor wafer.

[0013] Additional embodiments of the invention also comprise a method. The method comprises fabricating a device layer on a top portion of a semiconductor wafer that comprises a substrate. The device layer comprises active devices. The method also comprises forming a trap rich layer at a top portion of a handle wafer. The forming comprises etching the top portion of the handle wafer to form cavities in the top portion of the handle wafer. The method also comprises bonding a top surface of the handle wafer to a top surface of the semiconductor wafer with the active devices aligned with the cavities. The method also comprises removing a bottom substrate portion of the semiconductor wafer.

[0014] Additional embodiments of the invention comprise a semiconductor device. The device comprises a device layer layer-transferred and bonded onto a semiconductor wafer at an interface. The device layer comprises an active device. The semiconductor wafer comprises a trap rich layer and a substrate. The trap rich layer conforms to a structure in the substrate that varies separation between the device layer and the trap rich layer along the interface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a simplified cross section diagram of a prior art SOI structure.

[0016] FIG. 2 is a simplified cross section diagram of a portion of a first integrated circuit (IC) chip showing example structures therein that incorporate an embodiment of the present invention.

[0017] FIG. 3 is a simplified cross section diagram of a portion of a second IC chip showing example structures therein that incorporate another embodiment of the present invention.

[0018] FIG. 4 is a simplified cross section diagram of a portion of a third IC chip showing example structures therein that incorporate another embodiment of the present invention.

[0019] FIG. 5 is a simplified cross section diagram of a portion of a fourth IC chip showing example structures therein that incorporate another embodiment of the present invention.

[0020] FIG. 6 is a simplified cross section diagram of a portion of a fifth IC chip showing example structures therein that incorporate another embodiment of the present invention.

[0021] FIG. 7 is a simplified flow chart for an example process for fabricating one or more of the structures shown in FIGS. 2 and 6, according to embodiments of the present invention.

[0022] FIG. 8 is a simplified flow chart for an example process for fabricating one or more of the structures shown in FIGS. 3 and 4, according to embodiments of the present invention.

[0023] FIG. 9 is a simplified cross section diagram of a portion of a semiconductor substrate with through-semiconductor-vias (TSVs) that may be used with an embodiment of the present invention.

[0024] FIG. 10 is a simplified cross section diagram of a portion of a sixth IC chip including the semiconductor substrate shown in FIG. 9 bonded therein in accordance with another embodiment of the present invention.

[0025] FIG. 11 is a simplified cross section diagram of a portion of a seventh IC chip including the semiconductor substrate shown in FIG. 9 bonded therein in accordance with another embodiment of the present invention.

[0026] FIG. 12 is a simplified flow chart for an example process for fabricating one or more of the structures shown in FIGS. 9-11, according to embodiments of the present invention.

[0027] FIG. 13 is a simplified cross section diagram of a portion of an eighth IC chip including a variation on the semiconductor substrate shown in FIG. 9 bonded therein in accordance with another embodiment of the present invention.

[0028] FIG. 14 is a simplified cross section diagram of a portion of a ninth IC chip including a variation on the semiconductor substrate shown in FIG. 9 in accordance with another embodiment of the present invention.

[0029] FIG. 15 is a simplified cross section diagram of a portion of a tenth IC chip in accordance with another embodiment of the present invention.

[0030] FIG. 16 is a simplified flow chart for an example process for fabricating the structure shown in FIG. 15, according to embodiments of the present invention.

[0031] FIG. 17 is a simplified flow chart for another example process for fabricating the structure shown in FIG. 15, according to embodiments of the present invention.

[0032] FIG. 18 is a simplified cross section diagram of a portion of a semiconductor substrate with cavities that may be used with an embodiment of the present invention.

[0033] FIG. 19 is a simplified cross section diagram of a portion of an eleventh IC chip including the semiconductor substrate shown in FIG. 18 bonded therein in accordance with another embodiment of the present invention.

[0034] FIG. 20 is a simplified cross section diagram of a portion of a semiconductor substrate with cavities that may be used with an embodiment of the present invention.

[0035] FIG. 21 is a simplified cross section diagram of a portion of a twelfth IC chip including the semiconductor substrate shown in FIG. 20 bonded therein in accordance with another embodiment of the present invention.

[0036] FIG. 22 is a simplified flow chart for an example process for fabricating one or more of the structures shown in FIGS. 8-21, according to embodiments of the present invention.

DETAILED DESCRIPTION OF INVENTION

[0037] Reference now will be made in detail to example embodiments of the disclosed invention, one or more examples of which are illustrated in the accompanying drawings. Each example is provided by way of explanation of the present technology, not as a limitation of the present technology. In fact, it will be apparent to those skilled in the art that modifications and variations can be made in the present technology without departing from the spirit and scope thereof. For instance, features illustrated or described as part of one embodiment may be used with another embodiment to yield a still further embodiment. Thus, it is intended that the present subject matter covers all such modifications and variations within the scope of the appended claims and their equivalents.

[0038] Embodiments of the present invention generally inhibit parasitic surface conduction and enhance the RF performance of devices formed in one or more active layers of IC chips. Some embodiments of the present invention achieve these beneficial results by utilizing a layer transferred structure with a trap rich layer in a handle wafer of the layer transferred structure. In some embodiments of the present invention, the substrate is moved away from the active layer to a greater degree than in traditional SOI structures, thereby reducing the effect of substrate loss. In some embodiments of the present invention, the trap rich layer is introduced after active layer processing (e.g. CMOS processing, etc.) is complete, thereby preserving the efficacy of the trap rich

layer and minimizing disruption of the integrity of the overall IC chip. Some embodiments of the present invention improve the electrical performance of devices formed in the active layer, improve the efficacy of the trap rich layer for a given potential efficacy, and minimize the potential for manufacturing defects in the overall IC chip.

[0039] Some embodiments of the present invention can be described with reference to FIG. 2. FIG. 2 illustrates a structure 200 within a portion of an IC chip. The structure 200 may be formed by wafer bonding or layer transfer techniques, as described below. Therefore, the structure 200 generally comprises a handle wafer 201 bonded to a semiconductor wafer 202. The structure 200 can thus be referred to as a layer transfer structure. The semiconductor wafer 202 generally comprises an active layer 203 having a bottom side in contact with an insulator layer 204. The semiconductor wafer 202 is optionally capped by another insulator layer (not shown). In some embodiments, the semiconductor wafer 202 may be a silicon on sapphire wafer, a gallium arsenide wafer, an SOI wafer, etc. The handle wafer 201 generally comprises a handle substrate layer 205 and a bonding layer 206.

[0040] The active layer 203 may be a circuit layer that generally includes an active device layer 207 and a metallization or metal interconnect layer 208, which generally further include a combination of dopants, dielectrics, polysilicon, metal wiring, passivation, and other layers, materials and/or components that are present after circuitry has been formed therein. The circuitry may include metal wiring 209 (e.g. in the metal interconnect layer 208); passive devices such as resistors, capacitors, and inductors; and active devices such as a transistor 210 (e.g. in the active device layer 207). In other embodiments, the active layer 203 may be replaced with a circuit layer having Integrated Passive Devices (IPDs, a.k.a. Integrated Passive Components, IPCs) or a mix of active and passive devices. Such IPD circuit layers generally include functional blocks such as impedance matching circuits, harmonic filters, couplers and baluns and power combiners/dividers, etc. IPD circuit layers are generally fabricated using standard wafer fabrication technologies, such as thin film and photolithography processing, among others. IPD wafers can be designed as flip chip mountable or wire bondable components. Additionally, the substrates for IPD wafers usually are thin film substrates like silicon, alumina or glass. Furthermore, IPD wafers may be formed on quartz with no semiconductor material, so the wafer 202 may be an insulating wafer. Therefore, although the description herein refers to various semiconductor wafers (e.g.

202) and active layers (e.g. 203), other types of wafers and circuit layers (such as insulating wafers and IPD circuit layers, etc.) may be used in place thereof, where appropriate.

[0041] The bonding layer 206 can generally be a combination of one or more insulator layers and passivation layers used to isolate and protect the active layer 203. The bonding layer 206 may be a material used to bond a bottom exposed surface 211 of the handle wafer 201 to a top exposed surface 212 of the semiconductor wafer 202 during the wafer bonding or layer transfer procedure. In an alternative embodiment, the bonding layer 206 is added to the semiconductor wafer 202, instead of to the handle wafer 201, before wafer bonding or layer transfer. In some embodiments, the bonding layer 206 is formed by chemical vapor deposition (CVD) or thermal oxidation to create an oxide layer. Depending on the embodiment, as described herein, the bonding layer 206 may be formed before or after the trap rich layer 214. If the bonding layer 206 is formed before the trap rich layer 214, the benefit of the trap rich layer 214 will be slightly eroded due to the heat associated with forming the bonding layer 206. However, a single CVD or thermal oxidation process will not reduce trap density as much as will full active device processing.

[0042] The semiconductor wafer 202 may be a conventional semiconductor-on-insulator (SOI) wafer (with the insulator layer 204 formed as a buried oxide or other appropriate insulator or dielectric material) or a conventional bulk semiconductor wafer (with the insulator layer 204 implanted, deposited, grown, etc. as desired). Before bonding the handle wafer 201 to the semiconductor wafer 202, the structures of the active layer 203 are formed in or on a substrate of the semiconductor wafer 202. After bonding, a portion of the original semiconductor substrate (not shown) below the insulator layer 204 is removed such that a back side 213 of the insulator layer 204 is exposed. Once the underlying substrate is removed, the handle wafer 201 provides the required stabilizing force necessary to protect and preserve the electrical characteristics of devices or structures in the active layer 203. Additionally, further metallization or interconnect wiring (not shown) may extend through the insulator layer 204 and be deposited on the back side 213 of the insulator layer 204 for back side electrical connections to the components in the active layer 203.

[0043] An advantageous aspect of the configuration described with reference to FIG. 2 is that the resulting substrate (i.e. the handle substrate layer 205) of the structure 200 is further from the active layer 203 than in traditional SOI or bulk semiconductor

structures. This feature generally results because the bonding layer 206 is thicker than the insulator layers (similar to the insulator layer 204) of such traditional structures. Since the handle substrate layer 205 is relatively far away from the active layer 203, the effect of parasitic pathways and nonlinear capacitance is significantly lessened.

[0044] There are multiple reasons why the bonding layer 206 can be thicker than the insulator layer 204. For example, the insulator layer 204 is a high-quality insulator layer and the time and expense to form thick high-quality insulators is generally prohibitive. Also, the insulator layer 204 may be kept relatively thin because wafer warpage due to different thermal coefficients of expansion between the different layers in a semiconductor wafer or IC chip becomes a more pressing issue as the thickness of such an insulator layer (e.g. 204) increases. For an insulator layer thickness in excess of about 1 micrometer (.mu.m), this effect cannot be mitigated easily using ordinary semiconductor manufacturing techniques. Due to these and other constraints on the maximum thickness thereof, the insulator layer 204 cannot be made arbitrarily thick. Instead, a typical thickness for the insulator layer 204 may be about 0.1 to about 1 .mu.m. On the other hand, a typical thickness for the bonding layer 206, in accordance with some embodiments of the present invention, may be several micrometers thick.

[0045] The layer transfer structure 200 described with reference to FIG. 2 generally has fewer problems due to nonlinear substrate capacitance and substrate loss as compared to standard SOI structures. However, conventional layer transfer devices can still suffer from substrate loss due to the presence of the substrate (e.g. the handle substrate layer 205) in the handle wafer (e.g. 201). To increase the resistance of the structure 200 to these phenomena, a trap rich layer 214 may be provided within the handle substrate layer 205 generally adjacent the bonding layer 206 above the active layer 203. As used herein and in the appended claims the term "trap rich layer" generally refers to a layer having a high density of electrically active carrier traps.

[0046] As illustrated in FIG. 2, the trap rich layer 214 can be in contact with the bonding layer 206, and the bonding layer 206 can be in contact with the active layer 203. This configuration will effectively eliminate the effect of parasitic substrate conduction and substrate loss by inhibiting the movement of carriers that would otherwise occur at the interface of the handle substrate layer 205 and the bonding layer 206.

[0047] In general, a higher trap density within the trap rich layer 214 leads to a greater effect of minimizing nonlinear parasitic capacitance and parasitic surface conduction. In

some embodiments of the present invention, the trap rich layer 214 has a trap density of greater than 10.sup.11 cm.sup.-2 eV.sup.-1. Since embodiments in which the trap rich layer 214 is formed after the processing necessary to form structures in the active layer 203 do not suffer thermal degradation of the trap rich layer 214, these embodiments generally enable easier or more efficient methods of forming a higher trap density than is typical in the prior art.

[0048] In various embodiments of the present invention, the trap rich layer 214 is provided in variant forms. In some example embodiments, the trap rich layer 214 is formed through the deposition of high resistivity material on the surface of the handle substrate layer 205 before the handle wafer 201 is bonded to the semiconductor wafer 202. The deposited material could be polycrystalline semiconductor material or polycrystalline silicon and the handle substrate layer 205 could be very lightly doped silicon such that it has high resistivity.

[0049] In alternative embodiments, the trap rich layer 214 is formed through the implantation of high energy particles (e.g. a noble gas, Silicon, Oxygen, Carbon, Germanium, etc.) into the handle substrate layer 205 to create a damaged area in the handle substrate layer 205. The implantation can be done with or without the bonding layer 206 already present. However, the implantation is generally easier without the bonding layer 206, since some materials (e.g. an oxide) for the bonding layer 206 can impede the implantation. On the other hand, if the bonding layer 206 is a thermal oxide material, the heat from the formation of the bonding layer 206 after the implantation for the trap rich layer 214 could degrade the trap rich layer 214. In this case, the implantation is done after the thermal oxidation. For example, an implantation of Argon through about a 1000 .ANG. thermal oxide could be performed at about 1E15/cm.sup.2 and about 240 keV energy. The resulting damage in the silicon substrate will generally extend from the silicon surface to a depth of approximately 2000 .ANG..

[0050] The implanted particles could be Argon or Silicon or other suitable ions and the handle substrate layer 205 could be very lightly doped silicon such that it has high resistivity. Argon could beneficially be employed because it has a relatively large mass, so it will do substantial damage; but it is also inert, so it will not cause any unexpected side effects. Silicon, on the other hand, could be used as the implanted material for similar reasons in that the silicon will disrupt the silicon crystal structure of the handle substrate layer 205, but it will not have any other side effects. Oxygen or carbon could be beneficially used for implant because they can form a relatively stable trap density

with respect to subsequent thermal annealing due to the formation of Si--O or Si--C bonds, which disrupt the silicon crystal lattice, leaving some Si bonds dangling. In addition, with sufficient dose and subsequent thermal annealing, O atoms may start to coalesce, forming SiO.sub.x precipitates, which will form stable trap sites in the silicon lattice.

[0051] Additionally, multiple implant energies can be used to form the trap rich layer 214 from the bottom surface 211 (or the previous bottom surface before the bonding layer 206 is added) of the handle wafer 201 to a maximum desired depth or distance from the surface 211. Also, the dose can also be varied with the energy to create an almost constant trap density vs. depth. As an example of a two-implant sequence that results in an almost constant damage profile vs. depth, an implantation of Argon at 1E15/cm2 and 240 keV can be followed with a second implantation of Argon at 3E14/cm2 and 60 keV. This sequence will generally result in a damage profile that is almost constant from the silicon surface to a depth of about 3000 A. Furthermore, the implantation can be done with a low beam current and/or backside wafer cooling to prevent self-annealing of damage due to self-heating from the implant beam.

[0052] In other alternative embodiments, the trap rich layer 214 is comprised of the entire handle wafer 201. For example, in some embodiments of the present invention, the handle wafer 201 is comprised of high resistivity polysilicon, so the trap rich layer 204 extends through the entire extent of the handle wafer 201. These alternative embodiments would exhibit the advantageous characteristic of excellent performance and low cost because polysilicon wafers are less expensive than monocrystalline silicon wafers and because the traps would be located throughout the thickness of the entire handle wafer 201.

[0053] Some embodiments form the trap rich layer 214 throughout the entire handle wafer 201 by irradiating the handle wafer 201 by exposure to relatively high-energy ionizing radiation, such as gamma rays, X-rays or other suitable high-energy particle sources (e.g. MeV electrons, protons or other high-energy particle that can cause semiconductor lattice damage). Such radiation can cause damage to a semiconductor lattice, resulting in trap generation. A suitable gamma ray source, for example, may be Cobalt-60.

[0054] An advantage of using radiation is that it penetrates easily through the entire handle wafer 201, thereby forming the traps throughout the entire bulk of the handle wafer 201. This feature makes the trap density per unit volume relatively constant

throughout the thickness of the handle wafer 201 and can create a high integrated trap density per unit area of wafer surface, which is desirable. An alternative is to irradiate the surface of the handle wafer 201 with a low-energy radiation that cannot penetrate very deeply into the substrate layer 205, so only a surface layer of traps is formed.

[0055] Another benefit of irradiation is that it can be performed on a handle wafer with almost any type of surface films previously deposited thereon. Therefore, the bonding layer 206, for example, can already be present at the surface 211 of the handle wafer 201. Due to the high penetration depth of gamma rays, for example, most of the radiation will pass through the bonding layer 206 and into the substrate layer 205. This feature allows the trap rich layer 214 to be created after the deposition or thermal growth of the bonding layer 206. An additional benefit of trap creation after deposition or growth of the bonding layer 206 is that interface traps may be created at the Si--SiOx interface, causing an additional layer of traps at the bonding surface of the substrate layer 205. Having a layer of traps at this surface can be beneficial by preventing inversion or accumulation of free carriers at this surface. Another benefit of forming the trap rich layer 214 after thermal oxidation is that thermal oxidation requires high temperatures and long times which can result in annealing and degradation of previously created traps, which is counter to the general goal of high trap density. Also, although the bonding layer 206 could be formed by CVD, in some cases a thermally grown oxide for the bonding layer 206 may have more desirable properties than a CVD oxide.

[0056] Another benefit of irradiation for inducing trap formation is that because of the high penetration depth (e.g. of gamma rays), an entire box of wafers (typically 25 wafers in a box) can be irradiated as a batch, which saves time and money. Also, the wafer box can be left sealed during the irradiation procedure, since the radiation can penetrate the box, thereby preventing potential contamination of the wafers. This feature also allows irradiation to take place in an industrial environment, instead of in a clean room, thereby reducing cost and increasing the number of fabrication places that can be used for the procedure.

[0057] The irradiation technique could be used on SOI wafers in addition to bulk semiconductor wafers. However, the top semiconductor layer of the SOI wafer would be damaged too. A rapid top surface annealing could repair some of the damage to the top semiconductor layer. However, such annealing may not be allowable if CMOS processing of the top semiconductor layer has already occurred. On the other hand, if

the damage to devices made in the top semiconductor layer was acceptable, then the trap creation could take place after CMOS processing without a subsequent repair anneal. This option could be simpler and less expensive than creating a trap rich layer in an SOI wafer before CMOS processing. Irradiation could also be used in combination with other trap generation mechanisms to cause an overall increase in the effective resistivity. For example, after implant the wafer with the trap rich layer could be irradiated before bonding to the second wafer.

[0058] Some embodiments may create the trap rich layer 214 by mechanical damage methods inflicted on the surface of the handle substrate layer 205 before the bonding layer 206 is formed. (Similar mechanical damage methods are sometimes done by semiconductor wafer manufacturers for "extrinsic gettering" purposes.) The damage may be caused by any of several methods, such as brushing the surface of the handle substrate layer 205 with a metal or ceramic brush, impinging small balls of hard material onto the surface of the handle substrate layer 205 or grinding the surface of the handle substrate layer 205. The bonding layer 206 can then be deposited on the surface of the handle wafer 201 and planarized with chemical mechanical polishing (CMP) to allow proper fusion bonding to the top exposed surface 212 of the semiconductor wafer 202. Alternatively, a liquid adhesive bonding agent can be applied to the surface of the handle wafer 201, allowing the liquid to smooth out the bonding surface 211 of the handle wafer 201 over the mechanically roughened surface of the handle substrate layer 205.

[0059] In some embodiments, since the trap rich layer 214 is part of the handle wafer 201 that is bonded to the semiconductor wafer 202, the trap rich layer 214 is generally added to the semiconductor wafer 202 after most or all of the structures in the active layer 203 have been formed. Consequently, unlike in the prior art described above, the processing or fabrication methods used to form the structures in the active layer 203 generally do not affect the trap rich layer 214.

[0060] In various embodiments of the present invention, the bonding layer 206 is provided in variant forms. For example, in some embodiments, the bonding layer 206 consists of two layers of insulator material initially separately bonded to the handle wafer 201 and the semiconductor wafer 202. In some alternative embodiments, the trap rich layer 214 may be present on the top surface of the semiconductor wafer 202 and directly bonded to the handle wafer 201. In this case, the bonding layer 206 is completely absent. Alternatively, the trap rich layer 214 may be present on the

semiconductor wafer 202 and covered by a suitable bonding layer 206. In this case, the trap rich layer 214 is between the active layer 203 and the bonding layer 206. In some embodiments, the bonding layer 206 comprises silicon dioxide or any other appropriate type of insulator. In other embodiments, the bonding layer 206 comprises passivation layers and/or other auxiliary layers.

[0061] In various embodiments of the present invention, the active layer 203 can be provided in variant forms. In some embodiments, the active layer 203 contains one or more of the transistor 210, e.g. various appropriate combinations of metal oxide semiconductor (MOS) devices, bipolar devices, vertical diffused MOS (VDMOS) power devices, etc. Various forms of the transistor 210 generally comprise a gate region 215 and a body/channel region 216. In some embodiments of the present invention, the gate region 215 is between the body/channel region 216 and the trap rich layer 214. Also, in some embodiments of the present invention, the metal wiring 209 of the metal interconnect layer 208 is between the body/channel region 216 and the trap rich layer 214. These embodiments generally exhibit an advantageous characteristic in that the active device material forming the source, drain, and channel of the active devices in the active device layer 207 (e.g. the transistor 210) is further separated from the handle substrate layer 205 (compared to the active device layer 104 and the substrate layer 101 of FIG. 1), thereby improving the RF performance of the active devices as described above.

[0062] The previously described advantageous characteristic is enhanced in embodiments where the active device layer 207 is at the bottom of the active layer 203 and the active regions are contacted only by the lowest layer of metal in the metal interconnect layer 208. In other embodiments of the present invention, part or all of the metal interconnect layer 208 is added below the insulator layer 204, e.g. after the original underlying substrate material of the semiconductor wafer 202 is removed or thinned. In this case, the active device layer 207 is not as far separated from the handle substrate layer 205 as in the previously described embodiment. However, the thickness of the bonding layer 206 may be chosen to ensure a greater beneficial separation between the active device layer 207 and the handle substrate layer 205 compared to the active device layer 104 and the substrate layer 101 of FIG. 1.

[0063] In some embodiments of the present invention, the single structure 200 comprises multiple trap rich layers. For example, the structure 200 could comprise a trap rich layer below the insulator layer 204 in addition to the trap rich layer 214. This

additional trap rich layer may be formed according to the prior art described above or in accordance with embodiments described with reference to FIG. 5 below. In another example, the single structure 200 could comprise multiple active layers 203 (or active device layers 207) that are separated by trap rich layers in addition to the overlying trap rich layer 214. In addition to the mitigation of intra-layer cross talk as described above, these embodiments generally exhibit the additional advantageous characteristic of improving isolation between signals located in different active layers 203. This characteristic is of particular importance in situations where passive devices such as inductors are located in one of the active layers 203 because it is desirous to provide good isolation between these devices and the active devices in the active device layer(s) 207. The improved isolation thus formed by the trap rich layer(s) can additionally allow the passive devices to be closer to the active devices (e.g. the transistor 210) to thereby reduce parasitic capacitance while still maintaining a given desirable degree of isolation.

[0064] Some embodiments of the present invention can be described with reference to FIG. 3. FIG. 3 illustrates a structure 300 having multiple layers of signal processing circuitry. The structure 300 generally includes a semiconductor wafer 301 and a handle (or second semiconductor) wafer 302 bonded together by wafer bonding or layer transfer techniques.

[0065] The semiconductor wafer 301 generally includes an active layer 303, an insulator (e.g. an oxide or other dielectric) layer 304 and a substrate layer 305. The semiconductor wafer 301 is optionally capped by another insulator layer (not shown). The active layer 303 generally includes an active device layer 306 and a metallization or metal interconnect layer 307. The active layer 303 thus also generally includes signal processing circuitry, such as one or more active devices (e.g. a transistor 308) in the active device layer 306 and metal wiring 309 in the metal interconnect layer 307.

[0066] The handle wafer 302 generally includes an active layer 310, a bonding layer 311, a trap rich layer 312, and underlying and overlying insulator (e.g. an oxide or other dielectric) layers 313 and 314. The active layer 310 generally includes an active device layer 315 and a metallization or metal interconnect layer 316. The active layer 310 thus also generally includes signal processing circuitry, such as one or more active devices (e.g. a transistor 317) in the active device layer 315 and metal wiring 318 in the metal interconnect layer 316. The handle wafer 302 is, thus, a second semiconductor wafer in this embodiment.

[0067] According to various embodiments, the trap rich layer 312 is formed after the formation of one or both of the active layers 303 and 310. Additionally, the trap rich layer 312 is interposed between the two wafers 301 and 302 on the top side of the semiconductor wafer 301. Furthermore, the trap rich layer 312 may have any one or more of the characteristics and may be formed by any of the techniques described herein for the trap rich layer 214 (FIG. 2), depending on the requirements of a desired configuration or implementation.

[0068] In some embodiments, the handle wafer 302 is formed from an SOI or bulk semiconductor wafer. Accordingly, in some embodiments, the trap rich layer 312 is formed within a semiconductor substrate of the handle wafer 302 prior to the formation of the active layer 310. In this case, however, the subsequent formation of the structures in the active layer 310 may degrade the trap rich layer 312, as mentioned above. However, the formation of the active layer 303 in the semiconductor wafer 301 generally does not affect the trap rich layer 312, since the trap rich layer 312, as part of the handle wafer 302, is added to the semiconductor wafer 301 after the formation of the active layer 303.

[0069] In other embodiments, the trap rich layer 312 is formed after the formation of the active layer 310. For example, the trap rich layer 312 may be high resistivity material deposited onto a bottom surface of the insulator layer 313, e.g. after an additional handle wafer (not shown) is bonded to the top of the handle wafer 302 and the underlying semiconductor substrate is removed or thinned to expose the insulator layer 313. Alternatively, the underlying semiconductor substrate is not fully removed, and the trap rich layer 312 is formed in the remaining portion of the underlying semiconductor substrate, e.g. by implantation of high energy particles to create a damaged area in the underlying semiconductor substrate, as mentioned above. The additional handle wafer is subsequently removed either before or after the handle wafer 302 is bonded to the semiconductor wafer 301. In variations of these embodiments, the additional handle wafer is optional or the overlying insulator layer 314 originates as part of the bonding layer used to bond the additional handle wafer to the handle wafer 302. In each case, the formation of the active layer 303 in the semiconductor wafer 301 generally does not affect the trap rich layer 312, since the trap rich layer 312, as part of the handle wafer 302, is added to the semiconductor wafer 301 after the formation of the active layer 303. In other alternatives, the additional handle wafer remains attached to the handle wafer 302 immediately after bonding the semiconductor wafer 301 and the

handle wafer 302, and then either the additional handle wafer or the substrate layer 305 is removed or thinned.

[0070] In other alternative embodiments, the trap rich layer 312 is added to the handle wafer 302 by layer transfer techniques after the formation of the active layer 310. (See the dual layer transfer technique described below with reference to FIG. 5.) Thus, the trap rich layer 312 is formed as a layer in (or as the entire extent of) another handle wafer. The other handle wafer is then bonded to the handle wafer 302, e.g. with the insulator layer 313 (formed on either the other handle wafer or the handle wafer 302) serving as a bonding layer. Then any unnecessary thickness of the other handle wafer is removed, leaving the trap rich layer 312 as part of the handle wafer 302. Additionally, the bonding layer 311 may be formed in the other handle wafer along with the trap rich layer 312 before bonding the trap rich layer 302 to the handle wafer 302, or the bonding layer 311 may be formed on the trap rich layer 312 after such bonding (and optionally after the removal of any unnecessary thickness of the other handle wafer). Some of these embodiments generally enable the use of a low cost polysilicon wafer, or the use of radiation damaging techniques, to form the trap rich layer 312 in the other handle wafer. In each case, the formation of the active layer 303 in the semiconductor wafer 301 generally does not affect the trap rich layer 312, since the trap rich layer 312, as part of the handle wafer 302, is added to the semiconductor wafer 301 after the formation of the active layer 303.

[0071] In other embodiments, the trap rich layer 312 is added to the semiconductor wafer 301, instead of to the handle wafer 302 (after the active layer 303 is formed, but before the semiconductor wafer 301 and the handle wafer 302 are bonded together). In this case, the bonding layer 311 is an insulating layer, and the insulating layer 313 is a bonding layer. Additionally, the active layer 310 may be formed before the bonding, so the formation of neither active layer 303 nor 310 affects the trap rich layer 312.

[0072] The bonding layer 311 can generally be a combination of one or more insulator layers and passivation layers used to isolate and protect the active layers 303 and 310. The bonding layer 311 may also be a material used to bond a bottom exposed surface 319 of the handle wafer 302 to a top exposed surface 320 of the semiconductor wafer 301 during the wafer bonding or layer transfer procedure. In some embodiments, the bonding layer 311 comprises an etch-stop layer used when removing material (e.g. part or all of an underlying substrate layer) from the handle wafer 302 as described below. In other embodiments, the bonding layer 311 comprises a substrate material of the handle

wafer 302 that was not fully removed when the handle wafer 302 was prepared for bonding to the semiconductor wafer 301 as described below. In another alternative, the bonding layer 311 is added to the semiconductor wafer 301, instead of to the handle wafer 302, before wafer bonding or layer transfer.

[0073] In some embodiments, the signal processing circuitry in the active layer 310 of the handle wafer 302 is connected to the signal processing circuitry in the active layer 303 of the semiconductor wafer 301 through a metal-to-metal bond formed by a metal contact 321 between the metal wiring 309 and 318 in the metal interconnect layers 307 and 316. The metal contact 321 may thus be stacked metal layers formed by conventional CMOS metallization processes. Although a connection through the trap rich layer 312 may slightly decrease its efficacy, the benefits accruing from the use of a trap rich layer as described above will still be realized by this structure 300.

[0074] In various embodiments of the present invention, the wafers 301 and 302 that are on either side of the trap rich layer 312 may exhibit variant characteristics. In some embodiments of the present invention, the active layer 310 consists of passive devices such as inductors that are used for RF signal processing. The insulator layers 313 and 314 may be comprised of insulator material and passivation material meant to isolate the signal processing devices in the active layer 310. Also, in some embodiments of the present invention, additional layers (e.g. additional handle wafers) having other signal processing circuitry may overlay the handle wafer 302. Each such additional layer may also have an additional trap rich layer (e.g. similar to the trap rich layer 312) interposed between the additional layer and the underlying remainder of the structure 300.

[0075] Some embodiments of the present invention can be described with reference to FIG. 4. FIG. 4 illustrates a layer transfer structure 400 generally having multiple layers of signal processing circuitry among elements 401-420 (e.g. having similar descriptions as, but not necessarily being identical to, elements 301-320, respectively, of FIG. 3).

[0076] The trap rich layer 412 is generally interposed between the active layers 403 and 410, as described above with respect to elements 303, 310 and 312. The trap rich layer 412 may have any one or more of the characteristics and may be formed by any of the techniques described herein for the trap rich layer 214 or 312, depending on the requirements of a desired configuration or implementation.

[0077] Additionally, the multiple layers of signal processing circuitry in FIG. 4 may be connected between the metal wiring 409 and 418 within the metal interconnect layers 407 and 416 of the stacked wafers 401 and 402, respectively, using a through

semiconductor via (TSV) connection 421. The TSV connection 421 can be etched down through multiple layers of the stacked wafer 401 and 402 as needed, including through existing metallization, to which the TSV connection 421 can electrically connect. For example, the TSV connection 421 connects to circuitry in the active layer 410 of the handle (or second semiconductor) wafer 402 through a lateral contact (e.g. one or more portions of the metal wiring 418) and to circuitry in the active layer 403 of the semiconductor wafer 401 through a bottom contact (e.g. one or more portions of the metal wiring 409). The function of the lateral contact (418) can be implemented using metal sidewalls or platforms in the active layer 410. The TSV connection 421 generally allows for relatively easy connection of additional active layers (e.g. of additional handle wafers) that may overlay the active layer 410 in a fashion similar to that of the handle wafer 402 overlaying the semiconductor wafer 401, with additional trap rich layers interposed between each additional active layer and the underlying active layer.

[0078] Additionally, as before, the structure 400 may be capped by the insulator layer 414 which may help to isolate the signal processing circuitry in the active layer 410. The insulator layer 414 may comprise layers of passivation and insulator material.

[0079] Some embodiments of the present invention can be described with reference to FIG. 5. FIG. 5 illustrates a layer transfer structure 500 generally having a semiconductor wafer 501 bonded to a handle wafer 502.

[0080] The semiconductor wafer 501 generally has an active layer 503 and an insulator (e.g. an oxide or other dielectric) layer 504. The active layer 503 generally includes an active device layer 505 and a metallization or metal interconnect layer 506. The active device layer 505 generally has various active devices 507, such as various types of transistors. Additionally, the metal interconnect layer 506 generally has metal wiring 508. Furthermore, an insulating cap layer (not shown) may be formed on the top of the metal interconnect layer 506.

[0081] The handle wafer 502 generally has a bonding layer 509 and a substrate layer 510. The substrate layer 510 may include a trap rich layer 511 therein. The trap rich layer 511 may have any one or more of the characteristics and may be formed by any of the techniques described herein for the trap rich layers 214, 312 or 412, as may be appropriate or allowable depending on the requirements of a desired configuration or implementation. Additionally, the trap rich layer 511 may comprise only a portion of the substrate layer 510 (as shown) or the entire substrate layer 510.

[0082] The bonding layer 509 may have any one or more of the characteristics and may be formed by any of the techniques described herein for the bonding layers 206, 311 or 411, as may be appropriate or allowable depending on the requirements of a desired configuration or implementation. The bonding layer 509 generally bonds a top surface 512 of the handle wafer 502 to a bottom surface 513 of the semiconductor wafer 501. As an alternative, the bonding layer 509 may be formed on the bottom surface 513 of the semiconductor wafer 501, instead of on the handle wafer 502.

[0083] In some embodiments, the structure 500 is formed by a dual layer transfer or wafer bonding technique. In this case, after most or all of the processing to form the structures in the active layer 503, a temporary handle wafer (not shown) is bonded to a top surface 514 of the semiconductor wafer 501. The temporary handle wafer generally provides structural support for the semiconductor wafer 501 so that part or all of a semiconductor layer (not shown) underlying the insulator layer 504 can be removed. Then the handle wafer 502 is bonded to the bottom surface 513 of the semiconductor wafer 501, and part or all of the temporary handle wafer is removed. Any remaining part of the temporary handle wafer may, for example, form the insulating cap layer (not shown) on the top of the metal interconnect layer 506.

[0084] The general result of embodiments in accordance with FIG. 5 is that the structure 500 bears a greater resemblance to the prior art structure 100 (FIG. 1) than do the embodiments that accord with FIGS. 2, 3 and 4. This resemblance generally relates to the positioning of the trap rich layer 511 below, rather than above, the active layer 503. However, the difference in fabrication techniques enables some advantageous differences for the structure 500 compared to the prior art structure 100. For example, since the handle wafer 502 is bonded to the semiconductor wafer 501 after the formation of the active layer 503, the trap rich layer 511 is generally unaffected by the formation of the structures in the active layer 503. The trap rich layer 511 is thus generally subject to much less risk of degradation than is the prior art trap rich layer in region 110 due to any subsequent processing. Additionally, as mentioned above with respect to the insulator layer 204 and the bonding layer 206 of FIG. 2, the bonding layer 509 can generally be made of an insulating material that is considerably thicker than the insulator layer 504. The relatively large thickness of the bonding layer 509 generally ensures a greater beneficial separation between the active device layer 505 and the substrate layer 510 compared to that of the active device layer 104 and the substrate layer 101 of FIG. 1. Therefore, since the substrate layer 510 is relatively far away from

the active device layer 505, the effect of parasitic pathways and nonlinear capacitance is significantly lessened compared to that of the prior art structure 100. Additional advantages of the structure 500 may also be apparent.

[0085] In some variations on embodiments in accordance with FIG. 5, the structure 500 is generally an intermediary structure in a process for forming the structure 300 or 400 of FIG. 3 or 4. In this case, the substrate layer 510 is thinned or removed, and a bonding layer (e.g. 311 or 411) is formed on a bottom surface thereof in preparation for bonding to another semiconductor wafer (e.g. 301 or 401) having another active layer (e.g. 303 or 403). The active layer 503 is thus either active layer 310 or 410. Additionally, the trap rich layer 511 is thus either trap rich layer 312 or 412 and is formed after the active layers 303 and 310 or 403 and 410. The trap rich layer 511 is thus unaffected by the formation of either active layer 303 and 310 or 403 and 410.

[0086] In the prior art, an attempt has been made to form devices and material layers in a wafer, attach a support on top of the wafer, remove or thin portions of the wafer that underlie the devices and material layers, bond a substrate to the bottom of the wafer, and remove the top mounted support. The bottom mounted substrate has an insulator layer (such as silicon nitride or silicon oxide) on its bonding surface and comprises Au, Ag, or Li doped silicon that forms a high resistivity silicon substrate with deep level trapping sites under the insulator layer. However, the techniques described herein for forming the trap rich layer 511 generally produce a significantly higher trap density than is possible with this prior art technique. Therefore, embodiments in accordance with FIG. 5 have this significant advantage over this prior art technique. Also, Au, Ag and Li are generally considered harmful contaminants in almost all semiconductor fabrication facilities. Therefore, it is generally undesirable for wafers doped with these elements to be processed in most facilities due to concerns with cross-contamination to other processes.

[0087] Some embodiments of the present invention can be described with reference to FIG. 6. FIG. 6 illustrates a layer transfer structure 600 generally having a semiconductor wafer 601 bonded to a handle wafer 602.

[0088] The semiconductor wafer 601 generally has an active layer 603, underlying and overlying insulator (e.g. an oxide or other dielectric) layers 604 and 605 and a trap rich layer 606. The active layer 603 generally includes an active device layer 607 and a metallization or metal interconnect layer 608. The active device layer 607

generally has various active devices 609, such as various types of transistors. Additionally, the metal interconnect layer 608 generally has metal wiring 609. Furthermore, an insulating cap layer (not shown) may be formed on the top of the trap rich layer 606. The trap rich layer 606 may have any one or more of the characteristics and may be formed by any of the techniques described herein for the trap rich layers 214, 312, 412 or 511, as may be appropriate or allowable depending on the requirements of a desired configuration or implementation.

[0089] The handle wafer 602 generally has a substrate layer 611 and a bonding layer 612. The bonding layer 612 may have any one or more of the characteristics and may be formed by any of the techniques described herein for the bonding layers 206, 311, 411 or 509, as may be appropriate or allowable depending on the requirements of a desired configuration or implementation. The bonding layer 612 generally bonds a bottom surface 613 of the handle wafer 602 to a top surface 614 of the semiconductor wafer 601. As an alternative, the bonding layer 612 may be formed on the top surface 614 of the semiconductor wafer 601, instead of on the handle wafer 602.

[0090] The trap rich layer 606 is generally between the active layer 603 of the semiconductor wafer 601 and the substrate layer 611 of the handle wafer 602. Additionally, the trap rich layer 606 is formed after most or all of the structures of the active layer 603, so the trap rich layer 606 is generally unaffected by the formation of the structures in the active layer 603. Therefore, even though the trap rich layer 606 is formed on the semiconductor wafer 601, rather than on the handle wafer 602, the trap rich layer 606 is generally subject to much less risk of degradation than is the prior art trap rich layer in region 110 due to any subsequent processing.

[0091] FIG. 7 shows a flowchart for a process 700 for fabricating at least part of an integrated circuit chip (e.g. similar to structure 200 or 600, FIG. 2 or 6), according to some embodiments of the present invention. It is understood, however, that the specific process 700 is shown for illustrative purposes only and that other embodiments (in addition to specifically mentioned alternative embodiments) may involve other processes or multiple processes with other individual steps or a different order or combination of steps and still be within the scope of the present invention.

[0092] Upon starting (at 701), the semiconductor wafer 202 or 601 is prepared at 702. If the semiconductor wafer 202 or 601 is an SOI wafer, then the preparation (at 702) may simply be to provide a standard SOI wafer. If the semiconductor wafer 202 or 601 is a bulk semiconductor wafer, then the preparation (at 702) may include creating a buried

P+ layer in the bulk semiconductor wafer 202 or 601, e.g. by epitaxial growth or ion implantation methods. Epitaxial methods may involve epitaxially depositing a layer of P+ material on a P- or N- substrate. Then a layer of lightly-doped silicon may be epitaxially deposited to use as an active device layer. This layer may be thick enough so that up-diffusion from the P+ layer does not reach the active device layer 207 or 607 by the end of processing to form the structures in the active layer 203 or 603. Ion implantation methods, on the other hand, may involve performing a high-dose, high-energy ion (e.g. Boron, etc.) implant into the surface of the bulk semiconductor wafer, forming a buried P+ layer deep enough so it will not diffuse up to the active device layer 207 or 607 during processing to form the structures in the active layer 203 or 603.

[0093] At 703, the active layer 203 or 603 is formed to produce a circuit with a set of active devices in the semiconductor wafer 202 or 601. For an SOI wafer, the active layer 203 or 603 may be manufactured using a standard SOI process. For a bulk semiconductor wafer, the active layer 203 or 603 may be formed with a process that provides an etch stop for a subsequent substrate removal, such as the aforementioned P+ layer formed below the active device layer. Additionally, a chemical mechanical polishing is optionally performed of the top surface of the semiconductor wafer 202 or 601.

[0094] For embodiments according to FIG. 6, the trap rich layer 606 is formed (at 704) on the semiconductor wafer 601 above, and after the formation of, the active layer 603. Additionally, the insulator (e.g. an oxide or other dielectric) layer 605 may be formed beforehand. Also, an additional dielectric/oxide layer (not shown) may be formed over the trap rich layer 606. The trap rich layer 606, the insulator layer 605 and the additional dielectric/oxide layer may be deposited or epitaxially grown above the active layer 603 or added by layer transfer techniques from another handle wafer. If the trap rich layer 606 is added by layer transfer techniques, then the other handle wafer is processed separately to form the trap rich layer 606 and any adjacent dielectric or insulator layers. In this case, for example, the trap rich layer 606 may be polycrystalline semiconductor on dielectric on substrate or damaged single crystal top semiconductor on dielectric on substrate. After bonding the other handle wafer to the semiconductor wafer 601, the substrate of the other handle wafer may be removed, e.g. as described herein for removing semiconductor substrate material. The dielectric layer that was under the trap-rich layer 606 is optionally left in place. Additionally, another dielectric layer is

optionally deposited on the top surface exposed after removing the semiconductor substrate of the other handle wafer.

[0095] If direct bonding is subsequently to be performed to bond the semiconductor wafer 202 or 601 to the handle wafer 201 or 602, the top surface of the semiconductor wafer 202 or 601 may be planarized after 703 or 704. On the other hand, if an adhesive bond is to be performed, then planarization may not be necessary.

[0096] Separately from 702-704, the handle wafer 201 or 602 is prepared (at 705). Such preparation may include the formation (at 706) of the bonding layer 206 or 612 and, for embodiments according to FIG. 2, the formation (at 707) of the trap rich layer 214, by any appropriate method or in any appropriate order as described above.

[0097] At 708, the handle wafer 201 or 602 is bonded to the top surface of the semiconductor wafer 202 or 601. The bonding may be a direct oxide-oxide bond, an adhesive bond, an anodic bond, a low-temperature glass frit bond, a molecular bond, an electrostatic bond, etc., as appropriate for a given situation. For embodiments according to FIG. 2, therefore, even though the trap rich layer 214 may be formed in the handle wafer 201 at any time before, during or after the formation of the active layer 203 in the semiconductor wafer 202, the trap rich layer 214 is not added to the structure 200 until after the formation of the active layer 203.

[0098] At 709, the original underlying, or back side, portion (e.g. a semiconductor substrate) of the semiconductor wafer 202 or 601 is substantially removed or thinned. Most of the semiconductor substrate can be removed by back side grinding. A final portion of the semiconductor substrate can be removed by a wet etch, selective chemical mechanical polishing (CMP), a dry etch, etc., leaving at least the active device layer 207 or 607 (or the insulator layer 204 or 604, if it is part of the original semiconductor wafer 202 or 601). For embodiments using a bulk semiconductor wafer, the original underlying substrate is removed to the P+ layer (described above) using a wet chemical etch that is highly selective to P+ material (for example EDP, KOH, or TMAH). The etch can be either chemical or electro-chemical. Additionally, the P+ layer is optionally removed using any combination of grinding, polishing, CMP, dry etch, or non-selective wet etch. The P+ layer will only be a few microns in thickness, so a much better uniformity of a remaining relatively thin (e.g. less than 1 .mu.m) semiconductor film can be achieved than if the semiconductor wafer 202 or 601 was thinned mechanically. Furthermore, after removing/thinning the various layers or materials at 709, a

passivation dielectric layer(s) is optionally deposited on the newly-exposed surface to reduce effects due to moisture and ionic contamination ingress.

[0099] At 710, patterned contact and metallization are formed for any top or back side connections (e.g. top or bottom electrodes and contacts, etc., as desired). At 711, various passivation deposition techniques are performed and pad openings are formed, so the overall IC chip can be generally completed with bumps, pillars, or other post-processing metallization. The process 700 then ends at 712.

[00100] FIG. 8 shows a flowchart for a process 800 for fabricating at least part of an integrated circuit chip (e.g. similar to structure 300 or 400, FIG. 3 or 4), according to some embodiments of the present invention. It is understood, however, that the specific process 800 is shown for illustrative purposes only and that other embodiments (in addition to specifically mentioned alternative embodiments) may involve other processes or multiple processes with other individual steps or a different order or combination of steps and still be within the scope of the present invention.

[00101] Upon starting (at 801), the semiconductor wafer 301 or 401 is prepared at 802 and the active layer 303 or 403 is formed at 803. For example, 802 and 803 may be similar to 702 and 703, respectively, as described above for an SOI wafer or a bulk semiconductor wafer. At this point, if an electrical connection is to be made between the semiconductor wafer 301 or 401 and the handle wafer 302 or 402 (e.g. via the metal contact 321), then the semiconductor wafer 301 or 401 has metal exposed with the metal surface coplanar with a top dielectric surface.

[00102] Optionally, the trap rich layer 312 or 412 may be formed (at 804) on top of the semiconductor wafer 301 or 401, similar to the formation of the trap rich layer 606 (at 704), as described above, instead of forming the trap rich layer 312 or 412 in the handle (or second semiconductor) wafer 302 or 402, as described below. In this case, since the active layer 303 or 403 is formed before the trap rich layer 312 or 412, the trap rich layer 312 or 412 is unaffected by the processes that form the active layer 303 or 403. Additionally, since the active layer 310 or 410 is formed in the handle wafer 302 or 402 before bonding to the semiconductor wafer 301 or 401, the trap rich layer 312 or 412 is also unaffected by the processes that form the active layer 310 or 410.

[00103] If the trap rich layer 312 or 412 is added (at 804) by layer transfer techniques, then another handle wafer is processed separately to form the trap rich layer 312 or 412 and any adjacent dielectric or insulator layers. In this case, for example, the trap rich layer 312 or 412 may be polycrystalline semiconductor on dielectric on

substrate or damaged single crystal top semiconductor on dielectric on substrate. After bonding the other handle wafer to the semiconductor wafer 301 or 401, the substrate of the other handle wafer may be removed, e.g. as described herein for removing semiconductor substrate material. The dielectric layer that was under the trap-rich layer 312 or 412 is optionally left in place. Additionally, another dielectric layer is optionally deposited on the top surface exposed after removing the semiconductor substrate of the other handle wafer.

[00104] Separately from 802-804, the handle wafer 302 or 402 is prepared (at 805), e.g. similar to 702 or 802, as described above for an SOI wafer or a bulk semiconductor wafer. If the trap rich layer 312 or 412 is not formed at 804, then since the trap rich layer 312 or 412 is below the active layer 310 or 410, the trap rich layer 312 or 412 may optionally be formed (at 806) before the formation (at 807) of the active layer 310 or 410. Since the active layer 303 or 403 is formed in the semiconductor wafer 301 or 401 before bonding to the handle wafer 302 or 402, the trap rich layer 312 or 412 is unaffected by the processes that form the active layer 303 or 403. However, since the subsequent formation of the active layer 310 or 410 could degrade the trap rich layer 312 or 412, the trap rich layer 312 or 412 may be formed from the back side of the handle wafer 302 or 402 after the formation (at 807) of the active layer 310 or 410, as described below at 810.

[00105] The active layer 310 or 410 is formed at 807. The active layer 310 or 410 may have active devices, passive devices, or both, depending on the situation or embodiment. The active layer 310 or 410 (or the handle wafer 302 or 402 as a whole) may have similar or different material layer sequences to that of the active layer 303 or 403 (or of the semiconductor wafer 301 or 401 as a whole). Additionally, the active layer 310 or 410 may be based on SOI wafer (e.g. layers including a substrate, a buried oxide and device semiconductor material) or bulk semiconductor wafer (e.g. layers including a lightly doped substrate, a semiconductor layer doped P+ at the surface and device semiconductor material) types of processes, regardless of the types of wafer or processes used to form the active layer 303 or 403.

[00106] At 808, a second handle wafer (not shown) is bonded to a top surface of the handle wafer 302 or 402 at least after the formation (at 807) of the active layer 310 or 410 and optionally after the formation (at 806) of the trap rich layer 312 or 412. The second handle wafer may be permanent or temporary, depending on the situation or embodiment.

[00107] At 809, the original underlying, or back side, portion (e.g. a semiconductor substrate) of the handle wafer 302 or 402 is substantially removed or thinned. In some respects, this removal may be similar to 709 above. Most of the semiconductor substrate can be removed by back side grinding. A final portion of the semiconductor substrate can be removed by a wet etch, selective chemical mechanical polishing (CMP), a dry etch, etc. If the thickness of the remaining semiconductor material is not a critical parameter, then a mechanical stop may be sufficient.

[00108] If the trap rich layer 312 or 412 (or the bonding layer 311 or 411) has already been formed (at 806) in the handle wafer 302 or 402, then the removal/thinning of the underlying portion stops at this point. On the other hand, if the trap rich layer 312 or 412 is not already present, then the removal/thinning stops at least at the active device layer 315 or 415 (or the insulator layer 313 or 413, if it is part of the original handle wafer 302 or 402).

[00109] If the trap rich layer 312 or 412 has not been formed at 804 or 806, then the trap rich layer 312 or 412 may be formed at 810. In this case, since the underlying portion of the handle wafer 302 or 402 has been removed or thinned, the trap rich layer 312 or 412 can be formed on the back side of the handle wafer 302 or 402. The trap rich layer 312 or 412 may thus be formed by any appropriate method. If the trap rich layer 312 or 412 is formed by a dual layer transfer or wafer bonding technique as described with respect to FIG. 5, then the underlying substrate layer 510 may be removed or thinned before the handle wafer 302 or 402 is bonded to the semiconductor wafer 301 or 401.

[00110] Additionally, in this case, since the active layer 310 or 410 is formed before the trap rich layer 312 or 412 is added to the handle wafer 302 or 402, the trap rich layer 312 or 412 is unaffected by the processes that form the active layer 310 or 410. Furthermore, since the active layer 303 or 403 is formed in the semiconductor wafer 301 or 401 before bonding to the handle wafer 302 or 402, the trap rich layer 312 or 412 is also unaffected by the processes that form the active layer 303 or 403.

[00111] Prior to bonding the handle wafer 302 or 402 and the semiconductor wafer 301 or 401, the bonding layer 311 or 411 may be formed on the back side of the handle wafer 302 or 402 (or on the top side of the semiconductor wafer 301 or 401). Additionally, if an electrical connection is to be made between the semiconductor wafer 301 or 401 and the handle wafer 302 or 402 (e.g. via the metal contact 321), then the back side of the handle wafer 302 or 402 is processed to form metal surfaces coplanar

with the bottom dielectric surface. The handle wafer 302 or 402 is then bonded to the semiconductor wafer 301 or 401 at 811. If an electrical connection is to be made between the semiconductor wafer 301 or 401 and the handle wafer 302 or 402, then bond may be metal-to-metal, as well as dielectric-to-dielectric.

[00112] At 812, the second handle wafer may be removed from the top side of the handle wafer 302 or 402. However, if it is desired to have back side electrical connections (e.g. solder balls, bumps, pillars, etc.) for the structure 300 or 400, then the second handle wafer may be permanently left in place and an underlying portion of the insulator layer 305 or 405 may be removed or thinned (at 813).

[00113] The process 800 may optionally repeat 805-812 to stack additional active layers onto the structure 300 or 400. Each additional active layer may have a trap rich layer between it and the preceding underlying active layer. Additionally, active layers between two other active layers may have the metal contact 321 or the TSV connection 421 to electrically connect to at least one of the two other active layers.

[00114] At 814, patterned contact and metallization are formed for any top or back side connections (e.g. top or bottom electrodes and contacts, etc., as desired). In some embodiments, material layers may also be optionally etched from the exposed top or back side surface through one of the active layers 403 or 410 to the other active layer 410 or 403; thereby exposing metal (e.g. metal sidewalls and/or shelves) in the metal interconnect layer 407 or 416 through a deep hole or trench. The hole or trench may be filled with metal to form the TSV connection 421 to interconnect the active layers 403 and 410 together and optionally to provide an electrical connection to the active layers 403 and/or 410 from a source external to the structure 400.

[00115] At 815, various passivation deposition techniques are performed and pad openings are formed, so the overall IC chip can be generally completed with bumps, pillars, or other post-processing metallization. The process 800 then ends at 816.

[00116] Some embodiments of the present invention described above exhibit an advantageous aspect in that the efficacy of the trap rich layer 214, 312, 412, 511 or 606 is generally not mitigated by further semiconductor processing. As described above, in specific embodiments of the present invention the trap rich layer 214, 312, 412, 511 or 606 is formed on the top surface of the semiconductor wafer 202, 301, 401, 501 or 601 or is provided by the handle wafer 201, 302, 402, 502 or 602 after the semiconductor wafer 202, 301, 401, 501 or 601 has undergone active layer processing. By introducing the trap rich layer 214, 312, 412, 511 or 606 after active layer processing is complete,

the efficacy of the trap rich layer 214, 312, 412, 511 or 606 is preserved to a greater degree. Although bonding processes will sometimes require increased temperatures, these processes typically only require temperatures of 200.degree. C. to 400.degree. C. which will have a much more benign effect on the number of traps that are present in the trap rich layer 214, 312, 412, 511 or 606.

[00117] Some embodiments of the present invention described above exhibit an advantageous aspect in that the trap rich layer 214, 312, 412, 511 or 606 does not interfere with the production and composition of the insulator layer 204, 304, 313, 404, 413, 504 or 604 and the active layer 203, 303, 310, 403, 410, 503 or 603. In the prior art approaches (e.g. FIG. 1), the trap rich layer (e.g. in region 110) is formed below the insulator layer 102 and the insulator layer 102 is then grown or deposited on top of the trap rich layer in region 110. The uniformity of the insulator layer is of critical importance for the performance of the active devices in the active layer of the overall structure. Also, the uniformity of the insulator layer will affect the flatness of the surface of the overall structure if it is used in a layer transferred structure, and the flatness of the surface of the overall structure is important for wafer bonding. Due to the tight constraints placed on the insulator layer, the trap rich layer must also be extremely planar or other significant manufacturing processes must be employed to correct for irregularities in the insulator layer as it is formed over the trap rich layer. In addition, pin holes in the insulator layer can be disastrous in terms of their effect on the performance of devices in the active layer. The introduction of the trap rich layer at a later stage eliminates both of these concerns. First, the uniformity of the bonding layer has a much smaller effect on the performance of the circuitry in the active layer as compared to the uniformity of the insulator layer so the manufacturing process used with relation to these two layers can be significantly relaxed as compared to the prior art. In addition, if the trap rich layer causes pin holes in any insulating layer that is part of the bonding layer, they will not affect the circuit because the top surface of the semiconductor wafer is also generally covered in an insulator that will shield the circuitry located therein.

[00118] In some embodiments of the present invention, variations on the process 700 or 800 can be used to produce structures having multiple trap rich layers. Process flows used to produce a structure with multiple trap rich layers can be very similar to those described above. In some embodiments of the present invention, the process 700 or 800 can begin with the provisioning of a semiconductor wafer having a trap rich

layer below the insulator layer 204, 304, 404 or 604. As a result, the final layer transferred structure 200, 300, 400 or 600 will have a top side (or intermediate) trap rich layer 214, 312, 412 or 606 and a back side trap rich layer (not shown).

[00119] FIGS. 9-11 illustrate embodiments in which trap rich layers (TRLs) are combined with through-semiconductor-vias (TSVs) in a layer transfer structure. The semiconductor material may be any appropriate material, such as silicon, germanium, etc. Some portions of the semiconductors commonly contain free electronic carriers (holes and electrons) that can form a parasitic coupling path when influenced by a nearby electric field. The TRLs generally trap free carriers in the semiconductor material that would otherwise respond to an electric field from energized devices (active or passive). In general, the TSVs are enhanced with TRLs by placing a conformal layer of trap rich material on a semiconductor wafer containing TSVs after TSV etching but before TSV isolation deposition and conductive material fill. This technique may be used with almost any semiconducting substrate containing free carriers.

[00120] FIG. 9 shows a portion of a semiconductor substrate (a TRL-enhanced TSV wafer or "interposer") 900 with TSVs 901 that may be used with an embodiment of the present invention. The TSVs 901 (e.g. metal, doped polysilicon, etc.) are formed within TSV holes 905 that extend from a top surface 902 of the substrate 900 into the interior thereof. The TSVs 901 are surrounded by a trap rich layer 903. (Although the trap rich layer 903 is shown formed on the entire sidewalls and the bottom of the TSV holes 905, in some embodiments, the trap rich layer 903 extends only partially down the sidewalls and/or does not cover the bottom of the TSV holes 905.) In some embodiments, an isolation material 904 separates the TSVs 901 from the trap rich layer 903. In some embodiments, the TSVs 901 may be in direct contact with the trap rich layer 903. An additional oxide layer (not shown) may be deposited over the structure if appropriate for the particular embodiment.

[00121] FIG. 10 shows a portion of a sixth IC chip 1000 in accordance with an embodiment of the present invention. The IC chip 1000 generally includes the semiconductor substrate 900 (inverted) and a semiconductor wafer 1001. The semiconductor wafer 1001 generally includes an active layer 1002, an insulator (e.g. an oxide or other dielectric) layer 1003 and a substrate layer 1004. (Alternatively, the wafer 1001 is an insulating wafer and/or includes an IPD circuit layer, as mentioned above.) The active layer 1002 generally includes an active device layer 1005 and a metallization or metal interconnect layer 1006. The active layer 1002 thus also generally

includes signal processing circuitry, such as one or more active devices (e.g. a transistor 1007) in the active device layer 1005 and metal wiring 1008 and vias 1009 in the metal interconnect layer 1006. The top surface 902 of the inverted substrate 900 is bonded to a top surface 1010 of the semiconductor wafer 1001 by wafer bonding or layer transfer techniques, e.g. as described herein. The IC chip 1000 can thus be referred to as a layer transfer structure. Additionally, the TSVs 901 are in electrical contact with the metal wiring 1008 and vias 1009.

[00122] FIG. 11 shows a portion of a seventh IC chip 1100 in accordance with an embodiment of the present invention. The IC chip 1100 generally includes the semiconductor substrate 900 (inverted and thinned), the semiconductor wafer 1001 and a second semiconductor wafer 1101 (inverted and thinned). The second semiconductor wafer 1101 generally includes an active layer 1102, an insulator (e.g. an oxide or other dielectric) layer 1103. The active layer 1102 generally includes an active device layer 1104 and a metallization or metal interconnect layer 1105. The active layer 1102 thus also generally includes signal processing circuitry, such as one or more active devices (e.g. a transistor 1106) in the active device layer 1104 and metal wiring 1107 and vias 1108 in the metal interconnect layer 1105. A bottom exposed surface or edge 1109 of the inverted substrate 900 is bonded to a top surface or edge 1110 of the inverted second semiconductor wafer 1101 by wafer bonding or layer transfer techniques, e.g. as described herein. The IC chip 1100 can thus be referred to as a layer transfer structure.

[00123] The TSVs 901 are in electrical contact with the metal wiring 1107 and vias 1108, thereby providing an electrically conductive path between the metal wiring 1107 and vias 1108 of the inverted second semiconductor wafer 1101 and the metal wiring 1008 and vias 1009 of the first semiconductor wafer 1001. In this manner, a TRL-enhanced TSV wafer (e.g. 900) can be used as an interposer between any two circuit layers (e.g. CMOS, integrated passive components, etc.). Using TRL-enhanced TSV wafers to connect any number of semiconductor wafers can help to ensure that the semiconductor materials within the semiconductor wafers are isolated from the various active and passive devices by TRLs, thereby providing high isolation from non-linear substrate mechanisms.

[00124] The inverted second semiconductor wafer 1101 is not shown as having an underlying substrate layer similar to the substrate layer 1004 of the first semiconductor wafer 1001, since the illustrated embodiment assumes that such a substrate layer has been removed by back side etching (or other appropriate removal

techniques) after bonding the inverted second semiconductor wafer 1101 to the IC chip 1000. Thus, a back side 1111 of the insulator layer 1103 is exposed. Once the underlying substrate is removed, the first semiconductor wafer 1001 provides the required stabilizing force necessary to protect and preserve the electrical characteristics of devices or structures in the active layer 1102. Additionally, further metallization or interconnect wiring (not shown) may extend through the insulator layer 1103 and be deposited on the back side 1111 of the insulator layer 1103 for back side electrical connections to the components in the active layer 1102.

[00125] Additionally, the inverted substrate 900 (including a portion of the TSVs 901) is shown as having been thinned by back side etching (or other appropriate removal techniques) prior to bonding the inverted second semiconductor wafer 1101 to the IC chip 1000. The thinning of the inverted substrate 900 is generally done to expose the TSVs 901 and make them of a desired length. Furthermore, the inverted substrate 900 is shown as having an additional trap rich layer 1112 formed after the thinning and prior to bonding the inverted second semiconductor wafer 1101 to the IC chip 1000.

[00126] FIG. 12 shows a flowchart for a process 1200 for fabricating at least part of an integrated circuit chip (e.g. similar to structures 900, 1000 and/or 1100, FIGS. 9, 10 and/or 11), according to some embodiments of the present invention. It is understood, however, that the specific process 1200 is shown for illustrative purposes only and that other embodiments (in addition to specifically mentioned alternative embodiments) may involve other processes or multiple processes with other individual steps or a different order or combination of steps and still be within the scope of the present invention.

[00127] Upon starting (at 1201), preparation of the semiconductor substrate 900 (FIG. 9) begins. (For this embodiment, preparation of the semiconductor wafers 1001 and 1101 is assumed to occur separately and may be done in parallel with preparation of the semiconductor substrate 900.) At 1202, the holes for the TSVs 901 (including sufficient space for the TRL 903 and the isolation material 904) are patterned and etched into the semiconductor substrate 900.

[00128] At 1203, the TRL 903 is formed, e.g. by deposition of a conformal layer of TRL material onto the exposed surfaces of the semiconductor substrate 900, including on the walls and bottom of the TSV holes formed at 1202. In other embodiments, the TRL 903 includes the entire semiconductor material of the semiconductor substrate 900 and is formed by irradiating the semiconductor substrate

900 before or after the formation of the TSV holes at 1202. In still other embodiments, the TRL 903 is formed by ion implantation or by damaging the exposed surfaces of the semiconductor substrate 900. Alternatively, the TRL 903 may be formed by any other appropriate technique, including, but not limited to, those techniques described herein.

[00129] At 1204, the isolation material 904 is placed on the exposed surfaces of the TRL 903, e.g. by deposition of an appropriate material. At 1205, the metal material (or other conductive material) for the TSVs is 901 is filled into the remaining space of the TSV holes. Some of the metal material will accrue on areas outside the TSV holes, so the metal material is also etched back to remove this excess material and to make the metal material in the TSVs 901 generally coplanar with the rest of the top surface 902 of the substrate 900. Additionally, some or all of the isolation material 904 outside of the TSV holes may be etched back. The portions of the TRL 903 outside of the TSV holes, however, should not be significantly etched back.

[00130] An oxide or other suitable material may then be deposited on the top surface 902, if it is desired for the particular application. With or without the oxide, the top surface 902 is planarized (at 1206), e.g. by chemical-mechanical polishing (CMP) or other suitable technique.

[00131] At this point, the procedure 1200 has generally produced the semiconductor substrate 900 of FIG. 9. Additionally, preparation of the semiconductor wafer 1001 (FIG. 10) has occurred separately from that of the semiconductor substrate 900 to produce the semiconductor wafer 1001 with exposed conductors at the top surface 1010 thereof in a pattern that matches the pattern of the exposed TSVs 901 at the top surface 902 of the inverted semiconductor substrate 900. The top surface 902 of the semiconductor substrate 900 is then aligned with and bonded to (at 1207) the top surface 1010 of the semiconductor wafer 1001 to form the IC chip 1000.

[00132] At 1208, the back side of the inverted semiconductor substrate 900 is thinned or removed. Additionally, etching may be performed (at 1209) to expose the TSVs 901, e.g. down to the bottom surface 1109 of the inverted semiconductor substrate 900. (If the TRL 903 does not cover the entire sidewalls and/or bottom of the TSV holes 905, as mentioned above, then the etching at 1209 may generally be done at least down to a point at which the TRL 903 sufficiently surrounds the TSVs 901.) At 1210, the additional TRL 1112 is formed in or on the exposed portions of the semiconductor material at the bottom surface 1109 of the semiconductor substrate 900. The semiconductor material of the semiconductor substrate 900 is thereby generally

surrounded by the TRLs 903 and 1112, and the TSVs 901 are surrounded by the trap rich layer 903, except at top and bottom ends thereof.

[00133] Alternatively, instead of bonding the semiconductor substrate 900 to an active wafer (e.g. the semiconductor wafer 1001 as shown in FIG. 10), in some embodiments, after the semiconductor substrate 900 has been formed at 1206, the top surface 902 of the semiconductor substrate 900 may be bonded to a temporary substrate (not shown). The back side of the semiconductor substrate 900 may then be thinned or removed (e.g. at 1208) and the TSVs 901 may be exposed (e.g. at 1209). The additional TRL 1112 may also be formed (e.g. at 1210). The resulting structure is generally a different TRL-enhanced TSV wafer that may then be layer transferred to another semiconductor wafer.

[00134] In other embodiments, the wafer to which the TSV-containing semiconductor substrate 900 is bonded may be composed of an insulating material. For example, the wafer may be an IPD (as mentioned above) on quartz or sapphire. Or the wafer may be a silicon on sapphire wafer. Or the wafer may be composed of high thermal conductivity material for thermal behavior improvement. Other options are also possible.

[00135] Preparation of the second semiconductor wafer 1101 (FIG. 11) has occurred separately from that of the semiconductor substrate 900 and the first semiconductor wafer 1001 to produce the second semiconductor wafer 1101 with exposed conductors at the top surface 1110 (inverted) thereof in a pattern that matches the pattern of the exposed TSVs 901 at the bottom surface 1109 of the inverted semiconductor substrate 900. The top surface 1110 of the inverted second semiconductor wafer 1101 is then aligned with and bonded to (at 1211) the bottom surface 1109 of the inverted semiconductor substrate 900. At 1212, the underlying portion of the second semiconductor wafer 1101 is thinned or removed down to the insulator layer 1103 to form the IC chip 1100 as shown in FIG. 11.

[00136] At 1213, various passivation deposition techniques are performed and pad openings are formed on the back side 1111, so the overall IC chip 1100 can be generally completed with bumps, pillars, or other post-processing metallization. The process 1200 then ends at 1214. As an alternative, however, various conductors may be exposed on the back side 1111, so that another a TRL-enhanced TSV wafer (e.g. similar to the semiconductor substrate 900, but likely with a different exposed conductor pattern) can be bonded to the back side 1111, followed by bonding another

semiconductor wafer (e.g. similar to 1001 or 1101) thereto, as if repeating 1207 through 1212. Any appropriate number of semiconductor wafers (each separated by TRL-enhanced TSV wafers) may thus be stacked in this manner before proceeding to 1213.

[00137] In some alternative embodiments, the structure indicated by the reference number 1101 (FIG. 11) represents one or more layers of deposited materials of a circuit layer, instead of a second semiconductor wafer. In this case, after the additional TRL 1112 is formed at 1210, various layers of materials may be deposited and shaped to form an active device layer, an IPD layer, a circuit layer having mixed active and passive components, metal interconnect layers, etc. These embodiments thus provide a two-wafer (the first semiconductor wafer 1001 and the semiconductor substrate 900 with a deposited circuit layer) solution for forming an IC chip having two circuit layers, instead of a three-wafer (1001, 900 and 1101) solution. In some embodiments, the layers of materials may be similar to that described below with reference to FIG. 14.

[00138] Some embodiments of the present invention can be described with reference to FIG. 13. FIG. 13 illustrates a structure (e.g. part of an IC chip) 1300 having multiple layers of signal processing circuitry. The structure 1300 generally includes a first wafer 1301 and a second wafer 1302 bonded together by wafer bonding or layer transfer techniques. The second wafer 1302 may be non-inverted (as shown) or inverted.

[00139] The first wafer 1301 generally includes an active layer 1303, an insulator (e.g. an oxide or other dielectric) layer 1304 and a substrate layer 1305. The first wafer 1301 is optionally capped by another insulator layer (not shown). The active layer 1303 is a circuit layer that generally includes an active device layer 1306 and a metallization or metal interconnect layer 1307. The active layer 1303 thus also generally includes signal processing circuitry or circuit components, such as one or more active devices (e.g. a transistor 1308) in the active device layer 1306 and metal wiring 1309 in the metal interconnect layer 1307. In alternative embodiments, the active layer 1303 may be replaced with a circuit layer having IPDs or a mix of active and passive devices or circuit components, as described above.

[00140] The second wafer 1302 generally includes an active layer 1310, a bonding layer 1311, trap rich layers 1312, 1313 and 1314, a semiconductor substrate layer 1315 and underlying and overlying insulator (e.g. an oxide or other dielectric) layers 1316 and 1317. The active layer 1310 generally includes an active device layer 1318 and a metallization or metal interconnect layer 1319. The active layer 1310 thus also generally includes signal processing circuitry or circuit components, such as one or

more active devices (e.g. a transistor 1320) in the active device layer 1318 and metal wiring 1321 in the metal interconnect layer 1319. Alternatively, the active layer 1310 may be replaced with a circuit layer having IPDs or a mix of active and passive devices or circuit components, as described above.

[00141] The trap rich layers 1312 and 1313 generally cover the top and bottom, respectively, of the semiconductor substrate layer 1315 to prevent or mitigate the parasitic surface conduction effects within the semiconductor substrate layer 1315 that may be caused by the active layers 1303 and 1310, as described herein. Additionally, the trap rich layers 1312 and 1313 may have any one or more of the characteristics and may be formed by any of the techniques described herein for other trap rich layers, depending on the requirements of a desired configuration or implementation.

[00142] The second wafer 1302 also generally includes at least one TSV 1322 that extends from a bottom surface 1323 of the second wafer 1302 through the intervening layers (1311, 1313, 1315, 1312 and 1316) and into the active device layer 1318. Optionally, the TSV 1322 may extend into the metal interconnect layer 1319 or even to the top surface of the overlying insulator layer 1317, as indicated by the dashed lines. The TSV 1322 may thus electrically connect the metal interconnect layer 1319 or active device layer 1318 in the second wafer 1302 to the metal interconnect layer 1307 in the first wafer 1301. Additionally, if a third wafer (not shown) is stacked onto the structure 1300 and the TSV 1322 is exposed at the top surface of the insulator layer 1317, then the TSV 1322 may further connect to exposed electrical conductors at the bonding surface of the third wafer.

[00143] Since the TSV 1322 extends through the semiconductor substrate layer 1315, the trap rich layer 1314 is provided around the TSV 1322, thereby separating or isolating the conductive material of the TSV 1322 from the semiconductor material of the semiconductor substrate layer 1315. The trap rich layer 1314, thus, prevents or mitigates the parasitic surface conduction effects within the semiconductor substrate layer 1315 that may be caused by the TSV 1322. Additionally, although the trap rich layer 1314 is shown extending only from the bottom of the upper trap rich layer 1312 to the top of the lower trap rich layer 1313, it is understood that the trap rich layer 1314 may extend beyond these boundaries, depending on the requirements of the design, the fabrication processes used and other factors. In some embodiments, for example, the trap rich layer 1314 may extend throughout the entire length of the TSV 1322 or stop at any appropriate intermediate point within that length.

[00144] Since the second wafer 1302 includes the TSV 1322 surrounded at least partially by the trap rich layer 1314, the second wafer 1302 may be considered a variation on the semiconductor substrate 900 of FIG. 9. In some embodiments, therefore, the formation of the TSV 1322 and trap rich layer 1314 may occur as described from 1202 to 1205 in the process 1200 (FIG. 12), and the active layer 1310 and the trap rich layers 1312 and 1313 may be formed before or after the formation of the TSV 1322 and trap rich layer 1314, as appropriate. In other embodiments, the TSV 1322 may be formed by bottom side processing after formation of the active layer 1310 (and optionally after bonding a handle wafer to the top of the second wafer 1302 and/or optionally after thinning of the semiconductor substrate layer 1315).

[00145] In some embodiments, formation of the lower trap rich layer 1313, since it is near the bottom side of the second wafer 1302, may preferably (but not necessarily) be done by bottom side processing (before or after forming the bonding layer 1311, as appropriate). Additionally, if the TSV 1322 is also formed by bottom side processing, then the trap rich layer 1313 may be formed before or after forming the TSV 1322, as appropriate. Furthermore, the semiconductor substrate layer 1315 may be thinned, if necessary or desirable, prior to formation of the trap rich layer 1313.

[00146] In some embodiments, the upper trap rich layer 1312 is formed within the semiconductor substrate layer 1315 of the second wafer 1302 prior to the formation of the active layer 1310. In this case, however, the subsequent formation of the structures in the active layer 1310 may degrade the trap rich layer 1312, as mentioned above. In other embodiments, the trap rich layer 1312 is formed after the formation of the active layer 1310. For example, the trap rich layer 1312 may be high resistivity material deposited onto a bottom surface of the insulator layer 1316, e.g. after a handle wafer (not shown) is bonded to the top of the second wafer 1302 and the underlying semiconductor substrate is removed or thinned to expose the insulator layer 1316. Alternatively, the underlying semiconductor substrate is not fully removed, and the trap rich layer 1312 is formed in at least part of the remaining portion of the underlying semiconductor substrate, e.g. by implantation of high energy particles to create a damaged area in the underlying semiconductor substrate, as mentioned above. Additionally, if the formation of the upper trap rich layer 1312 requires removal of all or a substantial portion of a preexisting substrate, then additional semiconductor material may be deposited onto the bottom of the second wafer 1302 if needed to form the semiconductor substrate layer 1315 prior to formation of the lower trap rich layer 1313.

[00147] If a handle wafer is used with the processing of the second wafer 1302, it may be removed either before or after the second wafer 1302 is bonded to the first wafer 1301. In variations of these embodiments, the handle wafer is optional and/or the overlying insulator layer 1317 originates as part of the bonding layer used to bond the handle wafer to the second wafer 1302. In other alternatives, the handle wafer remains attached to the second wafer 1302 immediately after bonding the first wafer 301 and the second wafer 1302, and then either the handle wafer or the substrate layer 1305 is removed or thinned.

[00148] In other alternative embodiments, the trap rich layers 1312 and/or 1313 are added to the second wafer 1302 by one or more layer transfer processes after the formation of the active layer 1310. (See the dual layer transfer technique described with reference to FIG. 5.) Thus, the trap rich layers 1312 and/or 1313 may be formed as a layer in (or as the entire extent of) one or more other handle wafers. The other handle wafer(s) is then bonded to the second wafer 1302, e.g. with the insulator layer 1316 (formed on either the other handle wafer or the second wafer 1302) serving as a bonding layer. Then any unnecessary thickness of the other handle wafer(s) is removed, leaving the trap rich layers 1312 and/or 1313 as part of the second wafer 1302.

[00149] In each case, the trap rich layers 1312 and 1313, as part of the second wafer 1302, are added to the first wafer 1301 after the formation of the active layer 1303 in the first wafer 1301. Therefore, the formation of the active layer 1303 generally does not affect the trap rich layers 1312 and 1313.

[00150] In other embodiments, the lower trap rich layer 1313 is added to the first wafer 1301, instead of to the second wafer 1302 (after the active layer 1303 is formed, but before the first wafer 1301 and the second wafer 1302 are bonded together). Additionally, the active layer 1310 may be formed before the bonding, so the formation of neither active layer 1303 nor 1310 affects the lower trap rich layer 1313. Alternatively, both trap rich layers 1312 and 1313 and the semiconductor substrate layer 1315 are added to the first wafer 1301, instead of to the second wafer 1302.

[00151] The bonding layer 1311 can generally be a combination of one or more insulator layers and passivation layers. The bonding layer 1311 may also be a material used to bond the bottom exposed surface 1323 of the second wafer 1302 to a top exposed surface 1324 of the first wafer 1301 during the wafer bonding or layer transfer procedure. In some embodiments, the bonding layer 1311 comprises an etch-stop layer used when removing material (e.g. part the semiconductor substrate layer 1315) from

the second wafer 1302. In another alternative, the bonding layer 1311 is added to the first wafer 1301, instead of to the second wafer 1302, before wafer bonding or layer transfer.

[00152] Some embodiments of the present invention can be described with reference to FIG. 14. FIG. 14 illustrates a structure (e.g. part of an IC chip) 1400 having multiple layers of signal processing circuitry. The structure 1400 generally includes an inverted wafer 1401 with layers of material 1402 deposited onto a bottom side (inverted) 1403 thereof. The inverted wafer 1401 is formed in some respects similarly to the second wafer 1302 (FIG. 13) and the semiconductor substrate 900 (FIG. 9) as discussed above.

[00153] The inverted wafer 1401 generally includes an active layer 1404, trap rich layers 1405, 1406 and 1407, a semiconductor substrate layer 1408, underlying and overlying insulator (e.g. an oxide or other dielectric) layers 1409 and 1410 and at least one TSV 1411. The active layer 1404 generally includes an active device layer 1412 and a metallization or metal interconnect layer 1413. The active layer 1404 thus also generally includes signal processing circuitry or circuit components, such as one or more active devices (e.g. a transistor 1414) in the active device layer 1412 and metal wiring 1415 in the metal interconnect layer 1413. Alternatively, the active layer 1404 may be replaced with a circuit layer having IPDs or a mix of active and passive devices or circuit components, as described above.

[00154] The deposited material layers 1402 generally include insulator layers 1416 and 1417 and a circuit layer 1418. An interconnect 1419 through an opening in the insulator layer 1416 electrically connects the circuit layer 1418 to the TSV 1411.

[00155] After formation of the inverted wafer 1401, the insulator layer 1416 is placed on the side 1403. The insulator layer 1416, for example, may be thick SiO_2 to minimize capacitive parasitic coupling paths, AlN for surface acoustic wave (SAW) filter applications or other appropriate insulating materials.

[00156] The circuit layer 1418 is fabricated on top of the insulator layer 1416 after the interconnect 1419 is formed through the insulator layer 1416. The circuit layer 1418 is shown in a highly simplified manner because it may represent a wide variety of one or more layers of active devices, passive devices, metal interconnects and combinations thereof. For example, if the circuit layer 1418 is a passive device layer, it may be as simple as a single layer of thick metal for a high-Q inductor (e.g. a thick

copper layer) or as complex as a full IPD layer (which may feature resistors, capacitors, inductors, filters, etc.).

[00157] After formation of the circuit layer 1418, the insulator layer 1417 may be formed thereon. Additionally, various passivation deposition techniques may be performed and pad openings formed, so the overall IC chip 1400 can be generally completed with bumps, pillars, or other post-processing metallization. These embodiments thus provide a single-wafer solution for forming an IC chip having two circuit layers, instead of a three-wafer (1001, 900 and 1101) solution.

[00158] The trap rich layers 1405 and 1406 generally cover the top and bottom, respectively, of the semiconductor substrate layer 1408 to prevent or mitigate the parasitic surface conduction effects within the semiconductor substrate layer 1408 that may be caused by the circuit layers 1404 and 1418, as described herein. Additionally, the trap rich layers 1405 and 1406 may have any one or more of the characteristics and may be formed by any of the techniques described herein for other trap rich layers, depending on the requirements of a desired configuration or implementation.

[00159] The TSV 1411 generally extends from the bottom side (inverted) 1403 of the inverted wafer 1401 through the intervening layers (1406, 1408, 1405 and 1409) and into the active device layer 1412. Optionally, the TSV 1411 may extend into the metal interconnect layer 1413 or even to the top surface of the overlying insulator layer 1410, as indicated by the dashed lines. The TSV 1411 may thus electrically connect the metal interconnect layer 1413 or active device layer 1412 in the inverted wafer 1401 to the interconnect 1419 in the deposited material layers 1402. Additionally, if a another wafer (not shown) is stacked onto the structure 1400 and the TSV 1411 is exposed at the top surface (inverted) of the insulator layer 1410, then the TSV 1411 may further connect to exposed electrical conductors at the bonding surface of the other wafer.

[00160] Since the TSV 1411 extends through the semiconductor substrate layer 1408, the trap rich layer 1407 is provided around the TSV 1411, thereby separating or isolating the conductive material of the TSV 1411 from the semiconductor material of the semiconductor substrate layer 1408. The trap rich layer 1407, thus, prevents or mitigates the parasitic surface conduction effects within the semiconductor substrate layer 1408 that may be caused by the TSV 1411. Additionally, although the trap rich layer 1407 is shown extending only from the bottom (inverted) of the trap rich layer 1405 to the top (inverted) of the trap rich layer 1406, it is understood that the trap rich layer 1407 may extend beyond these boundaries, depending on the requirements of the

design, the fabrication processes used and other factors. In some embodiments, for example, the trap rich layer 1407 may extend throughout the entire length of the TSV 1411 or stop at any appropriate intermediate point within that length.

[00161] Since the inverted wafer 1401 includes the TSV 1411 surrounded at least partially by the trap rich layer 1407, the inverted wafer 1401 may be considered a variation on the semiconductor substrate 900 of FIG. 9. In some embodiments, therefore, the formation of the TSV 1411 and trap rich layer 1407 may occur as described from 1202 to 1205 in the process 1200 (FIG. 12) by bottom side processing after formation of the active layer 1404 (and optionally after bonding a handle wafer to the top of the inverted wafer 1401 and/or optionally after thinning of the semiconductor substrate layer 1408).

[00162] In some embodiments, formation of the trap rich layer 1406, since it is near the bottom side of the inverted wafer 1401, may preferably (but not necessarily) be done by bottom side processing (before or after forming the TSV 1411, as appropriate). Furthermore, the semiconductor substrate layer 1408 may be thinned, if necessary or desirable, prior to formation of the trap rich layer 1406.

[00163] In some embodiments, the trap rich layer 1405 is formed within the semiconductor substrate layer 1408 prior to the formation of the active layer 1404. In this case, however, the subsequent formation of the structures in the active layer 1404 may degrade the trap rich layer 1405, as mentioned above. In other embodiments, the trap rich layer 1405 is formed after the formation of the active layer 1404. For example, the trap rich layer 1405 may be high resistivity material deposited onto a bottom (inverted) surface of the insulator layer 1409, e.g. after a handle wafer (not shown) is bonded to the top of the inverted wafer 1401 and the underlying semiconductor substrate is removed or thinned to expose the insulator layer 1409. Alternatively, the underlying semiconductor substrate is not fully removed, and the trap rich layer 1405 is formed in at least part of the remaining portion of the underlying semiconductor substrate, e.g. by implantation of high energy particles to create a damaged area in the underlying semiconductor substrate, as mentioned above. Additionally, if the formation of the trap rich layer 1405 requires removal of all or a substantial portion of a preexisting substrate, then additional semiconductor material may be deposited onto the bottom of the inverted wafer 1401 if needed to form the semiconductor substrate layer 1408 prior to formation of the other trap rich layer 1406.

[00164] If a handle wafer is used with the processing of the inverted wafer 1401, it may be removed, if desired, e.g. after formation of the deposited material layers 1402. In variations of these embodiments, the handle wafer is optional and/or the overlying insulator layer 1417 originates as part of the bonding layer used to bond the handle wafer to the inverted wafer 1401.

[00165] In other alternative embodiments, the trap rich layers 1405 and/or 1406 are added to the inverted wafer 1401 by one or more layer transfer processes after the formation of the active layer 1404. (See the dual layer transfer technique described with reference to FIG. 5.) Thus, the trap rich layers 1405 and/or 1406 may be formed as a layer in (or as the entire extent of) one or more other handle wafers. The other handle wafer(s) is then bonded to the inverted wafer 1401, e.g. with the insulator layer 1409 (formed on either the other handle wafer or the inverted wafer 1401) serving as a bonding layer. Then any unnecessary thickness of the other handle wafer(s) is removed, leaving the trap rich layers 1405 and/or 1406 as part of the inverted wafer 1401.

[00166] Some embodiments of the present invention can be described with reference to FIG. 15. FIG. 15 illustrates a simplified embodiment of a semiconductor structure 1500 within a portion of an IC chip. The elements of the semiconductor structure 1500 are not necessarily to scale and may be shown in an idealized form, so some elements may be exaggerated and/or simplified for ease of illustration and description. Additionally, some elements that may be expected to be included in such a semiconductor structure may have been omitted or combined with other elements for ease of illustration and description.

[00167] Portions of the structure 1500 may be formed by wafer bonding or layer transfer techniques, as described herein. Similar to the structure 200 (FIG. 2) described above, the structure 1500 generally comprises a handle wafer 1501 bonded to a semiconductor wafer 1502. The structure 1500 can thus be referred to as a layer transfer structure. Additionally, this embodiment may have many, if not all, of the benefits and advantageous aspects mentioned below for the configuration described with reference to FIG. 2. However, those elements in the structure 1500 that are generally similar to elements in the structure 200 have been inverted in this embodiment. Also, an additional device layer 1503 is formed (by monolithic or layer-transfer processes described below) on the back or bottom side (inverted) of the semiconductor wafer 1502. The additional layer 1503 may add additional devices as well as additional types of devices (e.g.

additional CMOS devices or acoustic devices, acoustic filters and/or other MEMS devices) to the overall structure 1500 when compared with the structure 200.

[00168] The semiconductor wafer 1502 generally comprises an active/device layer 1504 having a bottom side in contact with an insulator layer 1505. The semiconductor wafer 1502 is optionally capped by another insulator layer (not shown). In some embodiments, the semiconductor wafer 1502 may be a silicon on sapphire wafer, a gallium arsenide wafer, an SOI wafer, etc. The handle wafer 1501 generally comprises a handle substrate layer 1506, a trap rich layer 1507, and a bonding layer 1508.

[00169] The additional layer 1503 generally comprises a device layer 1509, an interconnect layer 1510, and an insulator layer 1511. The device layer 1509 is illustrated as having a series acoustic filter 1512 and a shunt acoustic filter 1513. However, in some embodiments, the device layer 1509 may include only one of these filters 1512 or 1513. Also, alternatively or in combination the device layer 1509 may include any other appropriate types of components, e.g. active devices, passive devices, MEMS devices, etc. The interconnect layer 1510 is generally formed with layers of conductive materials 1514 (e.g. metals) and interlayer electrical connections (e.g. vias and TSVs 1515). The TSVs 1515, for example, may provide electrical connections between elements in the additional layer 1503 and elements in the active layer 1504.

[00170] The active layer 1504 may be a circuit layer that generally includes an active device layer 1516 and a metallization or metal interconnect layer 1517, which generally further include a combination of dopants, dielectrics, polysilicon, metal wiring, passivation, and other layers, materials and/or components that are present after circuitry has been formed therein. The circuitry may include metal wiring 1518 (e.g. in the metal interconnect layer 1517); passive devices such as resistors, capacitors, and inductors; and active devices such as a transistor 1519 (e.g. in the active device layer 1516). In other embodiments, the active layer 1504 may be replaced with a circuit layer having Integrated Passive Devices (IPDs, a.k.a. Integrated Passive Components, IPCs) or a mix of active and passive devices. Such IPD circuit layers generally include functional blocks such as impedance matching circuits, harmonic filters, couplers and baluns and power combiners/dividers, etc. IPD circuit layers are generally fabricated using standard wafer fabrication technologies, such as thin film and photolithography processing, among others. IPD wafers can be designed as flip chip mountable or wire bondable components. Additionally, the substrates for IPD wafers usually are thin film

substrates like silicon, alumina or glass. Furthermore, IPD wafers may be formed on quartz with no semiconductor material, so the wafer 1502 may be an insulating wafer. Therefore, although the description herein refers to various semiconductor wafers (e.g. 1502) and active layers (e.g. 1504), other types of wafers and circuit layers (such as insulating wafers and IPD circuit layers, etc.) may be used in place thereof, where appropriate.

[00171] The bonding layer 1508 (e.g. similar to the bonding layer 206 described above) can generally be a combination of one or more insulator layers and passivation layers used to isolate and protect the active layer 1504. The bonding layer 1508 may be a material used to bond a bottom (inverted) exposed surface 1520 of the handle wafer 1501 to a top (inverted) surface 1521 of the semiconductor wafer 1502 during the wafer bonding or layer transfer procedure. In an alternative embodiment, the bonding layer 1508 is added to the semiconductor wafer 1502, instead of to the handle wafer 1501, before wafer bonding or layer transfer. In some embodiments, the bonding layer 1508 is formed by chemical vapor deposition (CVD) or thermal oxidation to create an oxide layer. Depending on the embodiment, as described herein, the bonding layer 1508 may be formed before or after a trap rich layer 1507. If the bonding layer 1508 is formed before the trap rich layer 1507, the benefit of the trap rich layer 1507 may be slightly eroded due to the heat associated with forming the bonding layer 1508. However, a single CVD or thermal oxidation process will not reduce trap density as much as will full active device processing.

[00172] The semiconductor wafer 1502 may be a conventional semiconductor-on-insulator (SOI) wafer (with the insulator layer 1505 formed as a buried oxide or other appropriate insulator or dielectric material) or a conventional bulk semiconductor wafer. Before bonding the handle wafer 1501 to the semiconductor wafer 1502, the structures of the active layer 1504 are formed in and on a substrate of the semiconductor wafer 1502. After bonding, a portion of the original semiconductor substrate (not shown) below the insulator layer 1505 is removed such that a back (inverted) side 1522 of the insulator layer 1505 is exposed. Once the underlying substrate is removed, the handle wafer 1501 provides the required stabilizing force necessary to protect and preserve the electrical characteristics of devices or structures in the active layer 1504. Additionally, further metallization or interconnect wiring (not shown) may extend through the insulator layer 1505 and be deposited on the back side 1522 of the insulator layer 1505 for back side electrical connections between the components in the active

layer 1504 and components in the additional layer 1503. In some embodiments, cavities 1523 may be formed in the back side 1522 of the insulator layer 1505 after the thinning thereof. The cavities 1523 may be aligned with the acoustic filters 1512 and 1513.

[00173] FIG. 16 shows a flowchart for a process 1600 for fabricating at least part of an integrated circuit chip (e.g. similar to structure 1500, FIG. 15), according to some embodiments of the present invention. It is understood, however, that the specific process 1600 is shown for illustrative purposes only and that other embodiments (in addition to specifically mentioned alternative embodiments) may involve other processes or multiple processes with other individual steps or a different order or combination of steps and still be within the scope of the present invention.

[00174] Upon starting (at 1601), the semiconductor wafer 1502 is prepared at 1602. If the semiconductor wafer 1502 is an SOI wafer, then the preparation (at 1602) may simply be to provide a standard SOI wafer. If the semiconductor wafer 1502 is a bulk semiconductor wafer, then the preparation (at 1602) may include creating a buried P+ layer in the bulk semiconductor wafer 1502, e.g. by epitaxial growth or ion implantation methods. Epitaxial methods may involve epitaxially depositing a layer of P+ material on a P- or N- substrate. Then a layer of lightly-doped silicon may be epitaxially deposited to use as an active device layer. This layer may be thick enough so that up-diffusion from the P+ layer does not reach the active device layer 1516 by the end of processing to form the structures in the active layer 1504. Ion implantation methods, on the other hand, may involve performing a high-dose, high-energy ion (e.g. Boron, etc.) implant into the surface of the bulk semiconductor wafer, forming a buried P+ layer deep enough so it will not diffuse up to the active device layer 1516 during processing to form the structures in the active layer 1504.

[00175] At 1603, the active layer 1504 is formed to produce a circuit with a set of active devices in the semiconductor wafer 1502. For an SOI wafer, the active layer 1504 may be manufactured using a standard SOI process. For a bulk semiconductor wafer, the active layer 1504 may be formed with a process that provides an etch stop for a subsequent substrate removal, such as the aforementioned P+ layer formed below the active device layer. Additionally, a chemical mechanical polishing is optionally performed of the top surface of the semiconductor wafer 1502.

[00176] If direct bonding is subsequently to be performed to bond the semiconductor wafer 1502 to the handle wafer 1501, the top surface of the

semiconductor wafer 1502 may be planarized after 1603. On the other hand, if an adhesive bond is to be performed, then planarization may not be necessary.

[00177] Separately from 1602-1603, the handle wafer 1501 is prepared (at 1604). Such preparation may include the formation (at 1605) of the bonding layer 1508 and the formation (at 1606) of the trap rich layer 1507, by any appropriate method or in any appropriate order as described above.

[00178] At 1607, the handle wafer 1501 is bonded to the top surface of the semiconductor wafer 1502. The bonding may be a direct oxide-oxide bond, an adhesive bond, an anodic bond, a low-temperature glass frit bond, a molecular bond, an electrostatic bond, etc., as appropriate for a given situation. Therefore, even though the trap rich layer 1507 may be formed in the handle wafer 1501 at any time before, during or after the formation of the active layer 1504 in the semiconductor wafer 1502, the trap rich layer 1507 is not added to the structure 1500 until after the formation of the active layer 1504.

[00179] At 1608, the combined wafers 1501 and 1502 are inverted. At 1609, the original underlying, or back side, portion (e.g. a semiconductor substrate) of the semiconductor wafer 1502 is substantially removed or thinned. Most of the semiconductor substrate can be removed by back side grinding. A final portion of the semiconductor substrate can be removed by a wet etch, selective chemical mechanical polishing (CMP), a dry etch, etc., leaving at least the active device layer 1516 (or the insulator layer 1505, if it is part of the original semiconductor wafer 1502). For embodiments using a bulk semiconductor wafer, the original underlying substrate is removed to the P+ layer (described above) using a wet chemical etch that is highly selective to P+ material (for example EDP, KOH, or TMAH). The etch can be either chemical or electro-chemical. Additionally, the P+ layer is optionally removed using any combination of grinding, polishing, CMP, dry etch, or non-selective wet etch. The P+ layer will only be a few microns in thickness, so a much better uniformity of a remaining relatively thin (e.g. less than 1 .mu.m) semiconductor film can be achieved than if the semiconductor wafer 1502 was thinned mechanically.

[00180] At 1610, the cavities 1523 are formed in the back side of the semiconductor wafer 1502 (e.g. the thinned insulator layer 1505). Then the cavities 1523 are filled with a material that is selective to the surrounding material, so that a subsequent etch of the fill material will release the acoustic filter 1512 or 1513 or other MEMS device, if needed.

[00181] At 1611, the additional layer 1503 is monolithically formed onto the back side (inverted) of the semiconductor wafer 1502. Thus, the acoustic filter 1512 or 1513, other MEMS devices or other active devices of the device layer 1509 are built up onto the semiconductor wafer 1502. Additionally, the interconnect layer 1510 and the insulator layer 1511 are formed onto the device layer 1509. At an appropriate point, the fill material in the cavities 1523 is removed to release the acoustic filter 1512 or 1513 or other MEMS devices. Also, a passivation dielectric layer(s) is optionally deposited on the additional layer 1503 to reduce effects due to moisture and ionic contamination ingress.

[00182] At 1612, patterned contact and metallization are formed for any top or back side connections (e.g. top or bottom electrodes and contacts, etc., as desired). At 1613, various passivation deposition techniques are performed and pad openings are formed, so the overall IC chip can be generally completed with bumps, pillars, or other post-processing metallization. The process 1600 then ends at 1614.

[00183] FIG. 17 shows a flowchart for an alternative process 1700 for fabricating at least part of an integrated circuit chip (e.g. similar to structure 1500, FIG. 15), according to some embodiments of the present invention. It is understood, however, that the specific process 1700 is shown for illustrative purposes only and that other embodiments (in addition to specifically mentioned alternative embodiments) may involve other processes or multiple processes with other individual steps or a different order or combination of steps and still be within the scope of the present invention.

[00184] Upon starting (at 1701), the semiconductor wafer 1502 is prepared at 1702. If the semiconductor wafer 1502 is an SOI wafer, then the preparation (at 1702) may simply be to provide a standard SOI wafer. If the semiconductor wafer 1502 is a bulk semiconductor wafer, then the preparation (at 1702) may include creating a buried P+ layer in the bulk semiconductor wafer 1502, e.g. by epitaxial growth or ion implantation methods. Epitaxial methods may involve epitaxially depositing a layer of P+ material on a P- or N- substrate. Then a layer of lightly-doped silicon may be epitaxially deposited to use as an active device layer. This layer may be thick enough so that up-diffusion from the P+ layer does not reach the active device layer 1516 by the end of processing to form the structures in the active layer 1504. Ion implantation methods, on the other hand, may involve performing a high-dose, high-energy ion (e.g. Boron, etc.) implant into the surface of the bulk semiconductor wafer, forming a buried

P+ layer deep enough so it will not diffuse up to the active device layer 1516 during processing to form the structures in the active layer 1504.

[00185] At 1703, the active layer 1504 is formed to produce a circuit with a set of active devices in the semiconductor wafer 1502. For an SOI wafer, the active layer 1504 may be manufactured using a standard SOI process. For a bulk semiconductor wafer, the active layer 1504 may be formed with a process that provides an etch stop for a subsequent substrate removal, such as the aforementioned P+ layer formed below the active device layer. Additionally, a chemical mechanical polishing is optionally performed of the top surface of the semiconductor wafer 1502.

[00186] If direct bonding is subsequently to be performed to bond the semiconductor wafer 1502 to the handle wafer 1501, the top surface of the semiconductor wafer 1502 may be planarized after 1703. On the other hand, if an adhesive bond is to be performed, then planarization may not be necessary.

[00187] Separately from 1702-1703, the handle wafer 1501 is prepared (at 1704). Such preparation may include the formation (at 1705) of the bonding layer 1508 and the formation (at 1706) of the trap rich layer 1507, by any appropriate method or in any appropriate order as described above.

[00188] At 1707, the handle wafer 1501 is bonded to the top surface of the semiconductor wafer 1502. The bonding may be a direct oxide-oxide bond, an adhesive bond, an anodic bond, a low-temperature glass frit bond, a molecular bond, an electrostatic bond, etc., as appropriate for a given situation. Therefore, even though the trap rich layer 1507 may be formed in the handle wafer 1501 at any time before, during or after the formation of the active layer 1504 in the semiconductor wafer 1502, the trap rich layer 1507 is not added to the structure 1500 until after the formation of the active layer 1504.

[00189] At 1708, the combined wafers 1501 and 1502 are inverted. At 1709, the original underlying, or back side, portion (e.g. a semiconductor substrate) of the semiconductor wafer 1502 is substantially removed or thinned. Most of the semiconductor substrate can be removed by back side grinding. A final portion of the semiconductor substrate can be removed by a wet etch, selective chemical mechanical polishing (CMP), a dry etch, etc., leaving at least the active device layer 1516 (or the insulator layer 1505, if it is part of the original semiconductor wafer 1502). For embodiments using a bulk semiconductor wafer, the original underlying substrate is removed to the P+ layer (described above) using a wet chemical etch that is highly

selective to P+ material (for example EDP, KOH, or TMAH). The etch can be either chemical or electro-chemical. Additionally, the P+ layer is optionally removed using any combination of grinding, polishing, CMP, dry etch, or non-selective wet etch. The P+ layer will only be a few microns in thickness, so a much better uniformity of a remaining relatively thin (e.g. less than 1 .mu.m) semiconductor film can be achieved than if the semiconductor wafer 1502 was thinned mechanically.

[00190] At 1710, the cavities 1523 are formed in the back side 1522 of the semiconductor wafer 1502 (e.g. the thinned insulator layer 1505). Then the cavities 1523 are filled with a material that is selective to the surrounding material, so that a subsequent etch of the fill material will release the acoustic filter 1512 or 1513 or other MEMS device, if needed.

[00191] Separately from 1702-1710, a second handle wafer is prepared (at 1711). Such preparation may include the formation of the layers and components of the additional layer 1503. (In this embodiment, the additional layer 1503 in FIG. 15 represents a remaining portion of the second handle wafer, rather than monolithically formed elements.) For example, the device layer 1509 and the interconnect layer 1510 (and the insulator layer 1511) are formed in the second handle wafer at 1712. Thus, the acoustic filter 1512 or 1513, other MEMS devices or other active devices of the device layer 1509 are built up into and onto the second handle wafer. Additionally, a bonding layer may also be formed.

[00192] At 1713, the second handle wafer is bonded to the back side 1522 of the semiconductor wafer 1502. The bonding may involve precise alignment to ensure that the acoustic filter 1512 or 1513 or other MEMS devices are properly aligned with the cavities 1523.

[00193] At 1714, the fill material in the cavities 1523 is removed to release the acoustic filter 1512 or 1513 or other MEMS devices. Also, a passivation dielectric layer(s) is optionally deposited on the additional layer 1503 to reduce effects due to moisture and ionic contamination ingress.

[00194] At 1715, patterned contact and metallization are formed for any top or back side connections (e.g. top or bottom electrodes and contacts, etc., as desired). At 1716, various passivation deposition techniques are performed and pad openings are formed, so the overall IC chip can be generally completed with bumps, pillars, or other post-processing metallization. The process 1700 then ends at 1717.

[00195] FIGS. 18-21 illustrate embodiments in which a handle wafer that includes one or more isolation structures (e.g., cavities and other structural features) and one or more trap rich layers (TRLs) is bonded to a device-carrying semiconductor wafer to further inhibit parasitic surface conduction and enhance the RF performance of one or more devices formed in the semiconductor wafer. For essentially the same reasons explained above, the one or more TRLs reduce nonlinear parasitic capacitance and parasitic surface conduction in the handle wafer substrate. The one or more isolation structures, on the other hand, further reduce the impact of non-linear responses in the handle wafer substrate by reducing the permittivity and increasing the resistivity between the one or more devices and the handle wafer substrate to reduce capacitive interactions between the one or more devices and the handle wafer substrate.

[00196] In some examples, a handle wafer is composed of semiconductor material (e.g., silicon, germanium, etc.) that contains free electronic carriers (holes and electrons) that can form a parasitic coupling path when influenced by a nearby electric field. One or more cavities are etched in the semiconductor handle wafer at respective locations where they will align with devices in a transfer layer that will be bonded to the handle wafer. After cavity etching but before cavity isolation deposition (if used), a trap rich layer that conforms to the one or more cavities is formed. The resulting TRL traps free carriers in the semiconductor material that otherwise would respond to an electric field from energized devices (active or passive). The one or more cavities further reduce non-linear interactions with the aligned devices by respectively creating zones of low permittivity and high impedance between the devices and the handle wafer substrate by increasing separation between the device layer and the trap rich layer at locations along the interface between the handle wafer and the transfer layer that coincide with locations of active devices. This technique may be used with almost any type of semiconducting substrate containing free carriers.

[00197] FIG. 18 shows a portion of a handle wafer 1800 with cavities 1801, 1802. The cavities 1801, 1802 are formed in a top surface 1803 of the substrate 1806 into the interior thereof. A trap rich layer 1804 is formed in or over the cavities 1801, 1802. In the illustrated example, the trap rich layer 1804 extends along the entire length of the sidewalls and the bottoms of each of the cavities 1801, 1802; in other examples, however, the trap rich layer 1804 extends only partially along the lengths of the sidewalls and bottoms of the cavities 1801, 1802. In some embodiments, an isolation material 1805 (e.g., an electrically insulating layer, such as silicon dioxide) is formed

over the trap rich layer 1804. In some embodiments, the cavities 1801, 1802 may be in direct contact with the trap rich layer 1804. In some embodiments, the isolation material 1805 serves as an insulating bonding layer that assists in bonding the exposed, non-cavity regions of the top surface of the handle wafer to the transfer layer (see, e.g., the discussion above relating to the bonding layer 206 shown in FIG. 2). In the example shown in FIG. 18, the top surfaces of the cavities 1801, 1802 are open and, therefore, are filled with gas (e.g., air) from the ambient environment.

[00198] The trap rich layer 1804 can be formed in a variety of different ways, including by the methods described below and other parts of this disclosure. Such methods also may be used to form one or more of the other trap rich layers described herein.

[00199] In some examples, the trap rich layer 1804 is implanted into the handle wafer 1800 using particle implantation. In some examples, the implanted particles are one or more of argon, silicon, and other suitable ions, and the handle wafer substrate 1806 is a high-resistivity, very lightly doped silicon substrate. In these examples, argon could beneficially be employed because its relatively large mass can do substantial damage to the handle wafer substrate 1806 and its chemical inertness avoids introducing reactions that otherwise might be deleterious. Silicon also could be used in these examples as the implanted material for similar reasons--i.e., silicon will disrupt the silicon crystal structure of the handle wafer substrate 1806 without producing any deleterious reaction. Oxygen or carbon could be beneficially used for the implant species in these examples because they can form a relatively stable trap density after being thermal annealed to form Si--O or Si--C bonds, which disrupt the silicon crystal lattice, leaving some Si bonds dangling; in addition, with sufficient dose and subsequent thermal annealing, oxygen atoms may start to coalesce, forming SiO.sub.x precipitates, which will form stable trap sites in the silicon lattice of the handle wafer substrate 1806.

[00200] Multiple implant energies typically are used to form the trap rich layer 1804 from the top surface of the handle wafer substrate 1806 to a maximum desired depth or distance from the top surface. The dose also typically is varied with the applied implant energy to create a substantially constant trap density throughout the desired depth. In some examples, a two-implant sequence is used to produce a substantially constant damage profile in a very lightly doped silicon handle wafer substrate 1806. In some of these examples, an implantation of argon at 1E15/cm.sup.2 and 240 keV is followed by a second implantation of argon at 3E14/cm.sup.2 and 60 keV. This

sequence will generally result in a damage profile that is almost constant from the top surface of the handle wafer substrate 1806 to a depth of about 3000 .ANG.. Furthermore, the implantation can be done with a low beam current and/or backside wafer cooling to prevent self-annealing of damage due to self-heating from the implant beam.

[00201] In other embodiments, the entire handle wafer substrate 1806 constitutes the trap rich layer 1804. In some of these examples, the handle wafer substrate 1806 is high-resistivity polysilicon, which is characterized by high performance resulting from the pervasiveness of traps, and low cost relative to monocrystalline silicon wafer substrates. In other examples, the trap rich layer 1804 is formed throughout the entire handle wafer substrate 1806 by irradiating the handle wafer substrate 1806 with relatively high-energy ionizing radiation, such as gamma rays, X-rays or other suitable high-energy particle sources (e.g. MeV electrons, protons or other high-energy particle that can cause semiconductor lattice damage). Such radiation can cause damage to a semiconductor lattice, resulting in trap generation. A suitable gamma ray source, for example, may be cobalt-60. In some of these examples, the cavities 1801, 1802 may be formed after the trap rich layer 1804 is created throughout the entire handle wafer substrate 1806.

[00202] In other examples, the trap rich layer 1804 is formed using one or more of the methods described in co-pending U.S. application Ser. No. 14/013,000, filed Aug. 28, 2013. These methods include laser texturing, chemical etch, irradiation, nanocavity formation, porous Si-etch, semi-insulating polysilicon, thermal stress relief and mechanical texturing. Additionally, combinations of two or more of these techniques may be used to form a trap rich layer.

[00203] In some of these examples, the trap rich layer 1804 is formed through porous silicon etching techniques as described in a flowchart for a trap rich layer manufacturing process 1300 shown in FIG. 13 of U.S. application Ser. No. 14/013,000, filed Aug. 28, 2013, which is incorporated herein by reference along with its accompanying disclosure. Porous silicon etching techniques generally selectively etch a series of pores into the surface of a semiconductor substrate, typically with an electrochemical etch or anodization process, to form a porous silicon layer (PSL). For trap rich layer applications, dangling bonds at the sidewall surfaces of the pores generally provide the trap states.

[00204] In some examples of porous silicon etching processing, after preparing a semiconductor substrate, pores are etched in the semiconductor substrate to form a porous silicon layer. For vertical surfaces, such as the sidewalls of holes or trenches in the semiconductor substrate, an electrolytic etching cell for electrolytically controlled etching (ECE) may be set up to get the pores down into the holes and formed laterally. If the etch process leaves undesirable material inside the pores, then a treatment process may have to be performed to remove the remaining material. Additionally, a layer of sealing material is placed over the pores to ensure that no undesirable material enters the pores during subsequent processing. The sealing material may be an insulator layer or a bonding layer for a handle wafer. Alternatively, the sealing material may form a smooth surface on which the insulator or bonding layer may be formed.

[00205] In other examples, the trap rich layer 1804 is formed through chemical etching techniques as described in a flowchart for a trap rich layer manufacturing process 1600 shown in FIG. 16 of U.S. application Ser. No. 14/013,000, filed Aug. 28, 2013, which is incorporated herein by reference along with its accompanying disclosure. Chemical etching the semiconductor substrate (e.g. with fluorinated chemistry, also known as "texturing") tends to damage the semiconductor surface by forming bumps, short-wide pillars, or tall-narrow columns in a non-uniform randomized morphology, which increase the effective surface area.

[00206] In some examples of chemical etching processing, after preparing a semiconductor substrate, a seeding process is performed on the semiconductor substrate to cause some initial damage to the surface of the semiconductor substrate, e.g. by scratching the semiconductor substrate surface or impinging a mechanical force onto the surface to cause a relatively small amount of damage. The chemical etch is then performed. The chemical etch may be a plasma texturing/etch, a reactive ion etch (RIE), a wet chemical etch (e.g., with HF/HN03), a dry etch, a fluorinated plasma etch (e.g., with SF6I02) or other appropriate etch technique.

[00207] In still other examples, the trap rich layer 1804 is formed by depositing a layer of high resistivity material on the surface of the handle wafer substrate 1806 before the handle wafer 1800 is bonded to the device-carrying semiconductor wafer. In some of these examples, the deposited material is a polycrystalline semiconductor (e.g., polycrystalline silicon) and the handle wafer substrate 1806 is a high-resistivity, very lightly doped silicon substrate. In other examples, high-energy particles (e.g. a noble gas, silicon, oxygen, carbon, germanium, etc.) are implanted into the handle wafer

substrate 1806 to create damaged regions that form the trap rich layer 1804. In some examples in which the isolation material 1805 is present, the trap rich layer implantation can be performed before or after the isolation material 1805 has been deposited.

[00208] FIG. 19 illustrates a simplified embodiment of a semiconductor structure 1900 within a portion of an IC chip. Portions of the structure 1900 may be formed by wafer bonding or layer transfer techniques, as described herein. Similar to the structure 200 described above in connection with FIG. 2, the structure 1900 includes the handle wafer 1800 bonded to a device-carrying semiconductor structure 1901. The semiconductor structure 1900 is referred to herein as a layer transfer structure. Additionally, this embodiment 1900 may have many, if not all, of the benefits and advantageous aspects mentioned above for the configuration described in connection with FIG. 2.

[00209] The device-carrying semiconductor structure 1901 includes an active/device layer 1902 that has a bottom side in contact with an insulator layer 1903. In some examples, another insulator layer (e.g., a bonding layer; not shown) is disposed over active/device layer 1902. In general, the device-carrying semiconductor structure 1901 is formed on a semiconductor wafer (e.g., a silicon-on-sapphire wafer, a gallium arsenide wafer, or a semiconductor-on-insulator (SOI) wafer, and in some examples an insulating wafer). The device-carrying semiconductor structure 1901 typically is formed from either a conventional SOI wafer or a conventional bulk semiconductor wafer.

[00210] In the illustrated example, the device-carrying semiconductor structure 1901 includes an active layer 1902 and an insulator layer 1903. The active layer 1902 has an active device layer 1904 and an interconnect layer 1905. The insulator layer 1903 typically is formed as a buried oxide or other appropriate insulator or dielectric material. Before bonding the handle wafer 1800 to the device-carrying semiconductor structure 1901, the structures of the active layer 1902 are formed in and on the semiconductor wafer. After bonding, a portion of the original semiconductor wafer (not shown) below the insulator layer 1903 is removed such that a back side 1906 of the insulator layer 1903 is exposed. Once the underlying substrate is removed, the handle wafer 1800 provides the required stabilizing force necessary to protect and preserve the electrical characteristics of devices or structures in the active layer 1902. In some examples, metallization or interconnect wiring (not shown) may extend through the insulator layer 1903 and be deposited on the back side 1906 of the insulator layer 1903 for back side electrical connections between the components in the active layer 1902.

[00211] The active layer 1902 is a circuit layer that includes the active device layer 1904 and the metallization or metal interconnect layer 1905. These layers typically include a combination of dopants, dielectrics, polysilicon, metal wiring, passivation, and other layers, materials and/or components that are present after circuitry has been formed therein. The circuitry may include metal wiring 1907 (e.g. in the metal interconnect layer 1905), passive devices such as resistors, capacitors, and inductors, and active devices 1908, 1909 such as integrated circuit devices (e.g., transistors), acoustic devices (e.g., acoustic filters), and other MEMS devices (e.g. in the active device layer 1904).

[00212] In some examples, a bonding layer (which may be similar to the bonding layer 206 described above in connection with FIG. 2) is interposed between the handle wafer 1800 and the device-carrying semiconductor structure 1901 to bond a top exposed surface 1810 of the handle wafer 1800 to a top surface 1911 of the device-carrying semiconductor structure 1901 during a wafer bonding or layer transfer procedure. The bonding layer is formed before wafer bonding or layer transfer. In some examples, the bonding layer is formed on the handle wafer. In other examples, the bonding layer is formed on the semiconductor wafer.

[00213] In some examples, the bonding layer is deposited over the trap rich layer 1804 and the isolation material 1805 (if present) on the handle wafer 1800. The bonding layer may be formed from a combination of one or more insulator layers and passivation layers. In some examples, the bonding layer is an oxide layer formed by chemical vapor deposition (CVD) or thermal oxidation. In these examples, the trap rich layer 1804 typically is formed before the isolation and/or bonding layers are formed on the handle wafer because the types of materials (e.g. an oxide) typically used for the isolation and bonding layers tend to impede the TRL forming implantation process. If any of the isolation and bonding layers is a thermal oxide material, however, the trap rich layer 1804 typically is formed after the thermal oxidation process to mitigate potential degradation of the trap rich layer 1804 that might occur if the trap rich layer 1804 were exposed to the high temperatures typically used in such thermal oxidation processes.

[00214] As illustrated in the embodiment shown in FIG. 19, before bonding the handle wafer 1800 to the semiconductor substrate, the cavities 1801, 1802 are aligned vertically with respective ones of the active devices 1908, 1909 to maximally reduce the permittivity and increase the resistivity between the active devices 1908, 1909 and the handle wafer substrate 1806 and, thereby, reduce the capacitive interactions between the

one or more devices and the handle wafer substrate. In some examples, the two cavities 1801, 1802 are replaced by a single cavity that has the same lateral extent as the two cavities 1801, 1802 and is aligned over both of the active devices 1908, 1909. In still other examples, additional cavities may be provided over other active and/or passive devices in the active layer 1902 of the device-carrying semiconductor structure 1901.

[00215] In the device structures described in connection with FIGS. 18-19, the deleterious impact of the non-linear response characteristics of the handle wafer substrate that otherwise would occur across the interface of the handle wafer 1800 and the active layer 1902 are effectively eliminated. The effects are eliminated as a result of the combination of the permittivity reduction and the resistivity increase provided by the cavities, the parasitic substrate conduction and substrate loss reduction resulting from the inhibition of the movement of carriers provided by the trap rich layer 1804, and the additional isolation optionally provided by isolation layer 1805 and the optional insulating bonding layer discussed above.

[00216] FIGS. 20-21 show alternative embodiments in which a handle wafer 2000 that includes one or more cavities and one or more trap rich layers (TRLs) is bonded to a device-carrying semiconductor wafer to further inhibit parasitic surface conduction and enhance the RF performance of one or more devices formed in the semiconductor wafer. These embodiments are essentially the same as the embodiments described above in connection with FIGS. 18-19, except that the handle wafer 2000 has cavities 1801, 1802 that contain solid fill material 2001, 2002 instead of gas. Exemplary fill materials include: low dielectric constant materials; materials (e.g., aluminum oxide, silicon carbide, and aluminum nitride) that are characterized by high resistivity and high thermal conductivity; and electrical insulators (e.g., silicon dioxide). As shown in FIGS. 20-21, the top surface 2010 of the handle wafer 2000 is polished smooth before being bonded to the device-carrying semiconductor structure 1901 of the semiconductor structure 2100 within a portion of an IC chip.

[00217] It is noted that elements of the structures illustrated in FIGS. 18-21 are not necessarily to scale and may be shown in an idealized form, exaggerated, or simplified for ease of illustration and description. Additionally, some elements that may be expected to be included in such a semiconductor structure may have been omitted or combined with other elements for ease of illustration and description.

[00218] FIG. 22 shows an example of a method 2200 of fabricating at least part of an integrated circuit chip that includes a semiconductor structure of the type

exemplified by the structures 1900 and 2100 that are shown in FIGS. 19 and 21, respectively. The constituent processes of the method 2200 are merely illustrative of exemplary processes that may be used in fabricating the integrated circuit chip. Other methods for fabricating integrated circuit chips of essentially the same type may have one or more different constituent processes or may utilize a different ordering of the same processes shown in FIG. 22.

[00219] Initially, the semiconductor wafer used in forming the device-carrying semiconductor structure 1901 is prepared (FIG. 22, block 2202). If the semiconductor wafer is an SOI wafer, then the preparation process may simply involve providing a standard SOI wafer. In some examples, if the semiconductor wafer is a bulk semiconductor wafer, then the preparation process may include creating a buried P+ layer in the bulk semiconductor wafer, e.g. by epitaxial growth or ion implantation methods. Epitaxial methods may involve epitaxially depositing a layer of P+ material on a P- or N- substrate. Then a layer of lightly doped silicon may be epitaxially deposited to use as an active device layer. This layer may be thick enough so that up-diffusion from the P+ layer does not reach the active device layer 1904 by the end of processing to form the structures in the active layer 1902. Ion implantation methods, on the other hand, may involve performing a high-dose, high-energy ion (e.g. Boron, etc.) implant into the surface of the bulk semiconductor wafer, and forming a buried P+ layer deep enough so it will not diffuse up to the active device layer 1904 during processing to form the structures in the active layer 1902.

[00220] After the semiconductor wafer has been prepared (FIG. 22, block 2202), the active layer 1902 is formed to produce a circuit with a set of active devices 1908, 1909 in the semiconductor wafer. For an SOI wafer, the active layer 1902 may be manufactured using a standard SOI process. For a bulk semiconductor wafer, the active layer 1902 may be formed with a process that provides an etch stop for a subsequent substrate removal, such as the aforementioned P+ layer formed below the active device layer. Additionally, a chemical mechanical polishing is optionally performed of the top surface of the semiconductor wafer.

[00221] If direct bonding is subsequently to be performed to bond the semiconductor wafer to the handle wafer 1800, 2000, the top surface of the semiconductor wafer may be planarized after the active layer is formed (FIG. 22, block 2203). On the other hand, if an adhesive bond is to be performed, then planarization may not be necessary.

[00222] Independently of the processes 2202, 2203 that are performed with respect to the semiconductor wafer, the handle wafer 1800, 2000 is prepared (FIG. 22, block 2204). In some examples, this process involves providing a semiconductor wafer (e.g., a high-resistivity, very lightly doped silicon wafer).

[00223] After the handle wafer 1800, 2000 has been prepared (FIG. 22, block 2204), cavities 1801, 1802 are formed in the top surface 1810, 2010 of the handle wafer 1800, 2000 (FIG. 22, block 2205). The cavities 1801, 1802 may be formed in a variety of well-known ways, including using standard lithographic patterning and etching methods.

[00224] After the cavities 1801, 1802 have been formed in the handle wafer 1800, 2000 (FIG. 22, block 2205), a trap rich layer 1804 is formed over the top surface 1810, 2010 of the handle wafer 1800, 2000 (FIG. 22, block 2206). The trap rich layer may be formed in any of the variety of different ways described herein. The optional isolation layer 1805 (e.g., a dielectric layer or an oxide layer) may be formed over the trap rich layer 1804, as described above.

[00225] After the trap rich layer 1804 and the optional isolation layer 1805 have been formed (FIG. 22, block 2206), the cavities 1801, 1802 optionally may be filled, as described above (FIG. 22, block 2207). The top surface 1810, 2010 of the resulting handle wafer structure typically is polished to provide a suitable surface for bonding to the semiconductor wafer.

[00226] After the semiconductor wafer and the handle wafer 1800, 2000 have been individually processed (FIG. 22, blocks 2202-2207), the top surface 1810, 2010 of the handle wafer 1800, 2000 is bonded to the top surface of the semiconductor wafer (FIG. 22, block 2208). The bonding may be a direct oxide-oxide bond, an adhesive bond, an anodic bond, a low-temperature glass frit bond, a molecular bond, an electrostatic bond, etc., as appropriate for a given situation. Advantageously, by this method, the trap rich layer 1804 may be formed in the handle wafer 1800, 2000 at any time before, during or after the formation of the active layer 1902 in the semiconductor wafer 202; however, the handle wafer carrying the trap rich layer 1804 is not bonded to the device-carrying semiconductor structure 1901 until after the active layer 1902 has been formed.

[00227] After the semiconductor wafer and the handle wafer 1800, 2000 have been bonded to one another (FIG. 22, block 2208), the original bottom substrate portion of the semiconductor wafer is substantially removed or thinned (FIG. 22, block 2209).

Most of the semiconductor substrate can be removed by backside grinding. A final portion of the semiconductor substrate can be removed by a wet etch, selective chemical mechanical polishing (CMP), a dry etch, etc., leaving at least the active layer 1902. In examples in which the semiconductor wafer is a SOI wafer, the insulator layer 1903 also is left after thinning. For embodiments using a bulk semiconductor wafer, the original underlying substrate is removed to the P+ layer (described above) using a wet chemical etch that is highly selective to P+ material (for example EDP, KOH, or TMAH). The etch process can be either chemical or electro-chemical. Additionally, the P+ layer is optionally removed using any combination of grinding, polishing, CMP, dry etch, or non-selective wet etch. The P+ layer will only be a few microns in thickness, so a much better uniformity of a remaining relatively thin (e.g. less than 1 .mu.m) semiconductor film can be achieved than if the semiconductor wafer was thinned mechanically. In some examples, after the bottom substrate portion of the semiconductor wafer has been substantially removed or thinned (FIG. 22, block 2209), a passivation dielectric layer(s) optionally is deposited on the newly-exposed surface to reduce effects due to moisture and ionic contamination ingress.

[00228] After the bottom substrate portion of the semiconductor wafer has been substantially removed or thinned (FIG. 22, block 2209), patterned contact and metallization are formed for any top or backside connections (e.g. top or bottom electrodes and contacts, etc., as desired) (FIG. 22, block 2210) and various passivation deposition techniques are performed and pad openings are formed, so the overall IC chip can be generally completed with bumps, pillars, or other post-processing metallization (FIG. 22, block 2211).

[00229] In some examples, the semiconductor structure 1900, 2100 resulting from the method 220 of FIG. 22 is characterized by a device layer that has been layer-transferred and bonded onto a semiconductor wafer at an interface, where the device layer includes an active device, the semiconductor wafer includes a trap rich layer and a substrate, and the trap rich layer conforms to structure (e.g., cavities, columns, other structural features) in the substrate that varies separation between the device layer and the trap rich layer along the interface. The structure in the substrate typically is aligned with the active layer to produce a larger separation between the device layer and the substrate at a region along the interface adjacent the active device than at other locations along the interface.

[00230] Although embodiments of the present invention have been discussed primarily with respect to specific embodiments thereof, other variations are possible. Various configurations of the described system may be used in place of, or in addition to, the configurations presented herein. For example, additional layers of passivation and insulation could be disposed in-between described layers where appropriate. As another example, configurations were described with general reference to silicon substrates but any type of semiconductor material could be used in the place of silicon.

[00231] Those skilled in the art will appreciate that the foregoing description is by way of example only, and is not intended to limit the present invention. Nothing in the disclosure should indicate that the present invention is limited to systems that are implemented on a single wafer. Nothing in the disclosure should indicate that the present invention is limited to systems that require a particular form of semiconductor processing or to integrated circuits. In general, any diagrams presented are only intended to indicate one possible configuration, and many variations are possible. Those skilled in the art will also appreciate that methods and systems consistent with the present invention are suitable for use in a wide range of applications encompassing any related to improving the electrical performance of semiconductor structures.

[00232] While the specification has been described in detail with respect to specific embodiments of the present invention, it will be appreciated that those skilled in the art, upon attaining an understanding of the foregoing, may readily conceive of alterations to, variations of, and equivalents to these embodiments. These and other modifications and variations to the present invention may be practiced by those skilled in the art, without departing from the spirit and scope of the present invention, which is more particularly set forth in the appended claims.

Claims

What is claimed is:

1. A method comprising:

fabricating a device layer on a top portion of a semiconductor wafer that comprises a substrate, wherein the device layer comprises an active device;

forming a trap rich layer at a top portion of a handle wafer, wherein the forming comprises etching the top portion of the handle wafer to form a structure in the top portion of the handle wafer that configures the trap rich layer;

bonding a top surface of the handle wafer to a top surface of the semiconductor wafer; and removing a bottom substrate portion of the semiconductor wafer.

2. The method of claim 1, wherein the etching comprises etching the top surface of the handle wafer to form one or more columns in the top portion of the handle wafer.

3. The method of claim 1, wherein the etching comprises etching the top surface of the handle wafer to form one or more cavities in the top portion of the handle wafer.

4. The method of claim 1, wherein the forming comprises forming the trap rich layer by one or more of laser texturing, chemical etch, irradiation, nanocavity formation, porous Si-etch, semi-insulating polysilicon, thermal stress relief, and mechanical texturing.

5. The method of claim 1, further comprising:

before the bonding, forming one or more material layers at the top portion of the handle wafer above the trap rich layer.

6. The method of claim 5, wherein the one or more material layers are one or more of an isolation layer and a bonding layer.

7. The method of claim 1, wherein the bonding comprises bonding the top surface of the handle wafer to the top surface of the semiconductor wafer with the structure in the top portion of the handle wafer aligned with the active device.

8. A method comprising:

fabricating a device layer on a top portion of a semiconductor wafer that comprises a substrate, wherein the device layer comprises active devices;

forming a trap rich layer at a top portion of a handle wafer, wherein the forming comprises etching the top portion of the handle wafer to form cavities in the top portion of the handle wafer;

bonding a top surface of the handle wafer to a top surface of the semiconductor wafer with the active devices aligned with the cavities; and

removing a bottom substrate portion of the semiconductor wafer.

9. The method of claim 8, the forming comprises creating the trap rich layer by one or more of laser texturing, chemical etch, irradiation, nanocavity formation, porous Si-etch, semi-insulating polysilicon, thermal stress relief, and mechanical texturing.

10. The method of claim 8, further comprising: forming a fill material on the cavities.

11. The method of claim 10, wherein the fill material is one of aluminum oxide, silicon carbide, aluminum nitride, and silicon dioxide.

12. The method of claim 8, further comprising:

before the bonding, forming one or more material layers on the top portion of the handle wafer over the trap rich layer.

13. The method of claim 12, wherein the one or more material layers are one or more of an isolation layer and a bonding layer.

14. The method of claim 8, wherein the active devices comprise a radio frequency switch device.

15. A semiconductor device comprising:

a device layer layer-transferred and bonded onto a semiconductor wafer at an interface, wherein the device layer comprises an active device;

wherein the semiconductor wafer comprises a trap rich layer and a substrate, wherein the trap rich layer conforms to a structure in the substrate that varies separation between the device layer and the trap rich layer along the interface.

16. The semiconductor device of claim 15, wherein the structure in the substrate comprises one or more columns.

17. The semiconductor device of claim 15, wherein the structure in the substrate comprises one or more cavities.

18. The semiconductor device of claim 17, wherein the one or more cavities are unfilled with solid material.

19. The semiconductor device of claim 17, wherein the one or more cavities are filled with one of aluminum oxide, silicon carbide, aluminum nitride, and silicon dioxide.

20. The semiconductor device of claim 15, wherein:

the structure in the substrate is aligned with the active layer to produce a larger separation between the device layer and the substrate at a region along the interface adjacent the active device than at other locations along the interface.

FIG. 1
Prior Art

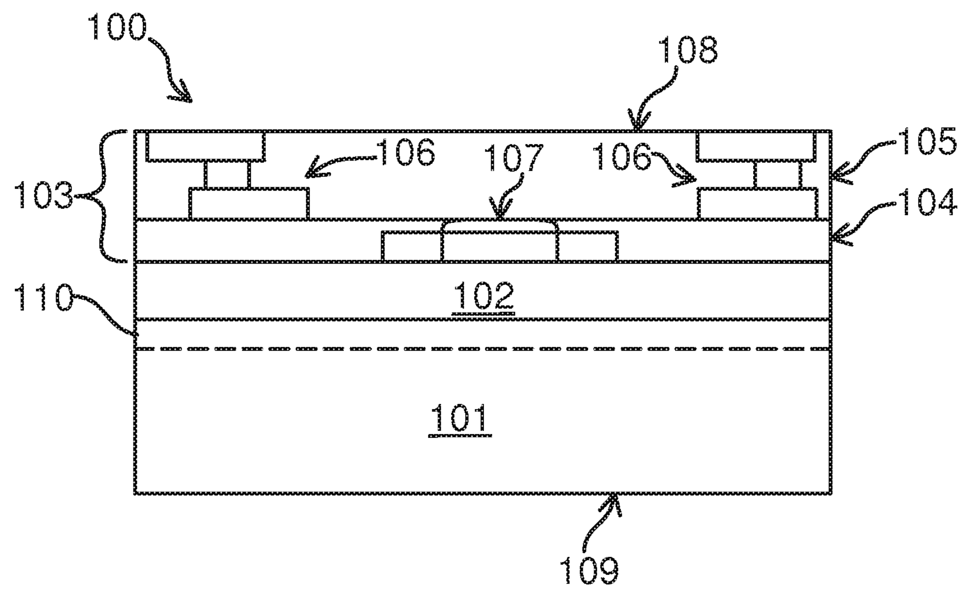


FIG. 2

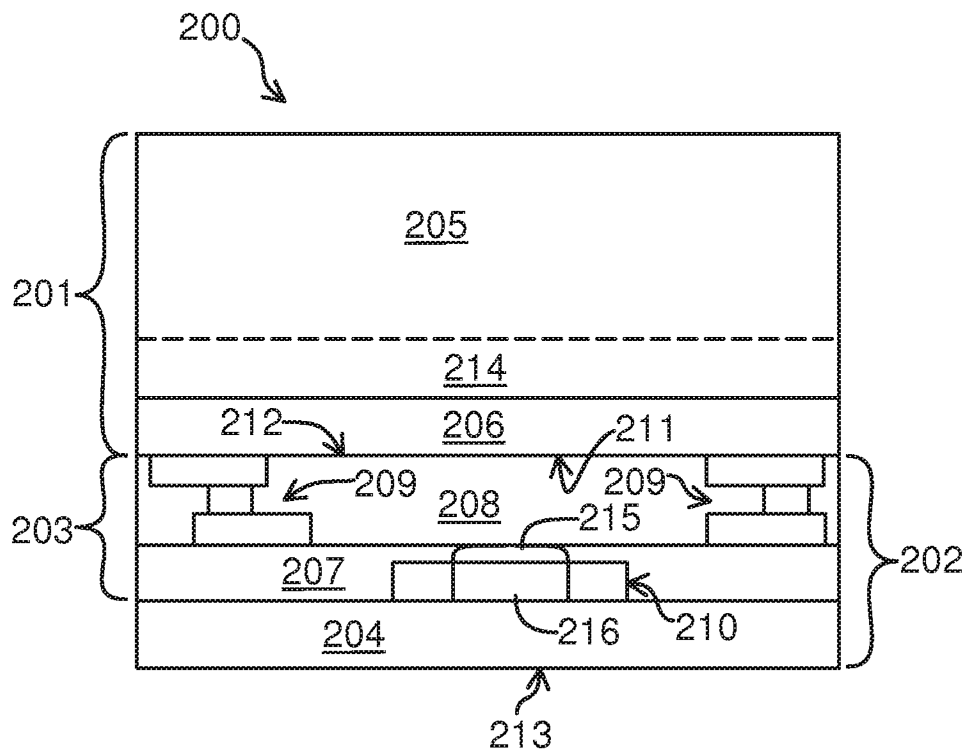


FIG. 3

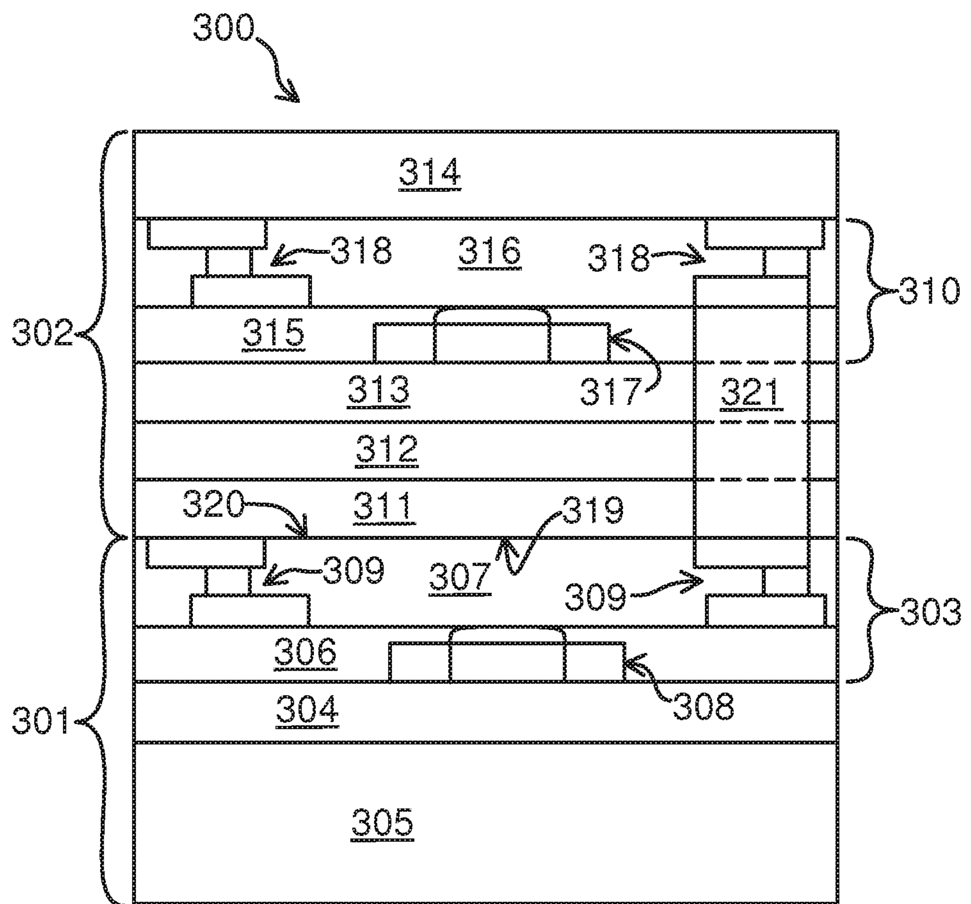


FIG. 4

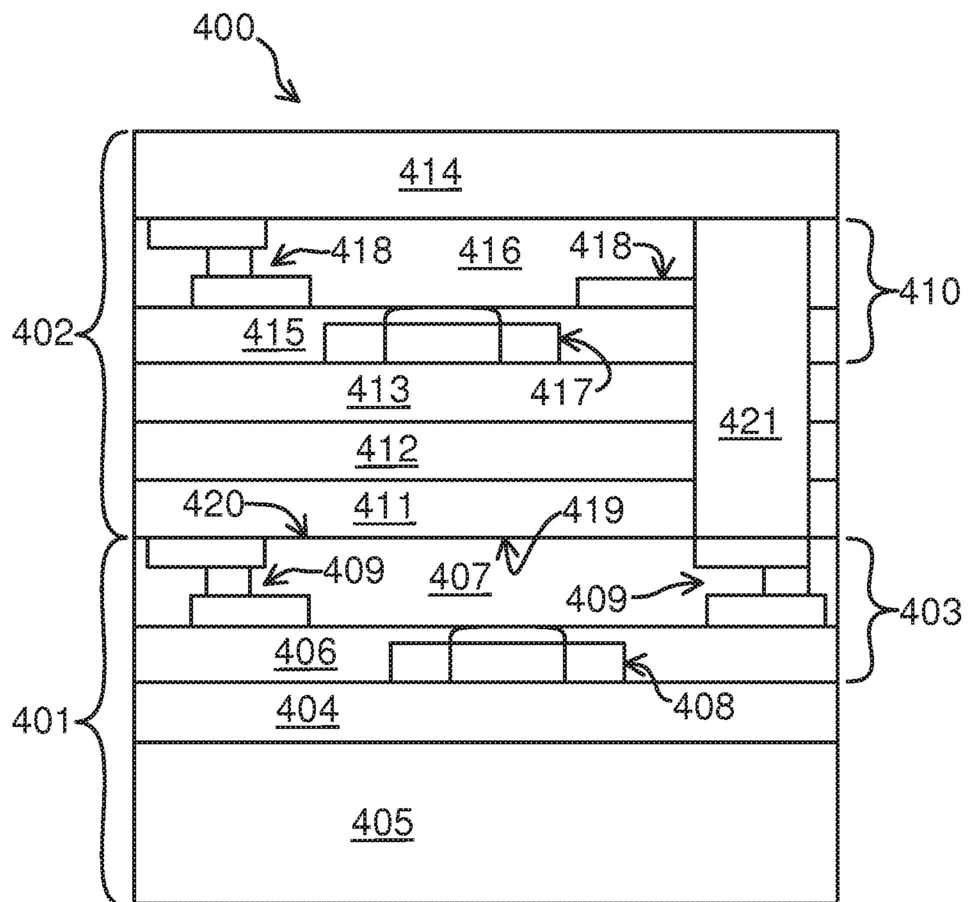


FIG. 5

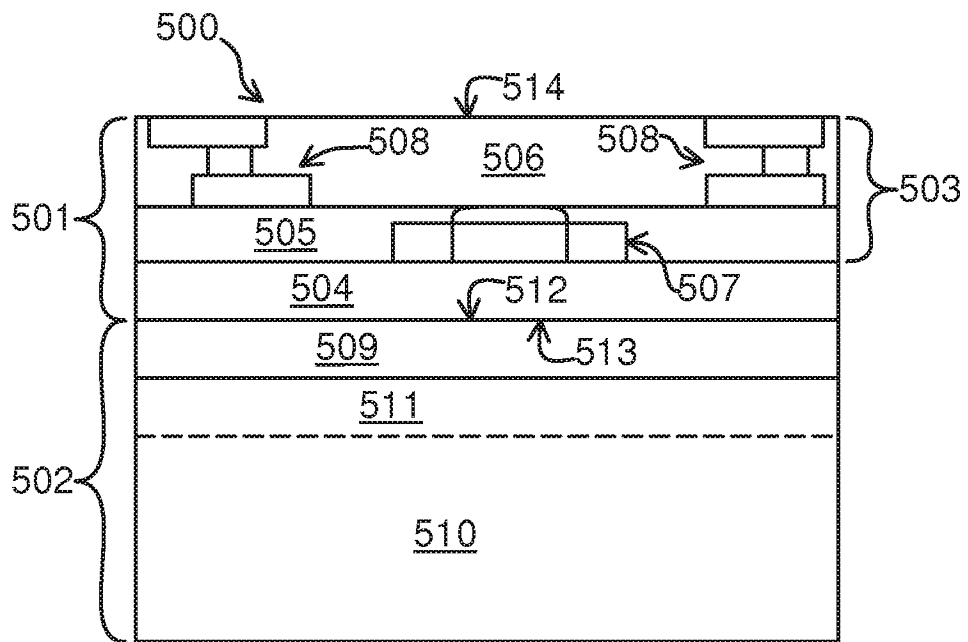
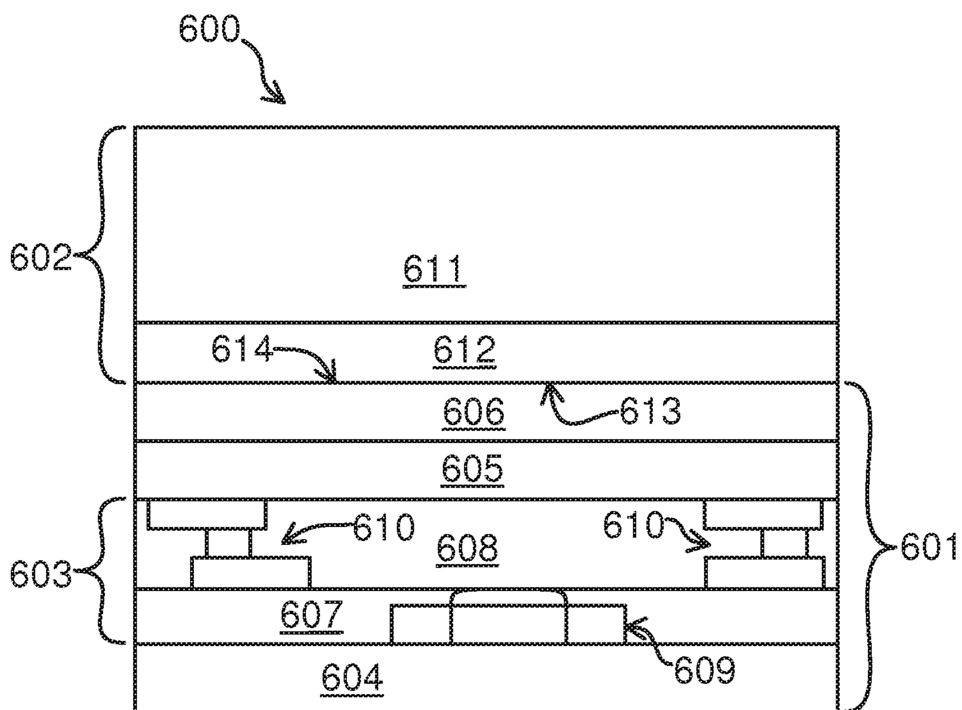


FIG. 6



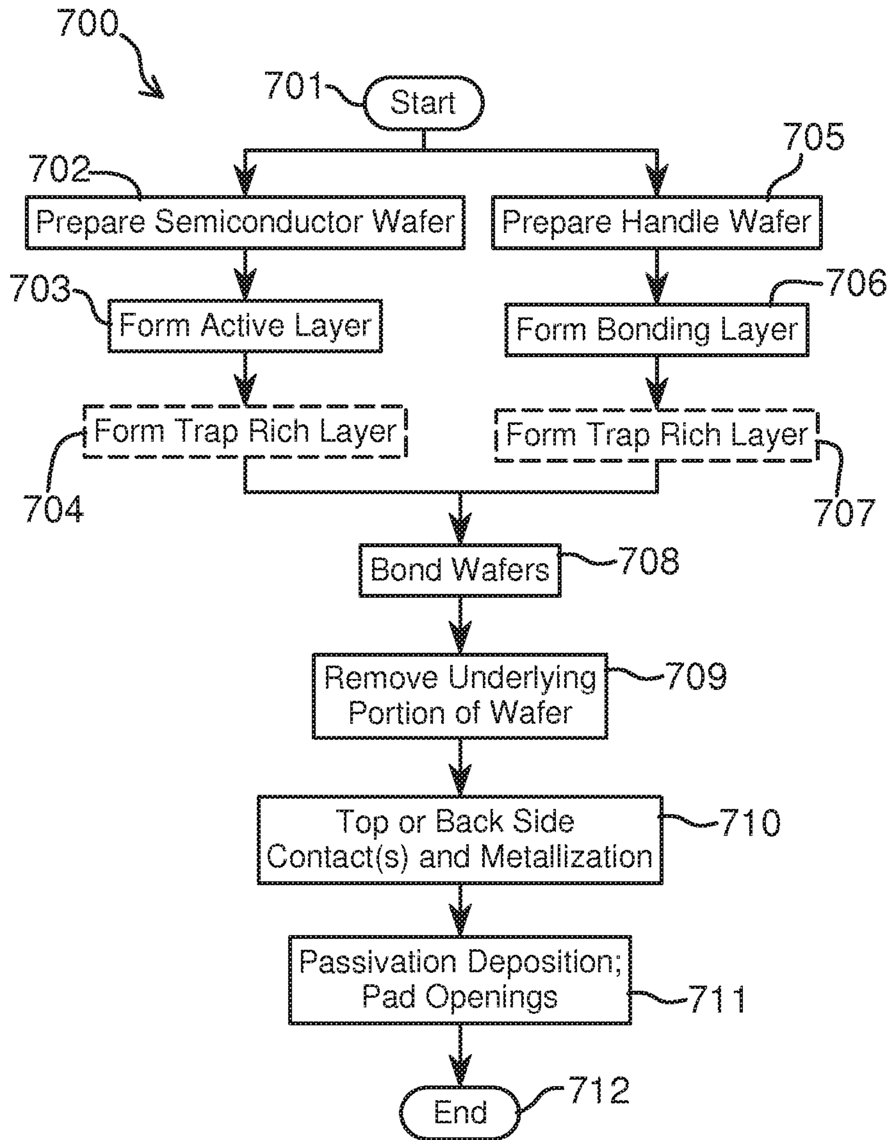


FIG. 7
700
701
Start
702
Prepare Semiconductor Wafer
705
Prepare Handle Wafer
703
Form Active Layer
706
Form Bonding Layer
Form Trap Rich Layer
704
Form Trap Rich Layer
707
Bond Wafers
708
Remove Underlying Portion of Wafer
709
Top or Back Side Contact(s) and Metallization
710
Passivation Deposition; Pad Openings
711
End
712

FIG. 8

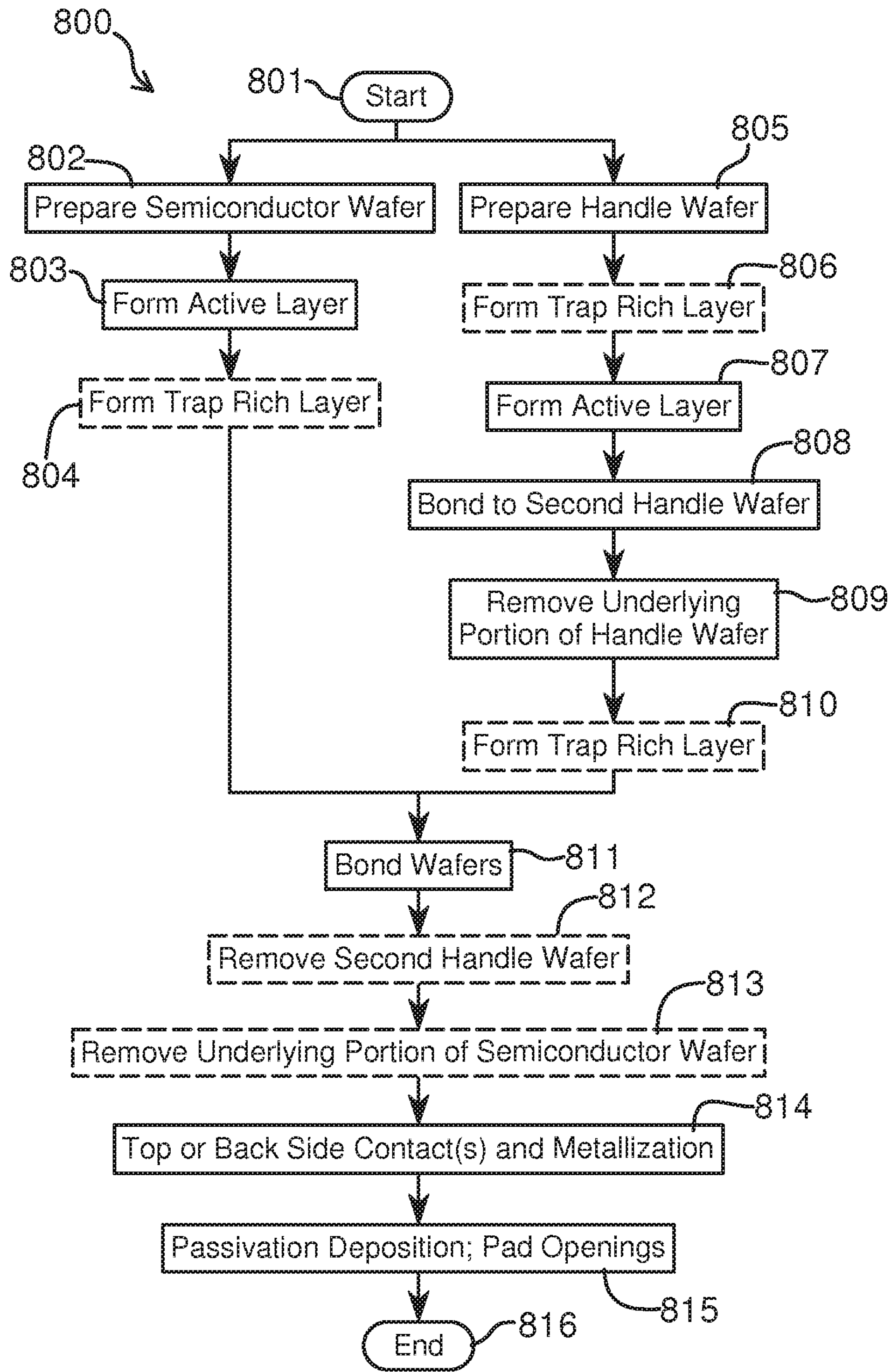


FIG. 9

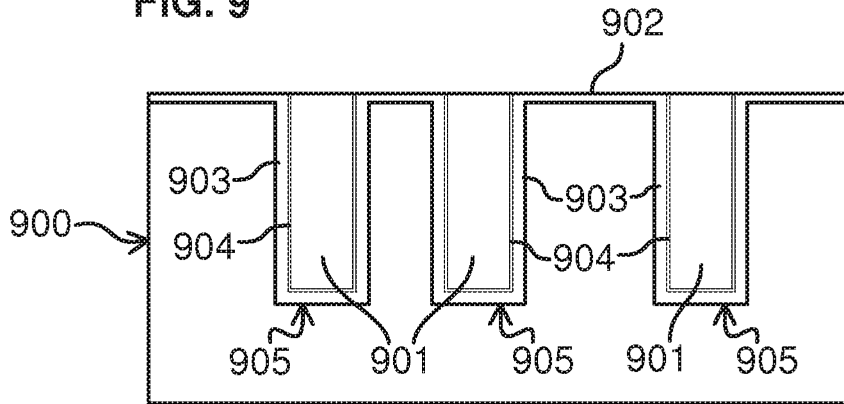
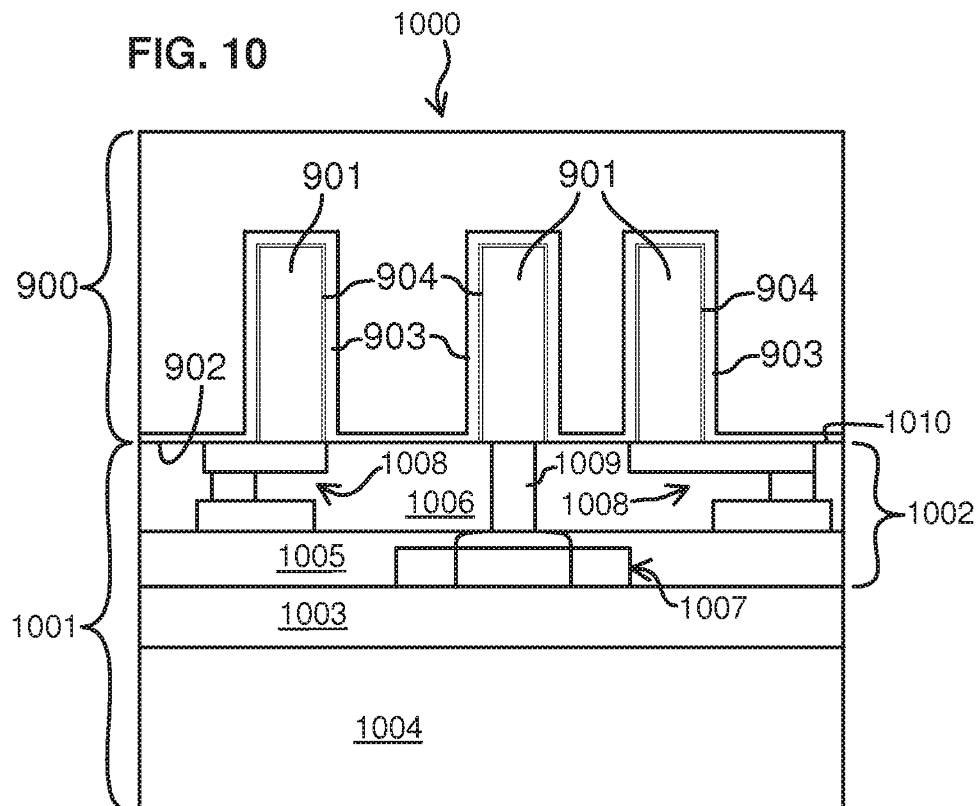


FIG. 10



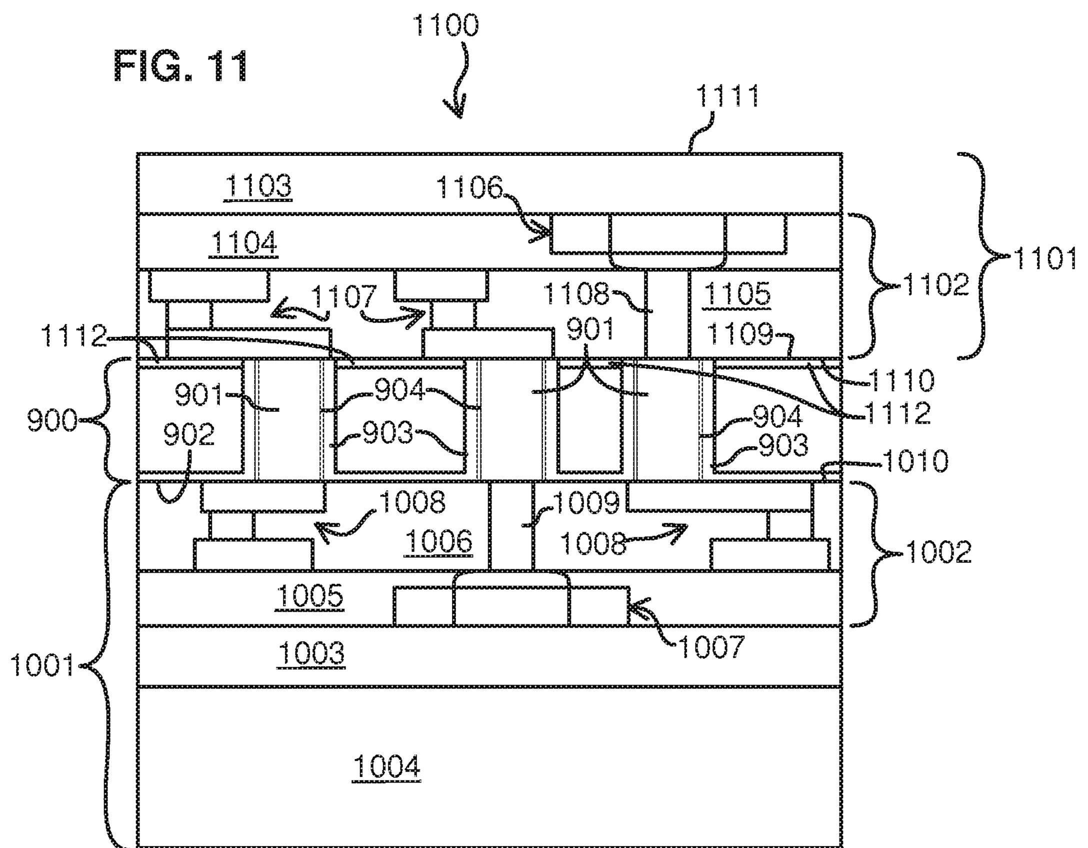


FIG. 11
1100
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904
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1010
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1003
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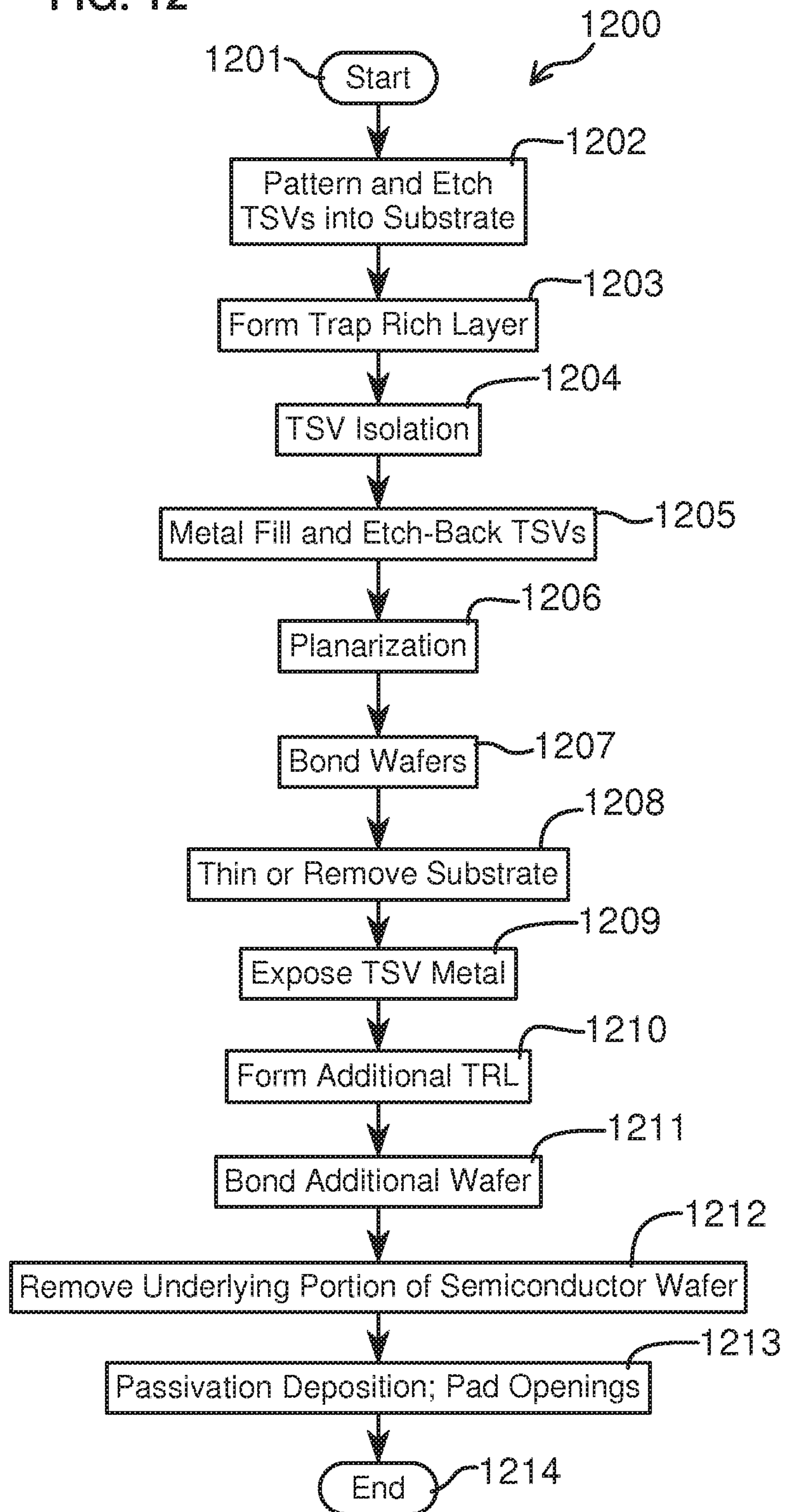
FIG. 12
1200
1201
Start
1202
Pattern and Etch TSVs into Substrate
1203
Form Trap Rich Layer
1204
TSV Isolation
1205
Metal Fill and Etch-Back TSVs
1206
Planarization
1207
Bond Wafers
1208
Thin or Remove Substrate
1209
Expose TSV Metal
1210
Form Additional TRL
1211
Bond Additional Wafer
1212
Remove Underlying Portion of Semiconductor Wafer
1213
Passivation Deposition; Pad Openings
1214
End

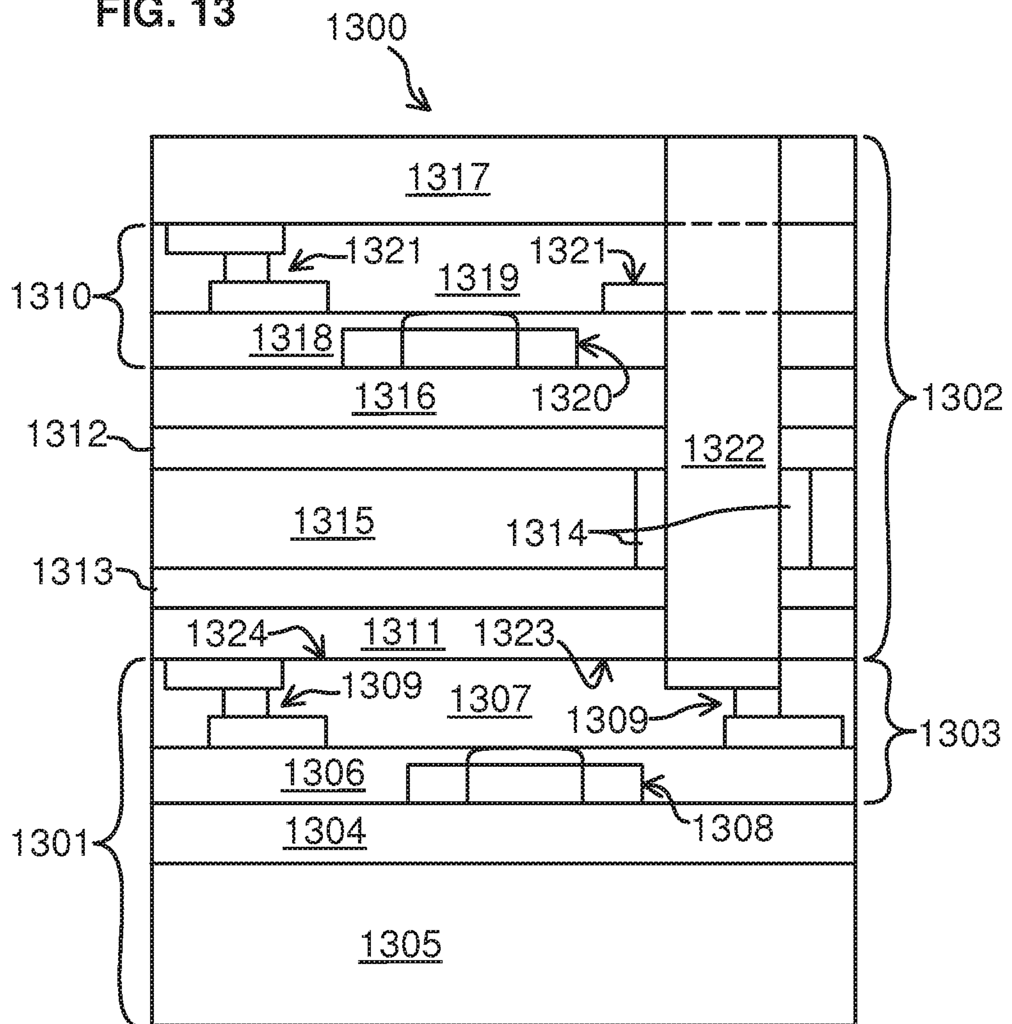
FIG. 13
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FIG. 14

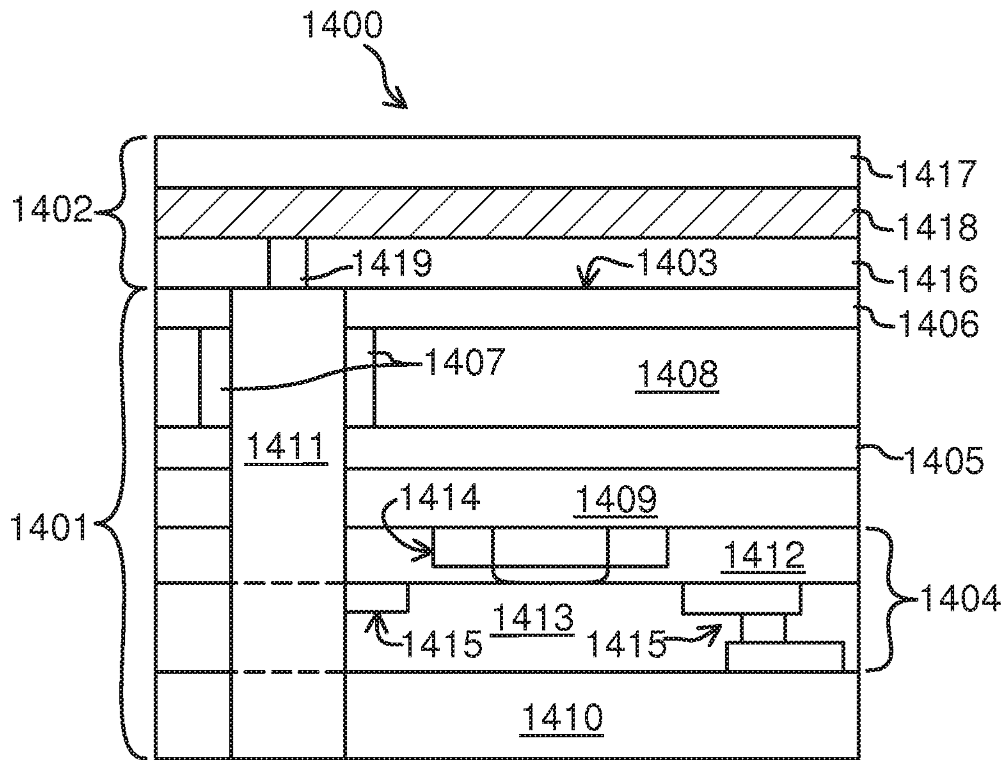


FIG. 15

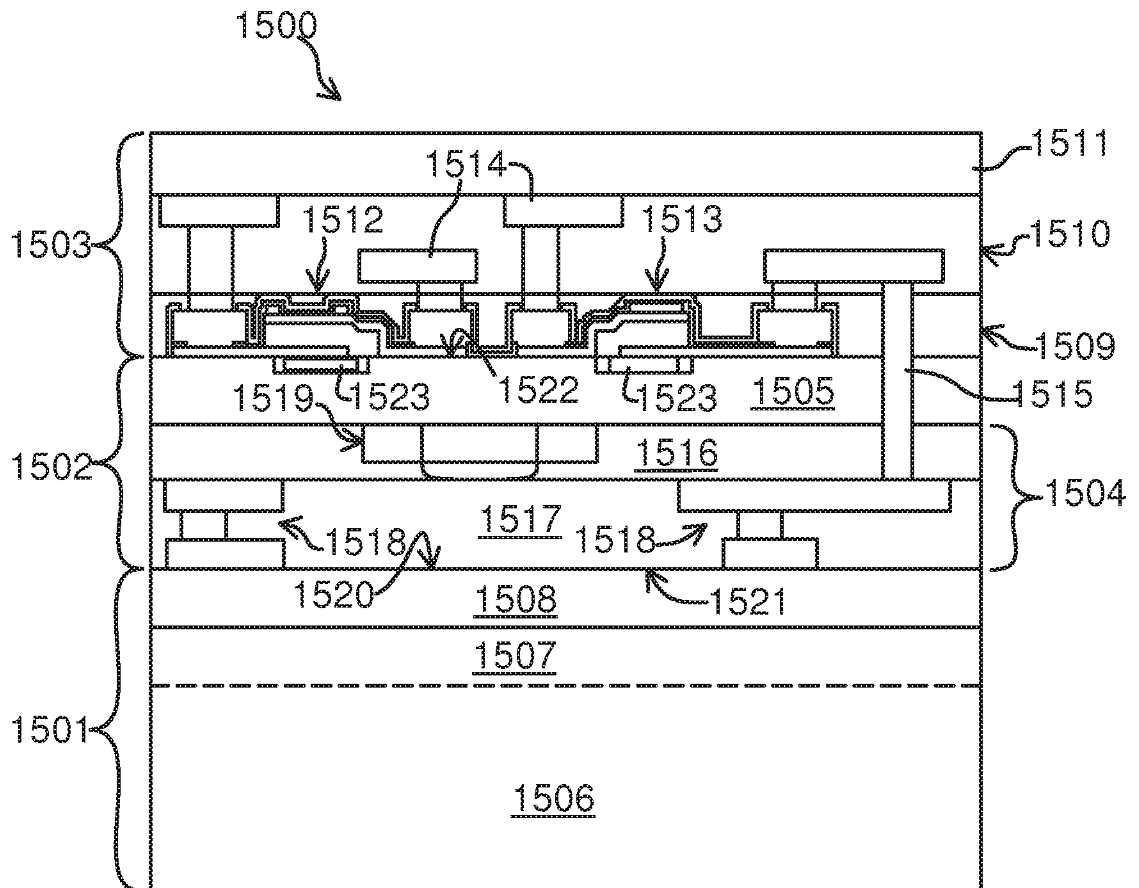


FIG. 16

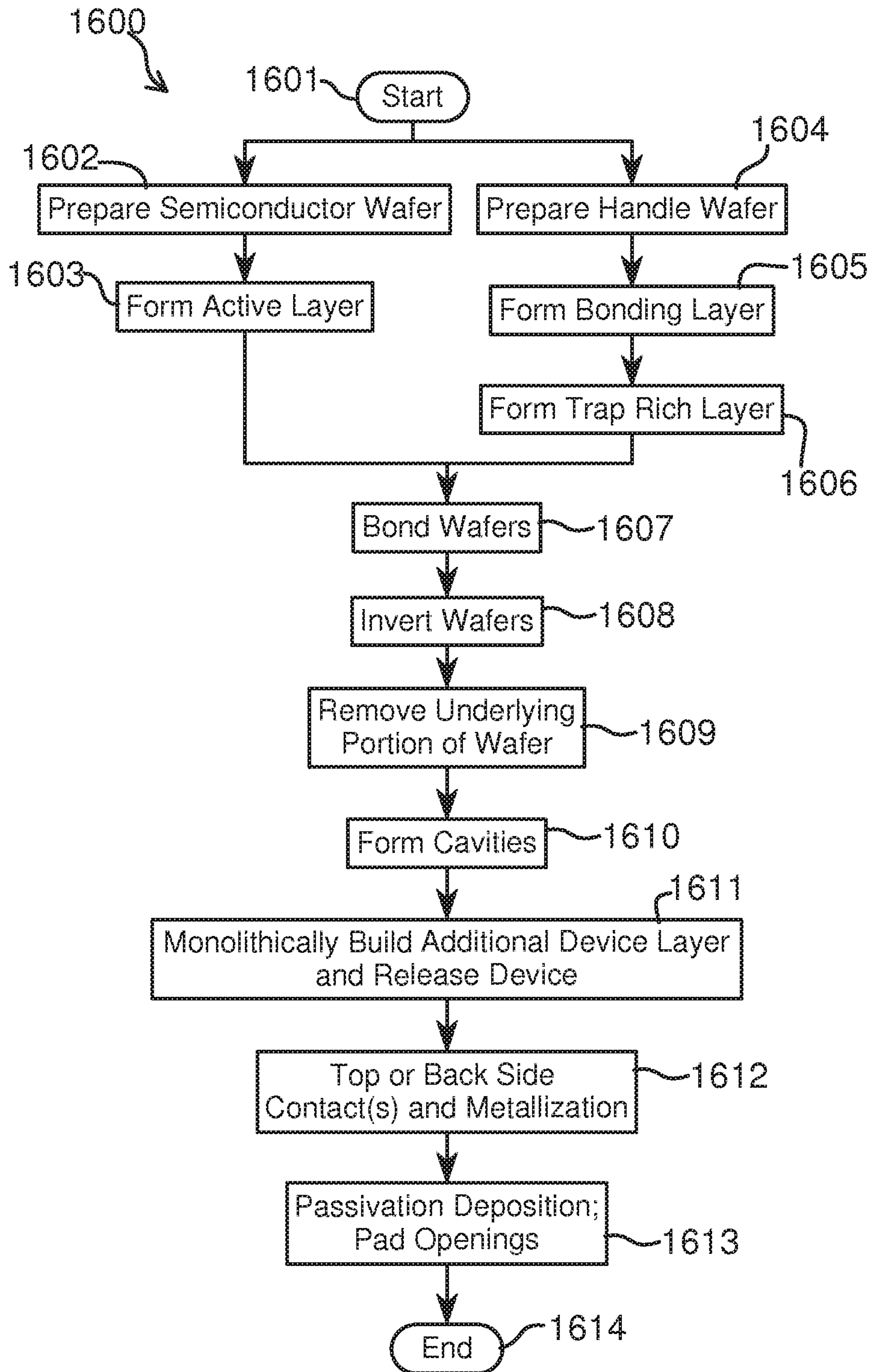
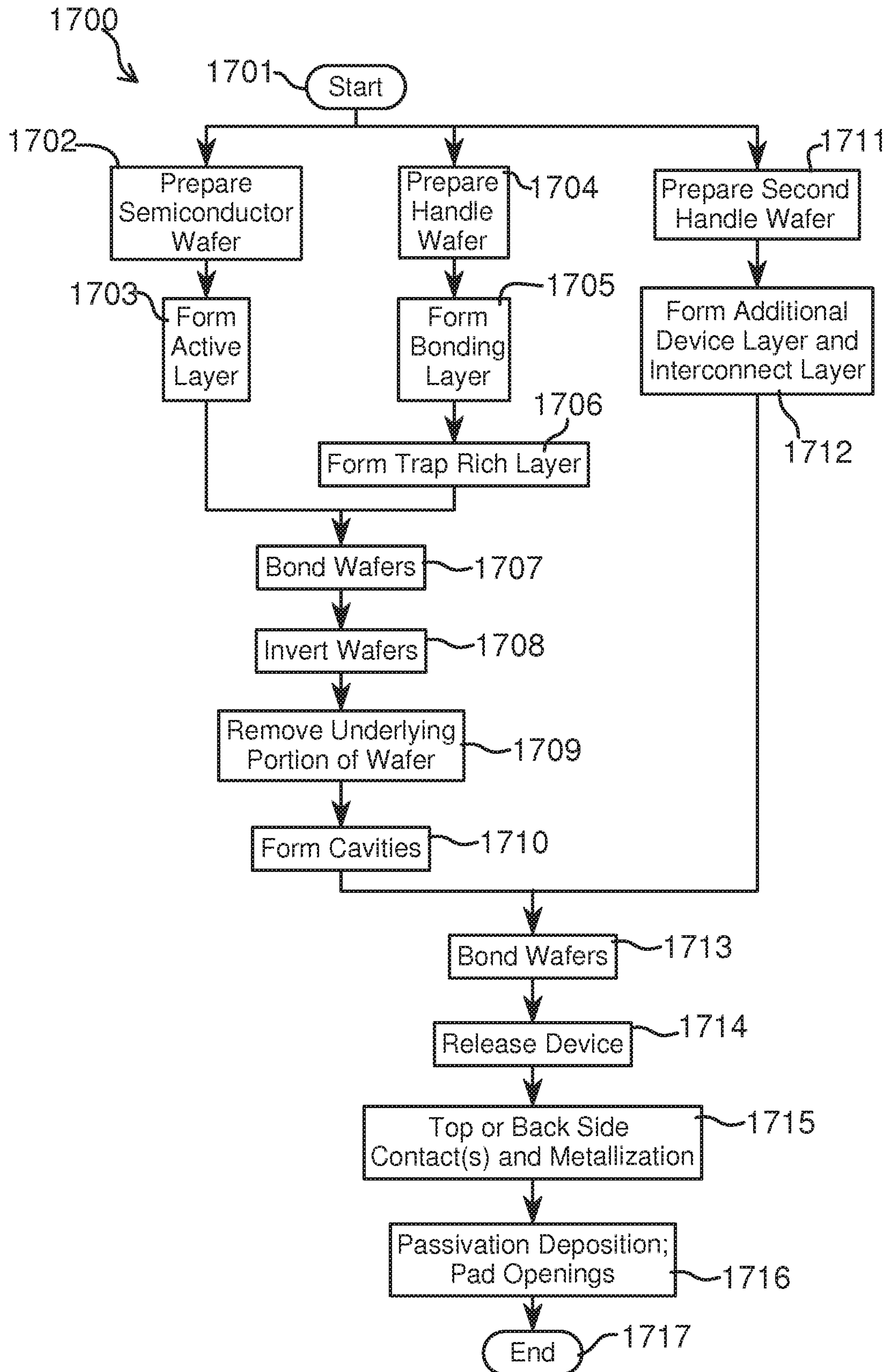


FIG. 17



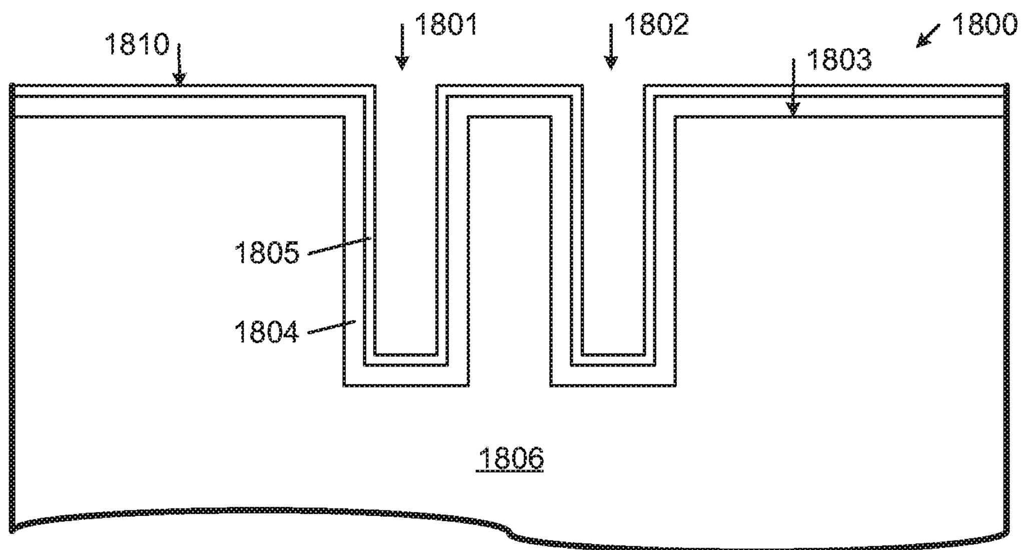


FIG. 18

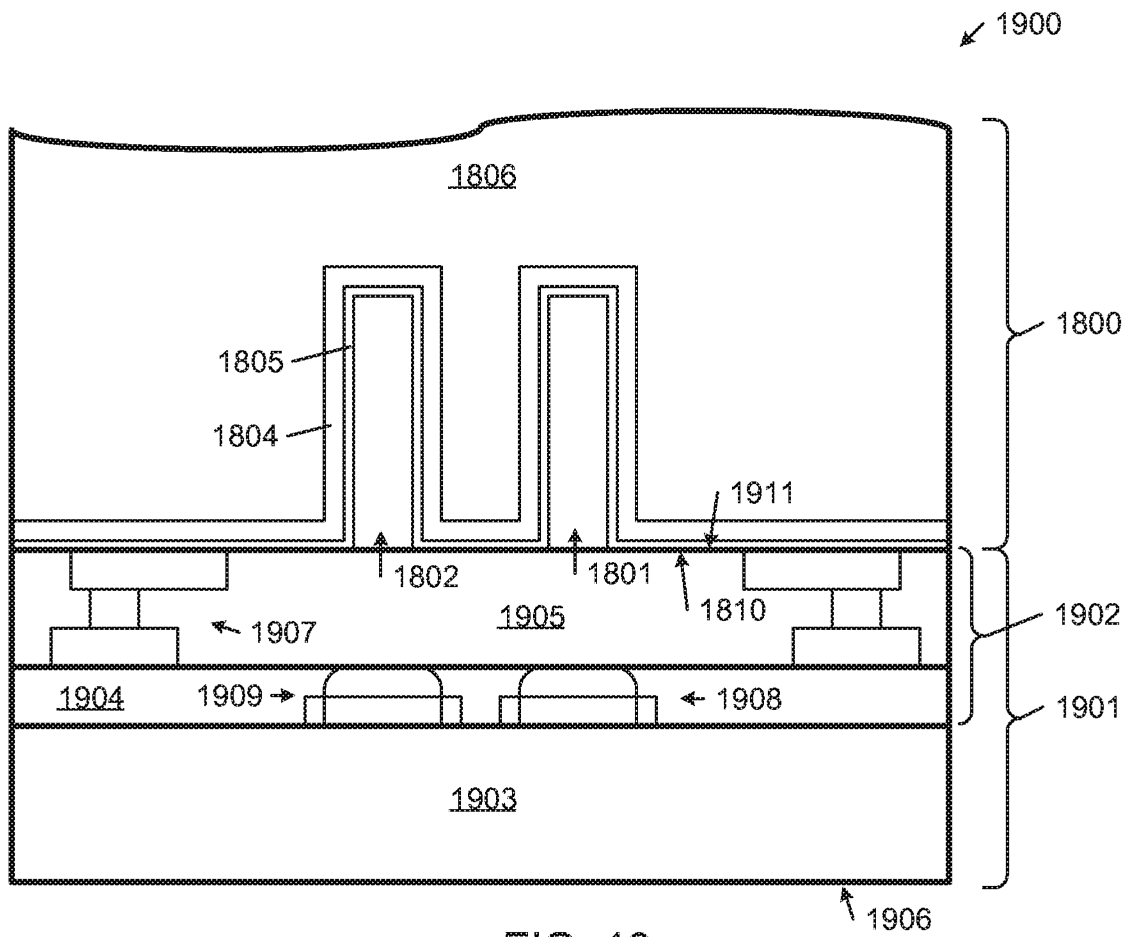


FIG. 19

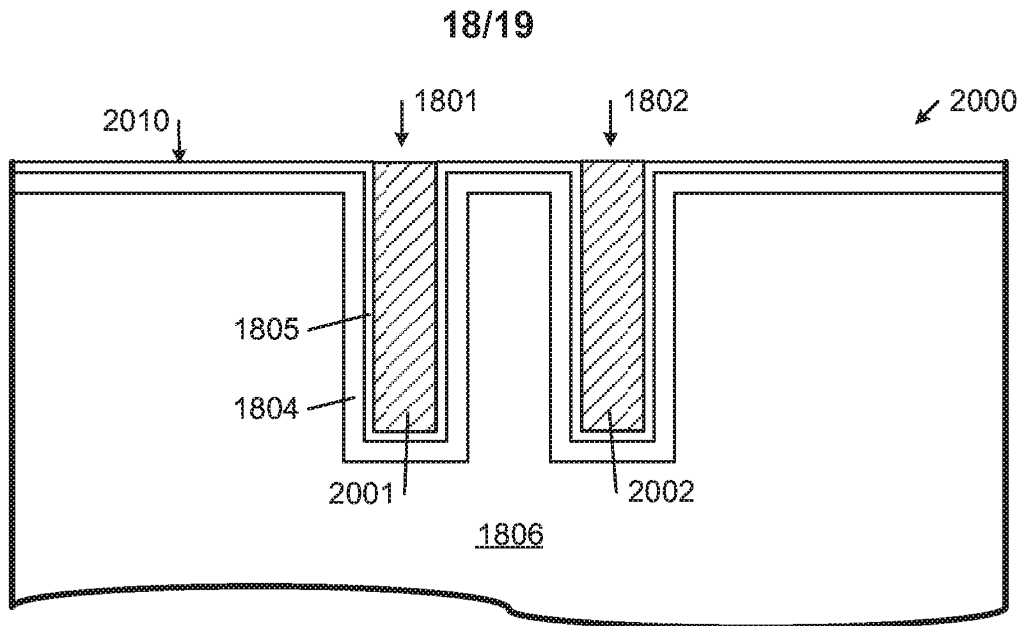


FIG. 20

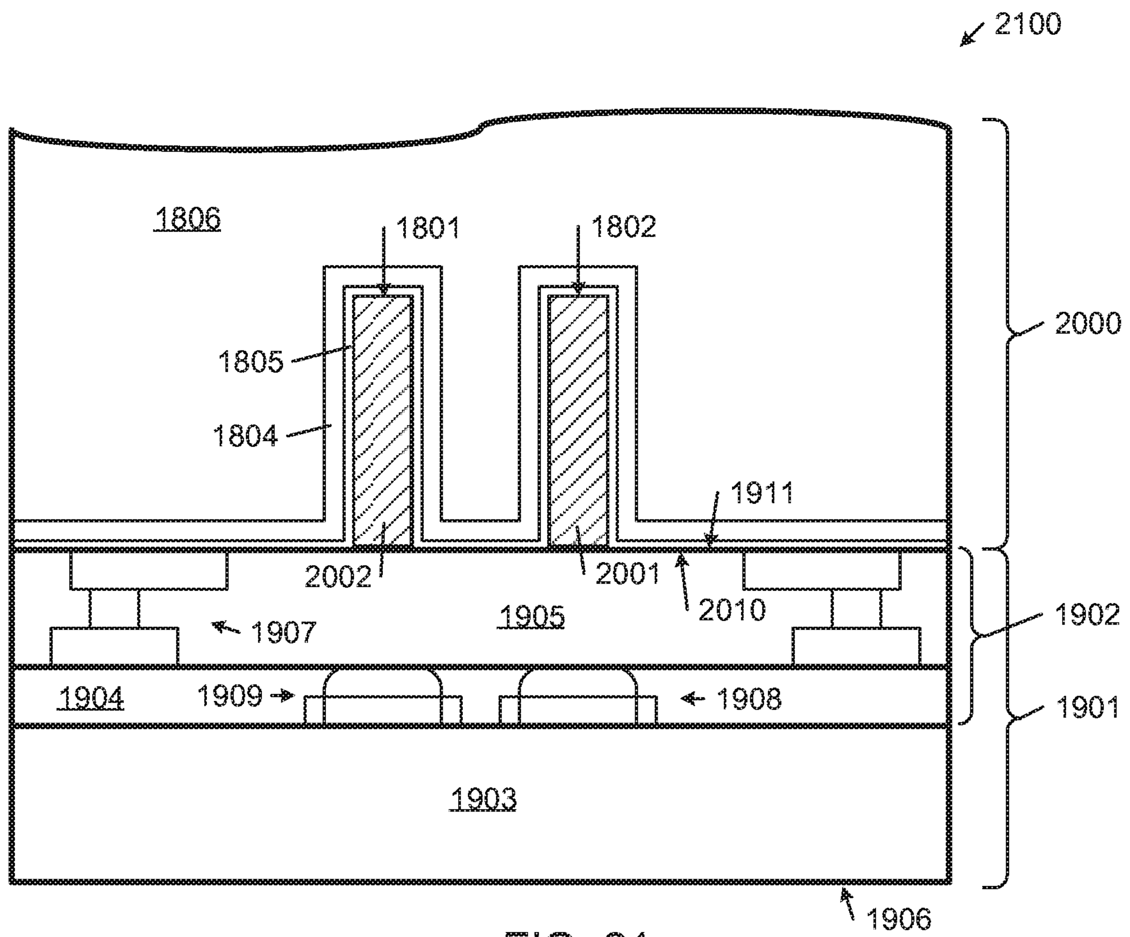


FIG. 21

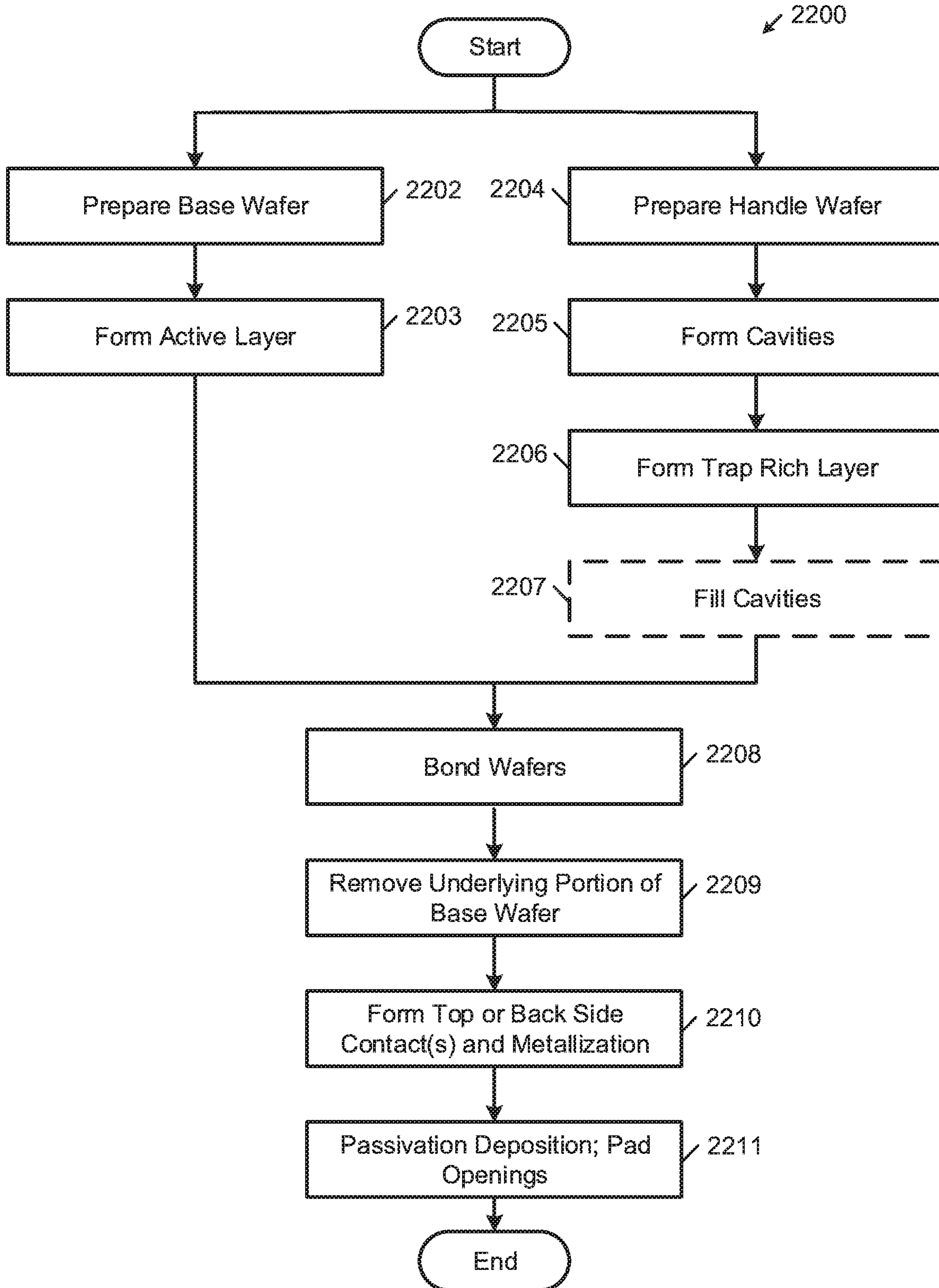


FIG. 22

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/019186

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/20 H01L21/84 H01L29/78 H01L27/12
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/084689 A1 (ARRIAGADA ANTON [US] ET AL) 4 April 2013 (2013-04-04) paragraphs [0006], [0029] - [0035], [0047], [0110], [0111], [0115]; figures 2-17 -----	1-20
A	US 2007/032040 A1 (LEDERER DIMITRI [BE]) 8 February 2007 (2007-02-08) paragraph [0117] - paragraph [0121]; figures 3,4 -----	1-20
A	US 2014/346622 A1 (STUBER MICHAEL A [US]) 27 November 2014 (2014-11-27) paragraphs [0110], [0111]; figures 9,10 -----	16-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
21 April 2016	03/05/2016

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1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/019186

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