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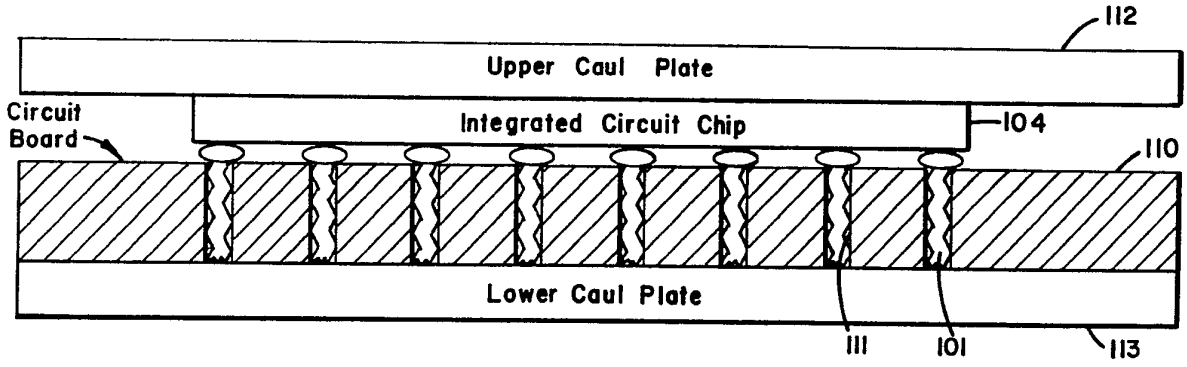

(57) Abstract

A method and apparatus for interconnecting electronic circuits using nearly pure soft annealed gold mechanically compressed within through-plated holes. The invention has its application in attaching integrated circuit dice (104) directly to circuit boards (110) by ball bonding gold wires (101) to the bonding pads of the integrated circuit dice in a substantially perpendicular relationship to the surfaces of the dice and inserting the gold leads into through-plated holes (111) of circuit boards (110) which provide an electrical and a mechanical connection once the leads are compressed within the through-plated holes. The present invention also finds its application in the interconnection of sandwiched circuit board assemblies where soft gold lead wires are inserted into axially aligned through-plated holes of the circuit boards and compressed so that the gold lead wires compress and buckle within the through-plated holes, forming an electrical connection between the circuit boards.

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FLYING LEADS FOR INTEGRATED CIRCUITS

TECHNICAL FIELD OF THE INVENTION

The present invention relates to the field of electrical circuit interconnect, and more specifically to a new apparatus and method for high-density packing and interconnect of integrated circuits on printed circuit (PC) boards and PC boards on PC boards.

BACKGROUND OF THE INVENTION

Integrated circuits are typically fabricated on wafers which are cut into individual integrated circuits and packaged within hermetically sealed ceramic or plastic packages. The signal and power lines from the integrated circuit are brought out to the pins of the package by means of leads attached to the bonding pads on the integrated circuit chips. The chips are then used to form larger circuits by interconnecting the integrated circuit packages by means of PC boards. The circuit boards contain interconnect lines or foils on the surfaces of the circuit boards or within planar layers. The circuit board is populated with integrated circuit packages which are soldered to plated via holes or on surface mounted pads on the circuit board. The soldering process forms an electrical and mechanical connection between the integrated circuit package and the circuit board.

To form larger circuits, circuit boards populated with integrated circuit packages are interconnected by a variety of connectors, jumper wires, or cables. The physical arrangement of the circuit boards in relation to one another is also accomplished in a

wide variety of configurations. One popular high-density interconnect technique is to stack the circuit boards in a sandwiched relationship to one another and electrically interconnect the circuit boards with inter-board connectors. This packing technique achieves a fair amount of packing density, limited by the inter-board spacing requirements of heat dissipation and connector spacing.

The aforementioned technique of forming larger circuits from individual integrated circuits using integrated circuit packages and circuit boards results in limited packing density of the actual area which is used for electrical circuits. The actual integrated circuit chips themselves are typically smaller than one-tenth of a square inch, and in total would cover only 10-20 percent of the board area. However, due to the inefficiencies of packaging of integrated circuit chips and connecting the integrated circuit chips to the circuit boards, it is difficult or impossible to increase the packing density on circuit boards to improve speed or spacing advantages. In addition, inter-board spacing is limited by the area consumed by the integrated circuit packages and inter-board connects. This limited packing density limits the inter-circuit signal speed due to the long propagation delays along the long interconnect lines.

The present invention provides a new apparatus and method for high-density interconnect of integrated circuit chips on circuit boards and between circuit boards which overcomes the wasted space and speed disadvantages of the prior art.

SUMMARY OF THE INVENTION

The present invention provides for placing unpackaged integrated circuit chips directly on circuit boards by using soft gold lead wires attached to the bonding pads to form the mechanical and electrical connection between the integrated circuit chips and the circuit boards. The present invention also provides for interconnection of sandwiched circuit boards by using soft gold jumper wires connected through the through-plated holes of the circuit boards.

Gold wires comprising nearly pure soft annealed gold are ball-bonded to the bonding pads of integrated circuit chips, and the soft gold wires are stretched to a substantially perpendicular position with respect to the surface of the integrated circuit chip, forming flying leads. The circuit boards to which the integrated circuit chips are to be attached are manufactured with plated holes having hole patterns substantially matching the bonding pad patterns of the integrated circuit chips. The integrated circuit chips with the flying leads are then positioned facing the circuit board and the flying leads are inserted through the plated holes such that the flying leads partially protrude from the circuit board. Caul plates are then positioned on the outer sides of this sandwich and pressed together so that the sticky or soft gold of the flying leads is compressed within the plated holes, causing the soft gold to deform against the surface of the plated holes and thereby forming a strong electrical and mechanical bond. The caul plates are then removed and the integrated circuit package remains firmly attached to the circuit board. This results in improved packing density of integrated circuit chips on circuit boards.

Gold wires comprising nearly pure soft annealed gold are inserted through axially aligned plated holes of two or more circuit boards in a substantially perpendicular direction to the planar surface of the boards. The gold wire is selected to be slightly longer than the distance through the axially aligned holes such that a portion of the wires protrude through one or both sides of the sandwich of circuit boards. Caul plates are then placed on the outer sides of the circuit board sandwich and pressed together so that the soft gold is compressed within the plated holes, causing the soft gold to deform against the inner surface of the plated holes to form an electrical connection between the circuit boards.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, where like numerals identify like components throughout the several views,

FIG. 1 is a side view of an integrated circuit die onto which flying gold leads are ball bonded and straightened by a ball bonding machine.

FIG. 2 shows the six steps that the flying lead ball bonder performs in order to attach a flying lead to an integrated circuit die.

FIG. 3 shows the bonding pad pattern on a typical integrated circuit along with the corresponding plated hole pattern on a circuit board which mates the integrated circuit chip to the circuit board.

FIG. 4 shows the relative positions of the integrated circuit chip and the circuit board prior to compression of the flying leads into the plated holes.

FIG. 4a is a closeup view of a single ball-bonded flying lead prior to compression within the

plated hole of the circuit board.

FIG. 5 shows the relative positions of the integrated circuit chip and the circuit board after the flying leads have been compressed inside the plated holes of the circuit board.

FIG. 5a is a closeup view of a ball-bonded flying lead that has been compressed into a plated hole on the circuit board.

FIG. 6 is a larger view of the compression process whereby a plurality of integrated circuit chips having flying leads are attached to a single printed circuit board through the application of seating force on caul plates which sandwich the circuit board/chip combination.

FIG. 7 is a plated hole pattern for a typical PC board onto which integrated circuit dice are attached in the preferred embodiment of the present invention.

FIG. 8 is a module assembly onto which a plurality of circuit boards populated with integrated circuit chips are placed.

FIG. 9 is a side view of the module assembly of Fig. 8 showing the details of the logic jumpers and power jumpers for logic and power interconnection between the sandwich assembly of printed circuit boards.

FIG. 10 is closeup view of a single logic jumper that has been compressed within the axially aligned plated holes of the sandwiched printed circuit boards of the module assembly of Fig. 9.

FIG. 11 shows the first two steps of the pressing operation for compressing the logic jumpers in a single stack assembly of PC boards on a module assembly.

FIG. 12 shows the second two steps of the compression of the logic jumpers on a single stack

assembly of four printed circuit boards on a module assembly.

FIG. 13 shows the method of compressing the power jumpers through the assembly of stacked printed circuit boards.

FIG. 14 shows the compression of the gold posts between the power plates and the power blades of the module assembly.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the present invention relates to the high-density packing of silicon or gallium arsenide (GaAs) integrated circuit chips on single-layer or multi-layer interconnect printed circuit boards with plated-through via holes and the high-density packing of circuit boards in a sandwiched arrangement. The application of this technology is designed for speed improvements, improved heat dissipation, and improved packing density required for modern supercomputers such as the Cray-3 manufactured by the assignee of the present invention.

The placing of the integrated circuit chips or dice directly on the circuit boards eliminates the bulky packaging normally found on integrated circuits and typically referred to as DIPs (dual inline packages), SIPs (single inline packages), SMDs (surface mount devices), leadless chip carriers, and the like. All of the aforementioned packages consume valuable circuit board real estate and in turn cause increased propagation delay between active circuits due to long signal paths. In addition, the aforementioned circuits present heat dissipation barriers which vary with the thermal

conductivity of the packaging material. By removing the chips from the packages and placing them directly on the circuit boards, the integrated circuit chips or dice can be surrounded by liquid coolant to improve cooling.

Flying Lead Construction

FIG. 1 shows the preferred embodiment for attaching the flying gold leads to the silicon or gallium arsenide packaged chip or die before attaching the die to the circuit board. The leads are made of soft gold wire which is approximately 3 mils in diameter. The GaAs chips used in the preferred embodiment contain 52 bonding pads which have a sputtered soft gold finish. The objective of the die bonding operation is to form a gold-to-gold bond between the wire and the pad. A Hughes automatic thermosonic (gold wire) ball bonding machine Model 2460-II is modified in the preferred embodiment to perform this operation, and is available from Hughes Tool Company, Los Angeles, California. This machine was designed and normally used to make pad-to-lead frame connections in IC packages and has been modified to perform the steps of flying lead bonding as described below. The modifications include hardware and software changes to allow feeding, flaming off, bonding and breaking heavy gauge gold bonding wire (up to 0.0030 dia. Au wire).

The Hughes automatic ball bonding machine has an X-Y positioning bed which is used to position the die for bonding. The die is loaded on the bed in a heated vacuum fixture which holds up to 16 dice. The Hughes bonding machine is equipped with a vision system which can recognize the die patterns without human intervention and position each bonding pad for processing. An

angular correction as well as an X-Y position is available to the machine.

The soft gold wire that is used for the flying leads in the preferred embodiment of the present invention is sometimes referred to as sticky gold or tacky gold. This gold bonding wire is formed from a 99.99% high-purity annealed gold. The process of annealing the high-purity gold results in a high elongation (20-25% stabilized and annealed), low tensile strength (3.0 mil., 50 gr. min.) gold wire which is dead soft. The wire composition (99.99% pure Au non-Beryllium doped) is as follows:

Gold	99.990% min.
Beryllium	0.002% max.
Copper	0.004% max.
Other Impurities (each)	0.003% max.
Total All Impurities	0.010% max.

This type of gold is available from Hydrostatics (HTX grade) or equivalent.

Referring to FIG. 1, the flying lead die bonding procedure begins with the forming of a soft gold ball at the tip of the gold wire. The wire is fed from a supply spool (not shown) through a nitrogen-filled tube 109 (shown in FIG. 2) to a ceramic capillary 100. The inside of the capillary is just slightly larger than the wire diameter. The nitrogen in the connecting tube 109 can be driven either toward the capillary or away from the capillary toward the supply spool. This allows the gold wire to be fed or withdrawn from the capillary tip.

The gold ball 106 formed at the end of the gold wire 101 is thermosonically bonded to bonding pad

105 of chip 104. The capillary tip 102 of capillary 100 is capable of heating the ball bond to 300°C concurrent with pressing the ball 106 onto the pad 105 and sonically vibrating the connection until a strong electrical and mechanical connection is formed. The capillary 100 is then withdrawn from the surface of the die 104 and the wire 101 is extruded from the tip 102. A notching mechanism, added to the Hughes ball bonder to perform the specific notching operation described herein, is used to make a notch 107 at the appropriate height of the flying lead to break the connection and to stiffen the lead. Wire clamp 108 grasps the gold wire 101 and the capillary is withdrawn upward, breaking the flying lead at 107 and concurrently performing a nondestructive test of the ball bond to bonding pad connection.

The sequence of steps required to make a flying lead bond to the package die is shown in FIG. 2. Step 1 begins with the feeding of a predetermined amount of wire through the capillary 100. A mechanical arm then positions an electrode 114 below the capillary tip 102 and a high-voltage electrical current forms an arc which melts the wire and forms a gold ball with a diameter of approximately 6 mils. This is termed electrostatic flame-off (EFO). Specified ball size range is attainable through EFO power supply output adjustment up to 10 milliamps. During this step, the clamps 108 are closed and the nitrogen drag is off. This action occurs above the surface of the integrated circuit chip so as to avoid any damage to the chip during the EFO ball forming process.

In step 2, the nitrogen drag 109 withdraws the supply wire 101 into the capillary 100 and tightens the ball against the capillary tip 102.

The capillary tip 102 is heated to 200°C

(range of ambient to 300°C) to assist in keeping the gold wire 101 in a malleable state. The die fixture is also heated to 200°C (range of ambient to 300°C) to avoid wire cooling during the bonding process. The die fixture is made of Teflon-coated aluminum. As shown in FIG. 1, a vacuum cavity or vacuum plate 103 holds the die 104 in position on the fixture during the bonding process.

In step 3, the bonding machine lowers the capillary 100 to the surface of a bonding pad 105 and applies high pressure (range of 30-250 grams) to the trapped gold ball 106 along with ultrasonic vibration at the capillary tip 102. The capillary tip 102 is flat, with a 4-mil inside diameter and an 8-mil outside diameter. The ball 106 is flattened to about a 3-mil height and a 6-mil diameter. Ultrasound is driven through the ceramic capillary 100 to vibrate the gold ball 106 and scrub the bonding pad surface. The sound is oriented so that the gold ball 106 moves parallel to the die surface. The Hughes ball bonding machine has the ability to vary the touch-down velocity, i.e., soft touch-down for bonding GaAs, which is program selectable. The ultrasonic application is also program selectable.

In step 4, the capillary 100 is withdrawn from the die surface 104, extending the gold wire 101 as the head is raised. The nitrogen drag is left off and the capillary is raised to a height to allow enough gold wire to form the flying lead, a tail length for the next flying lead, and a small amount of clearance between the tail length and the capillary tip 102. The Hughes ball bonder device is capable of selecting the height that the capillary tip can move up to a height of approximately 0.750 inch.

In step 5, an automatic notching mechanism 115 moves into the area of the extended gold wire 101 and strikes both sides of the wire with steel blades. This is essentially a scissor action which cuts most of the way through the gold wire 101, forming a notch 107. The notch 107 is made 27 mils above the surface of the die. The notching mechanism has been added to the Hughes ball bonder for the precise termination of the flying leads. The Hughes ball bonder has been modified to measure and display the notch mechanism height. The activation signal for the notch mechanism is provided by the Hughes ball bonder system for the proper activation during the sequence of ball bonding. The flying lead length is adjustable from between 0.0 mils to 50.0 mils. It will be appreciated by those skilled in the art that the notching function can be accomplished with a variety of mechanisms such the scissor mechanism disclosed above, a hammer-anvil system, and a variety of other mechanisms that merely notch or completely sever the wire 101.

In step 6, clamp 108 closes on the gold wire 101 above the capillary 100 and the head is withdrawn until the gold wire breaks at the notched point. This stretching process serves several useful purposes. Primarily, the gold wire is straightened by the stretching force and stands perpendicular to the die surface. In addition, the bond is non-destructively pull-tested for adhesion at the bonding pad. The lead 101 is terminated at a 27-mil height above the die surface 104 in the preferred embodiment. At the end of step 6, the capillary head for the bonding mechanism is positioned over a new bonding pad and the process of steps 1-6 begin again. The bonding wire 101 is partially retracted into the capillary once again, and the

clamps are closed, as shown in step 1, so that a new ball may be formed by the EFO.

The die positions are roughly determined by the loading positions in the vacuum fixture. The Hughes automatic bonding machine is able to adjust the X-Y table for proper bonding position of the individual die. An angular correction is automatically made to adjust for tolerance in placing the die in the vacuum fixture. This is done through a vision system which recognizes the die pad configurations. Using the modified Hughes automatic bonding machine with the current bonding technique, a minimum bonding rate of 2 die pads per second is possible.

Circuit Board Construction

Once the gold bonding leads are attached to the integrated circuit chip or die, the die is ready to be attached to the circuit board. As shown in FIG. 3, the bonding pattern of the integrated circuit die 104 matches the plated hole pattern on the circuit board 110. For example, the top view of integrated circuit die 104 in FIG. 3 shows the bonding pad 105 in the upper right corner. The circuit board 110 shown in FIG. 3 shows a corresponding plated hole 111 which is aligned to receive the bonding lead from bonding pad 105 when circuit board 110 is placed over integrated circuit 104 and the flying leads are inserted into the hole pattern on the circuit board. Thus, each bonding pad of integrated circuit 104 has a corresponding plated hole on circuit board 110 aligned to receive the flying leads.

The circuit board assembly operation begins with the die insertion in the circuit board. The cir-

cuit board is held in a vacuum fixture during the insertion process. This is to make sure that the board remains flat. Insertion can be done by hand under a binocular microscope or production assembly can be done with a pick-and-place machine.

Referring to FIG. 4, the circuit board 110 with the loosely placed die 104 is mounted on an aluminum vacuum caul plate (lower caul plate) 113. Steel guide pins (not shown) are placed in corner holes of the circuit board to prevent board motion during the assembly operation. A second (upper) caul plate 112 is then placed on the top side of the circuit board populated with chips to press against the tops (non-pad side) of the chips 104. The sandwich assembly comprising the circuit circuit board, the chip and the caul plates is then placed in a press and pressure is applied to buckle and expand the gold leads 101 in the plated holes 111 of the circuit board.

The side view of the sandwiched circuit board 110, integrated circuit chip 104, and caul plates 112 and 113 in FIGS. 4 and 5 illustrates the position of the gold leads 101 before and after the pressing operation, respectively. In the preferred embodiment there is a 7-mil exposure of gold lead 101 which upon compression will buckle and expand into the plated hole 111 of the circuit board 110. The 3-mil diameter wire 101 in a 5-mil diameter hole 111 means the initial fill is 36 percent of the available volume. After pressing, the fill has increased to 51 percent as a result of the 7-mil shortening of the gold lead 101. As shown in greater detail in FIGS. 4a and 4b, The lead typically buckles in two or more places, and these corners are driven into the sides of the plated hole 111 of the circuit board. The assembly is completed in one pressing

operation. The circuit board 110 can now be removed from the press with the integrated circuit chip 104 securely attached and electrically bonded to the plated holes of the circuit board.

FIG. 6 shows a broader view of the circuit board press which is used to attach the integrated circuits to the printed circuit board. The upper caul plate 112 is a Teflon-coated seating caul plate which is aligned through alignment pins 114 with the circuit board 110 and the lower caul plate 113 which is vacuum caul plate to hold the circuit board flat during the pressing process. The alignment pins 114 are used to prevent the printed circuit board 110 from sliding or otherwise moving during the pressing process. A seating force is applied to the top of upper caul plate 112 which forces the excess flying lead material into the plated holes of printed circuit board 110. Thus, integrated circuits 104 are mechanically and electrically bonded to printed circuit board 110.

It will be appreciated by those skilled in the art that many variations of the above-described pressing operation can be used which results in the same or equivalent connection of the flying leads to the PC boards. For example, the flying leads of the chips could be completely inserted into the through-plated holes of the PC board prior to the pressing operation with the excess gold leads protruding out the opposite side. The first caul plate could then be used to hold the chip onto the PC board while the second caul plate is used to compress the leads into the holes.

Module Assembly Construction

A sandwiched assembly of printed circuit boards populated with integrated circuit chips is interconnected using a technique similar to that used in bonding the integrated circuit chips to the circuit boards. As is more fully described below, soft gold wires are inserted through axially aligned plated holes between layered circuit boards which are compressed using caul plates to partially fill the plated holes with the soft gold wires to form an electrical connection substantially perpendicular to the planar surfaces of the printed circuit boards.

FIG. 7 is an example of a printed circuit board hole pattern for the type of circuit boards used in the Cray-3 computer manufactured by the assignee of the present invention. In the preferred embodiment of the present invention, each circuit board provides 16 plated hole patterns for the acceptance of 16 integrated circuits having flying leads. The 16 integrated circuits are attached to each of the circuit boards of the type found in FIG. 7 through the pressing process previously described for circuit board assembly. Caul plates of a size slightly larger than the circuit boards of the type shown in FIG. 7 are used during the pressing process to attach the integrated circuit chips to the circuit boards. Each plated hole pattern on circuit board 110 of FIG. 7 corresponds to the hole pattern disclosed in FIG. 3. Each corner of circuit board 110 includes four plated via holes which are used to distribute power and are used for alignment during the pressing operation.

In the preferred embodiment of the present invention, 16 of the circuit boards 110 shown in FIG. 7 are arranged in a module assembly 200 of the type shown

in FIG. 8. The circuit boards 110 are arranged in a 4 x 4 matrix on each level of the module. There are four levels of the module in which circuit boards are stacked, thus created an X-Y-Z matrix of 4 x 4 x 4 circuit boards. This results in 64 circuit boards for each module assembly 200 which in turn results in 1,024 integrated circuit chips per module assembly.

A module assembly is 4.76 inches wide, 4.22 inches long, and 0.244 inch thick. A top view of a module assembly is shown in FIG. 8. At one edge of the module assembly are four power blades 201a-201d. These machined metal blades are both the mechanical connection to the cabinet into which the module assemblies are placed and the electrical connection to the power supplies. At an opposite edge of the module assembly are 8 signal edge connectors 202a-202h. These connectors form the communication paths to the other module assemblies within the machine.

Electrical communication between the integrated circuit chips of each board 110 is accomplished by means of the prefabricated foil patterns on the surface and buried within each circuit board. The electrical communication between circuit boards 110 is between two logic plates sandwiched in the center of the module assembly. Communication between the circuit boards and the logic plates is through gold post jumpers along the Z-axis direction perpendicular to the planar surface of the circuit boards and the module assembly. The z-axis jumper wires are used for distribution of electrical communication signals and power distribution. The Z-axis jumpers are placed in any of the area on circuit boards 110 that is not occupied by an integrated circuit.

Due to the amount of force required to

compress the jumpers along the Z-axis of the module assembly, the jumpers are compressed for a 4-board stack at one of the 16 locations on the module 200 at a single time. The order in which the circuit boards are compressed is shown in FIG. 8 in the lower left corner of each circuit board stack 110. Sixteen separate pressings are performed to compress the gold Z-axis jumpers for one module 200.

FIG. 9 shows a side sectional view of a module assembly. The assembly 200 is constructed as a sandwich comprising four layers of circuit boards, two layers of circuit board interconnect layers, and several layers of support framing material. FIG. 9 depicts a completely assembled module assembly with the exception of the single edge connectors, which have been omitted for purposes of this discussion. The assembly 200 in application is stacked with other assemblies in a fluid cooling tank and positioned so that the planar surface of the module assembly is stacked in a vertical direction. Thus, in application, the view of the circuit board assembly 200 of FIG. 9 is actually a top-down look at the module in application. A type of cooling apparatus suitable for cooling the circuit board module assemblies of the present invention is described in U. S. Patent No. 4,590,538 assigned to the assignee of the present invention and incorporated herein by reference.

Eight cooling channels 230 are provided at the outer sections of the module assembly to allow the vertical rise of cooling fluid through the module assembly to remove the excess heat produced by the integrated circuits in operation. Heat transfer occurs between circuit boards 1 and 4 (levels 212 and 221 respectively) and the fluid passing through channels 230. There is also heat transfer from the ends of logic jumpers 231 to

the passing fluid in channels 230. The latter is the primary heat transfer vehicle from circuit boards 2 and 3 (levels 215 and 218, respectively). The power plates at levels 210 and 223 are spaced from the board stacks to form the fluid channels. Spacing is accomplished with acrylic strips 203 which are held in place by the power jumpers 232.

The module assembly 200 as shown in FIG. 9 depicts one of the four power blades 201 shown to the left. The outer plates shown as layers 210 and 223 are power distribution plates which connect to the four power blades and are used to distribute electrical power throughout the module for powering the integrated circuits. The connection between the integrated circuits and the power plates is by Z-axis power jumpers which are described in more detail below.

As was previously described, each module assembly consists of 16 board stacks. Each board stack consists of four circuit boards. The side edge view of the module assembly shown in FIG. 9 shows four board stacks exposed in a cut-away view. The four circuit board levels are labeled Nos. 212, 214, 219 and 221. Electrical communication between these boards is via two logic plates labeled 216 and 217. These plates are in the center of the module assembly and divide the board stacks in half. Communication between circuit boards 212, 214, 219 and 221 and logic plates 216 and 217 is via gold post jumpers or logic jumpers 231 in the Z-axis direction (relative to the X-Y axes lying on the planar surface of the circuit boards and logic plates). The logic plates as well as the circuit boards contain electrical interconnecting plated wiring patterns in the X-Y direction, and the Z-direction interconnect is thus performed by the logic jumpers.

The integrated circuits 104 are shown in FIG. 9 as the rectangles at levels 213, 215, 218 and 220. The flying leads from these integrated circuits are attached to circuit boards 212. 214, 219 and 221 respectively. Thus, the circuit board assembly of 212 with integrated circuits at level 213 are assumed to have been previously assembled with the aforementioned flying lead attachment of integrated circuits to circuit boards. The spaces between the integrated circuits at levels 213, 215, 218 and 220 contain through-plated holes which are axially aligned in the Z-axis direction and allow the gold post logic jumpers 231 to pass through the various levels of the module. The spaces between the integrated circuits on levels 213, 215, 218 and 220 are filled with a die frame which also contains corresponding axially aligned holes. This is a clear acrylic plate or block the size of the circuit boards approximately 10 mils thick. There are relief areas in the die frame for the integrated circuit packages and for the gold post jumpers which pass through the board stacks and through the die frames. The purpose of the die frame is to provide mechanical support for the circuit boards and for the gold post jumpers.

The jumpers are forced through the board stack under high pressure to interconnect all of the axially aligned through-plated holes on the circuit boards and on the logic plates. The gold jumpers 231 are made of the same soft gold used in the flying lead connection of the integrated circuit packages to the circuit boards described above. The soft gold jumpers are compressed through the axially aligned plated holes to form electrical connections in the Z-axis direction. The die frame prevents the soft gold of the jumper from escaping into the areas between the circuit boards adjacent the

integrated circuits.

Jumpers 231 in FIG. 9 are similar to the power jumpers 232 also shown in FIG. 9. The power jumpers 232 extend farther than the logic jumpers 231, since they need to connect to power plates 210 and 223 to supply power to the circuit boards.

FIG. 10 shows a closeup view of a single logic jumper through the various levels of assembly 200. This cross-sectional view of FIG. 10 is not drawn to scale and is offered as an illustration of how the gold leads are compressed within the plated holes of both the circuit boards and the logic plates. Spacers are used at levels 213, 215, 218 and 220 to prevent the gold jumper leads from expanding into the spaces between the circuit boards. Buried plated interconnect or surface interconnect on circuit boards and logic plates form the interconnection between the logic jumpers and the plated holes for the flying leads of integrated circuits. Logic or electrical communication between integrated circuits and the outside world is achieved therefrom. It will be appreciated by those skilled in the art that power jumpers will appear similar to the logic jumpers shown in FIG. 10, except that the power jumpers extend into the power plates of the assembly 200 and are somewhat larger in diameter.

Gold Post Jumper Installation

The module is assembled in two steps. The first step combines the circuit board stacks with the logic plates. This step is repeated 16 times for a module (once for each board stack). The second step connects the power plates and the module power blades. Both steps are described below.

The board stacks are assembled to the logic plates in two pressing operations. These pressing operations are shown in FIGS. 11 and 12. The pressing operation shown in FIGS. 13 and 14 presses the power jumpers through the assembly to form the necessary interconnect between the circuit board and logic plate layers and the power plate levels.

The four circuit boards, the four die frames, and the two logic plates are stacked on a metal caul plate with guide pins through the corner power jumper holes as shown from the side view of FIG. 11. This is in preparation for the first pressing operation. There is an assembly die frame spacer on the lower caul plate before the first circuit board. There is another assembly die frame spacer on the top of the stack just below the stamp caul plate, which is removed before the first pressing.

Soft gold post jumpers are then loaded into the stack in the positions where the jumpers are desired. These gold posts are in the preferred embodiment 5 mils in diameter and 192 mils long. The top assembly die frame spacer is removed and is replaced with the stamp caul plate. The assembly is then placed in a press and the jumpers are compressed such that the exposed 10 mils of the logic jumpers are compressed into the stack assembly. In this pressing operation, the 10 mils of the exposed gold post at the top of the stack assembly are compressed into the assembly and the gold posts expand in the jumper cavity to a nearly 100 percent fill. Excess gold is forced into a nail head configuration on the top of the outside circuit board. The assembly in FIG. 11 shows the stamp caul plate on the outer surface of circuit board 4 with the top assembly die frame spacer removed.

The pressing operations shown in FIGS. 11 and 12 are accomplished using levelers on the outer surfaces of the logic plates to ensure an even pressing operation. The guide pins are placed at various points through the power jumper holes along the logic plates to ensure that the circuit boards and logic plates do not move during the pressing operation.

FIG. 12 shows the second pressing operation. The board stack shown in FIG. 11 is turned over with the caul plates reversed. In the second pressing operation, the top assembly die frame spacer on the top side of the stack is now removed and another press cycle occurs, pressing the remaining 10 mils of the exposed jumper into the stack. The reason for the two-sided pressing operation is that the soft gold binds sufficiently in the jumper cavity so that it is not possible to make a reliable connection through the entire stack from one side only. The number of pressing operations of course would vary with the number of levels in the sandwiched assembly. In smaller (thinner) assemblies, one-sided pressing is possible.

With board stacks having a larger number of levels of circuit boards, logic plates and chips, longer logic jumpers and power jumpers may be used to interconnect along the Z-axis, however, more pressing operations may be required. For example, in an alternate embodiment of the present invention, four pressing operations may be required for logic jumpers. The first pressing operation would be similar to that shown in FIG. 11, except that two 10-mil spacers would be placed at the bottom of the board stack and two 10-mils spacers placed at the top of the board stack. The first pressing operation would press 10 mils of the logic jumpers into the board stack after the removal of the top spacer.

The second step would start with the removal of the second spacer on the top, and a second pressing operation would occur. The third pressing operation would begin with the board stack flipped over and the top 10-mil spacer removed for the third pressing step. The last pressing step would begin with the removal of the final 10-mil spacer and a final pressing operation would begin. In this application, 20 mils of exposed gold jumper could be pressed into a thicker board stack.

Power plates and module power blades are added to the partial module assembly in a manner similar to the pressing operation for the individual circuit board stacks. In this case, instead of a stamp caul plate of approximately the size of a single circuit board, caul plates the size of the entire assembly are used to press all of the power jumpers on the entire module assembly, as shown in FIG. 13. The power jumpers are loaded-and pressed in a four-step cycle as described above for the logic jumpers of a single circuit board stack assembly. The gold posts for this power jumper pressing operation are 14 mils in diameter and 284 mils long. The module power blades are attached as a last step by pressing gold posts or aluminum posts into cavities in the machined power blades, as shown in the final step of FIG. 14.

Those of ordinary skill in the art will recognize that other types of lead bonding processes may be substituted for the ball bonding process for flying leads described herein. Also, other types of malleable electrically conductive metals may be used in place of the soft gold described herein. In addition, the pressing process causing the gold to expand or buckle within the plated holes may be performed without having the gold leads protrude from the circuit board.

Compression fingers could be axially aligned with the plated holes in order to compress the gold leads within the plated holes without having the leads protruding before the process is begun.

While the present invention has described connection with the preferred embodiment thereof, it will be understood that many modifications will be readily apparent to those of ordinary skill in the art, and this application is intended to cover any adaptations or variations thereof. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

WHAT IS CLAIMED IS:

1. A method of electrically interconnecting electronic circuit assemblies comprising the steps of:

(a) inserting a conductive lead connected from a first assembly into a plated hole of a second assembly; and

(b) compressing the lead within the plated hole so that the lead contacts the interior surface of the plated hole and forms and electrical connection from the first assembly to the second assembly.

2. An interconnection apparatus comprising a conductive lead electrically connected to a first electronic assembly and mechanically compressed within a plated hole of a second electronic assembly so that the conductive lead contacts the interior surface of said plated hole and forms an electrical connection therebetween.

3. The apparatus according to claim 2 wherein both the first electronic assembly and the second electronic assembly are circuit boards and the conductive lead is further mechanically compressed within a plated hole of the first electronic assembly so that the conductive lead contacts the interior surface of said plated hole in said first electronic assembly and forms an electrical connection therebetween.

4. The apparatus according to claim 2 wherein the

first electronic assembly is an integrated circuit chip, the second electronic assembly is a circuit board, and the conductive lead is electrically connected to the bonding pad of the integrated circuit of the first electronic assembly.

5. A method of electrically and mechanically attaching integrated circuit chips to circuit boards comprising the steps of:

(a) bonding soft gold wires to the bonding pads of integrated circuit chips;

(b) inserting the soft gold wires into plated holes of the circuit boards; and

(c) compressing the soft gold wires within the plated holes of the circuit board so that the soft gold deforms enough to contact the plated holes.

6. A method of electrically and mechanically attaching integrated circuit chips to circuit boards, comprising the steps of:

(a) bonding soft gold wires to the bonding pads of integrated circuit chips so that the resulting bonded wires are substantially straight and perpendicular to the planar surface of the integrated circuit chips;

(b) inserting the substantially straight bonded wires into through-plated holes of the circuit board so that the bonded wires protrude through the other side of the through-plated holes of the circuit board; and

(c) compressing the bonded wires within the

through-plated holes of the circuit board so that the soft gold wires deform enough to contact the plated holes.

7. The method according to claim 6 wherein step (c) further comprises the substeps of:

(c)(i) holding the integrated circuit chip against the circuit board;

(c)(ii) positioning a caul plate against the protruding wires on the opposite side of the circuit board; and

(c)(iii) compressing the integrated circuit chip, the circuit board and the caul plate together so that the soft gold wires deform within the through-plated holes of the circuit board forming electrical connections rigid enough to hold the integrated circuit chip onto the circuit board.

8. The method according to claim 6 wherein step (c) further comprises the steps of:

(c)(i) holding the circuit board against a first caul plate;

(c)(ii) positioning a second caul plate against the back side of the integrated circuit chip; and

(c)(iii) compressing the integrated circuit chip, the circuit board, and the caul plates together so that the soft gold wires deform within the through-plated holes of the circuit board forming electrical con-

nections rigid enough to hold the integrated circuit chip onto the circuit board.

9. A method of attaching an integrated circuit chip to a circuit board, comprising the steps of:

(a) ball-bonding soft gold wires to the bonding pads of the integrated circuit chip;

(b) stretching the soft gold wires to a substantially perpendicular position with respect to the surface of the integrated circuit chip;

(c) manufacturing a circuit board with plated holes having a hole pattern substantially matching the bonding pad pattern of the integrated circuit chip;

(d) positioning the integrated circuit chip in relation to the circuit board so that the bonded gold wires of the integrated circuit are aligned with the plated holes of the circuit board;

(e) pressing the integrated circuit chip against the circuit board so that the bonded wires of the integrated circuit chip are inserted into the aligned plated holes of the circuit board;

(f) positioning a first caul plate to the back side of the integrated circuit chip and positioning a second caul plate to the back side of the circuit board; and

(g) pressing the caul plates together so that the soft gold wires of the integrated circuit chip are compressed into the plated holes of the circuit board, forming a rigid electrical and mechanical bond.

10. A method of attaching flying leads to integrated circuit chips, comprising the steps of:

(a) forming a gold ball on the end of a gold lead by rapidly heating the end of the lead;

(b) pressing the gold ball against the bonding pad of an integrated circuit chip so that the gold lead forms an electrical and mechanical bond to the bonding pad to the integrated circuit chip;

(c) notching the gold lead at a height above the gold ball; and

(d) stretching the gold lead so that it breaks at the notched position and straightens the gold lead forming a flying lead.

11. The method according to claim 10 wherein step (b) further includes the substeps of:

(b)(i) heating the integrated circuit chip;

(b)(ii) heating the gold ball of the gold lead to a temperature approximately matching that of the heated aperture of the integrated circuit chip; and

(b)(iii) pressing the ball end of the gold lead against the bonding pad of the integrated circuit chip and applying sonic energy to the point of connection so that the metal surfaces are scrubbed to aid in forming the connection.

12. The method according to claim 10 wherein notching the gold lead results in a gold lead that is not severed.

13. The method according to claim 10 wherein notching results in a severed gold lead.

14. A method of electrically connecting electronic circuit assemblies comprising the steps of:

(a) positioning two or more circuit board each having a plurality of through-plated holes so that a plurality of the through-plated holes of each circuit board are axially aligned;

(b) inserting conductive lead wires into the axially aligned through-plated holes of the circuit boards; and

(c) compressing the lead wires within the plated holes so that the leads contact the interior surfaces of the through-plated holes of the circuit boards and form an electrical connection between the circuit boards.

15. A method of electrically connecting two or more circuit boards, comprising the steps of:

(a) manufacturing the circuit boards with plated holes having hole patterns substantially matching and axially aligned;

(b) positioning the circuit boards so that their planar surfaces are substantially parallel;

(c) inserting soft gold wires into the axially aligned through-plated holes of the circuit boards;

(d) positioning a first caul plate against one planar side of one of the circuit boards;

(e) positioning a second caul plate against the planar surface of another of the circuit

boards; and

(f) pressing the caul plates together so that the soft gold wires are compressed into the plated holes of the circuit boards, forming an electrical connection.

16. An interconnection apparatus comprising a plurality of circuit boards having at least one through-plated hole on each circuit board and axially aligned with one another; and

a conductive lead mechanically compressed within said axially aligned through-plated holes of the circuit boards.

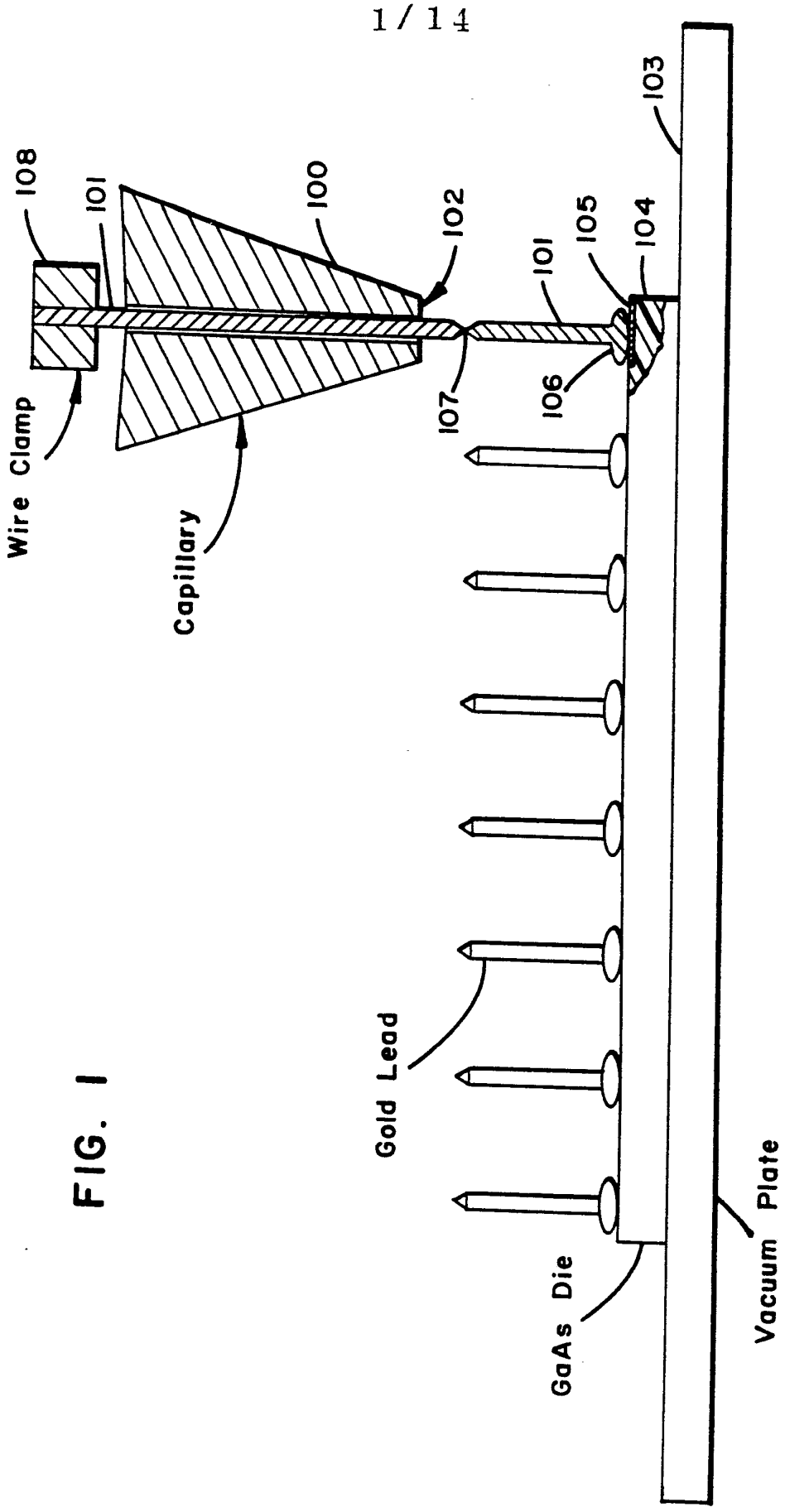

108
101
100
102
101
105
104
103
Wire Clamp
Capillary
107
106
Gold Lead
GaAs Die
Vacuum Plate

FIG. 1

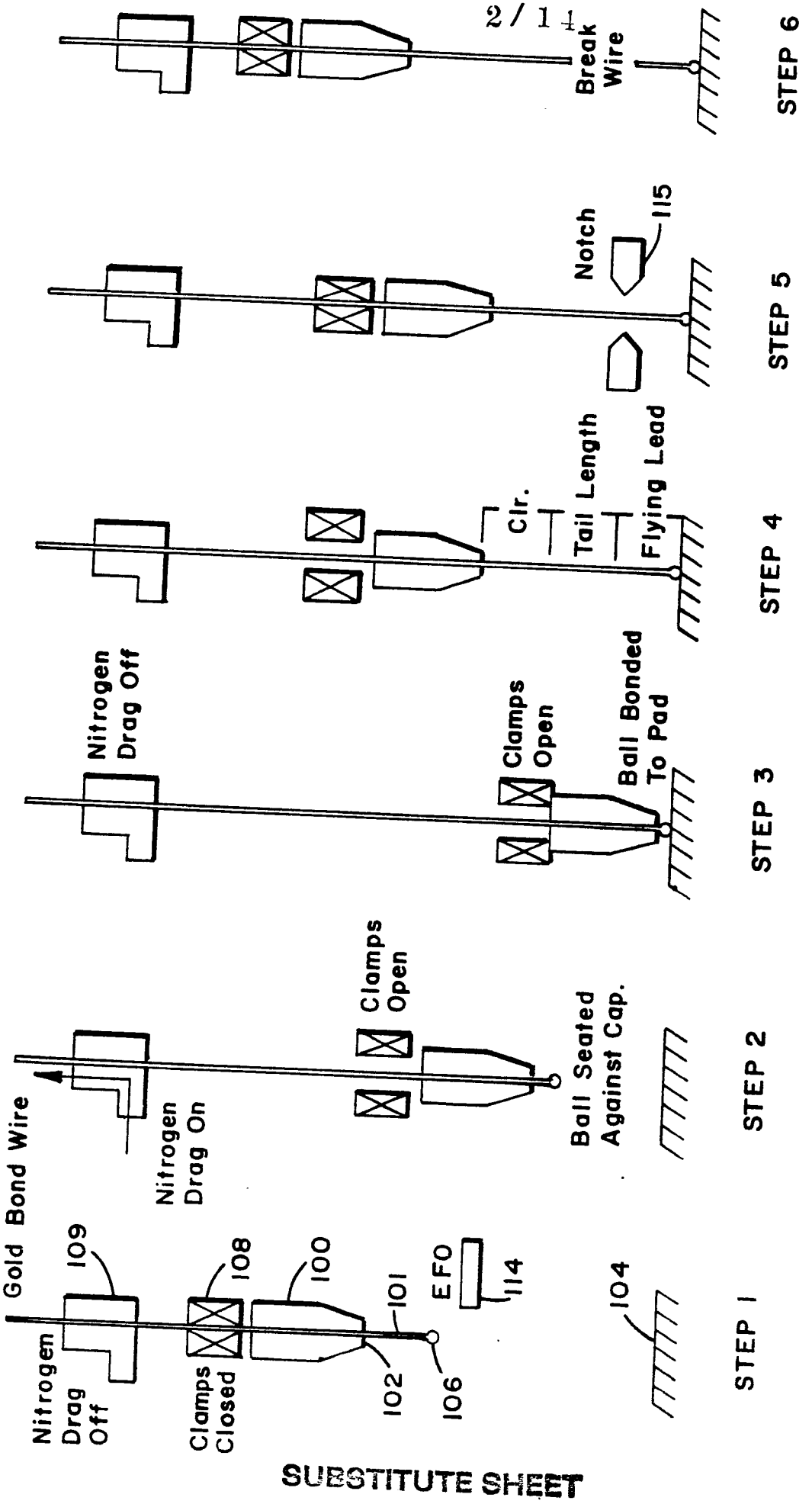

Gold Bond Wire
109
Nitrogen Drag Off
Clamps Closed
108
100
101
102
106
EFO
114
104
STEP 1
Nitrogen Drag On
Clamps Open
Ball Seated Against Cap.
STEP 2
Nitrogen Drag Off
Clamps Open
Ball Bonded To Pad
STEP 3
Clr.
Tail Length
Flying Lead
STEP 4
Notch
115
STEP 5
Break Wire
STEP 6

FIG. 2

FIG.3B

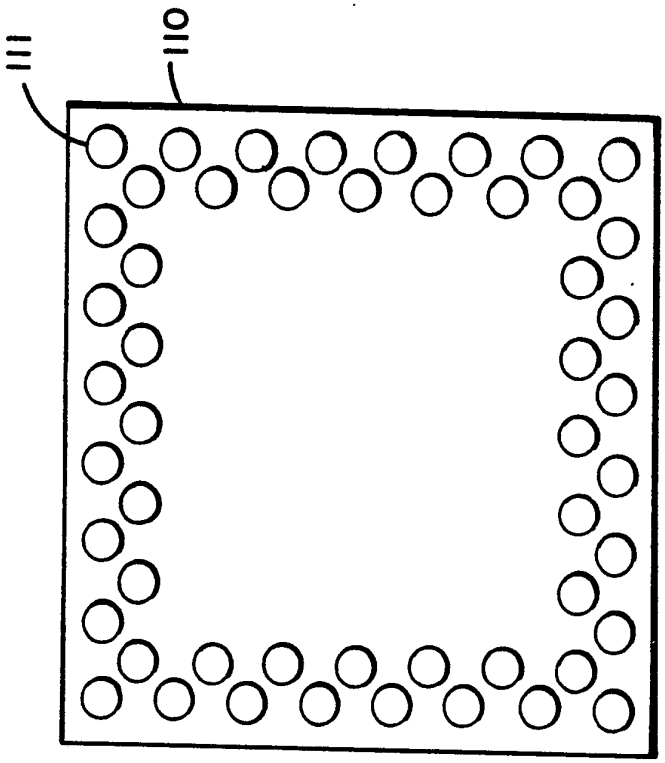
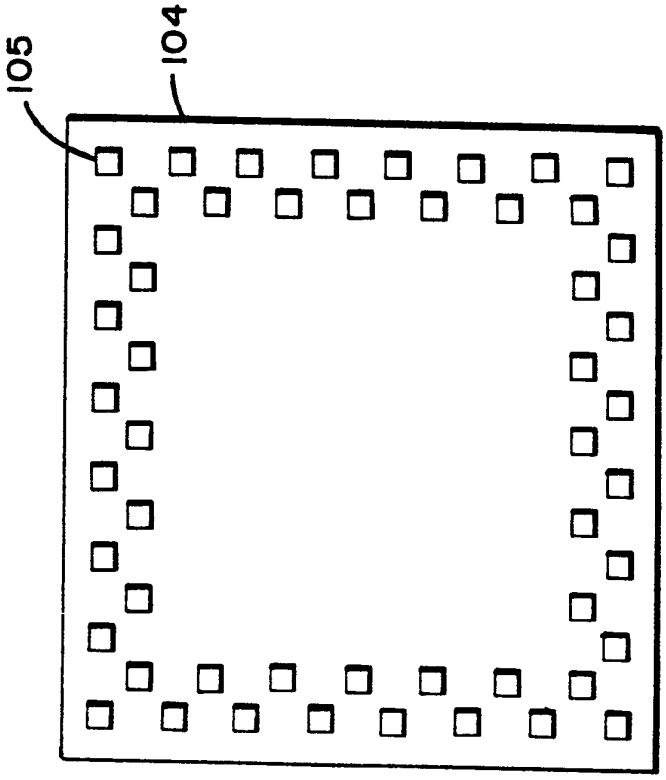

111
110
Plated Hole Pattern On Circuit Board

FIG.3A


105
104
Bonding Pad Pattern On Chip

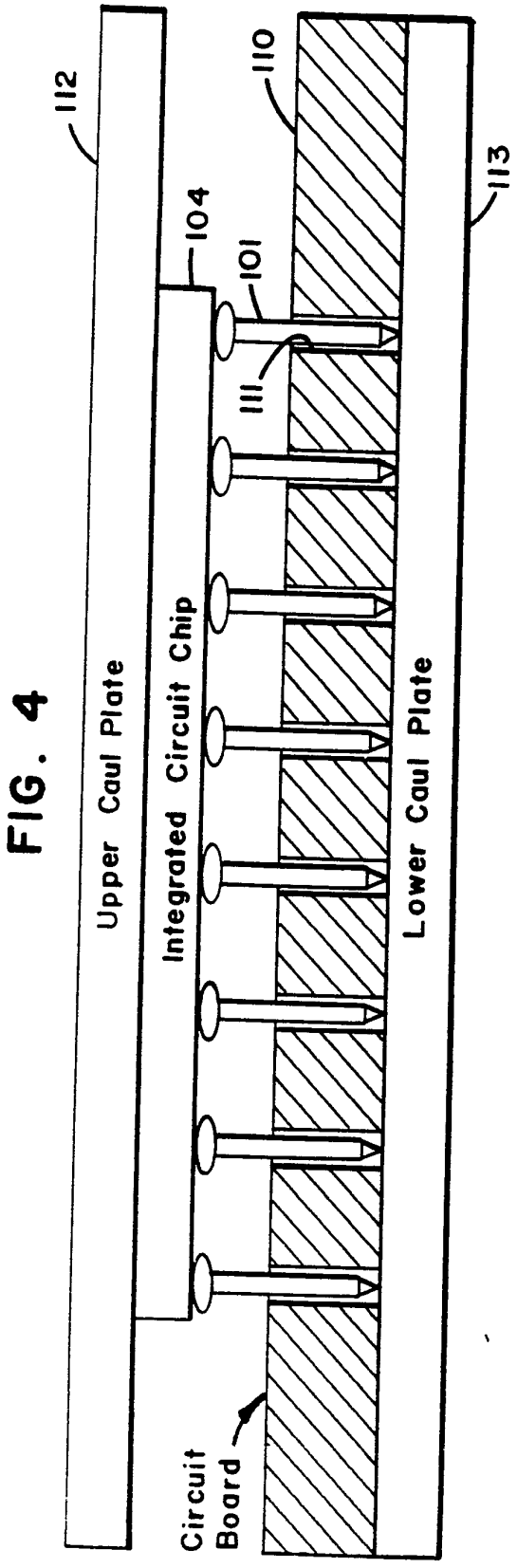

112
110
113
104
101
111
Upper Caul Plate
Integrated Circuit Chip
Lower Caul Plate
Circuit Board

FIG. 4

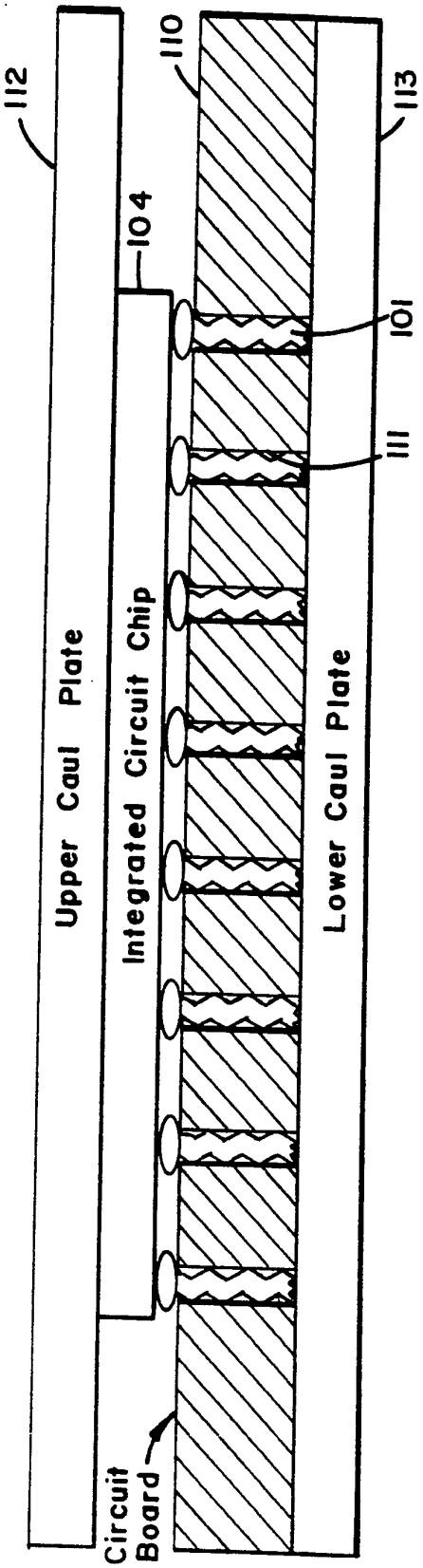

112
110
113
104
101
111
Upper Caul Plate
Integrated Circuit Chip
Lower Caul Plate
Circuit Board

FIG. 5

FIG. 5a

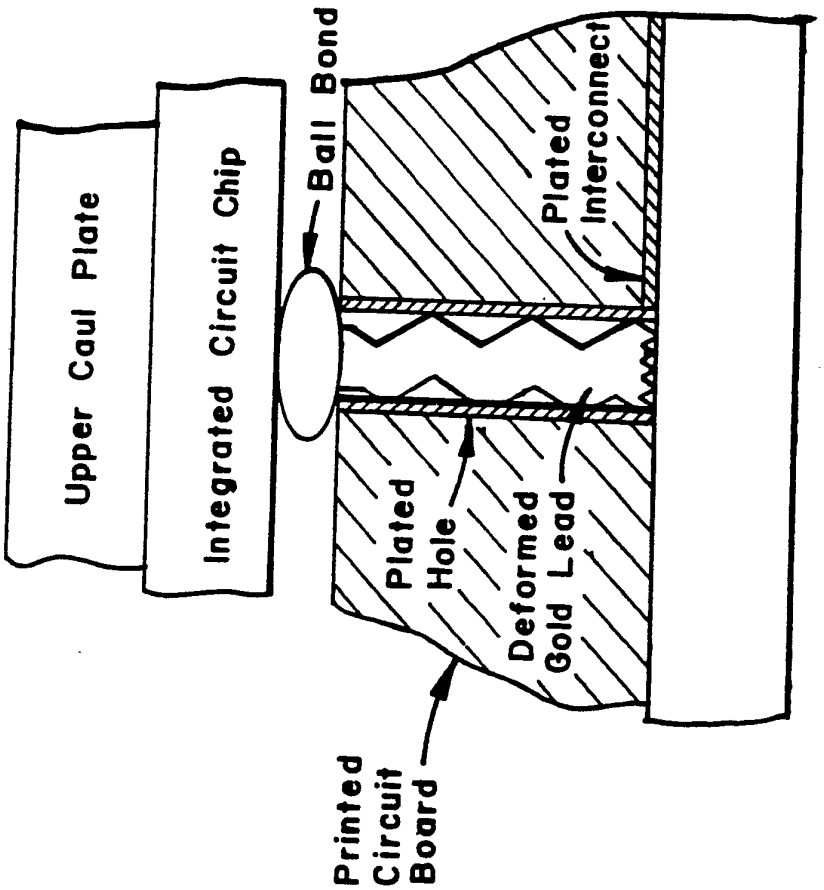
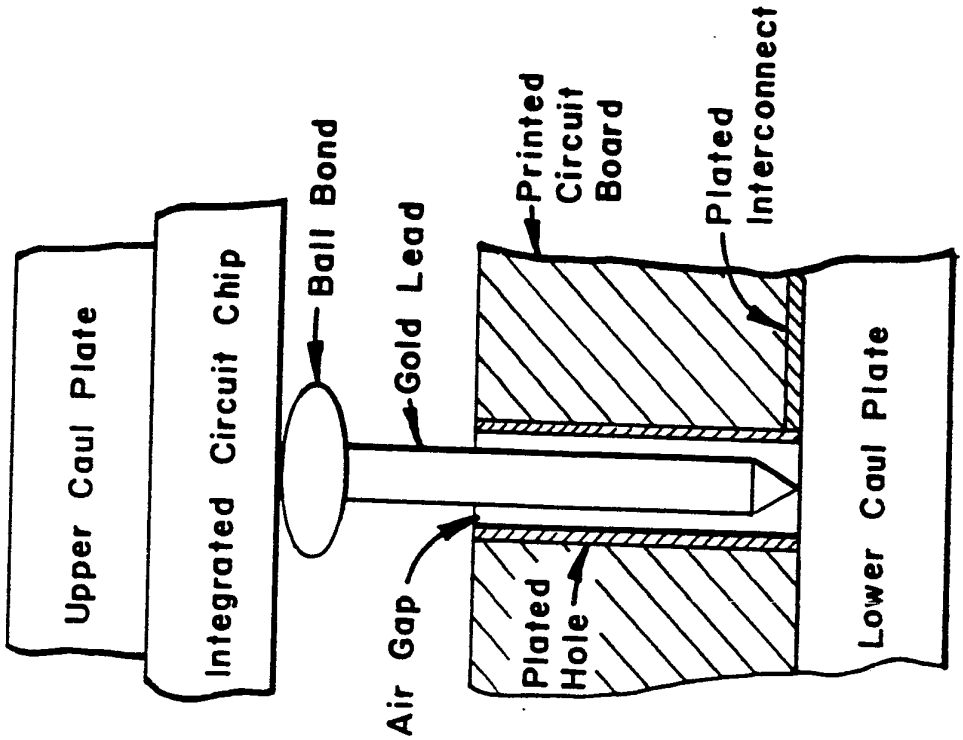

Upper Caul Plate
Integrated Circuit Chip
Ball Bond
Plated Interconnect
Plated Hole
Deformed Gold Lead
Printed Circuit Board

FIG. 4a


Upper Caul Plate
Integrated Circuit Chip
Ball Bond
Gold Lead
Printed Circuit Board
Plated Interconnect
Air Gap
Plated Hole
Lower Caul Plate

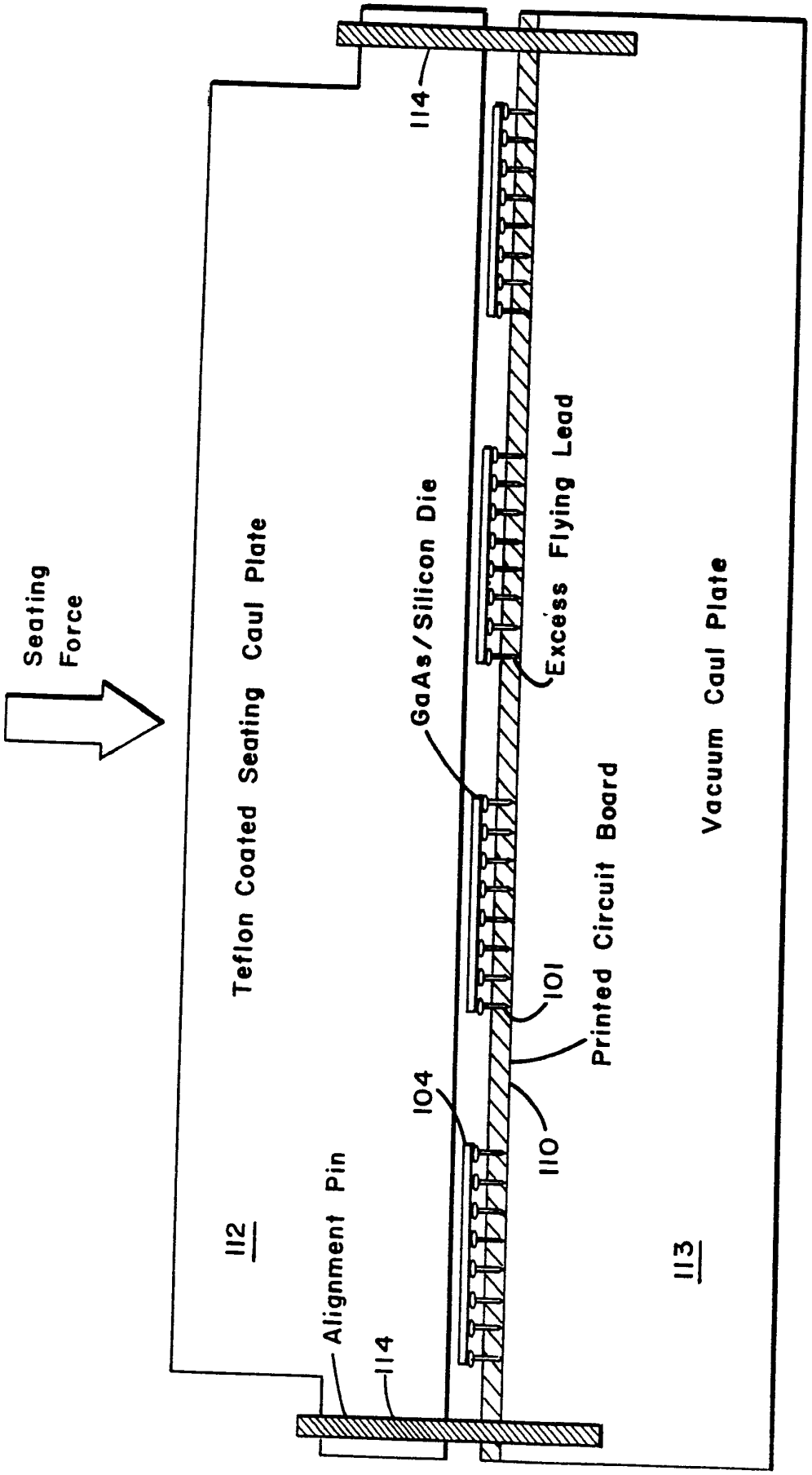

Seating Force
Teflon Coated Seating Caul Plate
GaAs/Silicon Die
Excess Flying Lead
Printed Circuit Board
Vacuum Caul Plate
114
101
104
110
Alignment Pin
114
112
113

FIG. 6

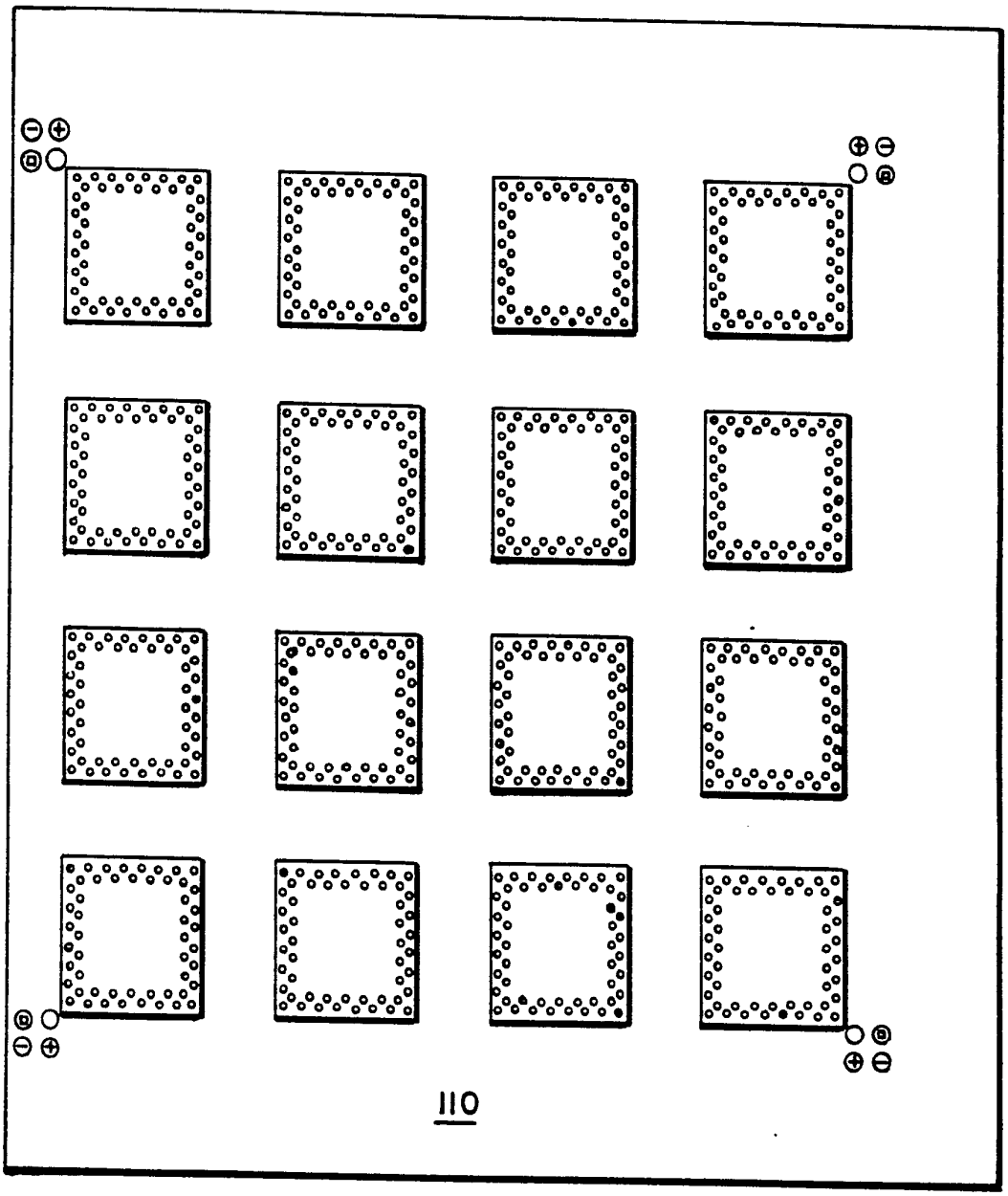


FIG. 7

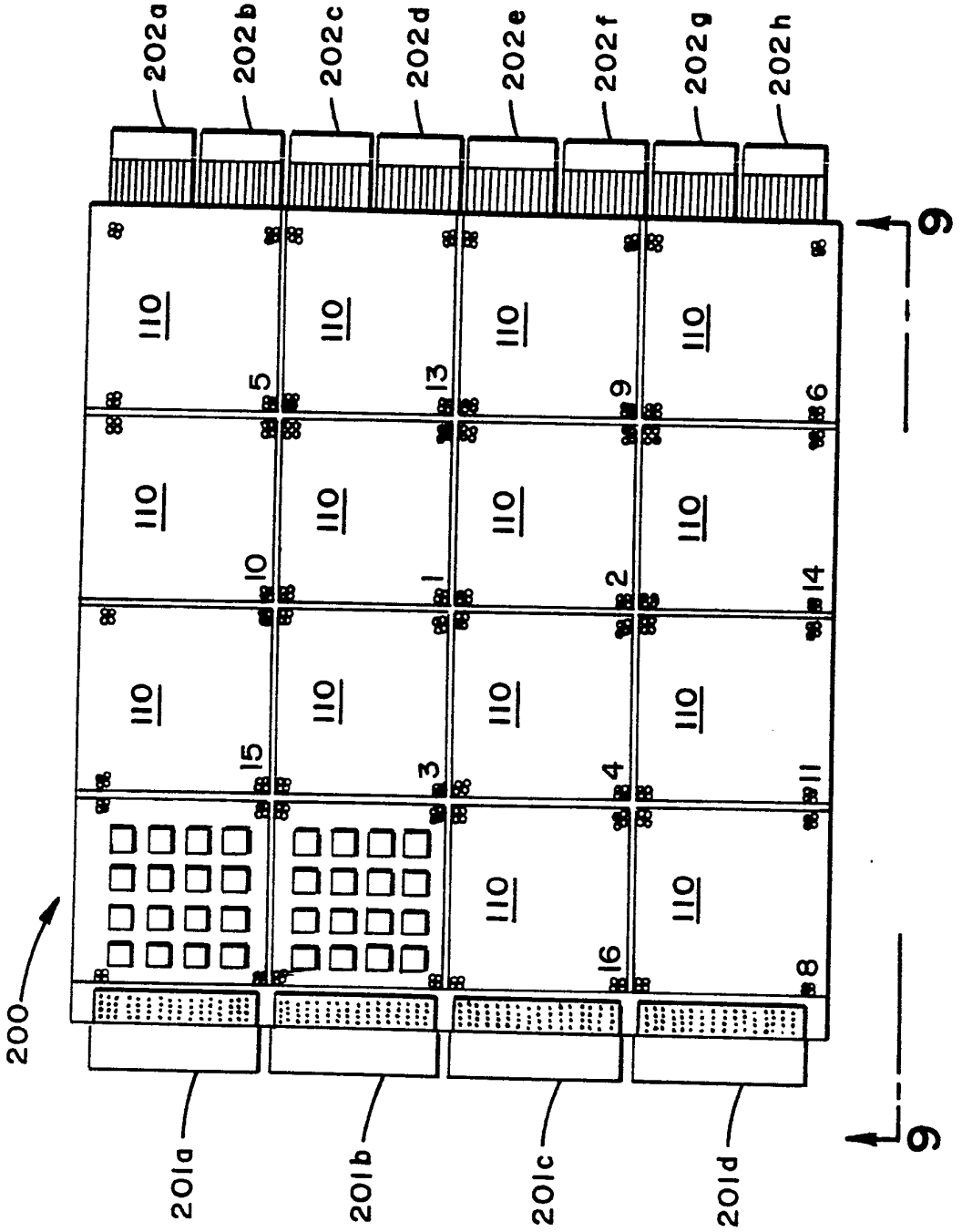

202a
202b
202c
202d
202e
202f
202g
202h
110
5
13
9
6
10
1
2
14
15
3
4
11
16
8
200
201a
201b
201c
201d
9
9

FIG. 8

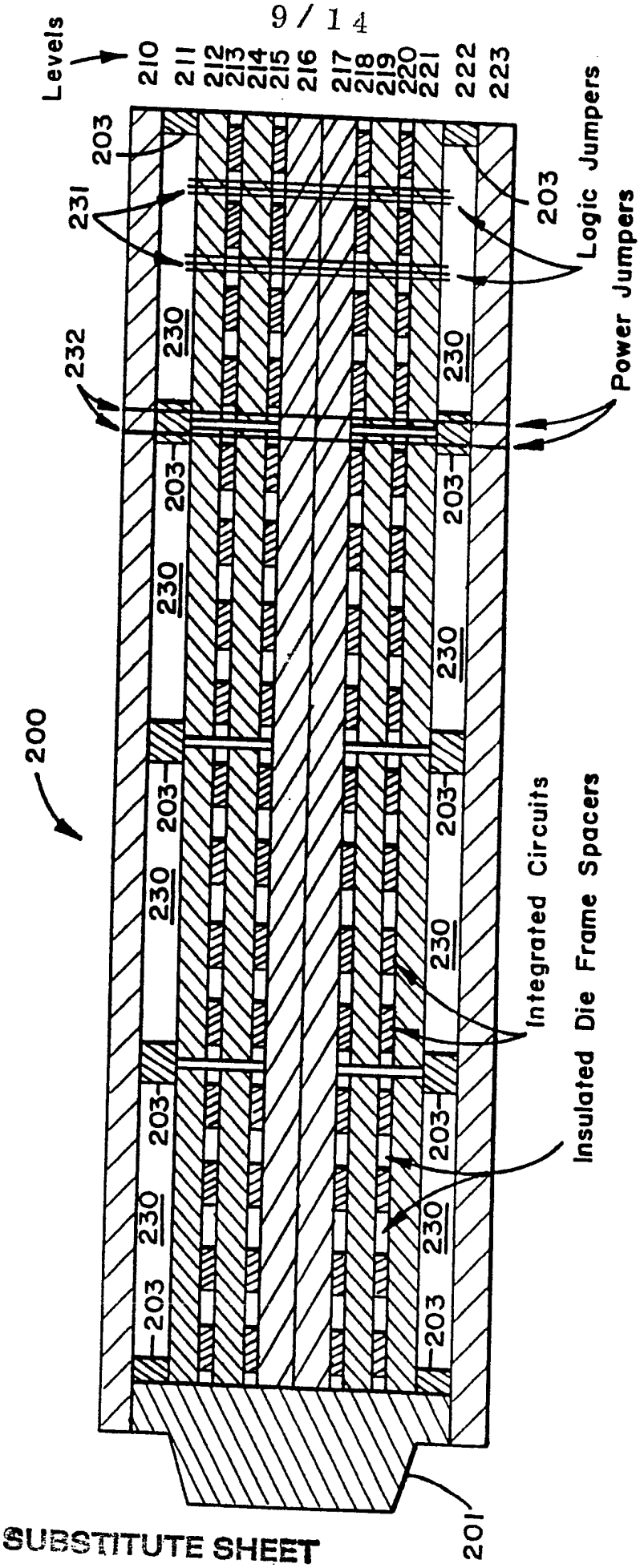
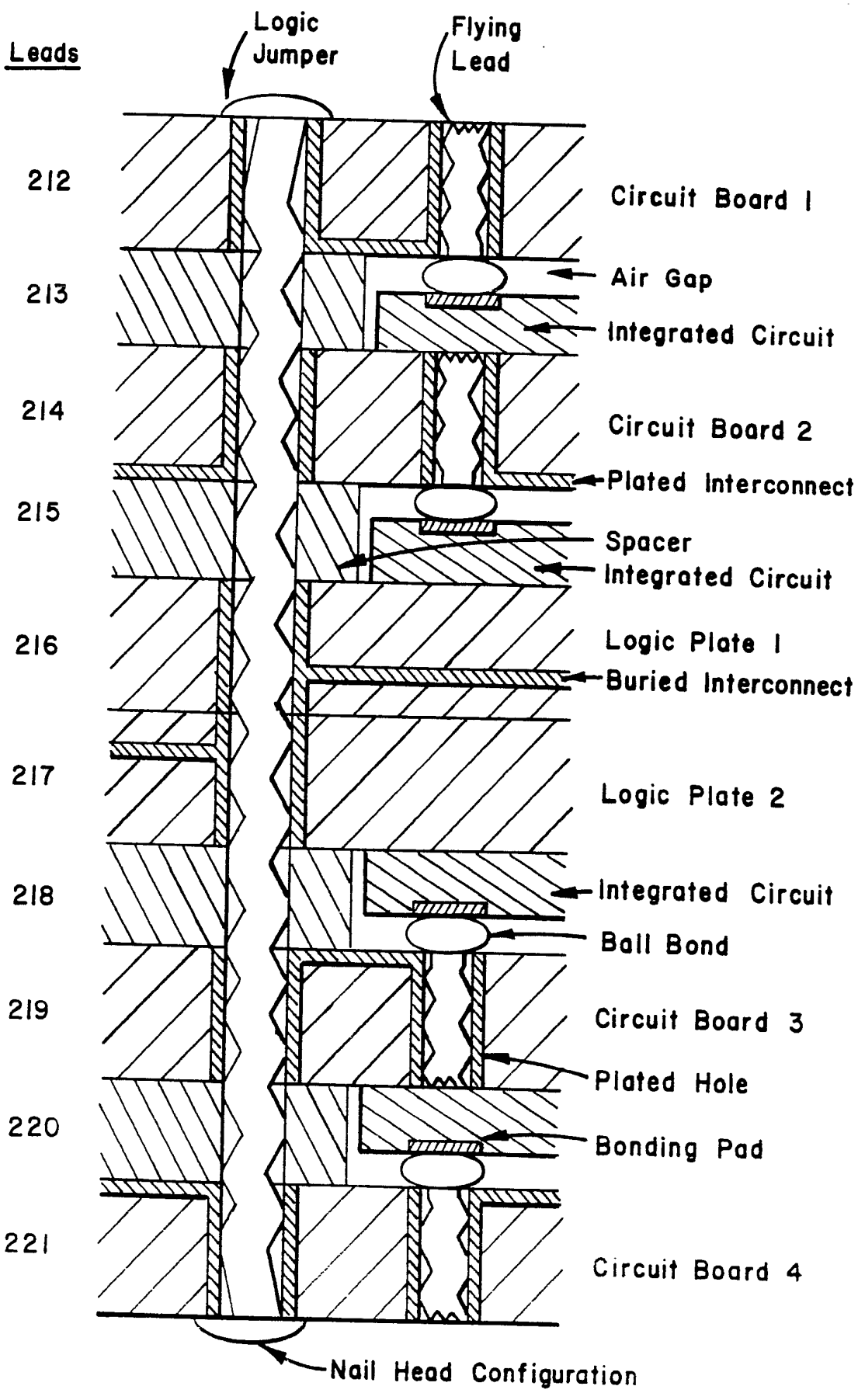

Levels
210
211
212
213
214
215
216
217
218
219
220
221
222
223
200
201
203
230
231
232
Logic Jumpers
Power Jumpers
Integrated Circuits
Insulated Die Frame Spacers

FIG. 9

FIG. 10 10/14


Leads
Logic Jumper
Flying Lead
212
213
214
215
216
217
218
219
220
221
Circuit Board 1
Air Gap
Integrated Circuit
Circuit Board 2
Plated Interconnect
Spacer
Integrated Circuit
Logic Plate 1
Buried Interconnect
Logic Plate 2
Integrated Circuit
Ball Bond
Circuit Board 3
Plated Hole
Bonding Pad
Circuit Board 4
Nail Head Configuration

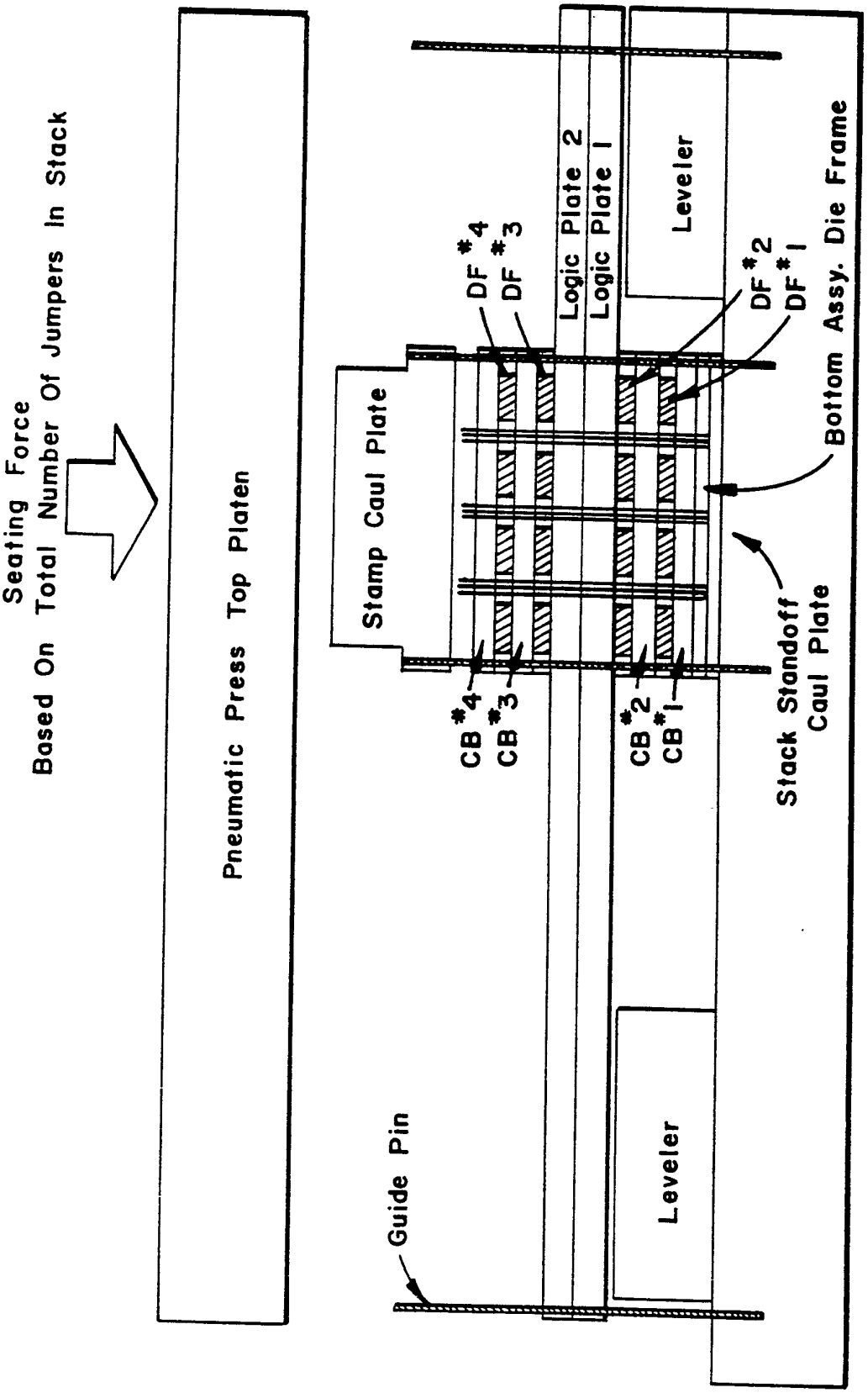

Seating Force
Based On Total Number Of Jumpers In Stack
Pneumatic Press Top Platen
Stamp Caul Plate
Guide Pin
DF *4
DF *3
DF *2
DF *1
CB *4
CB *3
CB *2
CB *1
Logic Plate 2
Logic Plate 1
Leveler
Leveler
Bottom Assy. Die Frame
Stack Standoff
Caul Plate

FIG. 11

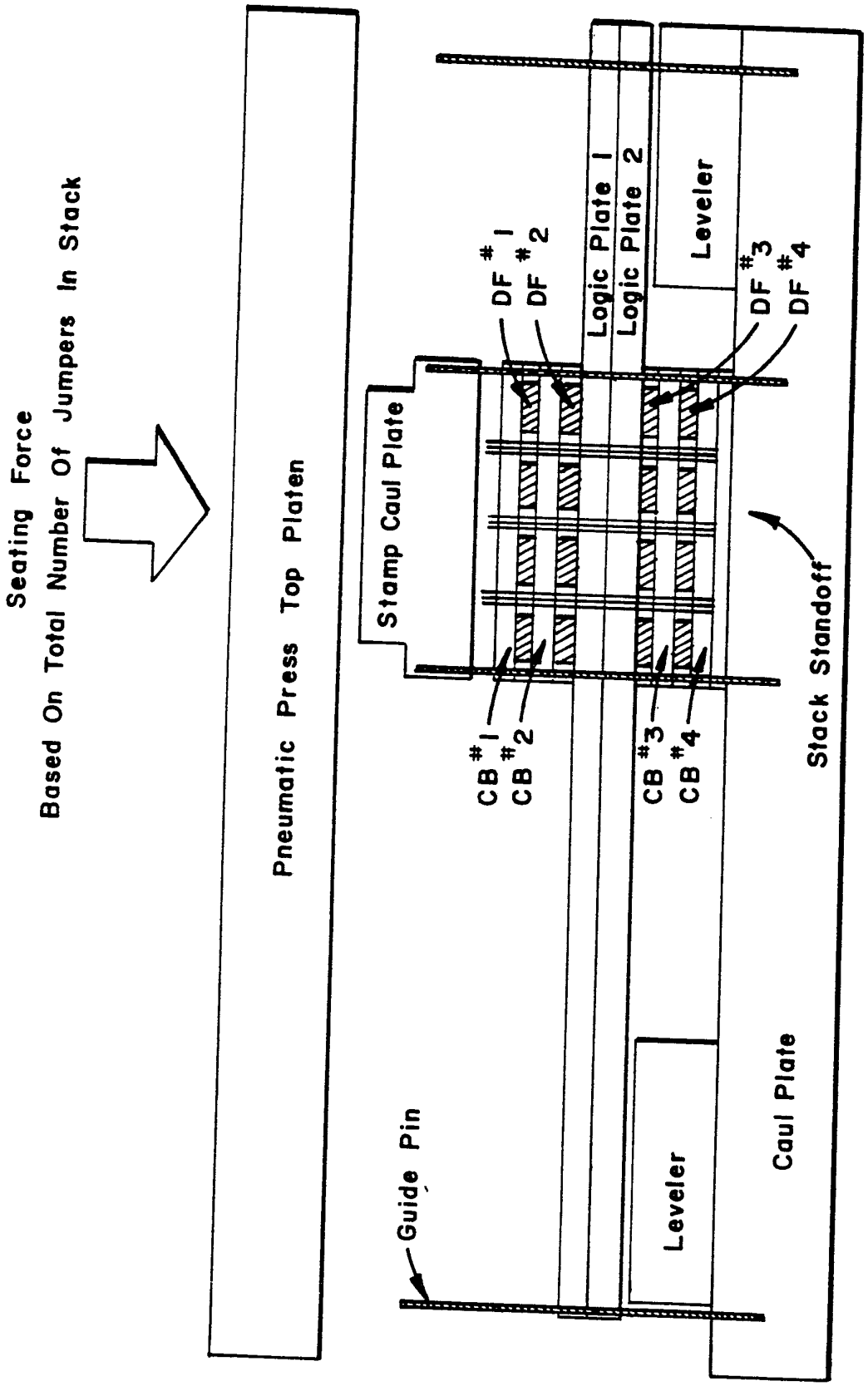

Seating Force
Based On Total Number Of Jumpers In Stack
Pneumatic Press Top Platen
Stamp Caul Plate
Guide Pin
DF #1
DF #2
DF #3
DF #4
Logic Plate 1
Logic Plate 2
Leveler
Leveler
CB #1
CB #2
CB #3
CB #4
Stack Standoff
Caul Plate

FIG. 12

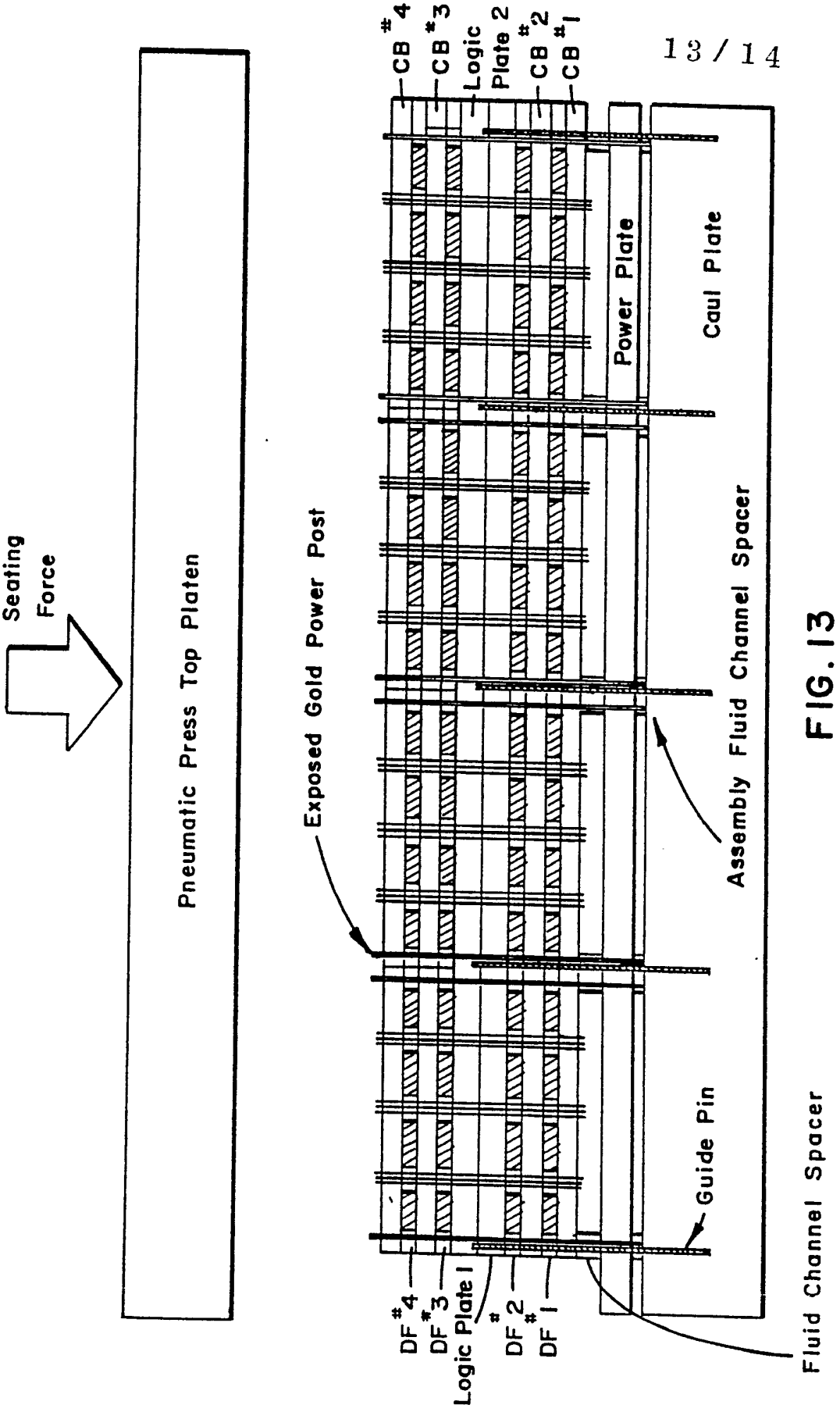

Seating Force
Pneumatic Press Top Platen
Exposed Gold Power Post
CB #4
CB #3
Logic Plate 2
CB #2
CB #1
Power Plate
Caul Plate
Assembly Fluid Channel Spacer
Guide Pin
Fluid Channel Spacer
DF #4
DF #3
Logic Plate 1
DF #2
DF #1

FIG. 13

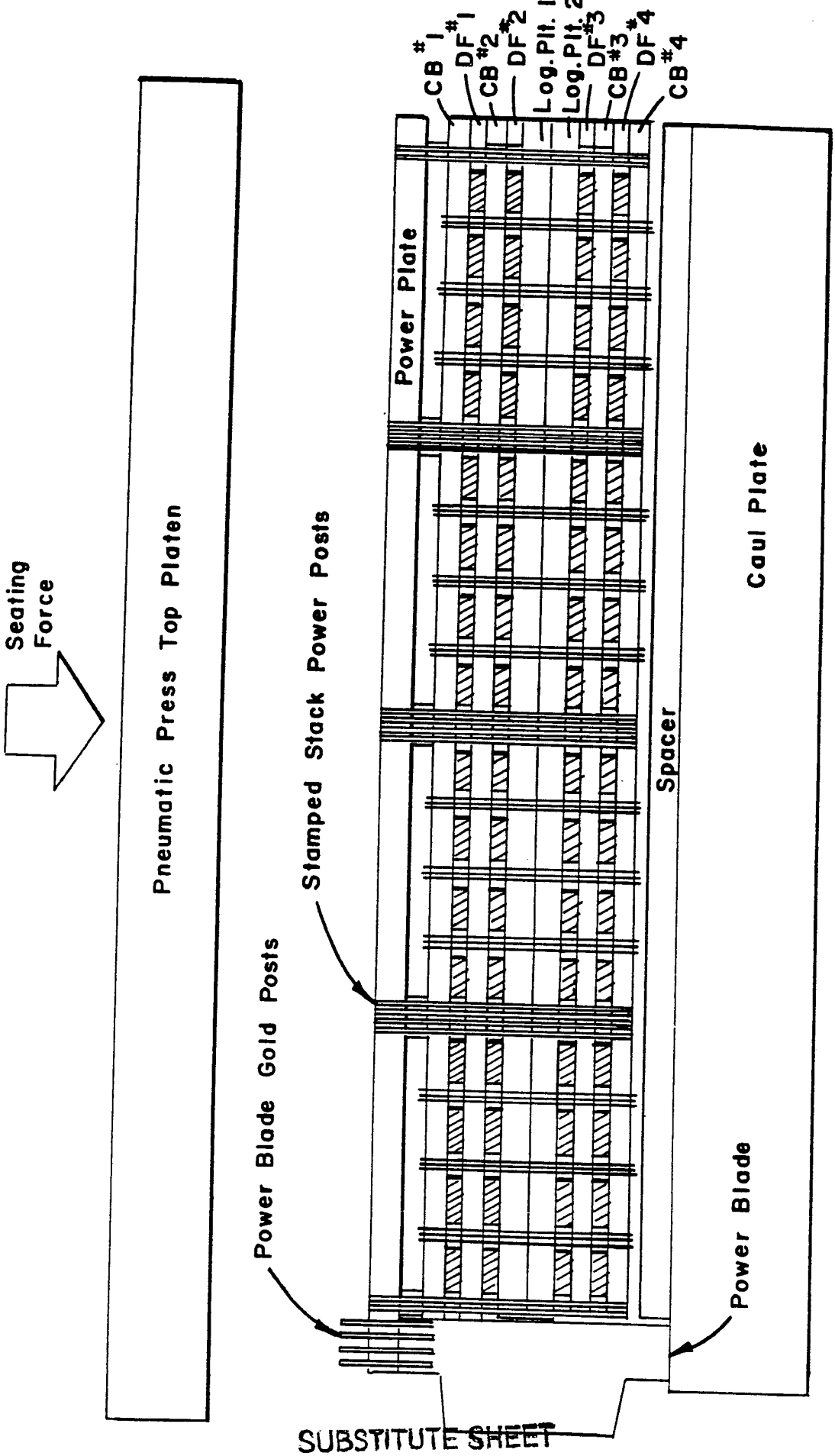

Seating Force
Pneumatic Press Top Platen
Power Plate
CB #1
DF #1
CB #2
DF #2
Log. Plt. 1
Log. Plt. 2
DF #3
CB #3
DF #4
CB #4
Stamped Stack Power Posts
Power Blade Gold Posts
Spacer
Caul Plate
Power Blade

FIG. 14

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 90/03572

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: H 01 L 23/538, 23/498

II. FIELDS SEARCHED

Minimum Documentation Searched [7]	
Classification System	Classification Symbols
IPC[5]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	Patent Abstracts of Japan, volume 11, no. 99 (E-493)(2546), 27 March 1987, & JP, A, 61248454 (HITACHI LTD) 5 November 1986 see the abstract	1-3
A	--	14,15
A	US, A, 4667219 (TRILOGY COMPUTER) 19 May 1987 see figure 8; column 4, line 44 - column 5, line 5	1,2,4
	--	
A	EP, A, 0284820 (CANON) 5 October 1988 see figure 39A; column 131, lines 25-42	5
	--	
A	EP, A, 0289102 (LSI LOGIC) 2 November 1988 see claims 1,11	5
	-- ./.	

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
28th September 1990	24. 10. 90
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. Peis M. PEIS

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	Patent Abstracts of Japan, volume 10, no. 121 (E-401)(2178), 7 May 1986, & JP, A, 60254762 (FUJITSU) 16 December 1985 see the abstract --	16
A	EP, A, 0069505 (FUJITSU) 12 January 1983 --	
A	Patent Abstracts of Japan, volume 10, no. 283 (E-440)(2339), 26 September 1986 & JP, A, 61101060 (HITACHI) 19 May 1986 --------	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 9003572

SA 38272

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 15/10/90
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4667219	19-05-87	None	
EP-A- 0284820	05-10-88	JP-A- 63207368	26-08-88
		JP-A- 63207371	26-08-88
		JP-A- 63207369	26-08-88
		JP-A- 63216351	08-09-88
		JP-A- 63304582	12-12-88
		JP-A- 63228726	22-09-88
		JP-A- 63231888	27-09-88
		JP-A- 63239787	05-10-88
		JP-A- 63231890	27-09-88
		JP-A- 63232279	28-09-88
		JP-A- 63232439	28-09-88
		JP-A- 63237373	03-10-88
		JP-A- 63237374	03-10-88
		JP-A- 63237537	04-10-88
		JP-A- 63245874	12-10-88
		JP-A- 63245875	12-10-88
		JP-A- 63244850	12-10-88
		JP-A- 63246835	13-10-88
		JP-A- 63246836	13-10-88
		JP-A- 63246837	13-10-88
EP-A- 0289102	02-11-88	US-A- 4790897	13-12-88
EP-A- 0069505	12-01-83	JP-A- 58002054	07-01-83
		US-A- 4530002	16-07-85