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(54) **RECONFIGURABLE MEMORY WITH SELECTABLE ERROR CORRECTION STORAGE**

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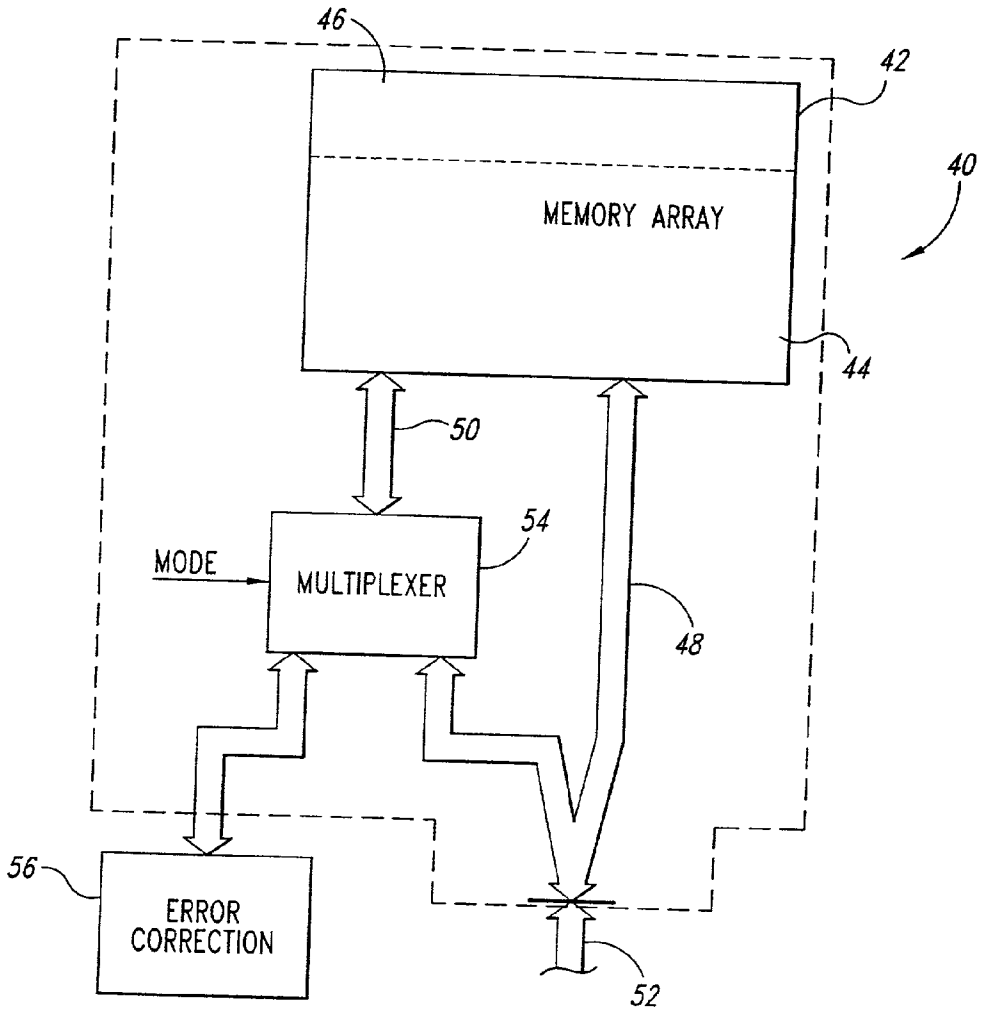
(57) **ABSTRACT**

A memory structure includes a memory module divided into low order banks and high order banks. The low order banks are used as conventional memory. The high order banks are used as either conventional memory or ECC memory, depending upon routing of data. In one embodiment, data from the high order banks are routed through a primary multiplexer to a data bus when the high order banks are used as conventional memory. When the high order banks are used as ECC memory, data from the auxiliary section is routed through the primary multiplexer to an error correction circuit. A secondary multiplexer combines ECC bits from the auxiliary section of the module or a dedicated ECC memory on a motherboard. The auxiliary section thus supplements the onboard ECC memory to provide support for an effectively larger ECC memory for use with error intolerant applications that require error correction.



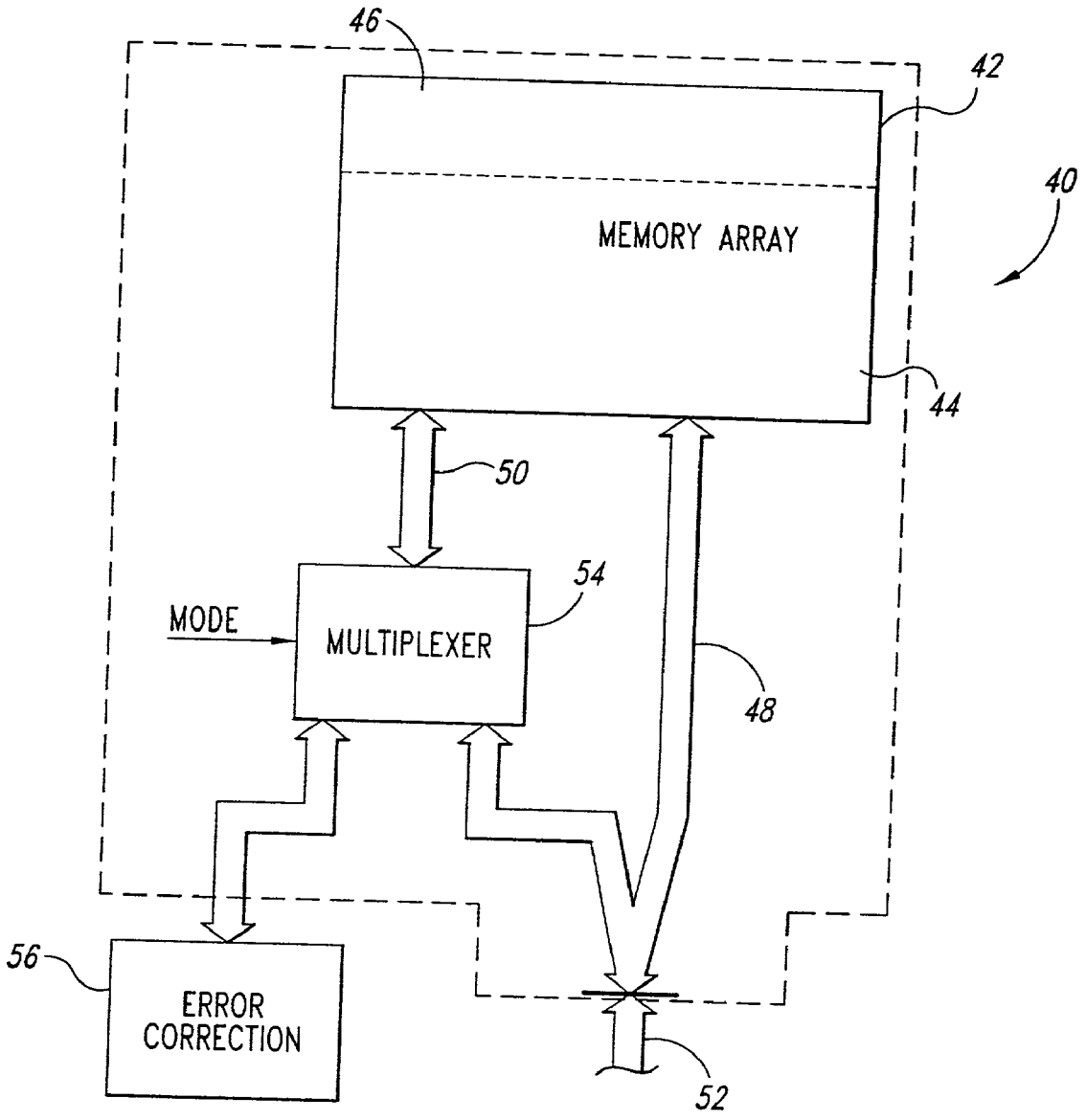

46
42
40
MEMORY ARRAY
44
50
54
MODE
MULTIPLEXER
48
56
ERROR
CORRECTION
52

Fig. 1

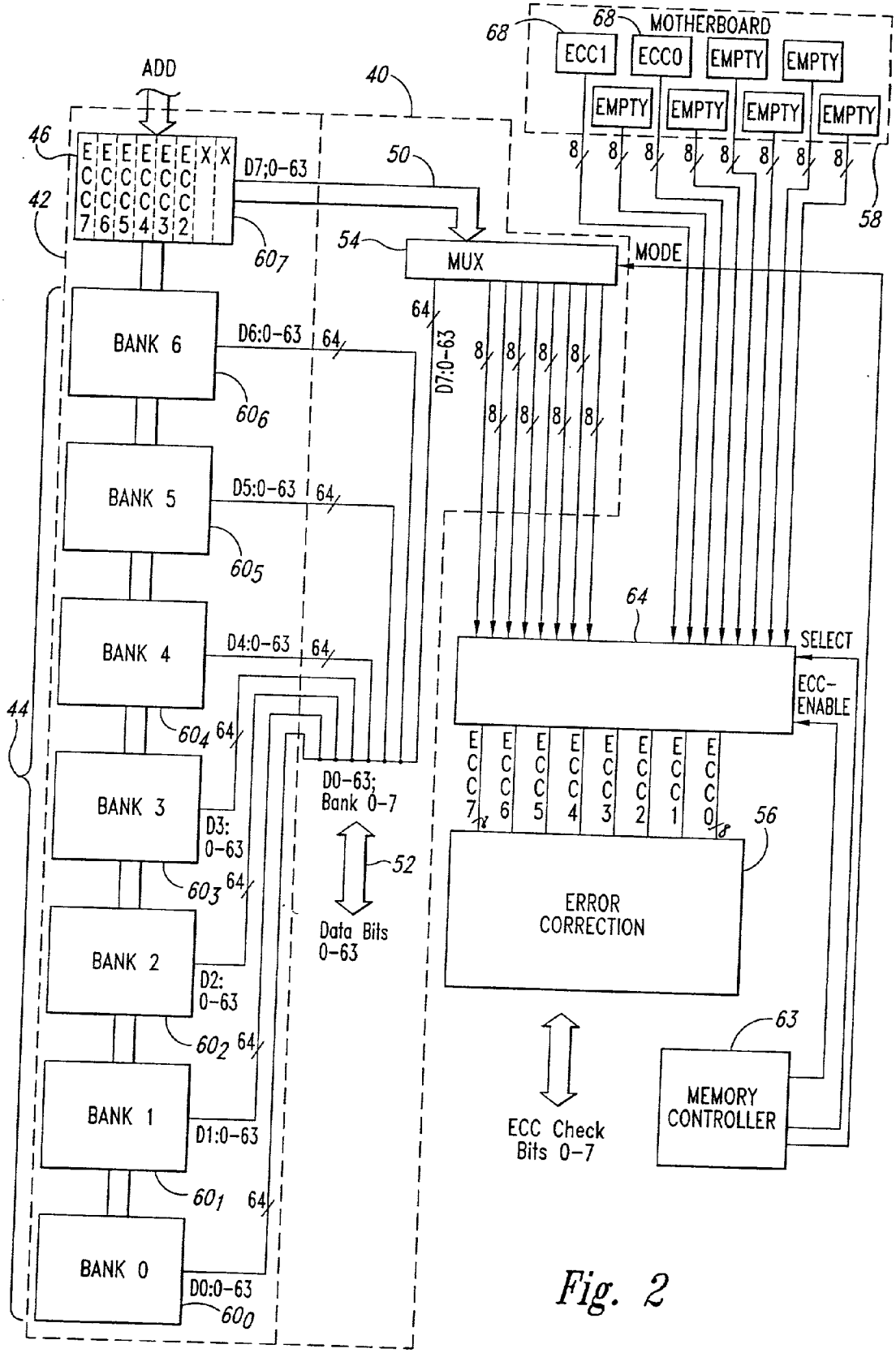

ADD
40
46
42
ECC7 ECC6 ECC5 ECC4 ECC3 ECC2 X X
D7;0-63
50
607
54
MUX
MODE
68
MOTHERBOARD
ECC1
ECC0
EMPTY
EMPTY
EMPTY
EMPTY
EMPTY
EMPTY
EMPTY
EMPTY
58
BANK 6
D6:0-63
64
606
BANK 5
D5:0-63
64
605
BANK 4
D4:0-63
64
604
BANK 3
D3: 0-63
603
BANK 2
D2: 0-63
602
BANK 1
D1:0-63
601
BANK 0
D0:0-63
600
44
D7:0-63
64
D0-63; Bank 0-7
52
Data Bits 0-63
64
SELECT
ECC-ENABLE
ECC7 ECC6 ECC5 ECC4 ECC3 ECC2 ECC1 ECC0
56
ERROR CORRECTION
ECC Check Bits 0-7
63
MEMORY CONTROLLER

Fig. 2

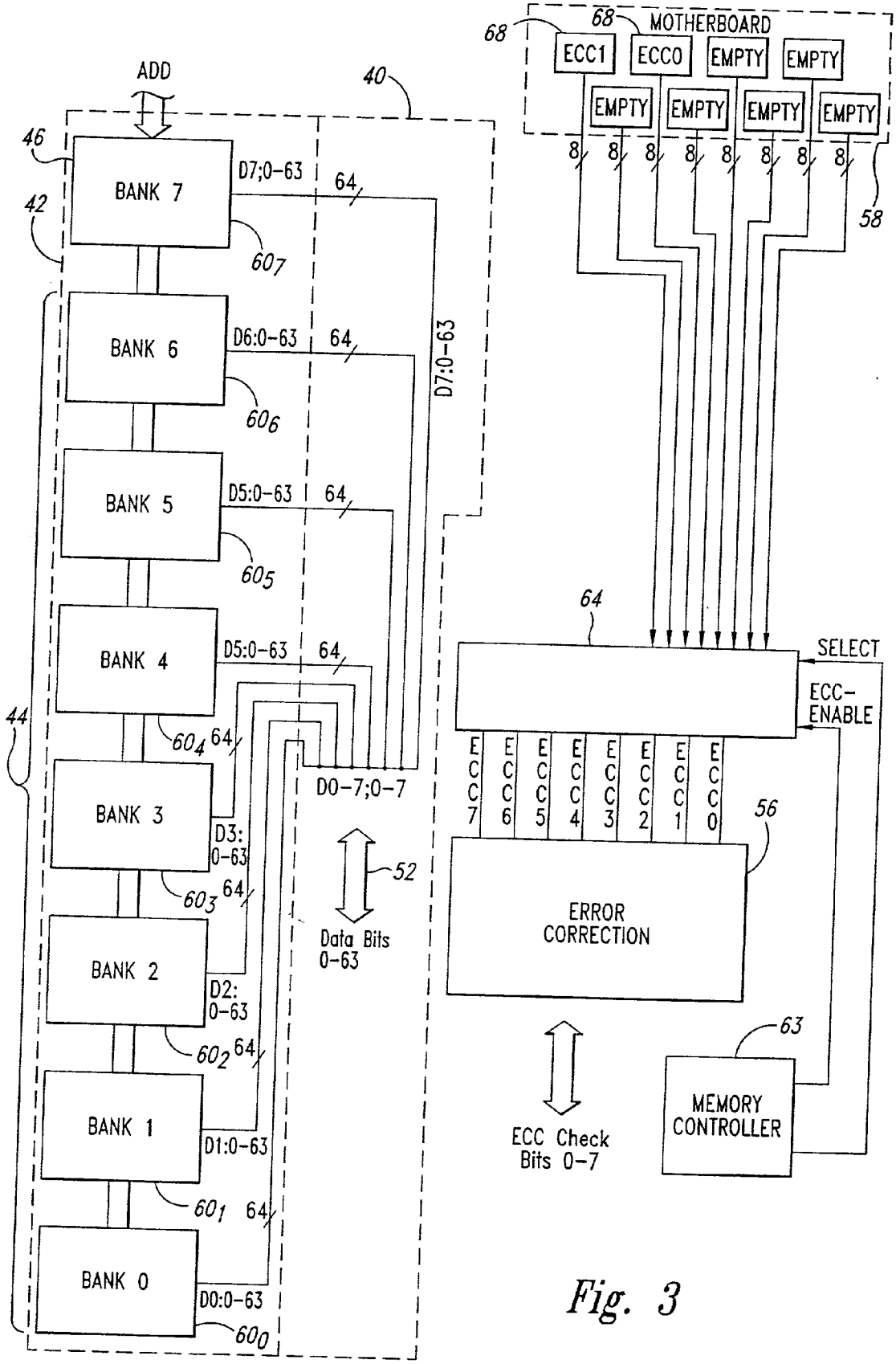

ADD
40
46
42
BANK 7
D7;0-63
64
607
BANK 6
D6:0-63
64
606
BANK 5
D5:0-63
64
605
BANK 4
D5:0-63
64
604
64
44
BANK 3
D3:
0-63
603
64
BANK 2
D2:
0-63
602
64
BANK 1
D1:0-63
601
64
BANK 0
D0:0-63
600
D7:0-63
D0-7;0-7
52
Data Bits
0-63
68
68
MOTHERBOARD
ECC1
ECC0
EMPTY
EMPTY
EMPTY
EMPTY
EMPTY
EMPTY
EMPTY
EMPTY
8
58
64
SELECT
ECC-
ENABLE
ECC7
ECC6
ECC5
ECC4
ECC3
ECC2
ECC1
ECC0
56
ERROR
CORRECTION
63
MEMORY
CONTROLLER
ECC Check
Bits 0-7

Fig. 3

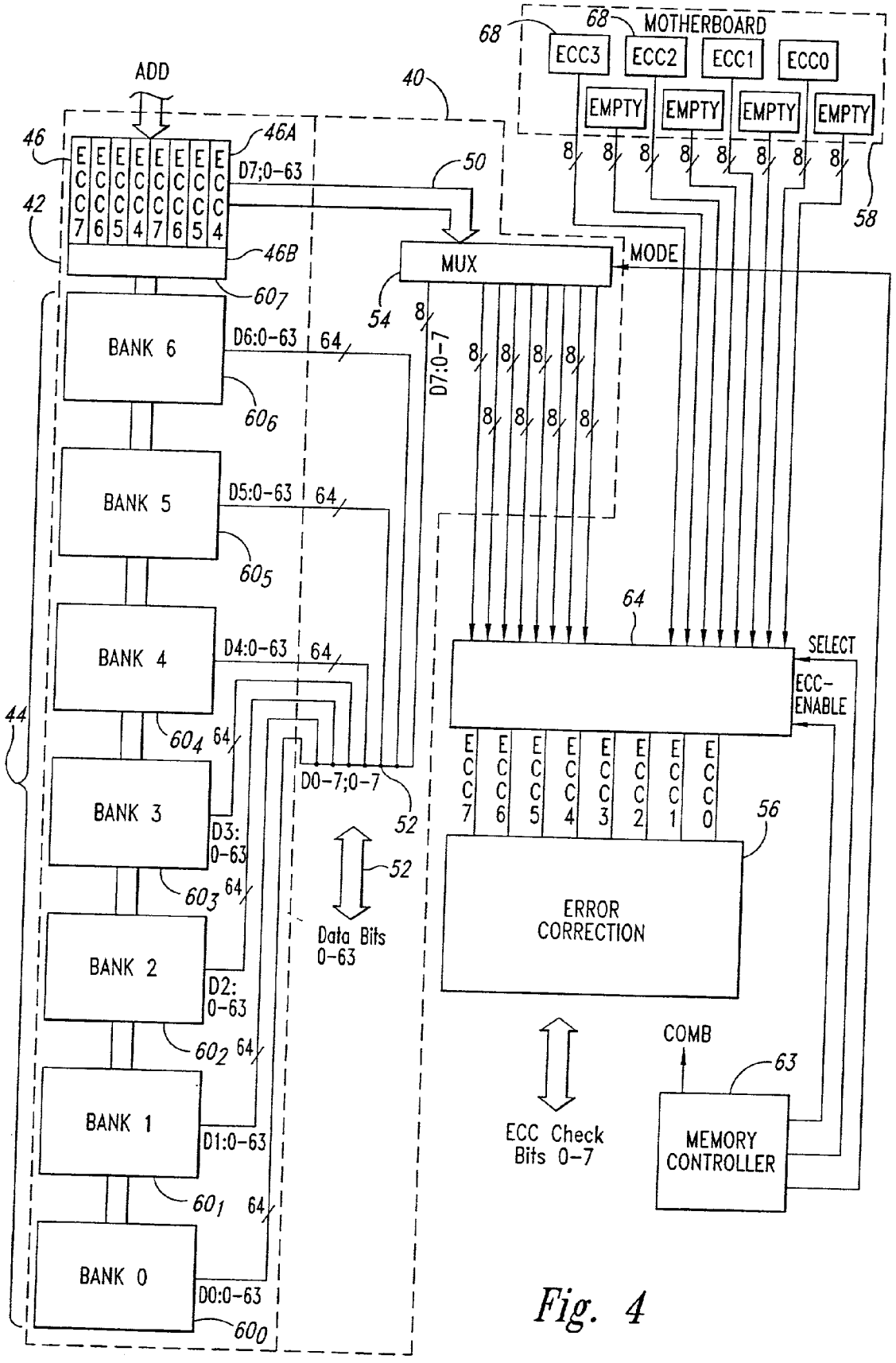

MOTHERBOARD
ECC3
ECC2
ECC1
ECC0
EMPTY
EMPTY
EMPTY
EMPTY
ADD
40
46
46A
D7;0-63
50
42
46B
MUX
MODE
607
54
BANK 6
D6:0-63
64
606
D7:0-7
BANK 5
D5:0-63
605
BANK 4
D4:0-63
604
44
SELECT
ECC-ENABLE
BANK 3
D3:0-63
603
D0-7;0-7
52
Data Bits 0-63
BANK 2
D2:0-63
602
ERROR CORRECTION
56
BANK 1
D1:0-63
601
COMB
63
ECC Check Bits 0-7
MEMORY CONTROLLER
BANK 0
D0:0-63
600
58

Fig. 4

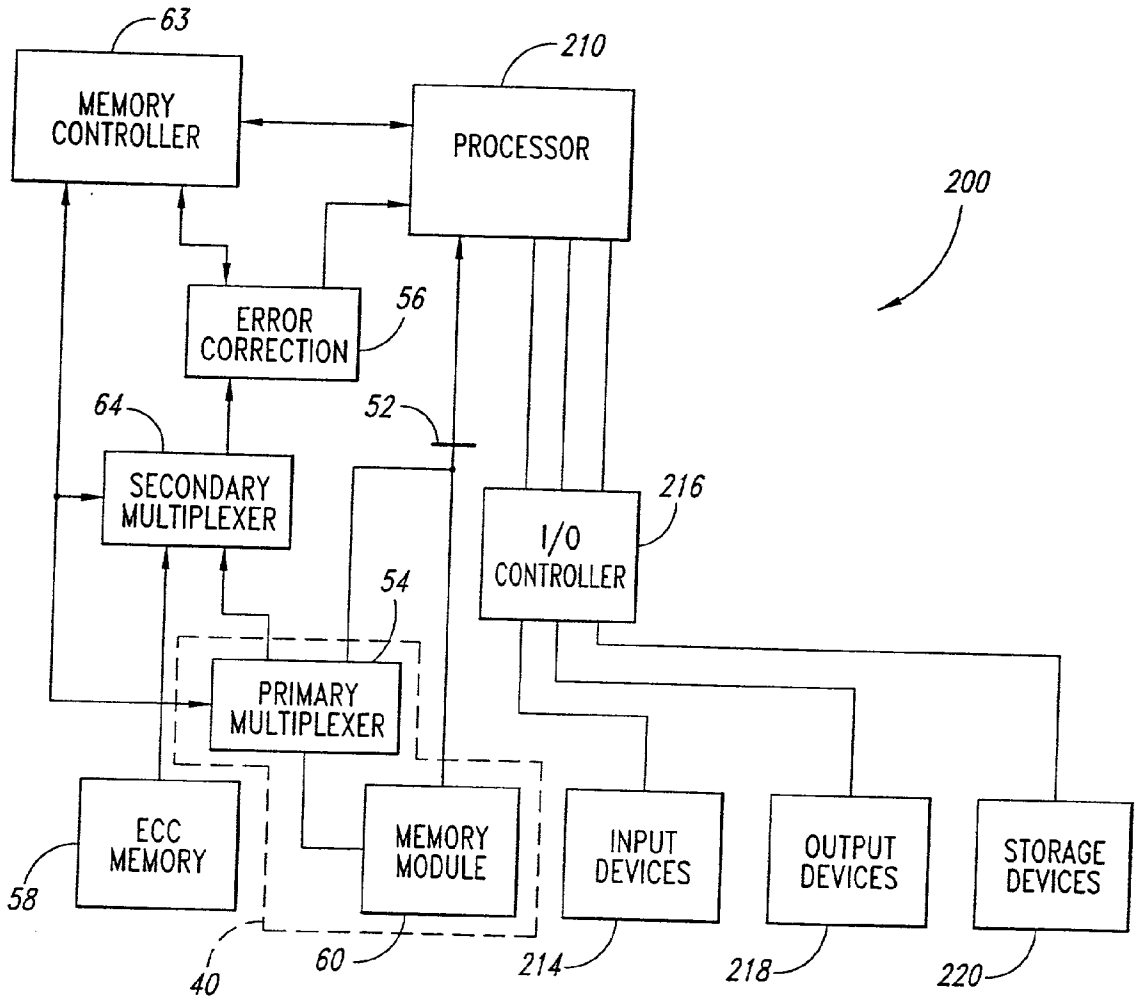

63
MEMORY CONTROLLER
210
PROCESSOR
200
ERROR CORRECTION
56
64
52
SECONDARY MULTIPLEXER
216
I/O CONTROLLER
54
PRIMARY MULTIPLEXER
ECC MEMORY
58
MEMORY MODULE
INPUT DEVICES
OUTPUT DEVICES
STORAGE DEVICES
40
60
214
218
220

Fig. 5

RECONFIGURABLE MEMORY WITH SELECTABLE ERROR CORRECTION STORAGE

TECHNICAL FIELD

[0001] The present invention relates to memory structures for computers, and more particularly, to error correction in computer memories.

BACKGROUND OF THE INVENTION

[0002] Semiconductor memory systems are subject to errors. That is, data retrieved from the memory does not always match data that was originally written to the memory. Such errors can be caused by stray alpha particles, damage to the memory devices or by a variety of operating conditions, such as power supply fluctuations, noise, etc. Regardless of the source, such errors are clearly undesirable. Consequently, most modem memory systems include error detection and/or error correction capabilities.

[0003] Typical approaches to detecting and correcting errors in memory rely upon some form of error correction code to identify and correct such data errors. Such error correction codes typically include a mathematical algorithm that is applied to the data to be checked and corrected, and additional error correction code ("ECC") bits. Usually, the ECC bits are stored in a separate memory dedicated to the ECC bits. The amount of memory dedicated to storing the ECC bits can be significant. For example, the memory overhead for the ECC bits can often exceed 10%.

[0004] The amount of ECC bits required can depend upon the type of error correction code being utilized. In some applications, very little or no error correction is desired. For example, in video games, occasional image data errors are unlikely to significantly affect the images perceived by a user. Rather than devote processor power to error correction calculations and memory to ECC bits, such applications largely ignore image data errors to increase the speed of play. Such applications will be referred to herein as error tolerant applications. Error tolerant applications typically use no error correction calculations or limited error correction algorithms that require little or no ECC memory.

[0005] Other applications can tolerate little or no data errors. For example, data errors can be extremely undesirable in accounting programs. Such applications will be referred to herein as error intolerant applications. Error intolerant applications usually utilize robust error correction algorithms requiring a substantial amount of ECC memory.

[0006] Typically, memory devices for storing ECC bits are segregated from memory devices for conventional data. For example, 144 pin 4-MB×64 double in-line memory module ("DIMM") not used to store ECC bits could be implemented using 16 4-MB×4 dynamic random access memories ("DRAMs"). However, the same data storage capacity plus the capacity to store ECC bits would require a 4-MB×72 DIMM implemented using 18 4-MB×4 DRAMs. Thus, implementing ECC requires two additional DRAMs.

[0007] One problem with such memory architectures is that they do not fully utilize the available memory capacity. For example, error tolerant applications do not need nor use the extra memory provided to store ECC bits. Thus, valuable memory capacity is left unused. In the above example, 11% of the DRAMs on the DIMM are wasted when the DIMM is not used to store ECC bits.

[0008] On the other hand, error intolerant applications require more memory and are often limited by the amount of available ECC memory. Consequently, the speed with which the application runs can be increased by increasing the amount of available ECC memory. Adding such memory can be costly. Moreover, adding such memory capacity increases the amount of unused memory in error tolerant applications.

SUMMARY OF THE INVENTION

[0009] A software or hardware controlled reconfigurable memory system includes an auxiliary section of one or more data banks that can be selectively utilized as conventional memory or ECC memory, depending upon the particular application. In one embodiment, the auxiliary section is part of a memory module that includes a primary section directly coupled to an output data bus for conventional memory uses. A primary multiplexer selectively couples the auxiliary section to either the output data bus or to an error checking circuit, depending upon the selected configuration of the system. If the system runs an error intolerant application employing a robust error correction algorithm, the auxiliary section is coupled to the error correction circuit to store ECC data for ECC calculations. In error tolerant applications not requiring error correction, the auxiliary section is coupled to the output data bus to supplement the conventional memory, thereby providing increased memory capacity and improving speed of the system.

[0010] One embodiment of the invention also includes a dedicated ECC memory, which could be located on the motherboard. A secondary multiplexer receives data from the dedicated ECC memory at one input and data from the primary multiplexer at a second input. The primary and secondary multiplexers are controlled by software or hardware to establish the amount of ECC memory being used. For error intolerant applications, the primary multiplexer is activated to couple data from the auxiliary section to one input of the secondary multiplexer. The secondary multiplexer is then activated to couple data from both the primary multiplexer and the dedicated ECC memory to the error correction circuit. Thus, the auxiliary section is used to supplement the dedicated ECC memory in error intolerant applications where additional ECC memory is desirable.

[0011] In one embodiment, the second input of the secondary multiplexer is coupled to a set of memory sockets on the motherboard. The secondary multiplexer selectively couples only those sockets containing memory chips to the error correction circuit. Also, the primary and secondary multiplexers are controlled to select an appropriate portion of the auxiliary section to supplement the dedicated ECC memory, according to the ECC data requirements of an application and the amount of available dedicated ECC memory.

[0012] In one embodiment, the auxiliary section is segmented into two sections. The first section is used to supplement the dedicated ECC memory from the motherboard. The second section is used as a supplement to the conventional memory. To accommodate the difference in word length caused by segmenting of the auxiliary section, the second section is "double-written" and "double-read" so that data is written to and read from the second section in

two or more pieces. When reading the data, the two or more pieces are combined to form the complete written data.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] **FIG. 1** is a block diagram of a memory system according to an embodiment of the invention on which a memory device is selectively coupled to either an output data bus or to an error correction circuit by a primary multiplexer.

[0014] **FIG. 2** is a more detailed block diagram of the memory system of **FIG. 1** coupled to a memory controller.

[0015] **FIG. 3** is a block diagram of another embodiment of the memory system of **FIG. 1**.

[0016] **FIG. 4** is a block diagram of still another embodiment of the memory system of **FIG. 1**.

[0017] **FIG. 5** is a block diagram of a computer system according to one embodiment of the invention including input and output devices, a processor, and the memory system of **FIG. 1**.

DETAILED DESCRIPTION OF THE INVENTION

[0018] As shown in **FIG. 1, a** memory system **40** according to an embodiment of the invention includes as its central storage element a memory array **42** having at least one low-order bank **44** and at least one high-order bank **46**. The memory array **42** is formed from one or more integrated memory devices. The devices may be any suitable type of memory device, such as dynamic random access memories (DRAMs), static RAMs (SRAMs), or non-volatile memory devices. The memory devices may also be synchronous or asynchronous, or some other variety of memory device.

[0019] Data that are to be written to and read from the memory array **42** are coupled to and from the array **42** along a 64-bit primary data path **48** and a 64-bit auxiliary data path **50**, respectively. The primary data path **48** extends directly from the low order banks **44** to a data bus **52**. Although the embodiment of **FIG. 1** uses 64-bit buses **48**, **50**, it will be better understood that higher or lower capacity buses may be used.

[0020] The auxiliary data path **50** is coupled to a primary multiplexer **54**, which is a 64-bit, 1-to-2 multiplexer. In response to a mode select input MODE, the primary multiplexer **54** selectively couples data from the high order banks **46** to either the data bus **52** or to an error correction circuit **56**. The high order banks **46** can therefore provide storage for ECC bits or can provide storage to supplement the primary section **44**.

[0021] **FIG. 2** shows the memory system **40** of **FIG. 1** in greater detail in conjunction with a separate error correction memory (ECC memory) **58**. In this embodiment, the memory array **42** includes eight memory banks $\mathbf{60}_0$-$\mathbf{60}_7$ where the first seven banks $\mathbf{60}_0$-$\mathbf{60}_6$ correspond to the low order banks of **FIG. 1** and the eighth memory bank $\mathbf{60}_7$ corresponds to the high order bank **46** of **FIG. 1**. The output of the eighth bank $\mathbf{60}_7$ is input to the primary multiplexer **54** through the auxiliary data path **50** while the outputs of the first seven banks $\mathbf{60}_0$-$\mathbf{60}_6$ are connected directly to the data bus **52**.

[0022] Switching of the primary multiplexer **54** is controlled by a memory controller **63** through a mode signal MODE, in response to either software or hardware commands. Depending upon the state of the mode signal MODE, the primary multiplexer **54** couples data from the eighth data bank $\mathbf{60}_7$ to either the data bus **52** or to a secondary multiplexer **64**. If the mode signal MODE is high, the primary multiplexer **54** directs data to the data bus **52**. If the mode signal MODE is low, the primary multiplexer **54** directs data to the secondary multiplexer **64**.

[0023] Like the primary multiplexer **54**, the secondary multiplexer **64** includes eight, 8-bit 2-to-1 multiplexers, rather than eight, 8-bit 1-to-2 multiplexers. Thus, the **64** outputs of the primary multiplexer **54** are coupled to a first set of **64** inputs of the secondary multiplexer **64**. The second set of **64** inputs of the secondary multiplexer **64** is coupled to the ECC memory **58**. When enabled by the mode signal MODE and by an error correction enable signal ECCENABLE, the secondary multiplexer **64** couples one of eight 8-bit bytes of ECC data to the error correction circuit **56** as determined by a SELECT input from the memory controller. The first two 8-bit bytes of ECC data are supplied by respective ECC chips **68** in the ECC memory **58**. The remaining six 8-bit bytes are supplied by the high order banks **46** through the primary multiplexer **54**.

[0024] The error correction circuit **56** operates on the 8 bits of ECC data ECC_0-ECC_7 to identify and correct errors according to conventional error correction techniques, such as Hamming code or similar correction algorithms. The error correction circuit **56** may be implemented as dedicated hardware or as a software program in a processor **210** (**FIG. 5**).

[0025] In operation, the memory system **40** can operate in either an error tolerant mode or an error intolerant mode. In the error tolerant mode, the primary multiplexer **54** couples the high order bank $\mathbf{60}_7$ to the data bus **52** so that all 8 banks $\mathbf{60}_0$-$\mathbf{60}_7$ are used for storing data. In the error intolerant mode, the primary multiplexer **54** couples the high order bank $\mathbf{60}_7$ to the secondary multiplexer **64**, the secondary multiplexer **64** then couples the high order bank $\mathbf{60}_7$ to the error correction circuit **56**. Alternatively, the secondary multiplexer **64** can couple the ECC memory **68** to the error correction circuit **56**. In either case, when data are written to the low order banks $\mathbf{60}_0$-$\mathbf{60}_6$, 8 ECC check bits are applied to the error correction circuit **56**. The error correction circuit **56** then couples 64 bits to the high order banks $\mathbf{60}_7$ through the secondary multiplexer **64** and the primary multiplexer **54**.

[0026] During a read operation, data are coupled from the low order banks $\mathbf{60}_0$-$\mathbf{60}_6$ to the data bus **52**, and corresponding ECC data are coupled from the high order bank $\mathbf{60}_7$ through the multiplexer **54**, **64** to the error correction circuit **56**. The error correction circuit **56** then checks the 8 ECC bits in a conventional manner to detect and correct errors in the data coupled to the data bus **52**.

[0027] **FIG. 3** shows the system of **FIG. 2** where the error correction implementation is less robust, i.e., ECC data is supplied only by the ECC memory **58** on the mother board. Consequently, the two ECC chips **68** in the ECC memory **58** provide the ECC data for banks $\mathbf{60}_0$ and $\mathbf{60}_1$ only. The secondary multiplexer **64** thus outputs only the ECC data for the banks $\mathbf{60}_0$ and $\mathbf{60}_1$ to the error correction circuit **56**. More

memory chips would need to be added to ECC memory **58** in order to support more databanks $\mathbf{60}_2$-$\mathbf{60}_6$.

[**0028**] **FIG. 4** shows another embodiment of the invention in which the ECC memory **58** includes four ECC chips **68** and which uses an error correction algorithm involving 8-bits of ECC data ECC_0-ECC_7. The four ECC chips **68** supply the ECC data for banks $\mathbf{60}_0$-$\mathbf{60}_3$. Therefore, only half of the high order bank $\mathbf{60}_7$ is used for error correction of banks $\mathbf{60}_4$-$\mathbf{60}_7$, leaving half of the high order bank $\mathbf{60}_7$ free for conventional memory use. Instead of leaving half of the high order bank $\mathbf{60}_7$ unused, the high order bank $\mathbf{60}_7$ is broken into two subsections **46**A, **46**B where the first subsection **46**A contains ECC data and the second subsection **46**B is used as conventional memory to supplement the low order banks $\mathbf{60}_0$-$\mathbf{60}_6$. The first subsection **46**A provides the second four 8-bit bytes of error correction data used for memory bank $\mathbf{60}_0$-$\mathbf{60}_3$ to the secondary multiplexer **64** through the primary multiplexer **54** in a similar fashion to that described above for **FIG. 2**. The secondary multiplexer **64** selects either the onboard ECC data for banks $\mathbf{60}_4$-$\mathbf{60}_7$ or the auxiliary ECC data for banks $\mathbf{60}_0$-$\mathbf{60}_3$.

[**0029**] The second subsection **46**B of the high order bank $\mathbf{60}_7$ is not wasted. Instead, the second subsection **46**B provides data to the data bus **52** through the primary multiplexer **54**. One skilled in the art will recognize that the second subsection **46**B will only be comprised of a memory bank that is half the depth of the banks $\mathbf{60}_0$-$\mathbf{60}_6$. Since the high order bank $\mathbf{60}_7$ cannot both supply data and ECC bits simultaneously, the on board ECC memory **58** must supply the ECC data for the second subsection of the high order bank $\mathbf{60}_7$.

[**0030**] **FIG. 5** is a block diagram of a computer system **200** that uses one of the embodiments of **FIG. 2**-**4**. The computer system **200** includes a processor **210** for performing computer functions, such as executing software to perform desired calculations and tasks. The processor **210** accesses the memory module **40** and ECC memory **58** through the data bus **52** by activating the memory controller **63** which, in turn, controls the multiplexers **54**, **64**. The memory module **40** and the ECC memory **58** are preferably mounted at separate locations within the computer system **200** with the ECC memory **58** being mounted to a common board with the processor **210**. The memory module **40** and ECC memory **58** are coupled to the processor **210** through the data bus **52**. The processor **210** is also coupled to the error correction circuit **56** to receive error detection and correction information that the processor **210** uses to control the memory controller **63**. One or more input devices **214**, such as a keypad or a mouse, are coupled to the processor **210** through an I/O controller **216** and allow an operator (not shown) to manually input data thereto. One or more output devices **218** are coupled to the processor **210** through the I/O controller to provide to the operator data generated by the processor **210** or retrieved from the memory module **40**. Examples of output devices **218** include a printer and a video display unit. One or more mass data storage devices **220** are preferably coupled to the processor **210** through the I/O controller **216** to store data in or retrieve data from the storage device **220**. Examples of the storage devices **220** include disk drives and compact disk read-only memories (CD-ROMs).

[**0031**] While the present invention has been described herein by way of exemplary embodiments, various modifications may be made without departing from the scope of the invention. For example, the number of ECC chips **68** in the ECC memory **58** may be larger or smaller. Also, the secondary multiplexer **64** can be configured to vary the multiplexing of the ECC data in response to the enable signal ECC ENABLE, so that the combination of bits from the ECC memory **58** and auxiliary section **46** can be controlled remotely by the memory controller **63**. Additionally, the high order bank **46** may include more than one bank of the memory array **42**. Further, the memory array **42** may include fewer or more than eight banks. And, the ECC memory **58** can be located off the motherboard in some applications. Moreover, the error correction circuit **56** and/or the memory controller **63** can be implemented in whole or in part by the processor **210** in response to software. Also, the number of bits in each bank or on the data busses may be fewer than or more than the 64-bit bus structure described herein. Accordingly, the invention is not limited except as by the appended claims.

1. A memory control circuit for a computer system, comprising:

a memory system having a plurality of memory locations corresponding to respective addresses;

an error correction circuit;

a data bus coupled to a first set of memory locations of the memory system; and

a coupling device coupling a second set of memory locations of the memory system to the error correction circuit.

2. The memory control circuit of claim 1 wherein the coupling device comprises a first switching circuit having a first data port coupled to the second set of memory locations of the memory system, a second data port coupled to the data bus, a third data port coupled to the error correction circuit, and a mode select input, the switching circuit being operable responsive to a first mode select signal to couple the first data port to the second data port, and being operable responsive to a second mode select signal to couple the first data port to the third data port.

3. The memory control circuit of claim 2 further comprising an error correction memory, and wherein the coupling circuit further comprises a second switching circuit having a first data port coupled to the third data port of the first switching circuit, a second data port coupled to the error correction memory, a third data port coupled to the error correction circuit, and a control input, the second switching circuit being operable responsive to a first control signal to couple the first data port to the third data port, and being operable responsive to a second control signal to couple the second data port to the third data port.

4. The memory control circuit of claim 3 wherein the data ports of the first switching circuit comprise a first plurality of sets of data lines, and the second data port of the second switching circuit comprises a second plurality of sets of data lines, the second switching circuit being operable responsive

to the first control signal to couple one of the sets in the first plurality of sets of data lines to the error correction circuit, and being operable responsive to the second control signal to couple one of the sets in the second plurality of sets of data lines to the error correction circuit.

5. The memory control circuit of claim 2 further comprising an error correction memory, and wherein the switching circuit comprises:

a first multiplexer having a first data port coupled to the second set of locations of the memory system, a second data port coupled to the data bus, a third data port, and a control input, the first multiplexer being operable responsive to a first control signal applied to the control input to couple the first data port to the second data port, and being operable responsive to a second control signal to couple the first data port to the third data port; and

a second multiplexer having a first data port coupled to the third data port of the first multiplexer, a second data port coupled to the error correction memory, a third data port coupled to the error correction circuit, and a control input, the second multiplexer being operable responsive to a third control signal applied to the control input to couple the first data port to the third data port, and being operable responsive to a fourth control signal to couple the second data port to the third data port.

6. The memory control circuit of claim 1 wherein the memory system comprises a memory device having a plurality of banks.

7. The memory control circuit of claim 6 wherein the first set of memory locations of the memory system comprise a first set of banks of the memory device, and the second set of memory locations of the memory system comprise a second set of banks of the memory device.

8. The memory control circuit of claim 7 wherein the second set of banks comprises a single bank.

9. The memory control circuit of claim 7 wherein the second set of banks comprise a first set of memory locations coupled to the data bus, and a second set of memory locations coupled to the error correction circuit.

10. The memory control circuit of claim 1 wherein the memory system comprises:

a first memory device having a plurality of banks, a first set of banks of the first memory device being coupled to the data bus; and

a set of second memory devices.

11. The memory control circuit of claim 10 wherein the coupling device comprises a switching circuit having a plurality of first data ports coupled to respective second memory devices in the set of second memory devices, a second data port coupled to the error correction circuit, and a control input, the switching circuit being operable responsive to a control signal applied to the control input to couple one of the first data ports to the second data port responsive to a corresponding control signal.

12. An memory system operable in either normal mode or an error correcting mode, comprising:

a memory device having a plurality of banks;

a data bus coupled to a first set of banks of the memory device;

an error correction circuit;

a first switching circuit having a first port coupled to at least one bank of the memory device, a second port coupled to the data bus, a third port coupled to the error correction circuit, and a mode input coupled to receive a mode signal having a first state indicative of the normal mode and a second state indicative of the error correcting mode, the first switching circuit being structured to couple the first port to the second port responsive to a mode signal having the first state and to couple the first port to the third port responsive to a mode signal having the second state.

13. The memory system of claim 12 wherein the bank of the memory device to which the first port of the first switching circuit is coupled comprises a bank of the memory device other than an bank in the first set.

14. The memory system of claim 12 wherein the bank of the memory device to which the first port of the first switching circuit is coupled comprises one of the banks in the first set of banks of the memory device, a first plurality of memory locations in the bank being coupled to the data bus and a second plurality of memory locations in the bank being coupled to the first port of the first switching circuit.

15. An memory system operable in either normal mode or an error correcting mode, comprising:

a first memory device having a plurality of banks;

a second memory device;

a data bus coupled to a first set of banks of the first memory device;

an error correction circuit;

a first switching circuit having a first port coupled to at least one bank of the first memory device, a second port coupled to the data bus, a third port, and a mode input coupled to receive a mode signal having a first state indicative of the normal mode and a second state indicative of the error correcting mode, the first switching circuit being structured to couple the first port to the second port responsive to a mode signal having the first state and to couple the first port to the third port responsive to a mode signal having the second state; and

a second switching circuit having a first plurality of signal terminal sets coupled to the third port of the first switching circuit, a second plurality of signal terminal sets coupled to the second memory device, a set of signal terminals coupled to the error correction circuit, and a select input coupled to receive a select signal, the second switching circuit being structured to couple the one of the signal terminal sets in the first plurality or one of the signal terminal sets in the second plurality to the error correction circuit responsive to the select signal.

16. The memory system of claim 15 wherein the bank of the memory device to which the first port of the first switching circuit is coupled comprises a bank of the memory device other than an bank in the first set.

17. The memory system of claim 15 wherein the bank of the memory device to which the first port of the first switching circuit is coupled comprises one of the banks in the first set of banks of the memory device, a first plurality of memory locations in the bank being coupled to the data

bus and a second plurality of memory locations in the bank being coupled to the first port of the first switching circuit.

18. A computer system, comprising:

a processor;

a data bus;

a peripheral device coupled to the processor;

a memory system having a plurality of memory locations, a first set of the memory locations being coupled to the data bus;

an error correction circuit;

a coupling device coupling a second set of memory locations of the memory system to the error correction circuit.

19. The computer system of claim 18, wherein the memory correction circuit includes a memory correction port, and wherein the processor is coupled to the memory correction port and to the data bus, the processor being structured to couple data to or from the data bus and a corresponding error correction code to or from the memory correction port, respectively.

20. The computer system of claim 18 wherein the coupling device comprises a first switching circuit having a first data port coupled to the second set of memory locations of the memory system, a second data port coupled to the data bus, a third data port coupled to the error correction circuit, and a mode select input, the switching circuit being operable responsive to a first mode select signal to couple the first data port to the second data port, and being operable responsive to a second mode select signal to couple the first data port to the third data port.

21. The computer system of claim 19 further comprising an error correction memory, and wherein the coupling circuit further comprises a second switching circuit having a first data port coupled to the third data port of the first switching circuit, a second data port coupled to the error correction memory, a third data port coupled to the error correction circuit, and a control input, the second switching circuit being operable responsive to a first control signal to couple the first data port to the third data port, and being operable responsive to a second control signal to couple the second data port to the third data port.

22. The computer system of claim 21 wherein the data ports of the first switching circuit comprise a first plurality of sets of data lines, and the second data port of the second switching circuit comprises a second plurality of sets of data lines, the second switching circuit being operable responsive to the first control signal to couple one of the sets in the first plurality of sets of data lines to the error correction circuit, and being operable responsive to the second control signal to couple one of the sets in the second plurality of sets of data lines to the error correction circuit.

23. The computer system of claim 20 further comprising an error correction memory, and wherein the switching circuit comprises:

a first multiplexer having a first data port coupled to the second set of locations of the memory system, a second data port coupled to the data bus, a third data port, and a control input, the first multiplexer being operable responsive to a first control signal applied to the control input to couple the first data port to the second data port, and being operable responsive to a second control signal to couple the first data port to the third data port; and

a second multiplexer having a first data port coupled to the third data port of the first multiplexer, a second data port coupled to the error correction memory, a third data port coupled to the error correction circuit, and a control input, the second multiplexer being operable responsive to a third control signal applied to the control input to couple the first data port to the third data port, and being operable responsive to a fourth control signal to couple the second data port to the third data port.

24. The computer system of claim 18 wherein the memory system comprises a memory device having a plurality of banks.

25. The computer system of claim 24 wherein the first set of memory locations of the memory system comprise a first set of banks of the memory device, and the second set of memory locations of the memory system comprise a second set of banks of the memory device.

26. The computer system of claim 25 wherein the second set of banks comprises a single bank.

27. The computer system of claim 25 wherein the second set of banks comprise a first set of memory locations coupled to the data bus, and a second set of memory locations coupled to the error correction circuit.

28. The computer system of claim 18 wherein the memory system comprises:

a first memory device having a plurality of banks, a first set of banks of the first memory device being coupled to the data bus; and

a set of second memory devices.

29. The computer system of claim 28 wherein the coupling device comprises a switching circuit having a plurality of first data ports coupled to respective second memory devices in the set of second memory devices, a second data port coupled to the error correction circuit, and a control input, the switching circuit being operable responsive to a control signal applied to the control input to couple one of the first data ports to the second data port responsive to a corresponding control signal.

30. A method of storing and retrieving data in a memory system operable in either an error tolerant mode or an error intolerant mode, the method comprising:

coupling a first plurality of locations of the memory system to a data bus so that data applied to the data bus can be written to the first plurality of locations of the memory system and data read from the first plurality of locations of the memory system can be applied to the data bus;

coupling a second plurality of locations of the memory system to the data bus when the memory system is operating in the error tolerant mode; and

coupling the second plurality of locations of the memory system to an error correction circuit when the memory system is operating in the error intolerant mode.

31. The method of claim 30 wherein the first and second plurality of locations of the memory system comprise different banks of a single memory device.

32. The method of claim 30 wherein the first and second plurality of locations of the memory system comprise different memory devices.

33. The method of claim 30, further comprising:

applying data to the data bus when the memory system is operating in the error intolerant mode;

applying a corresponding error correction code to the error correction circuit, the error correction code coupling corresponding error correction bits to the second plurality of locations of the memory system;

writing the data in at least some of the memory locations in the first plurality of locations of the memory system;

writing the error correction bits in at least some of the memory locations in the second plurality of locations of the memory system;

reading data from at least some of the memory locations in the first plurality of locations of the memory system;

reading error correction bits from at least some of the memory locations in the second plurality of locations of the memory system, the read error correction bits corresponding to the data read from the memory locations in the first plurality;

determining from the error correction bits if the read data is in error; and

if the read data is determined to be in error, correcting the read data.

34. A method of storing data in a memory device having first and second memory portions, comprising:

selecting either an error correction mode or a non-error correction mode;

storing data in the first memory portion;

if the error correction mode is selected, storing error correction bits corresponding to the data in the second memory portion; and

if the non-error correction mode is selected, storing information data in the second memory portion.

35. The method of claim 34 further comprising:

retrieving data from the first memory portion;

if the error correction mode is selected, retrieving error correction bits corresponding to the data from the second memory portion; and

if the non error correction mode is selected, retrieving data from the second memory portion.

36. The method of claim 35 further comprising, if the error correction mode is selected:

determining from the error correction bits if the retrieved data is in error; and

if the retrieved data is determined to be in error, correcting the retrieved data using the error correction bits.

37. The method of claim 34 wherein the storing of data in the second memory portion comprises:

storing a first segment of a data byte in a first location having a first address in the second memory portion; and

storing a second segment of the data byte in a second location having a second address in the second memory portion.

38. The method of claim 37, further comprising:

retrieving the stored first segment from the first location at a first time;

retrieving the stored second segment from the second location at a second time different from the first time; and

combining the retrieved first and second segments.

39. A method of retrieving data from a memory device having first and second memory portions, comprising:

selecting either an error correction mode or a non-error correction mode;

retrieving data from the first memory portion;

if the error correction mode is selected, retrieving error correction bits corresponding to the data from the second memory portion; and

if the non-error correction mode is selected, retrieving data from the second memory portion.

40. The method of claim 39 further comprising, if the error correction mode is selected:

determining from the error correction bits if the retrieved data is in error; and

if the retrieved data is determined to be in error, correcting the retrieved data using the error correction bits.

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