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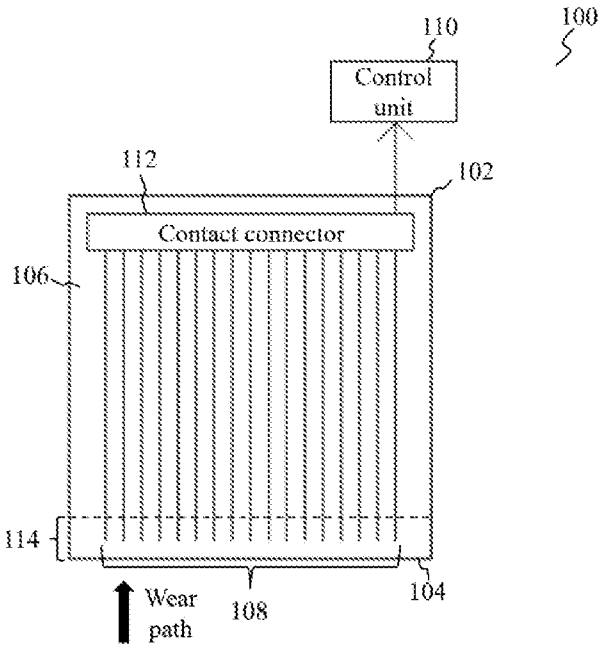
US 6384721 B1 US 2020/0039027 A1 GB 2553585 A WO 87/04236 A1 JP 2020148774 A

(57) Tiivistelmä - Sammandrag - Abstract

Esillä oleva julkaisu koskee kulumisen havaitsevaa laitetta (100; 200; 300; 400), joka sallii yhden tai useamman kulumispinnan (104; 204; 304, 306, 308; 404) kulumisasteen seuraamisen tehokkaasti niin makromittakaavassa kuin myös mikromittakaavassa ja nanomittakaavassa. Tätä varten laite (100; 200; 300; 400) käsittää ryhmän (108; 208; 312; 408) pitkänomaisia tasomaisia johtimia, jotka ulottuvat keskenään yhdensuuntaisesti dielektrisen alustan (102; 202; 302; 402) kuvioidulla pinnalla (106; 206; 310; 406) dielektrisen materiaalikerroksen alla. Jokainen johtimista on kytketty ohjausyksikköön (110; 210; 314; 410). Kun kulumista tapahtuu dielektrisen alustan (102; 202; 302; 402) ainakin yhdellä kulumispinnalla (104; 204; 304, 306, 308; 404), joka on kuvioidun pinnan (106; 206; 310; 406) vieressä, ohjausyksikkö (110; 210; 314; 410) määrittää kulumisasteen seuraamalla ja analysoimalla jokaisen kahden vierekkäisen johtimen välistä kapasitanssia. Ohjausyksikkö (110; 210; 314; 410) antaa sitten kulumisasteen käyttäjälle. Erityisessä suoritusmuodossa ohjausyksikkö (110; 210; 314; 410) voi käyttää seurattuja kapasitansseja sen määrittämiseksi, onko ainakin kaksi johdinta ryhmästä (108; 208; 312; 408) johtimia tullut suoraan sähköiseen kontaktiin kulumisen aikana, ja antaa käyttäjälle vastaavan signaalin.

The present disclosure relates to a wear sensing apparatus (100; 200; 300; 400) that allows a wear rate of one or more wear surfaces (104; 204; 304, 306, 308; 404) to be efficiently monitored not only at macroscales but also at microscales and nanoscales. For this purpose, the apparatus (100; 200; 300; 400) comprises an array (108; 208; 312; 408) of elongated planar conductors extending parallel to each other on a patterned surface (106; 206; 310; 406) of a dielectric substrate (102; 202; 302; 402) under a layer of dielectric material. Each of the conductors is coupled to a control unit (110; 210; 314; 410). When wear occurs on at least one wear surface (104; 204; 304, 306, 308; 404) of the dielectric substrate (102; 202; 302; 402) which is adjacent to the patterned surface (106; 206; 310; 406), the control unit (110; 210; 314; 410) determines a wear rate by monitoring and analysing a capacitance between each two adjacent conductors. The control unit (110; 210; 314; 410) then outputs the wear rate to a user. In a particular embodiment, the control unit (110; 210; 314; 410) may use the monitored capacitances to determine whether at least two conductors of the array (108; 208; 312; 408) of conductors have been brought into a direct electric contact during the wear, and output a corresponding signal to the user.



WEAR SENSING APPARATUS

TECHNICAL FIELD

The present disclosure relates generally to techniques for monitoring characteristics of machine or tool components and other materials which are exposed to mechanical wear. More particularly, the present disclosure relates to an apparatus for sensing the mechanical wear of such components or materials not only at macroscales but also at microscales and nanoscales.

BACKGROUND

Mechanical wear is a typical physical phenomenon observed in a variety of mechanical systems, such, for example, as industrial, agricultural and other machines or tools, tribology testing equipment, surface finishing equipment, etc. The mechanical wear consists in the damaging and gradual removal of material from contacting solid surfaces of machine or tool components. In particular, the relative motion of two contacting solid surfaces can cause damage to one or both of them. This damage manifests itself as a progressive loss of material, i.e., as material particles detached from the contacting solid surface(s). The detached material particles are also referred to as wear debris.

Given this, it is usually necessary to monitor a degree of wear (also referred to as a wear rate or wear depth) associated with a particular mechanical system. This monitoring may be performed by manual inspection or by using wear sensors. In some situations where the manual inspection is physically impossible or requires significant machine or equipment downtime, the wear sensors are the only viable option to use.

The existing wear sensors are usually based on using an electrical circuit of resistive or capacitive

elements that are connected in parallel on or under a wear surface. When wear occurs on such a wear sensor, the resistive or capacitive elements (typically, surface mount resistors or capacitors) are electrically decoupled from the circuit one by one, thereby changing a total measurable electrical characteristic (e.g., total measurable resistance or capacitance) of the circuit.

The existing wear sensors are good to monitor the degree of wear at macroscales but may not be as effective at microscales and nanoscales due to the above-described sensor design.

SUMMARY

This summary is provided to introduce a selection of concepts in a simplified form that are further described below in the detailed description. This summary is not intended to identify key features of the present disclosure, nor is it intended to be used to limit the scope of the present disclosure.

The objective of the present disclosure is to provide a wear sensing apparatus that allows a wear rate of one or more wear surfaces to be efficiently monitored (in real time) not only at macroscales but also at microscales and nanoscales.

The objective above is achieved by the features of the independent claim in the appended claims. Further embodiments and examples are apparent from the dependent claims, the detailed description and the accompanying drawings.

According to a first aspect, a wear sensing apparatus is provided. The apparatus comprises a dielectric substrate having at least one wear surface and a patterned surface adjacent to the at least one wear surface. The apparatus further comprises an array

of conductors extending parallel to each other on the patterned surface of the dielectric substrate. Each conductor of the array of conductors has an elongated planar shape. The apparatus further comprises a dielectric material covering the patterned surface of the dielectric substrate together with the array of conductors, and a control unit coupled to each conductor of the array of conductors. The control unit is configured, when wear occurs on the at least one wear surface of the dielectric substrate, to monitor a capacitance between each two adjacent conductors of the array of conductors and use the monitored capacitances to determine a wear rate of the dielectric substrate. The control unit is further configured to output the wear rate to a user. The apparatus thus configured may be efficiently used to monitor the wear rate not only at macroscales but also at microscales and nanoscales, without having to inspect the wear surface(s) with any additional equipment, e.g., a microscope. Furthermore, the apparatus thus configured may allow one to observe or detect scratches, cracks and relief when wear occurs on the at least one wear surface of the dielectric substrate.

In one exemplary embodiment, the control unit is further configured to use the monitored capacitances to determine whether at least two conductors of the array of conductors have been brought into a direct electric contact during the wear. If the at least two conductors of the array of conductors have been brought into the direct electric contact during the wear, the control unit is further configured to output a signal (e.g., visual, acoustic, vibration, or any combination thereof) to the user. In response to such a signal, the user may terminate or properly tune a wear process. Furthermore, this functionality of the control unit may allow the apparatus to be used not only for monitoring the wear but also for detecting the occurrence of

smearing (surface deformation or plastic deformation). The possibility of detecting the occurrence of smearing is especially important when processing materials (e.g., during cutting, grinding and polishing processes).

In one exemplary embodiment, the at least one wear surface comprises a single wear surface, and each conductor of the array of conductors is straight and extends perpendicular to the wear surface. This conductor configuration may be efficiently used if it is required to monitor the wear rate of the single wear surface.

In one exemplary embodiment, each conductor of the array of conductors has a curved shape. This may provide a variety of conductor configurations, each of which may be useful in a particular apparatus application.

In one exemplary embodiment, the at least one wear surface comprises a single wear surface, and each conductor of the array of conductors comprises a first portion perpendicular to the wear surface and a second portion parallel to the wear surface. This conductor configuration may be efficiently used if it is required to monitor the wear rate of the single wear surface.

In one exemplary embodiment, the at least one wear surface comprises two or three wear surfaces, and each conductor of the array of conductors has a circular shape. This circular conductor configuration may be efficiently used if it is required to monitor the wear rate of the two or more wear surfaces.

In one exemplary embodiment, the at least one wear surface comprises a single wear surface, and each conductor of the array of conductors comprises a first portion and a second portion. The first portion and the second portion originate from a single point and diverge in a direction away from the wear surface. This conductor configuration may be efficiently used if it

is required to monitor the wear rate of the single wear surface.

In one exemplary embodiment, each conductor of the array of conductors has a triangular shape. The triangular shape of the parallel conductors may be efficiently used if it is required to monitor the wear rate of the single wear surface.

In one exemplary embodiment, the array of conductors has an equal inter-conductor spacing. The equal inter-conductor spacing may allow the user to monitor the wear rate (and the smearing effect, if present) in percentage terms. For example, if there are 100 conductors extending parallel to each other on the dielectric substrate, and if the capacitance measurements show that only the first 32 conductors (when counted from the wear surface, e.g., in case of any of the above-indicated curved conductor configurations) were subjected to wear, then the wear rate may be set to 32%.

In one exemplary embodiment, the array of conductors has a varying inter-conductor spacing. The varying inter-conductor spacing may allow the user to monitor the wear rate (and the smearing effect, if present) in length units (e.g., in microns). For example, if each subsequent inter-conductor spacing is greater than the previous one by 1 μm, and if the capacitance measurements show that only the first 3 conductors (when counted from the wear surface, e.g., in case of any of the above-indicated curved conductor configurations) were subjected to wear, then the wear rate may approximately (without considering the conductor width) be set to $3 \times (x + 1)$ μm, where x is the width of the first inter-conductor spacing.

In one exemplary embodiment, the array of conductors has a varying inter-conductor spacing that increases or decreases in a direction away from each of the at least one wear surface of the dielectric

substrate. By using such an increasing or decreasing inter-conductor spacing, it is possible to provide different levels of granularity (resolution) for the monitored wear rate in the direction from the wear surface (i.e., within a wear path). In other words, the inter-conductor spacing may be selected based on how finely the user wants to monitor the material removal from the wear surface(s) within the wear path. For example, a higher level of granularity may be required if the wear rate reaches a critical level. Thus, the conductors may be arranged closer to each other at a certain position within the wear path compared to the conductors at another position.

In one exemplary embodiment, the inter-conductor spacing ranges from about 5 nm to about 10 mm (or varies within any subranges of this spacing range, such, for example, as from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm, etc.). By using this spacing range, it is possible to monitor the wear rate (and the smearing effect, if present) at an acceptable level of granularity.

In one exemplary embodiment, the array of conductors comprises a first subarray of conductors and a second subarray of conductors. The first subarray of conductors and the second subarray of conductors are non-overlapping. In this embodiment, the first subarray of conductors has an equal inter-conductor spacing and the second subarray of conductors has a varying inter-conductor spacing. By using such inter-conductor spacings for the first and second subarrays of conductors, it is possible to provide different levels of granularity (resolution) for the monitored wear rate within the wear path.

In one exemplary embodiment, the inter-conductor spacing of each of the first subarray of

conductors and the second subarray of conductors ranges from about 5 nm to about 10 mm (or varies within any subranges of this spacing range, such, for example, as from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm, etc.). By using this spacing range, it is possible to monitor the wear rate (and the smearing effect, if present) at an acceptable level of granularity.

In one exemplary embodiment, the array of conductors comprises a first subarray of conductors and a second subarray of conductors. The first subarray of conductors and the second subarray of conductors are non-overlapping. In this embodiment, the first subarray of conductors has a first equal inter-conductor spacing and the second subarray of conductors has a second equal inter-conductor spacing. The second equal inter-conductor spacing is different from the first equal inter-conductor spacing. By using such inter-conductor spacings for the first and second subarrays of conductors, it is possible to provide different levels of granularity (resolution) for the monitored wear rate within the wear path.

In one exemplary embodiment, each of the first equal inter-conductor spacing and the second equal inter-conductor spacing ranges from about 5 nm to about 10 mm (or varies within any subranges of this spacing ranges, such, for example, as from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm, etc.). By using this spacing range, it is possible to monitor the wear rate (and the smearing effect, if present) at an acceptable level of granularity.

In one exemplary embodiment, each conductor of the array of conductors is made of a ductile material (e.g., gold, silver, aluminum, copper, titanium, nickel,

any alloy thereof, as well as any conducting polymer, conducting co-polymer, or any semiconductor material belonging to groups III-V of Mendeleev's periodic table, etc.). The ductile material may be advantageous especially when the apparatus is also used for detecting and monitoring the smearing effect. Moreover, ductile material may simplify the fabrication of different curved conductors on the dielectric substrate, if required.

In one exemplary embodiment, the dielectric substrate is made of glass, silicon, SiO_2, epoxy, a polymer, a semiconductor, ceramics, SiC, a nonconducting polymer, a nonconducting copolymer, or any combination thereof. These materials have proper dielectric properties, thereby allowing no direct electric contact between the conductors through the substrate.

In one exemplary embodiment, each conductor of the array of conductors has a width ranging from about 5 nm to about 10 mm, and a thickness ranging from about 5 nm to about 10 mm. It should be noted the width and thickness of each conductor may vary within any subranges of this range, such, for example, from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm, etc. By using these conduction dimensions, it is possible to monitor the wear rate (and the smearing effect, if present) at an acceptable level of granularity.

Other features and advantages of the present disclosure will be apparent upon reading the following detailed description and reviewing the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is explained below with reference to the accompanying drawings in which:

FIG. 1 shows a schematic block diagram of a wear sensing apparatus in accordance with a first exemplary embodiment;

FIG. 2 shows a schematic block diagram of a wear sensing apparatus in accordance with a second exemplary embodiment;

FIG. 3 shows a schematic block diagram of a wear sensing apparatus in accordance with a third exemplary embodiment;

FIG. 4 shows a schematic block diagram of a wear sensing apparatus in accordance with a fourth exemplary embodiment; and

FIG. 5 shows a schematic block diagram of a wear sensing apparatus in accordance with a fifth exemplary embodiment.

DETAILED DESCRIPTION

Various embodiments of the present disclosure are further described in more detail with reference to the accompanying drawings. However, the present disclosure may be embodied in many other forms and should not be construed as limited to any certain structure or function discussed in the following description. In contrast, these embodiments are provided to make the description of the present disclosure detailed and complete.

According to the detailed description, it will be apparent to the ones skilled in the art that the scope of the present disclosure encompasses any embodiment thereof, which is disclosed herein, irrespective of whether this embodiment is implemented independently or in concert with any other embodiment of the present disclosure. For example, the apparatus disclosed herein may be implemented in practice using any numbers of the embodiments provided herein. Furthermore, it should be understood that any embodiment of the present disclosure may be implemented using one

or more of the elements presented in the appended claims.

The word "exemplary" is used herein in the meaning of "used as an illustration". Unless otherwise stated, any embodiment described herein as "exemplary" should not be construed as preferable or having an advantage over other embodiments.

Any positioning terminology, such as "left", "right", "top", "bottom", "above" "below", "upper", "lower", etc., may be used herein for convenience to describe one element's or feature's relationship to one or more other elements or features in accordance with the figures. It should be apparent that the positioning terminology is intended to encompass different orientations of the apparatus disclosed herein, in addition to the orientation(s) depicted in the figures. As an example, if one imaginatively rotates the apparatus in the figures 90 degrees clockwise, elements or features described as "left" and "right" relative to other elements or features would then be oriented, respectively, "above" and "below" the other elements or features. Therefore, the positioning terminology used herein should not be construed as any limitation of the present disclosure.

Although the numerative terminology, such as "first", "second", etc., may be used herein to describe various embodiments, elements or features, these embodiments, elements or features should not be limited by this numerative terminology. This numerative terminology is used herein only to distinguish one embodiment, element or feature from another embodiment, element or feature. Thus, a first embodiment discussed below could be called a second embodiment, and vice versa, without departing from the teachings of the present disclosure.

As used in the embodiments disclosed herein, mechanical wear (hereinafter referred to as wear for

short) may refer to the continuing loss of a material from the surface of a solid body due to a mechanical action, such, for example, as the contact and relative movement of a solid or fluid counter body. In general, the term "wear" may be used for both an abrasion or attrition process and its consequences. The surface subjected to the wear is herein referred to as a wear surface, and a direction in which the wear occurs (i.e., the direction away from the wear surface) is herein referred to as a wear path. The wear thus defined may be observed in different mechanical systems relating to tribology, tool wear monitoring, surface finishing, machine wear monitoring, etc. It should be also noted that the wear may be accompanied by scratches, cracks and relief, as well as by the so-called smearing effect which may be a big problem in metallographic sample preparation from ductile materials.

As used in the embodiments disclosed herein, smearing may refer to a surface deformation/damage/wear mechanism of a material (especially, ductile materials), which is caused by plastic deformation where the material is pushed across a wear surface but, at the same time, the pushed material remains attached to the wear surface. Correspondingly, smear may be considered as a thin layer of such surface deformation/damage/wear on the surface of a prepared sample. It is commonly developed during mid to late preparation stages (e.g., diamond polishing and oxide polishing). For example, critical factors for the formation of the smearing in polishing processes are an applied load, a lubrication amount, rotation speeds and directions of a polishing plate and a sample plate, properties of a polishing pad, the amount and properties of a polishing liquid, etc.

The exemplary embodiments disclosed herein provide a technical solution that allows mitigating or even eliminating the drawbacks of the prior art which are mentioned in the description part “Background”. In

particular, the technical solution disclosed herein relates to a wear sensing apparatus that allows a wear rate of one or more wear surfaces to be efficiently monitored not only at macroscales but also at microscales and nanoscales. For this purpose, the apparatus comprises an array of elongated planar conductors extending parallel to each other on a patterned surface of a dielectric substrate. Each of the conductors is coupled to a control unit. When wear occurs on at least one wear surface of the dielectric substrate which is adjacent to the patterned surface, the control unit determines a wear rate by monitoring and analysing a capacitance between each two adjacent conductors. The control unit then outputs the wear rate to a user. In a particular embodiment, the control unit may use the monitored capacitances to determine whether at least two conductors of the array of conductors have been brought into a direct electric contact during the wear, and output a corresponding signal to the user.

FIG. 1 shows a schematic block diagram of a wear sensing apparatus 100 in accordance with a first exemplary embodiment. The apparatus 100 comprises a dielectric substrate 102 having a (bottom) wear surface 104 and a (front) patterned surface 106 adjacent to the wear surface 104. The term “adjacent” used herein means that the wear surface and the patterned surface have a common boundary or edge. The dielectric substrate 102 may be made of glass, silicon, SiO_2, epoxy, a polymer, a semiconductor, ceramics, SiC, a nonconducting polymer, a nonconducting copolymer, or any combination thereof. The apparatus 100 further comprises an array 108 of conductors extending parallel to each other on the patterned surface 106 of the dielectric substrate 102. More specifically, each conductor of the array 108 of conductors has a planar straight-line shape and extends perpendicular to the wear surface 104. The name of the patterned surface 106 is caused exactly by that it has

such a conductor pattern formed thereon. Preferably, each conductor of the array 108 of conductors may be made of a ductile material. The examples of the ductile material include, but are not limited to, gold, silver, aluminum, copper, titanium, hafnium, nickel, zirconium, or any alloy or combination thereof, as well as any conducting polymer, conducting co-polymer, or any semiconductor material belonging to groups III-V of Mendeleev's periodic table (e.g., Ge, Si). A layer of dielectric material (not shown in FIG. 1) is provided on the patterned surface 106 of the dielectric substrate 102 such that it covers not only each conductor of the array 108 of conductors but also each inter-conductor spacing. Given this, the structure formed by each two adjacent conductors and the dielectric material therebetween may be considered as a capacitor. The inter-conductor spacing may range from about 5 nm to about 10 mm, or may vary within any subranges of this spacing range, such, for example, as from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm etc. Moreover, each conductor of the array 108 of conductors may have a width and thickness both falling within the same range from about 5 nm to about 10 mm or within any subranges of this range (e.g., like the ones indicated above in respect of the inter-conductor spacing). In general, the lower limit of this range is determined by the capabilities of the existing fabrication technologies, such as lithography (e.g., photolithography), 3D-printing, atomic layer deposition (ALD), Chemical Vapor Deposition (CVD), Ultra-High Vacuum CVD (UHV-CVD), Chemical Beam Epitaxy (CBE), laser ablation, electron lithography, sputtering, electrolytic deposition (e.g., electroplating), etc. As for the upper limit of this range, it is mainly determined by what spacing is practical in a particular sensor application.

Let us now give one example of how to form the array 108 of aluminum conductors (and, if required, aluminum contact pads for the conductors) on the patterned surface 106 of the dielectric substrate 102 represented by a SiO_2 substrate. The aluminum conductors may be formed by sputtering a 100 nm thick layer of aluminum onto the SiO_2 substrate. After sputtering, the aluminum-coated SiO_2 substrate is covered with a positive photoresist (e.g., Positive-20). The photoresist is then exposed to ultraviolet (UV) light for 5 minutes using a proper patterned photomask. After said exposure, the photoresist is developed using 1% NaOH, after which the layer of aluminum is etched using a phosphoric acid-based aluminum etchant. Finally, the whole sample is cleaned with acetone to remove the leftover photoresist. Subsequently, a layer of dielectric material (e.g., epoxy, or any other dielectric material, or any combination of dielectric materials) may be formed on the SiO_2 substrate such that the aluminum conductors and the spacings therebetween are covered with the layer of dielectric material.

Those skilled in the art would recognize that the above-given example of the sample fabrication does not limit anyhow the present disclosure. In some other embodiments, any other lithography techniques (e.g., those based on using X-rays, gamma rays or electron beams instead of UV or extreme UV (EUV) light) may be used to prepare the same conductor pattern on the patterned surface 106 of the dielectric substrate 102. As one more non-restrictive example, the same conductor pattern may be formed by using any of direct laser writing, multiphoton lithography, soft lithography, or nanoimprint lithography; each of these techniques allows one to obtain relatively thick conductors, while still providing precise patterning of the conductors.

As also shown in FIG. 1, the apparatus 100 further comprises a control unit 110 coupled to each

conductor of the array 108 of conductors via a contact connector 112. Any existing contact connector may be used, which allows many conductors or wires to be individually coupled to a certain measurement device (like the control unit 110). In one alternative embodiment, wire bonding or a similar technique for connecting the array 108 of conductors with the control unit 110 may be used instead of forming the actual contact connector directly on the dielectric substrate 102; in this case, each conductor of the array 108 of conductors may have a contact pad at its one end (the contact pad is a wider area of the conductor which allows a bonding wire to be mounted thereon). In another alternative embodiment, if advanced lithography, an Ultra-High Vacuum (UHV) chamber, or Molecular Beam Epitaxy (MBE) is used to make the wear sensor 100, at least part (e.g., measurement means) of the control unit 110 may be provided directly on the dielectric substrate 102 (e.g., on the patterned surface 106 of the dielectric substrate 102).

As for the control unit 110, it may comprise a display, a processor and a memory coupled to the processor. The memory may store processor-executable instructions which, when executed by the processor, cause the processor to determine a wear rate within a wear path (see the solid arrow in FIG. 1), as will be discussed below in more detail.

The processor may be implemented as a CPU, general-purpose processor, memristor, neuromorphic computing chip, Artificial Intelligence (AI) chip (also referred to as AI hardware), single-purpose processor, microcontroller, microprocessor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), digital signal processor (DSP), complex programmable logic device, etc. It should be also noted that the processor may be implemented as any combination of one or more of the aforesaid. As an example, the

processor may be a combination of two or more microprocessors.

The memory may be implemented as a classical nonvolatile or volatile memory used in the modern electronic computing machines. As an example, the nonvolatile memory may include Read-Only Memory (ROM), ferroelectric Random-Access Memory (RAM), Programmable ROM (PROM), Electrically Erasable PROM (EEPROM), solid state drive (SSD), flash memory, magnetic disk storage (such as hard drives and magnetic tapes), memristor, optical disc storage (such as CD, DVD and Blu-ray discs), etc. As for the volatile memory, examples thereof include Dynamic RAM, Synchronous DRAM (SDRAM), Double Data Rate SDRAM (DDR SDRAM), Static RAM, non-volatile Resistive RAM (RRAM), Spin Torque Transfer Magneto-resistive (STT-MRAM), Phase-Change Memory (PCM), etc.

The processor-executable instructions stored in the memory may be configured as a computer-executable program code which causes the processor to perform the aspects of the present disclosure. The computer-executable program code for carrying out operations or steps for the aspects of the present disclosure may be written in any combination of one or more programming languages, such as Java, C++, or the like. In some examples, the computer-executable program code may be in the form of a high-level language or in a pre-compiled form and be generated by an interpreter (also pre-stored in the memory) on the fly. In other examples, if the processor is implemented as an AI chip or a neuromorphic computing chip, the computer-executable program code may be generated by the AI chip or the neuromorphic computing chip on the fly.

The display may be implemented as a liquid-crystal display (LCD), light-emitting diode (LED) display, organic LED (OLED) display, plasma display, etc.

It should be noted that the display may be excluded from the control unit 110. Instead, the control unit 110 may further comprise a transceiver, with the aid of which the control unit 110 may be configured to provide working results (i.e., the wear rate) to a user mobile device (e.g., via a mobile application installed on a user mobile phone) by using any available wireless communication standard (e.g., Bluetooth, Near-Field Communications (NFC), Radio Frequency Identification (RFID), etc.).

The operational principle of the wear sensing apparatus 100 is as follows.

At first, the dielectric substrate 102 may be attached to or otherwise arranged near a wear-prone object of interest (e.g., a machine or tool component, a material sample to be subjected to surface finishing, such as polishing, etc.) such that the dielectric substrate 102 is exposed to the same wear process as the object of interest (i.e., the dielectric substrate 102 is machined/grinded/abraded with (or against) the object of interest). Said attachment or arrangement may be implemented by a variety of ways. For example, there may be a cavity formed on the wear surface of the object of interest, and the dielectric substrate 102 may be installed in this cavity such that the wear surface 104 faces against the wear direction. As another example, the dielectric substrate 102 may be adhered near the wear surface of the object of interest such that the wear surface 104 faces against the wear direction.

When wear occurs on the wear surface 104 of the dielectric substrate 102, it is gradually abraded, thereby leading to the gradual abrasion of the conductors on the patterned surface 106. Due to this abrasion, the conductor lengths and the area between some adjacent conductors may change, which causes a change in corresponding selective capacitances. For example, it is well-known that the capacitance of a

plate capacitor is directly proportional to a surface area of its plates, so the rate of the capacitance change is directly proportional to the rate of the surface area decrease. In this case, the plates are replaced with the adjacent conductors, and the rate of their length decrease depends on the wear rate of the wear surface 104.

During the wear on the wear surface 104, the control unit 110 is configured to monitor the capacitance of each capacitor formed on the patterned surface 106 of the dielectric substrate 102 (i.e., each structure formed by the two adjacent conductors and the dielectric material therebetween). Then, the control unit 110 is configured to use the monitored capacitances to determine a wear rate (or, in other words, a wear depth) of the dielectric substrate 102 within a wear path (see the solid arrow in FIG. 1). The control unit 110 is further configured to output (e.g., via the display) the wear rate to a user.

As noted above, the wear may be accompanied by the smearing effect. In FIG. 1, it is assumed that the smearing effect causes the occurrence of a thin layer 114 of plastic surface deformation. This may result in the situation when at least some of the conductors of the array 108 of conductors may be brought into direct electric contact in the proximity of the wear surface 104. In one embodiment, the control unit 110 may be further configured to use the monitored capacitances to detect the occurrence of such short circuits between the conductors during the wear. Moreover, the control unit may be further configured to output a signal (e.g., visual, acoustic, vibration, or any combination thereof) indicative of the occurrence of the short circuits between the conductors to the user.

It should be noted that the short circuits between the conductors may be also caused not only by the smearing effect but also if the object of interest

(to which the dielectric substrate 102 is attached, or near which the dielectric substrate 102 is arranged such that it is exposed to the same wear process as the object of interest) is made of a conducting material. In this case, to distinguish between the short circuits (or direct electric contacts) caused by the smearing effect and the contact of the conductors with the conducting material, one may move the conducting object of interest along the wear surface 104 or otherwise move it away from the wear surface 104. The smearing-induced direct electric contacts will remain constant even after removing the contact with the conducting object of interest. For example, in case of using a machining (usually metal) tool to perform surface machining of a sample, the wear sensor 100 may be arranged on or near the sample such that the wear surface 104 of the dielectric substrate 102 is also machined with the tool; in this example, the direct electric contact between the tool and the wear sensor 100 may cause the short circuits between the conductors of the wear sensor 100. When the tool moves away, the smearing-induced direct electric contacts will remain constant, while the tool-induced direct electric contacts will disappear. Furthermore, for example, when monitoring the smearing effect in polishing processes, a polishing pad is not as conducting as smearing-induced inter-conductor contacts.

In one embodiment, the array 108 of conductors may have an equal inter-conductor spacing. The equal inter-conductor spacing may allow the user to monitor the wear rate (and the smearing effect, if present) in percentage terms. In another embodiment, the array 108 of conductors may have a varying inter-conductor spacing. The varying inter-conductor spacing may allow the user to monitor the wear rate (and the smearing effect, if present) in length units (e.g., in microns). It should be noted that the varying inter-conductor

spacing may be especially useful for smearing-effect monitoring.

FIG. 2 shows a schematic block diagram of a wear sensing apparatus 200 in accordance with a second exemplary embodiment. The apparatus 200 comprises a dielectric substrate 202 having a (bottom) wear surface 204 and a (front) patterned surface 206 adjacent to the wear surface 204. The dielectric substrate 202 may be made of the same material as the dielectric substrate 102. The apparatus 200 further comprises an array 208 of conductors extending parallel to each other on the patterned surface 206 of the dielectric substrate 202. More specifically, each conductor of the array 208 of conductors comprises a first planar straight-line portion extending perpendicular to the wear surface 204 and a second planar straight-line portion extending parallel to the wear surface 204. Similar to the conductors of the apparatus 100, the conductors of the apparatus 200 may be made of a ductile material by using any existing lithography technique (e.g., in accordance with the above-given example of the sample fabrication). Similarly, a layer of dielectric material (not shown in FIG. 2) is provided on the patterned surface 206 of the dielectric substrate 202 such that it covers not only each conductor of the array 208 of conductors but also each inter-conductor spacing. The inter-conductor spacing may again range from about 5 nm to about 10 mm, or may vary within any subranges of this spacing range, such, for example, as from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm, etc. Moreover, each conductor of the array 208 of conductors may again have a width and thickness both falling within the same range from about 5 nm to about 10 mm or any subranges of this range (e.g., like the ones indicated above in respect of the inter-conductor spacing).

As also shown in FIG. 2, the apparatus 200 further comprises a control unit 210 coupled to each conductor of the array 208 of conductors via a contact connector 212. Any existing contact connector may be used, which allows many conductors or wires to be individually coupled to a certain measurement device (like the control unit 210). In one alternative embodiment, wire bonding or a similar technique for connecting the array 208 of conductors with the control unit 210 may be used instead of forming the actual contact connector directly on the dielectric substrate 202; in this case, each conductor of the array 208 of conductors may have a contact pad at its one end, to which a bonding wire is mounted. In another alternative embodiment, if advanced lithography, an UHV chamber, or MBE is used to make the wear sensor 200, at least part (e.g., measurement means) of the control unit 210 may be provided directly on the dielectric substrate 202 (e.g., on the patterned surface 206 of the dielectric substrate 102).

As for the control unit 210, it may be implemented in the same manner as the control unit 110, as well as may be configured to operate in the same manner as the control unit 110. More specifically, the control unit 210 may be configured to monitor the capacitance of each capacitor formed on the patterned surface 206 of the dielectric substrate 202 (i.e., each structure formed by the two adjacent conductors and the dielectric material therebetween), determine the wear rate of the dielectric substrate 202 within the wear path (see the solid arrow in FIG. 2) based on the monitored capacitances, and output the wear rate to the user. The control unit 210 may be also configured to detect and monitor the smearing effect in the same manner as the control unit 110. For example, the smearing effect may result in the situation when the second (parallel) portion of the conductor closest to

the wear surface 204 will be brought into direct electric contact with the second (parallel) portion of the next conductor.

It should be noted that the configuration of the array 208 of conductors allows one to simultaneously monitor a general wear depth by detecting how many conductors have “lost” their second portions (parallel to the wear surface 204) during wear on the wear surface 104. If one conductor “loses” its second portion, it will lead to a major loss of the mutual capacitance between this conductor and the next conductor. In turn, the configuration of the array 108 of conductors allows one to determine the wear rate by monitoring a decrease in the mutual capacitance between each two adjacent conductors, which probably gives less accurate results.

FIG. 3 shows a schematic block diagram of a wear sensing apparatus 300 in accordance with a third exemplary embodiment. The apparatus 300 comprises a dielectric substrate 302 having more than one wear surface, namely: a left-side wear surface 304, a bottom wear surface 306, and a right-side wear surface 308. Thus, unlike the dielectric substrates 102 and 202, the dielectric substrate 302 is intended to be abraded on two or three sides. The dielectric substrate 302 also has a (front) patterned surface 310 adjacent to each of the wear surfaces 304, 306, and 308. The dielectric substrate 302 may be made of the same material as the dielectric substrate 102. The apparatus 300 further comprises an array 312 of conductors extending parallel to each other on the patterned surface 310 of the dielectric substrate 302. More specifically, each conductor of the array 312 of conductors comprises has a planar circular shape. Similar to the conductors of the apparatus 100, the conductors of the apparatus 300 may be made of a ductile material by using any existing lithography technique (e.g., in accordance with the above-given example of the sample fabrication).

Similarly, a layer of dielectric material (not shown in FIG. 3) is provided on the patterned surface 310 of the dielectric substrate 302 such that it covers not only each conductor of the array 312 of conductors but also each inter-conductor spacing. The inter-conductor spacing may again range from about 5 nm to about 10 mm, or may vary within any subranges of this spacing range, such, for example, as from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm, etc. Moreover, each conductor of the array 312 of conductors may again have a width and thickness both falling within the same range from about 5 nm to about 10 mm or within any subranges of this range (e.g., like the ones indicated above in respect of the inter-conductor spacing). It is the combination of the circular conductor configuration and the layer of dielectric material which enables the capacitance measurements on two or more sides of the dielectric substrate 302.

As also shown in FIG. 3, the apparatus 300 further comprises a control unit 314 coupled to each conductor of the array 312 of conductors via a contact connector 316. Any existing contact connector may be used, which allows many conductors or wires to be individually coupled to a certain measurement device (like the control unit 314). In one alternative embodiment, wire bonding or a similar technique for connecting the array 312 of conductors with the control unit 314 may be used instead of forming the actual contact connector directly on the dielectric substrate 302; in this case, each conductor of the array 312 of conductors may have a contact pad at its one end, to which a bonding wire is mounted. In another alternative embodiment, if advanced lithography, an UHV chamber, or MBE is used to make the wear sensor 300, at least part (e.g., measurement means) of the control unit 314 may

be provided directly on the dielectric substrate 302 (e.g., on the patterned surface 310 of the dielectric substrate 302).

As for the control unit 314, it may be implemented in the same manner as the control unit 110, as well as may be configured to operate in the same manner as the control unit 110. More specifically, the control unit 314 may be configured to monitor the capacitance of each capacitor formed on the patterned surface 310 of the dielectric substrate 302 (i.e., each structure formed by the two adjacent conductors and the dielectric material therebetween), determine the wear rate of the dielectric substrate 302 within each wear path (see the solid arrows in FIG. 3) based on the monitored capacitances, and output the wear rate to the user. The control unit 314 may be also configured to detect and monitor the smearing effect in the same manner as the control unit 110. For example, the smearing effect may result in the situation when the outermost circular conductor (closest to each of the wear surfaces 304, 306, and 308) will be brought into direct electric contact with the next circular conductor in one or more points.

FIG. 4 shows a schematic block diagram of a wear sensing apparatus 400 in accordance with a fourth exemplary embodiment. The apparatus 400 comprises a dielectric substrate 402 having a (bottom) wear surface 404 and a (front) patterned surface 406 adjacent to the wear surface 404. The dielectric substrate 402 may be made of the same material as the dielectric substrate 102. The apparatus 400 further comprises an array 408 of conductors extending parallel to each other on the patterned surface 406 of the dielectric substrate 402. More specifically, each conductor of the array 408 of conductors has a planar triangular shape. Similar to the conductors of the apparatus 100, the conductors of the apparatus 400 may be made of a ductile material by using

any existing lithography technique (e.g., in accordance with the above-given example of the sample fabrication). Similarly, a layer of dielectric material (not shown in FIG. 4) is provided on the patterned surface 406 of the dielectric substrate 402 such that it covers not only each conductor of the array 408 of conductors but also each inter-conductor spacing. The inter-conductor spacing may again range from about 5 nm to about 10 mm, or may vary within any subranges of this spacing range, such, for example, as from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm, etc. Moreover, each conductor of the array 408 of conductors may again have a width and thickness both falling within the same range from about 5 nm to about 10 mm or within any subranges of this range (e.g., like the ones indicated above in respect of the inter-conductor spacing).

As also shown in FIG. 4, the apparatus 400 further comprises a control unit 410 coupled to each conductor of the array 408 of conductors via a contact connector 412. Any existing contact connector may be used, which allows many conductors or wires to be individually coupled to a certain measurement device (like the control unit 410). In one alternative embodiment, wire bonding or a similar technique for connecting the array 408 of conductors with the control unit 410 may be used instead of forming the actual contact connector directly on the dielectric substrate 402; in this case, each conductor of the array 408 of conductors may have a contact pad at its one end, to which a bonding wire is mounted. In another alternative embodiment, if advanced lithography, an UHV chamber, or MBE is used to make the wear sensor 400, at least part (e.g., measurement means) of the control unit 410 may be provided directly on the dielectric substrate 402

(e.g., on the patterned surface 406 of the dielectric substrate 402).

As for the control unit 410, it may be implemented in the same manner as the control unit 110, as well as may be configured to operate in the same manner as the control unit 110. More specifically, the control unit 410 may be configured to monitor the capacitance of each capacitor formed on the patterned surface 406 of the dielectric substrate 402 (i.e., each structure formed by the two adjacent triangular conductors and the dielectric material therebetween), determine the wear rate of the dielectric substrate 402 within the wear path (see the solid arrow in FIG. 4) based on the monitored capacitances, and output the wear rate to the user. The control unit 410 may be also configured to detect and monitor the smearing effect in the same manner as the control unit 110. For example, the smearing effect may result in the situation when the first (when counted from the wear surface 404) two adjacent triangular conductors may be brought into direct electric contact in the proximity of the triangle vertices.

FIG. 5 shows a schematic block diagram of a wear sensing apparatus 500 in accordance with a fifth exemplary embodiment. The apparatus 500 comprises a substrate 502 configured as a multi-layered structure which is formed by plate-like conductors 504 alternating with dielectric layers 506. In this multi-layered structure, it is assumed that a wear surface (not shown in FIG. 5) is a bottom one, and the plate-like conductors 504 are arranged parallel to each other and perpendicular to the wear surface. The dielectric layers 506 may be made of the same material as the dielectric substrate 102. Similar to the conductors of the apparatus 100, the conductors 504 of the apparatus 500 may be made of a ductile material. The inter-conductor spacing (or, in other words, the width of each

dielectric layer 506) may again range from about 5 nm to about 10 mm, or may vary within any subranges of this spacing range, such, for example, as from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, from about 50 nm to about 5 mm, etc. Moreover, each plate-like conductor 504 may have a width falling within the same range from about 5 nm to about 10 mm or within any subranges of this range (e.g., like the ones indicated above in respect of the inter-conductor spacing). In general, the substrate 502 may be fabricated by using any deposition technique that allows one to stack alternating conductor and dielectric layers.

As also shown in FIG. 5, the apparatus 500 further comprises a control unit 508 coupled to each plate-like conductor 504 via a corresponding bonding wire 510. In one alternative embodiment, instead of the bonding wires 510, any existing contact connector may be used, which allows many plate-like conductors to be individually coupled to a certain measurement device (like the control unit 508).

As for the control unit 508, it may be implemented in the same manner as the control unit 110, as well as may be configured to operate in the same manner as the control unit 110. More specifically, the control unit 508 may be configured to monitor the capacitance of each capacitor present in the substrate 502 (i.e., each structure formed by the two adjacent plate-like conductors 504 and the dielectric layer 506 therebetween), determine the wear rate of the substrate 502 within the wear path (see the solid arrow in FIG. 5) based on the monitored capacitances, and output the wear rate to the user. The control unit 508 may be also configured to detect and monitor the smearing effect in the same manner as the control unit 110. For example, the smearing effect may result in the situation when

some or each two adjacent plate-like conductors 504 may be brought into direct electric contact in the proximity of the bottom wear surface.

The apparatus 500 is especially advantageous in terms of smearing effect detection and monitoring. In each of the apparatuses 100-400, there is only a thin layer of conducting material (i.e., planar conductors) formed on the patterned surface, for which reason it would be difficult for the smearing effect to "move" the conducting material so that at least two conductors are brought into direct electric contact. This is because there is a little amount of the conducting material which may be smeared in the first place. Conversely, in the multi-layered structure used in the apparatus 500, the smearing effect would be more pronounced because there is a larger wear surface with the conductor material that is able to be smeared.

It should be noted that the present disclosure is not limited to the conductor configurations shown in FIGs. 1-5. In some other embodiments, any other conductor configurations are possible. For example, each conductor may have any other curved shape, such as trapezoidal, square, etc., which allows the conductors to be formed on the patterned surface of the dielectric substrate with no initial direct contact therebetween. As another example, each conductor may comprise a first portion and a second portion that originate from a single point and diverge in a direction away from the wear surface (the triangular conductor shape shown in FIG. 4 is one particular example of such configuration).

Furthermore, in some embodiments, the inter-conductor spacing may increase or decrease within the wear path(s). For example, the array of conductors (any of those shown in FIGs. 1-5) may comprise two (first and second) non-overlapping subarrays of conductors, each of which may have a different inter-conductor spacing. For example, the first subarray of conductors may have

a first equal inter-conductor spacing and the second subarray of conductors may have a second equal inter-conductor spacing different from the first equal inter-conductor spacing. Alternatively, the first subarray of conductors may have an equal inter-conductor spacing, while the second subarray of conductors may have a varying inter-conductor spacing. Furthermore, in case of the arrays of conductors shown in FIGs. 2-4, the first and second subarray of conductors may be arranged differently relative to the wear surface(s) (e.g., the first subarray of conductors may be provided closer to each wear surface than the second subarray of conductors, or vice versa).

In some additional embodiments, the apparatuses 100-500 may further comprise an accelerometer and/or a gyroscope mounted on the dielectric substrate 102-502, respectively (e.g., in case of the apparatus 100, on the patterned surface 106 in the proximity of the array 108 of conductors). The accelerometer and/or the gyroscope may have a built-in transmitter (e.g., a Bluetooth transmitter) to be able to transmit measurement data to a mobile user device (e.g., via a mobile application installed on a mobile phone).

Although the exemplary embodiments of the present disclosure are described herein, it should be noted that various changes and modifications could be made in these embodiments, without departing from the scope of legal protection which is defined by the appended claims. In the appended claims, the word “comprising” does not exclude other elements or operations, and the indefinite article “a” or “an” does not exclude a plurality. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS

1. A wear sensing apparatus (100; 200; 300; 400) comprising:

a dielectric substrate (102; 202; 302; 402) having at least one wear surface (104; 204; 304, 306, 308; 404) and a patterned surface (106; 206; 310; 406) adjacent to the at least one wear surface (104; 204; 304, 306, 308; 404);

an array (108; 208; 312; 408) of conductors extending parallel to each other on the patterned surface (106; 206; 310; 406) of the dielectric substrate (102; 202; 302; 402), each conductor of the array (108; 208; 312; 408) of conductors having an elongated planar shape;

a dielectric material covering the patterned surface (106; 206; 310; 406) of the dielectric substrate (102; 202; 302; 402) together with the array (108; 208; 312; 408) of conductors; and

a control unit (110; 210; 314; 410) coupled to each conductor of the array (108; 208; 312; 408) of conductors and configured, when wear occurs on the at least one wear surface (104; 204; 304, 306, 308; 404) of the dielectric substrate (102; 202; 302; 402), to:

monitor a capacitance between each two adjacent conductors of the array (108; 208; 312; 408) of conductors;

based on the monitored capacitances, determine a wear rate of the dielectric substrate (102; 202; 302; 402); and

output the wear rate to a user;

characterized in that the control unit (110; 210; 314; 410) is further configured to:

based on the monitored capacitances, determine whether at least two conductors of the array (108; 208; 312; 408) of conductors have been brought into a direct electric contact with each other during the wear; and

if the at least two conductors of the array (108; 208; 312; 408) of conductors have been brought into the direct electric contact with each other during the wear, output a signal to the user.

2. The apparatus (100) of claim 1, wherein the at least one wear surface comprises a single wear surface (104), and wherein each conductor of the array (108) of conductors is straight and extends perpendicular to the wear surface (104).

3. The apparatus (200; 300; 400) of claim 1, wherein each conductor of the array (208; 312; 408) of conductors has a curved shape.

4. The apparatus (200) of claim 3, wherein the at least one wear surface comprises a single wear surface (204), and wherein each conductor of the array (208) of conductors comprises a first portion perpendicular to the wear surface (204) and a second portion parallel to the wear surface (204).

5. The apparatus (300) of claim 3, wherein the at least one wear surface comprises two or three wear surfaces (304, 306, 308), and wherein each

conductor of the array (312) of conductors has a circular shape.

6. The apparatus (400) of claim 3, wherein the at least one wear surface comprises a single wear surface (404), and wherein each conductor of the array (408) of conductors comprises a first portion and a second portion, the first portion and the second portion originating from a single point and diverging in a direction away from the wear surface (404).

7. The apparatus (400) of claim 6, wherein each conductor of the array (408) of conductors has a triangular shape.

8. The apparatus (100; 200; 300; 400) of any one of claims 1 to 7, wherein the array (108; 208; 312; 408) of conductors has an equal inter-conductor spacing.

9. The apparatus (100; 200; 300; 400) of any one of claims 1 to 7, wherein the array (108; 208; 312; 408) of conductors has a varying inter-conductor spacing.

10. The apparatus (100; 200; 300; 400) of any one of claims 3 to 7, wherein the array (108; 208; 312; 408) of conductors has a varying inter-conductor spacing that increases or decreases in a direction away from each of the at least one wear surface (104; 204; 304, 306, 308; 404) of the dielectric substrate (102; 202; 302; 402).

11. The apparatus (100; 200; 300; 400) of any one of claims 8 to 10, wherein the inter-conductor spacing ranges from about 5 nm to about 10 mm, more preferably from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, or from about 50 nm to about 5 mm.

12. The apparatus (100; 200; 300; 400) of any one of claims 1 to 7, wherein the array (108; 208; 312; 408) of conductors comprises a first subarray of conductors and a second subarray of conductors, the first subarray of conductors and the second subarray of conductors being non-overlapping, the first subarray of conductors having an equal inter-conductor spacing and the second subarray of conductors having a varying inter-conductor spacing.

13. The apparatus (100; 200; 300; 400) of claim 12, wherein the inter-conductor spacing of each of the first subarray of conductors and the second subarray of conductors ranges from about 5 nm to about 10 mm, more preferably from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, or from about 50 nm to about 5 mm.

14. The apparatus (100; 200; 300; 400) of any one of claims 1 to 7, wherein the array (108; 208; 312; 408) of conductors comprises a first subarray of conductors and a second subarray of conductors, the first subarray of conductors and the second

subarray of conductors being non-overlapping, the first subarray of conductors having a first equal inter-conductor spacing and the second subarray of conductors having a second equal inter-conductor spacing, the second equal inter-conductor spacing being different from the first equal inter-conductor spacing.

15. The apparatus (100; 200; 300; 400) of claim 14, wherein each of the first equal inter-conductor spacing and the second equal inter-conductor spacing ranges from about 5 nm to about 10 mm, more preferably from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, or from about 50 nm to about 5 mm.

16. The apparatus (100; 200; 300; 400) of any one of claims 1 to 15, wherein each conductor of the array (108; 208; 312; 408) of conductors is made of a ductile material.

17. The apparatus (100; 200; 300; 400) of any one of claims 1 to 16, wherein the dielectric substrate (102; 202; 302; 402) is made of glass, silicon, SiO_2, epoxy, a polymer, a semiconductor, ceramics, SiC, a nonconducting polymer, a nonconducting copolymer, or any combination thereof.

18. The apparatus (100; 200; 300; 400) of any one of claims 1 to 17, wherein each conductor of the array (108; 208; 312; 408) of conductors has a width ranging from about 5 nm to about 10 mm and a

thickness ranging from about 5 nm to about 10 mm, more preferably from about 10 nm to about 9 mm, from about 20 nm to about 8 mm, from about 30 nm to about 7 mm, from about 40 nm to about 6 mm, or from about 50 nm to about 5 mm.

PATENTTIVAATIMUKSET

1. Kulumisen havaitseva laite (100; 200; 300; 400), joka käsittää:

dielektrisen alustan (102; 202; 302; 402), jossa on ainakin yksi kulumispinta (104; 204; 304, 306, 308; 404) ja ainakin yhden kulumispinnan (104; 204; 304, 306, 308; 404) vieressä oleva kuvioitu pinta (106; 206; 310; 406);

ryhmän (108; 208; 312; 408) johtimia, jotka ulottuvat keskenään yhdensuuntaisesti dielektrisen alustan (102; 202; 302; 402) kuvioidulla pinnalla (106; 206; 310; 406), jossa jokaisella johtimella ryhmästä (108; 208; 312; 408) johtimia on pitkänomainen tasomainen muoto;

dielektrisen materiaalin, joka peittää dielektrisen alustan (102; 202; 302; 402) kuvioitua pintaa (106; 206; 310; 406) yhdessä ryhmän (108; 208; 312; 408) johtimia kanssa; ja

ohjausyksikön (110; 210; 314; 410), joka on kytketty jokaiseen johtimeen ryhmästä (108; 208; 312; 408) johtimia ja sovitettu, kun kulumista tapahtuu dielektrisen alustan (102; 202; 302; 402) ainakin yhdellä kulumispinnalla (104; 204; 304, 306, 308; 404):

seuraamaan ryhmän (108; 208; 312; 408) johtimia jokaisen kahden vierekkäisen johtimen välistä kapasitanssia;

määrittämään seurattujen kapasitanssien perusteella dielektrisen alustan (102; 202; 302; 402) kulumisaste; ja

antamaan kulumisaste käyttäjälle;

tunnettu siitä, että ohjausyksikkö (110; 210; 314; 410) on edelleen sovitettu:

määrittämään seurattujen kapasitanssien perusteella, onko ainakin kaksi johdinta ryhmästä (108; 208; 312; 408) johtimia tullut suoraan sähköiseen kontaktiin toistensa kanssa kulumisen aikana; ja

jos ainakin kaksi johdinta ryhmästä (108; 208; 312; 408) johtimia on tullut suoraan sähköiseen kontaktiin toistensa kanssa kulumisen aikana, antamaan käyttäjälle signaali.

2. Patenttivaatimuksen 1 mukainen laite (100), jossa ainakin yksi kulumispinta käsittää yksittäisen kulumispinnan (104), ja jossa jokainen johdin ryhmästä (108) johtimia on suora ja ulottuu kohtisuorasti kulumispintaan (104) nähden.

3. Patenttivaatimuksen 1 mukainen laite (200; 300; 400), jossa jokaisella johtimella ryhmästä (208; 312; 408) johtimia on kaareva muoto.

4. Patenttivaatimuksen 3 mukainen laite (200), jossa ainakin yksi kulumispinta käsittää yksittäisen kulumispinnan (204), ja jossa jokainen johdin ryhmästä (208) johtimia käsittää ensimmäisen osuuden, joka on kohtisuora kulumispintaan (204) nähden ja toisen osuuden, joka on yhdensuuntainen kulumispinnan (204) kanssa.

5. Patenttivaatimuksen 3 mukainen laite (300), jossa ainakin yksi kulumispinta käsittää kaksi tai kolme

kulumispintaa (304, 306, 308), ja jossa jokaisella johtimella ryhmästä (312) johtimia on pyöreä muoto.

6. Patenttivaatimuksen 3 mukainen laite (400), jossa ainakin yksi kulumispinta käsittää yksittäisen kulumispinnan (404), ja jossa jokainen johdin ryhmästä (408) johtimia käsittää ensimmäisen osuuden ja toisen osuuden, jotka ensimmäinen osuus ja toinen osuus alkavat yhdestä pisteestä ja eroavat suunnassa, joka on poispäin kulumispinnasta (404).

7. Patenttivaatimuksen 6 mukainen laite (400), jossa jokaisella johtimella ryhmästä (408) johtimia on kolmikulmainen muoto.

8. Jonkin patenttivaatimuksista 1 – 7 mukainen laite (100; 200; 300; 400), jossa ryhmällä (108; 208; 312; 408) johtimia on samansuuruinen johdintenvälinen etäisyys.

9. Jonkin patenttivaatimuksista 1 – 7 mukainen laite (100; 200; 300; 400), jossa ryhmällä (108; 208; 312; 408) johtimia on muuttuva johdintenvälinen etäisyys.

10. Jonkin patenttivaatimuksista 3 – 7 mukainen laite (100; 200; 300; 400), jossa ryhmällä (108; 208; 312; 408) johtimia on muuttuva johdintenvälinen etäisyys, joka kasvaa tai pienenee suunnassa, joka on poispäin jokaisesta dielektrisen alustan (102; 202; 302; 402) ainakin yhdestä kulumispinnasta (104; 204; 304, 306, 308; 404).

11. Jonkin patenttivaatimuksista 8 – 10 mukainen laite (100; 200; 300; 400), jossa johdintenvälinen etäisyys on noin 5 nm – noin 10 mm, edullisemmin noin 10 nm – noin 9 mm, noin 20 nm – noin 8 mm, noin 30 nm – noin 7 mm, noin 40 nm – noin 6 mm, tai noin 50 nm – noin 5 mm.

12. Jonkin patenttivaatimuksista 1 – 7 mukainen laite (100; 200; 300; 400), jossa ryhmä (108; 208; 312; 408) johtimia käsittää johtimien ensimmäisen aliryhmän ja johtimien toisen aliryhmän, jotka johtimien ensimmäinen aliryhmä ja johtimien toinen aliryhmä ovat ei-päällekkäiset, jolla johtimien ensimmäisellä aliryhmällä on samansuuruinen johdintenvälinen etäisyys ja jolla johtimien toisella aliryhmällä on muuttuva johdintenvälinen etäisyys.

13. Patenttivaatimuksen 12 mukainen laite (100; 200; 300; 400), jossa johtimien ensimmäisestä aliryhmästä ja johtimien toisesta aliryhmästä kummankin johdintenvälinen etäisyys on noin 5 nm – noin 10 mm, edullisemmin noin 10 nm – noin 9 mm, noin 20 nm – noin 8 mm, noin 30 nm – noin 7 mm, noin 40 nm – noin 6 mm, tai noin 50 nm – noin 5 mm.

14. Jonkin patenttivaatimuksista 1 – 7 mukainen laite (100; 200; 300; 400), jossa ryhmä (108; 208; 312; 408) johtimia käsittää johtimien ensimmäisen aliryhmän ja johtimien toisen aliryhmän, jotka johtimien ensimmäinen aliryhmä ja johtimien toinen aliryhmä ovat ei-päällekkäiset, jolla johtimien

ensimmäisellä aliryhmällä on ensimmäinen samansuuruinen johdintenvälinen etäisyys ja jolla johtimien toisella aliryhmällä on toinen samansuuruinen johdintenvälinen etäisyys, joka toinen samansuuruinen johdintenvälinen etäisyys on eri kuin ensimmäinen samansuuruinen johdintenvälinen etäisyys.

15. Patenttivaatimuksen 14 mukainen laite (100; 200; 300; 400), jossa kumpikin ensimmäisestä samansuuruisesta johdintenvälisestä etäisyydestä ja toisesta samansuuruisesta johdintenvälisestä etäisyydestä on noin 5 nm – noin 10 mm, edullisemmin noin 10 nm – noin 9 mm, noin 20 nm – noin 8 mm, noin 30 nm – noin 7 mm, noin 40 nm – noin 6 mm, tai noin 50 nm – noin 5 mm.

16. Jonkin patenttivaatimuksista 1 – 15 mukainen laite (100; 200; 300; 400), jossa jokainen johdin ryhmästä (108; 208; 312; 408) johtimia on tehty taipuisasta materiaalista.

17. Jonkin patenttivaatimuksista 1 – 16 mukainen laite (100; 200; 300; 400), jossa dielektrinen alusta (102; 202; 302; 402) on tehty jostakin seuraavien joukosta: lasi, pii, SiO_2, epoksi, polymeeri, puolijohde, keramiikka, SiC, johtamaton polymeeri, johtamaton kopolymeeri tai niiden mikä tahansa yhdistelmä.

18. Jonkin patenttivaatimuksista 1 – 17 mukainen laite (100; 200; 300; 400), jossa jokaisella johtimella ryhmästä (108; 208; 312; 408) johtimia

on leveys, joka on noin 5 nm – noin 10 mm ja paksuus, joka on noin 5 nm – noin 10 mm, edullisemmin noin 10 nm – noin 9 mm, noin 20 nm – noin 8 mm, noin 30 nm – noin 7 mm, noin 40 nm – noin 6 mm, tai noin 50 nm – noin 5 mm.

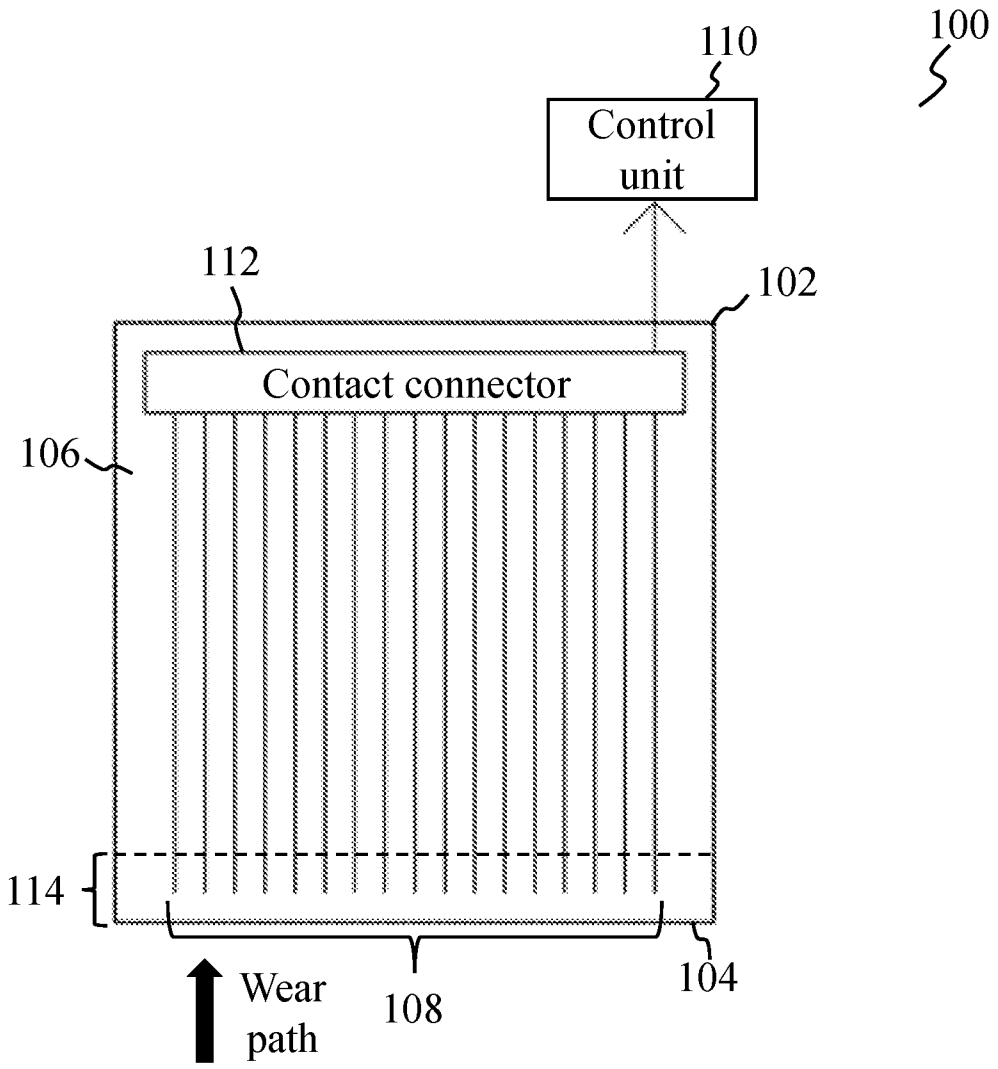


FIG. 1

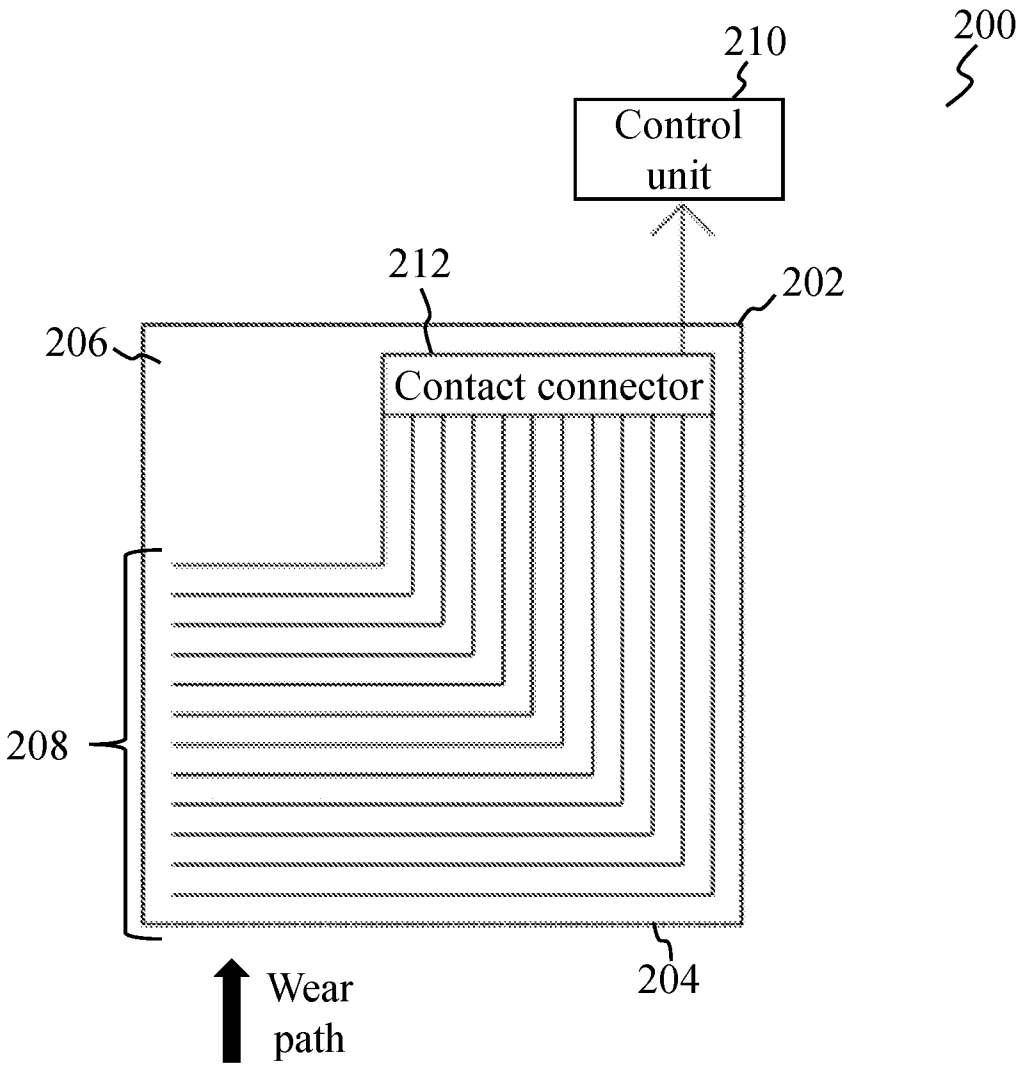


FIG. 2

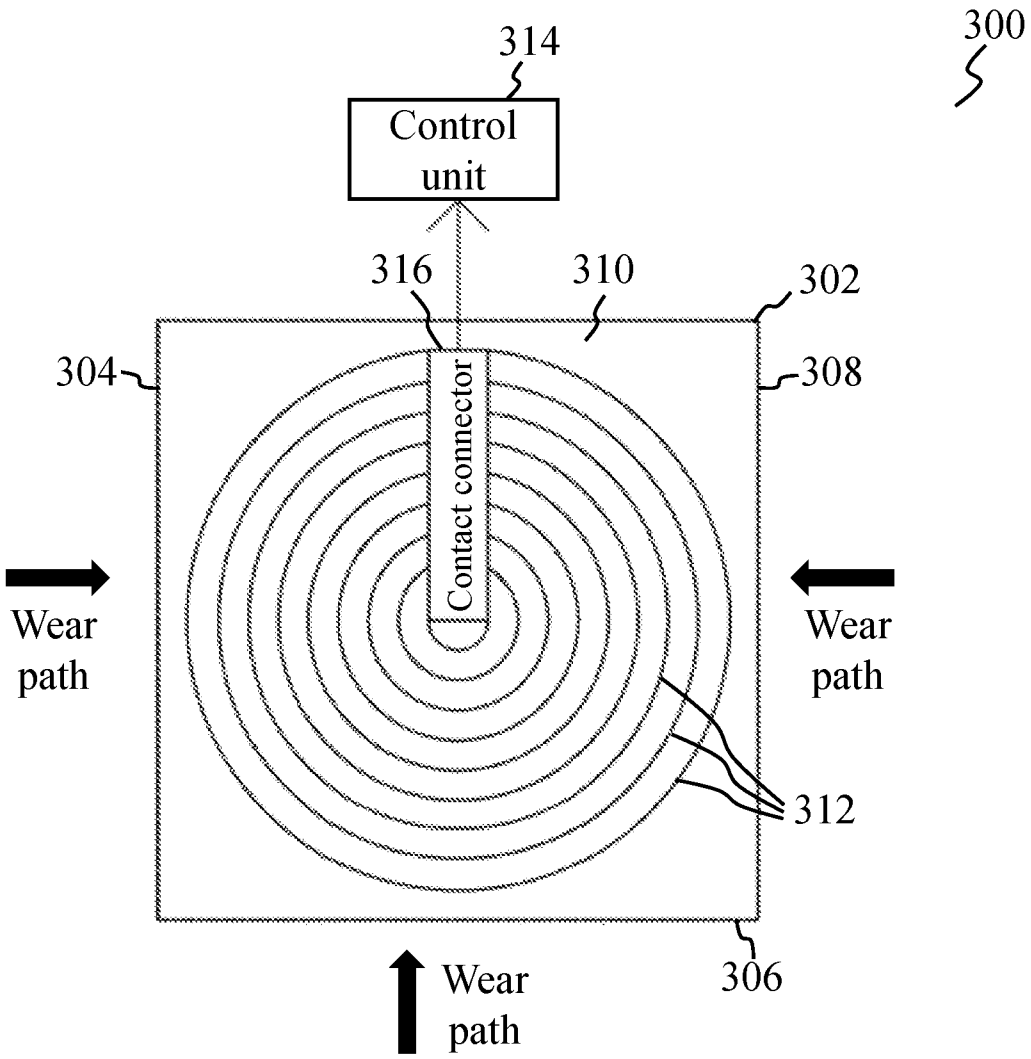


FIG. 3

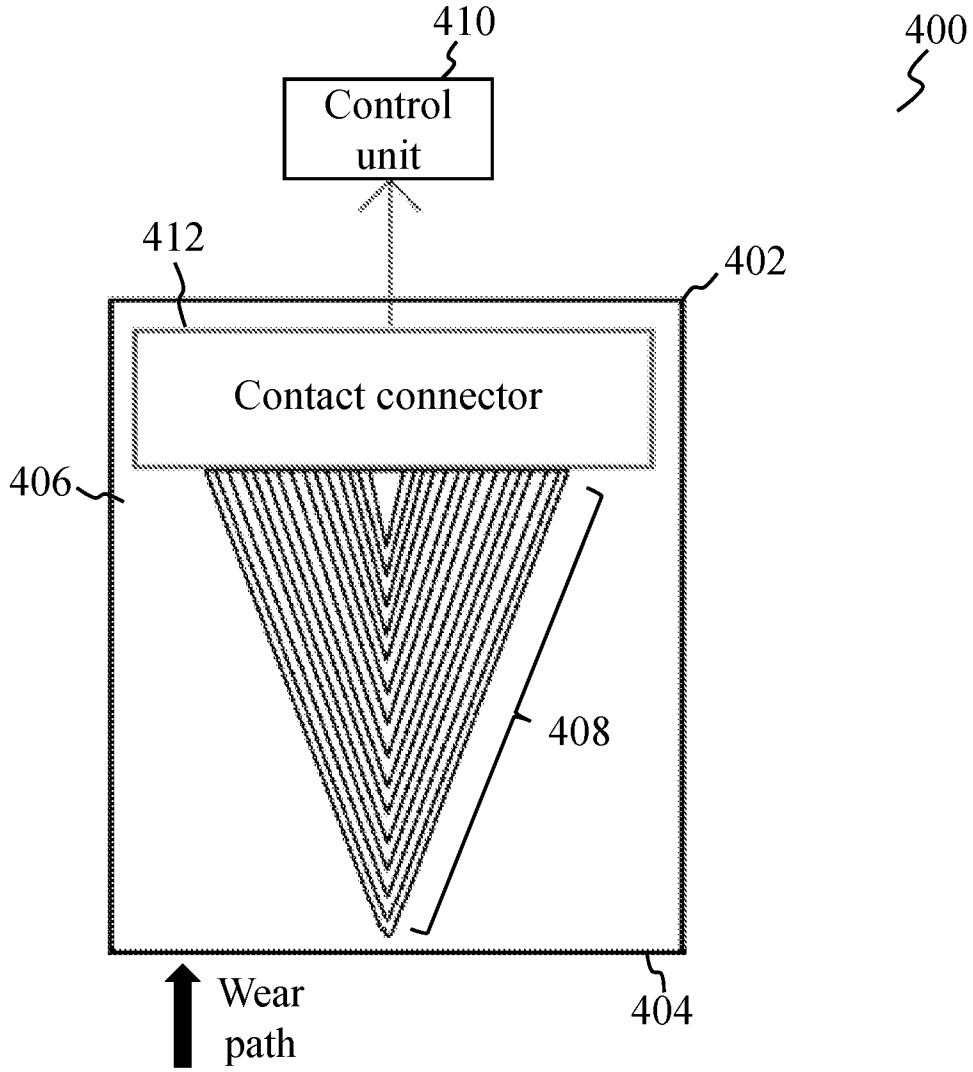


FIG. 4

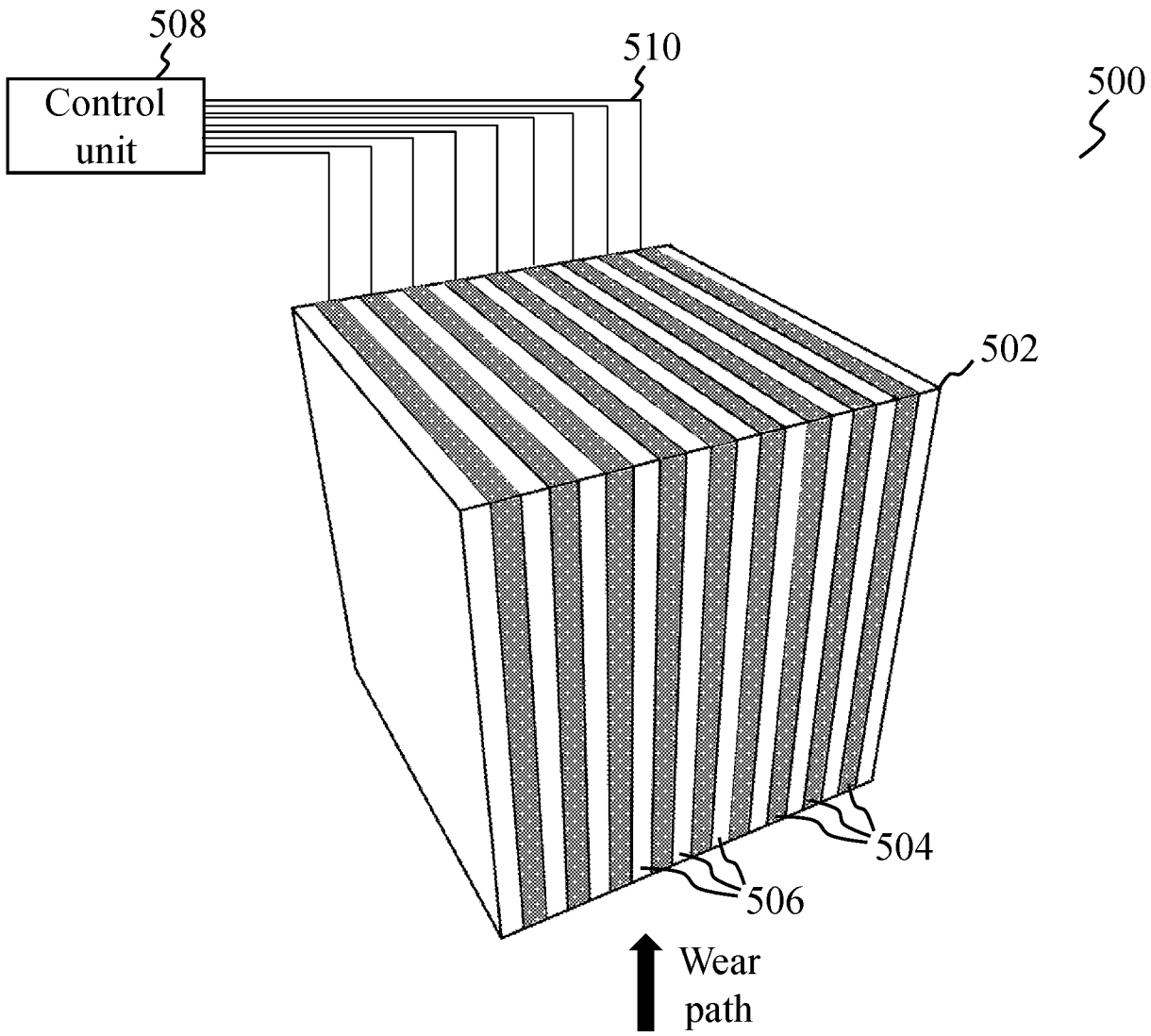


FIG. 5