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2004 05 27

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(74)
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(54)

1 2 , 1 ;
, 1 , 1 ;
2 ; 1 2 ; 2 ; 2 1 ;
2 2 ; 2 ; 2 ;
2 ; 1 2 , .

4

, , , , ,

1 DDR .

2a

2b 2a

3

4

5 4

6 4

7 6

8 6 2

9

10 16

11 10

12 10

13 12

14 10

15 10

가

가

1 DDR(Double Date Rate)

1 , DDR

400) (400) , (300) (300) (500) , (500) , (

(100) (700) (100) , (600) , (500) (600) (600) (100)

(200) , (100)

(rising edge) (falling edge) 가 DDR(Double Data rate)

(100)가 (700) (500) (500) (100)

(100) (100) 가 (CAS Latency) 가

2a

2a (100a) (20_1,20_2,...,20_n) (20'_1,20'_2,...,20'_n) (1~n) (10_1,10_2,...,10_n) (20'_1,20'_2,...,20'_n) (20_1,20_2,...,20_n, 20'_1,20'_2,...,20'_n) (30_1 ~ 30_n) (30_1 ~ 30_n) (1~n) (1~n) (1~n) (1~n) (30_1 ~ 30_n) (40_1,40_2, ...,40_n, 40'_1,40'_2,...,40'_n)

2b 2a (100a) (200a)

2b (200a) n 2n n 2n n

2a 2b

가 (100a) (1~n) n (1~n) 2n (10_1,10_2,...,10_n, 10'_1,10'_2,...,10'_n)가 (20_1,20_2,...,20_n, 20'_1,20'_2,...,20'_n) (200a) n (1~n) n (30_1,30_2,...,30_n) (20_1,20_2,...,20_n, 20'_1,20'_2,...,20'_n)

(200a) n (1~n) n (1~n) (1~n) (1~n) (40_1,40_2,...,40_n, 40'_1,40'_2,...,40'_n)가 (1~n) n (1~n) (1~n)

(100a) 가 (200a) (200a) 가

16 :8, :8) 16 (:8, :8) (:8, :8) (8 가 , 16 (가 , :8)

가

3 (100b) (200b)

3 (100b)
 (50_1,50_2,...,50_n) , (50_1,50_2,...,50_n)
 (60_1,...,60_n-1) ,
 (50'_1,50'_2,...,50'_n) , (50'_1,50'_2,...,50'_n)
 (60_1,...,60_n-1) , n

(50_n,50'_n)
 (60a)

(200b) 2(n-1) ,

3 (100b)

가 , 가 (1
 00b) , (50_1,50_2,...,50_n) (50'_1,50'_2,
 ...,50'_n) (200b) 가
 (50_1,50_2,...,50_n, 50'_1,50'_2,...,50'_n) (40 ~ 43)
 n-1 (1~n-1) n-1 (1~n-1) .
 (200b) 가 (60a) (50_n,
 50'_n) (1 700) ,
 (100b) 가 가

16 가 (100b) , 14
 16 , 16 , 8)가 (100a) 40 (16 (10
 0b)가 (100a) 1 , 1) 가 ,
 (100a) 가 .
 , 가
 , (100b) , 가
 , (100b) , 가
 , (100b) (100a)
 , 가 가

가 가 가

(70a) (100c) (70a) (70c₁~70c_k) (70b) (70c₁~70c_k) (70'a) (70'b) (70c₁~70c_k) (70'b) (70c₁~70c_k) (70c₁~70c_k, 70'c₁~70'c_k) (80) (200c)

(200c) n-2

(70c₁~70c_k, 70'c₁~70'c_k)

(70c₁) (70a) (70c_{1_1}) (70c_{1_1}) (70c_{1_1}',70c_{1_2}',...,70c_{1_m}') (70c_{1_1}',70c_{1_2}',...,70c_{1_m}') (70c_{1_2},70c_{1_3},...,70c_{1_m}) (70b) (70c_{1_m+1}) (70c_{1_m}') (70c₁~70c_k, 70'c₁~70'c_k) (70c_{1_m+1}) 가 'k'

(m=(n-2)/k) (100c) (n) 2 (n-2) (k)

(200c)

(200c) (a₁~a_k,b₁~b_k) (210) (a₁~a_k,b₁~b_k) (70c₁~70c_k, 70'c₁~70'c_k) (220₁~220_k, 220'₁~220'_k)

(220₁~220_k, 220'₁~220'_k)

(70c₁) (220₁) (a₁) (70c_{1_1},70c_{1_2},...,70c_{1_m+1}) (m+1) (m+1) (220_{1a})

(70c_1) 1 3 (70c_1_1,70c_1_2 ,...,70c_1_m+1)
 m+1 (220_1b) .

8 6 (220_1~220_k, 220'_1~220'_k) 2

8 (220_1b) 가 (220_1') 7 (220_1) (220 m+
 1 (220_1a) 가 (220_1c) , m+1 (220_1a) m+1
 (220_1b) 가 (220_1b) , (220_1c)

9 9
 16 9 8 , 8 ,
 , 8 8 가 , 8 8 ,
 8 가 16 , 32가 ,
 가 8 가 32 가 40 가
 , 8 가 가 8 가
 8 8 가 가
 8 7 가 14 14 8 가 가
 16 가 16 2 가 가
 , 12 1 6 16 2 , 2 가
 , 18 3 18 가 2 가
 0 가 18 2 , 2
 , 가 2

(:40,
 :20),
 가 ,
 가

3) , (Sync)가 (A1 ~ A3)

14 10 , 2

14 (A1~ A3) (70a_1) (70c_1a) (B1~B3) (70c_2a) (70c_3a)

70a_1) (C1~C3) (70b_1) (70c_1a, 70c_2a, 70c_3a) (80_1)

) (80_1) (70b_1,70'b_1)

15 10 가

(B1~B3) (A1~A3) (220a_2) (220a_1) (C1~C3)

(220a_3)

15 (A,B,C,..)가 (2

00d) 9 (A1~A3,B1~B3,C1~C3)

(70c_1a,70c_2a,70c_3a) 6 (70b_1) (70a_1)

(70b_1) (200d)

1 (70a_1) 1 (A)가 3 (

70c_1a) , (70c_1a) 1 (A)가

1 (70a_1) 가 2 (B)

가 (70c_2a) 가

가 가

가

(57)

1.

1 2 ,

1 1 ;

1 ; , 1 ,
 1 ;
 2 2 ;
 2 ; , 2 ,
 2 ;
 1 2 ;
 1 2 ,

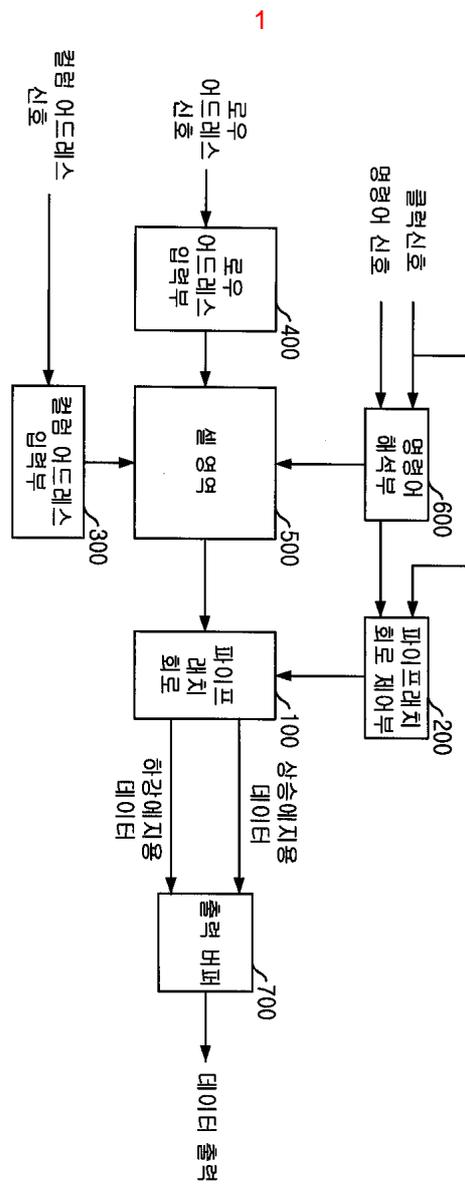
2.
 1 ,
 1
 1 1 ;
 1 ;
 2 ; ,
 3 1

3.
 2 ,
 ; ,
 1 3 가 1 .

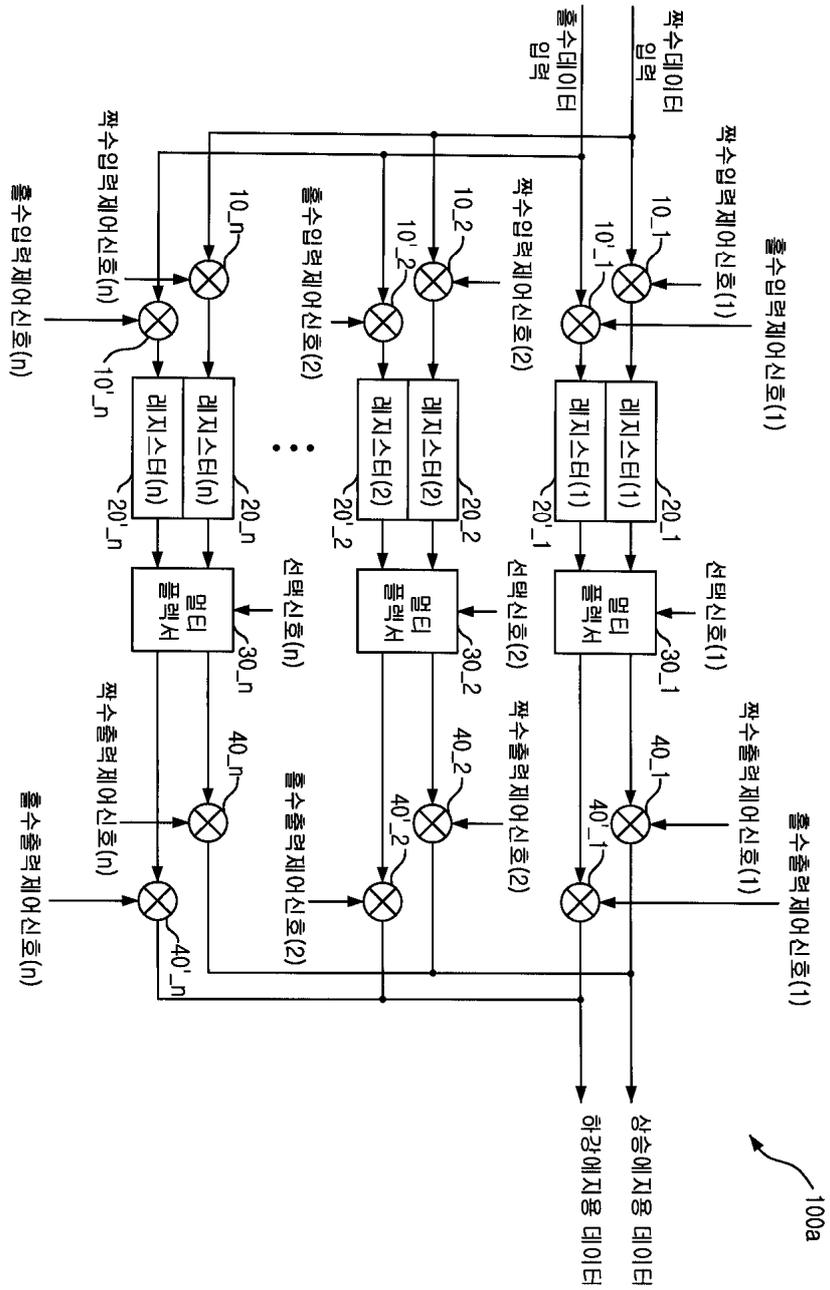
4.
 3 ,
 ;
 1 3
 1 3 .

5.

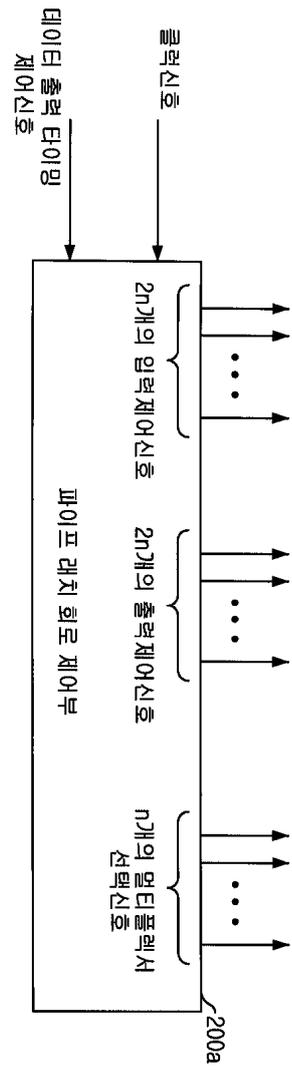
4
 1 2
 2
 6.
 4
 1 2
 2

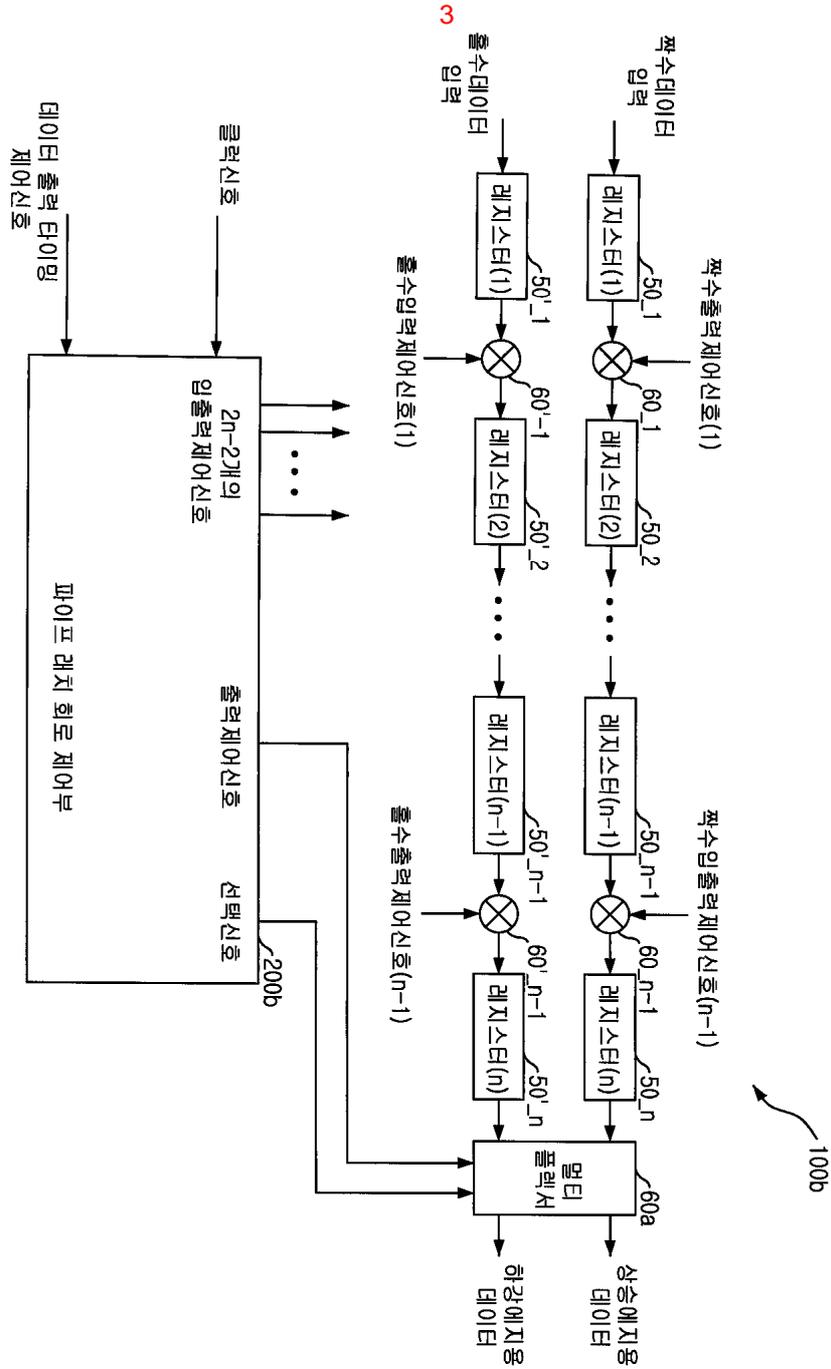


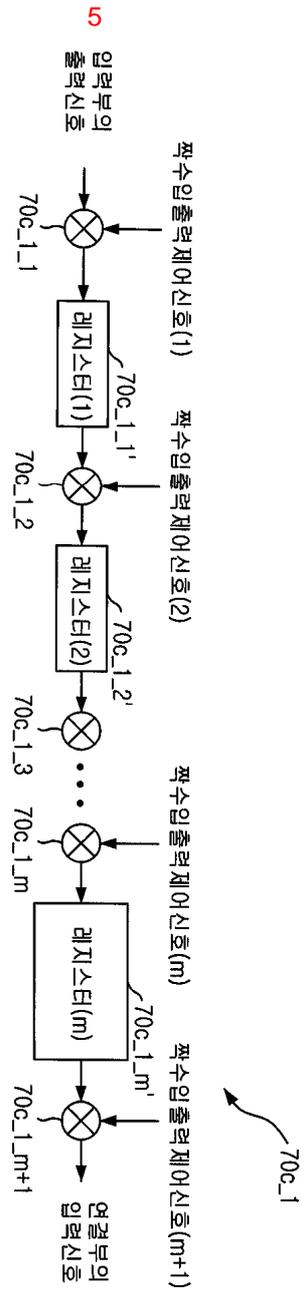
2a



2b



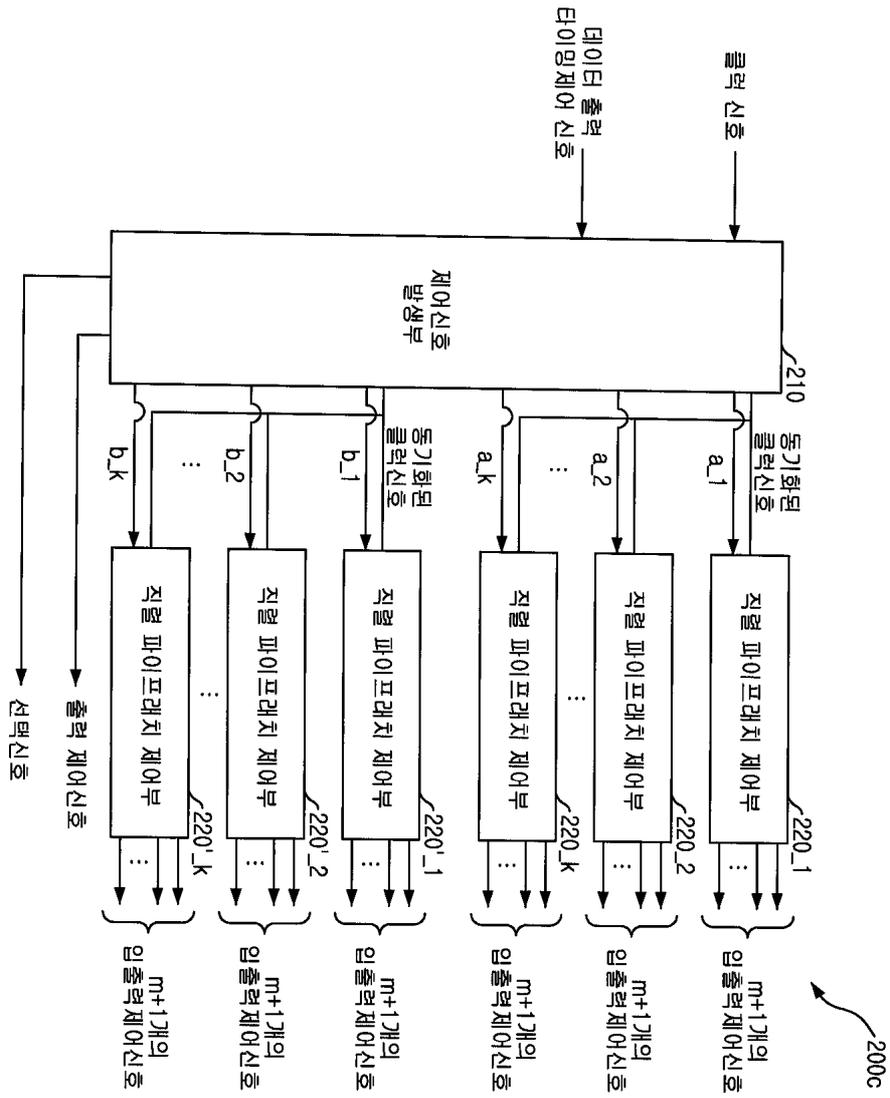


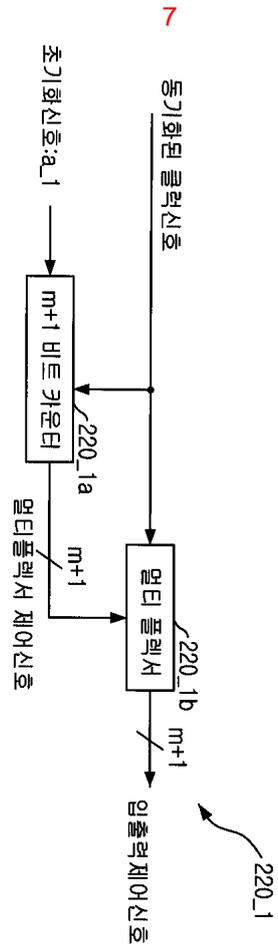


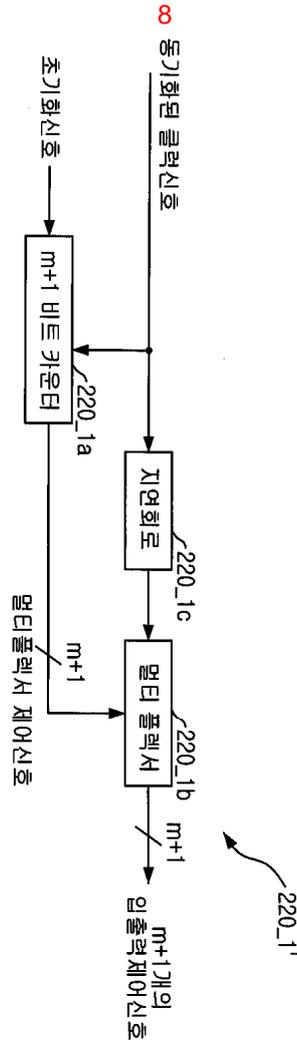
$$m = (n-2) / k$$

(n: 레지스터 수)
(k: 직렬 파이프라인 수)

9



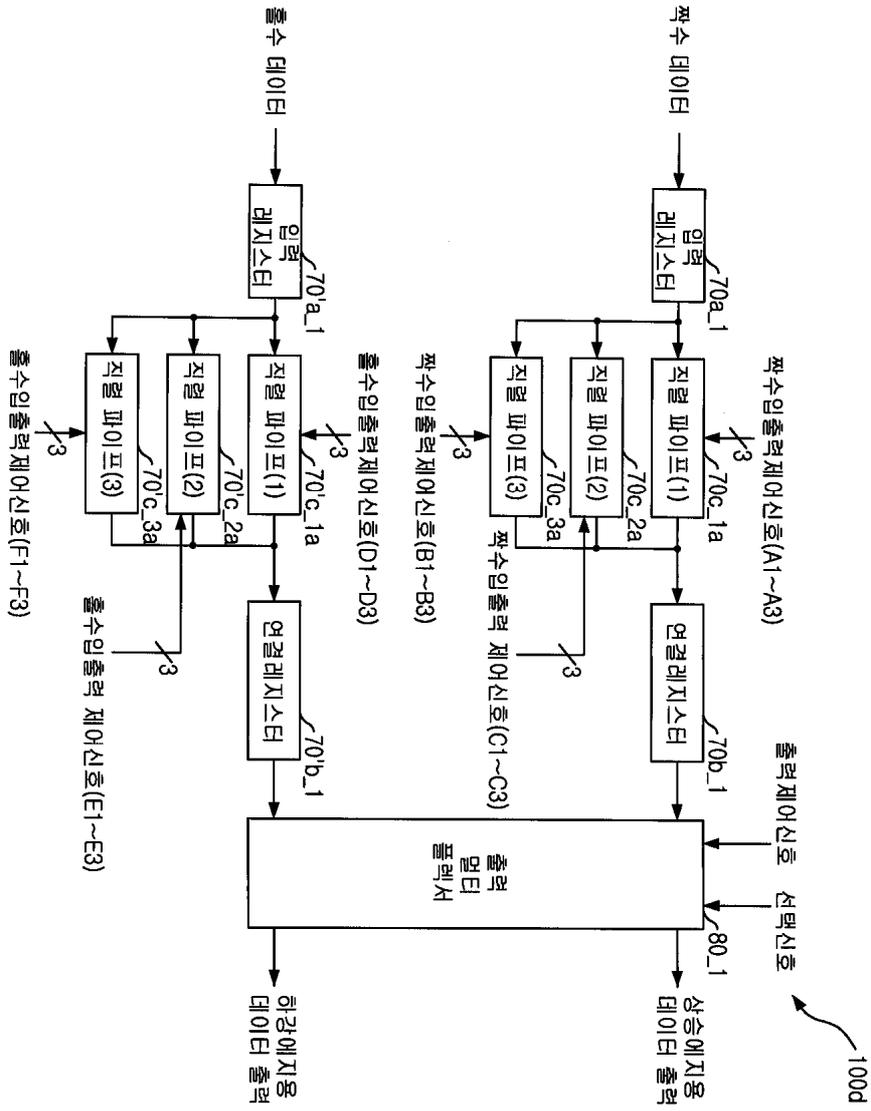




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	종래의 파이프래치		본 발명의 파이프 구조
	병렬	직렬	
레지스터	2n(16)	2n(16)	2n(16)
멀티 플렉서	n(8)	1(1)	1(1)
패스회로	4n(32)	2n-2(14)	(2n-4)+2k(18)
계	7n(56)	4n-1(31)	(4n-3)+2k(35)
제어신호개수	4n(40)	2n-2(16)	(2n-4)+2k(18)

- ()은 짝출수 데이터패스에 레지스터가 각각 8개인 경우
- k는 짝출수 데이터패스 각각에 구비되는 직렬파이프래치수



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