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(54) **METHOD OF FORMING CMOS INTEGRATED CIRCUITRY**

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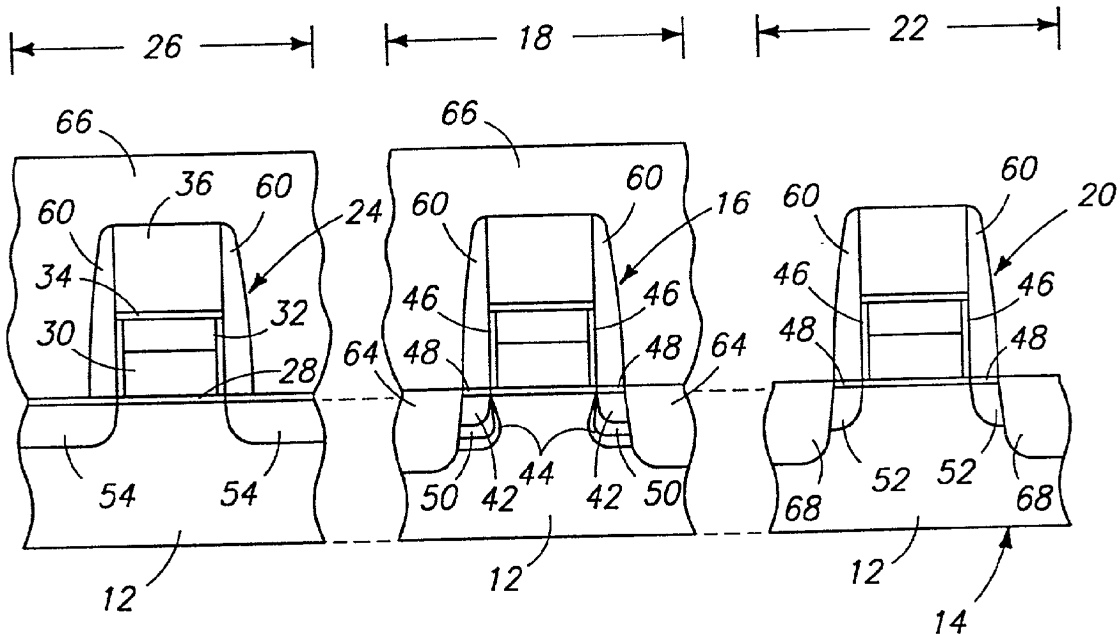
(57) **ABSTRACT**

A method of forming CMOS integrated circuitry includes, a) providing a series of gate lines over a semiconductor substrate, a first gate line being positioned relative to an area of the substrate for formation of an NMOS transistor, a second gate line being positioned relative to an area of the substrate for formation of a PMOS transistor; b) masking the second gate line and the PMOS substrate area while conducting a p-type halo ion implant into the NMOS substrate area adjacent the first gate line, the p-type halo ion implant being conducted at a first energy level to provide a p-type first impurity concentration at a first depth within the NMOS substrate area; and c) in a common step, blanket ion implanting phosphorus into both the NMOS substrate area and the PMOS substrate area adjacent the first and the second gate lines to form both NMOS LDD regions and PMOS n-type halo regions, respectively, the phosphorus implant being conducted at a second energy level to provide an n-type second impurity concentration at a second depth within both the PMOS substrate area and the NMOS substrate area, the first energy level and the first depth being greater than the second energy level and the second depth, respectively. Methods of forming memory and other CMOS integrated circuitry are also disclosed involving optimization of different NMOS transistors.



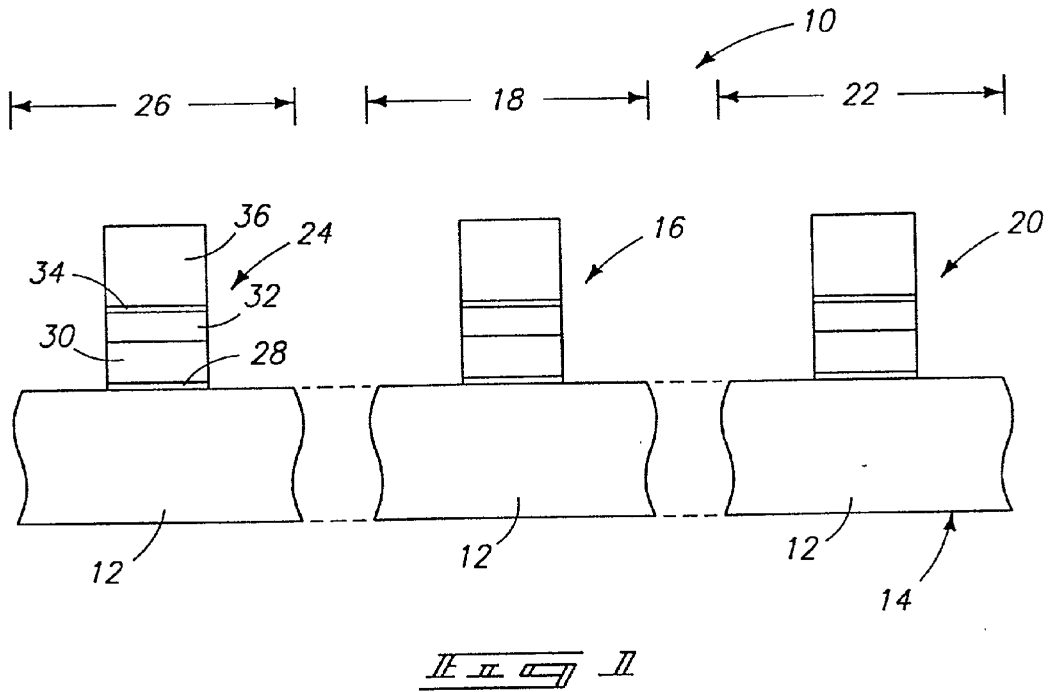


Fig 1

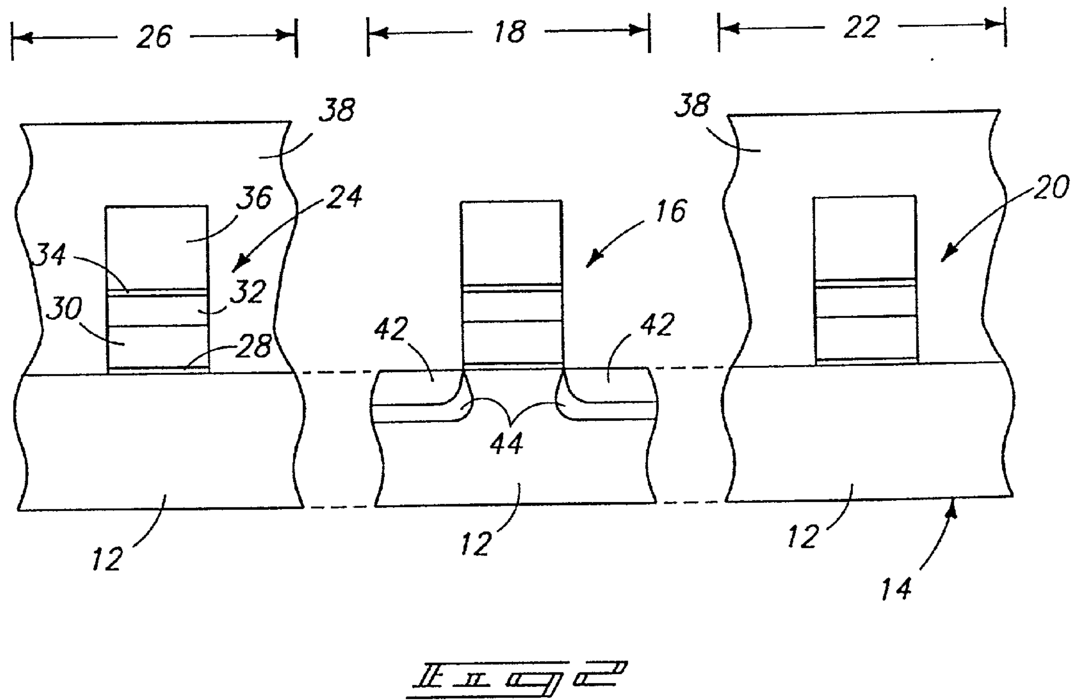


Fig 2

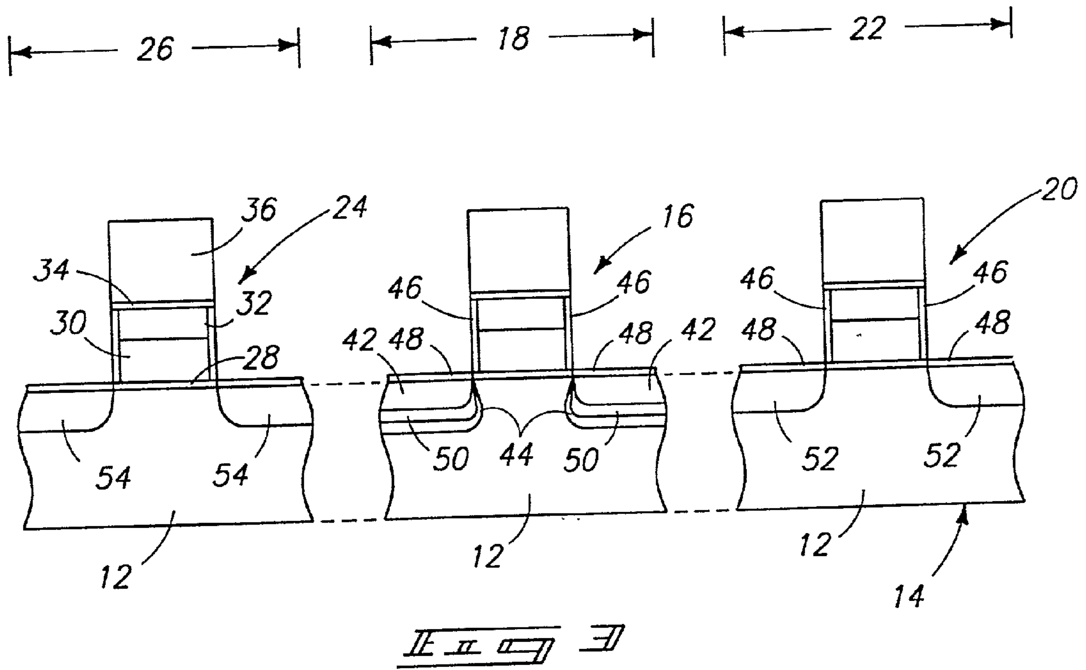


FIG. 3

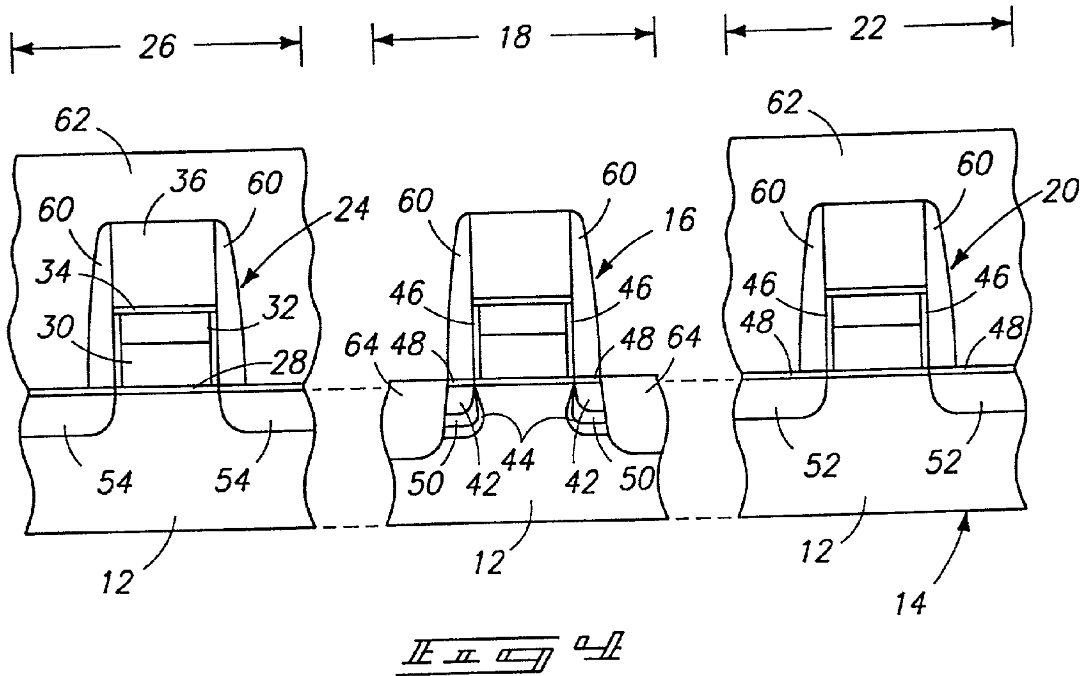


FIG. 4

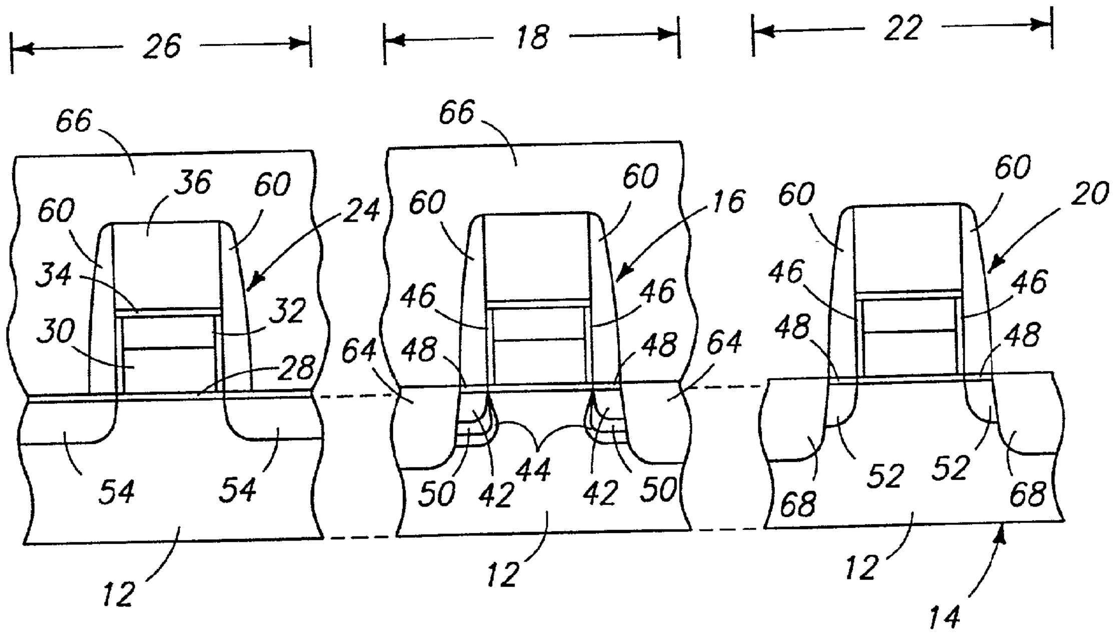


Fig 5

METHOD OF FORMING CMOS INTEGRATED CIRCUITRY

TECHNICAL FIELD

[0001] This invention relates to methods of forming complementary metal oxide semiconductor (CMOS) integrated circuitry, and to methods of forming field effect transistors.

BACKGROUND OF THE INVENTION

[0002] An MOS (metal-oxide-semiconductor) structure in semiconductor processing is created by superimposing several layers of conducting, insulating and transistor forming materials. After a series of processing steps, a typical structure might comprise levels of diffusion, polysilicon and metal that are separated by insulating layers.

[0003] CMOS is so-named because it uses two types of transistors, namely an n-type transistor (NMOS) and a p-type transistor (PMOS). These are fabricated in a semiconductor substrate, typically silicon, by using either negatively doped silicon that is rich in electrons or positively doped silicon that is rich in holes. Different dopant ions are utilized for doping the desired substrate regions with the desired concentration of produced holes or electrons.

[0004] NMOS remained the dominant MOS technology as long as the integration level devices on a chip was sufficiently low. It is comparatively inexpensive to fabricate, very functionally dense, and faster than PMOS. With the dawning of large scale integration, however, power consumption in NMOS circuits began to exceed tolerable limits. CMOS represented a lower-power technology capable of exploiting large scale integration fabrication techniques.

[0005] CMOS fabrication does however present a number of challenges to the fabricator as compared to using PMOS or NMOS alone. Specifically, typically independent or separate masking steps are utilized for masking one of the p-type regions while the n-type region is being doped. Also, the n-type regions are separately masked when the p-type regions are being doped. Accordingly, typical transistor flows use one mask each to form the n-channel and p-channel transistor source and drain regions. Higher levels of integration result in denser and denser circuits, leading CMOS fabrication to more difficulties.

[0006] It would be desirable to develop methods which further facilitate formation of complementary source and drain regions within a semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0008] **FIG. 1** is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

[0009] **FIG. 2** is a view of the **FIG. 1** wafer at a processing step subsequent to that shown by **FIG. 1**.

[0010] **FIG. 3** is a view of the **FIG. 1** wafer at a processing step subsequent to that shown by **FIG. 2**.

[0011] **FIG. 4** is a view of the **FIG. 1** wafer at a processing step subsequent to that shown by **FIG. 3**.

[0012] **FIG. 5** is a view of the **FIG. 1** wafer at a processing step subsequent to that shown by **FIG. 4**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0013] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

[0014] In accordance with one aspect of the invention, a method of forming CMOS memory integrated circuitry comprises the following steps:

> [0015] providing a series of gate lines over a semiconductor substrate, the gate lines comprising memory array gate lines and peripheral circuitry gate lines, a first gate line being positioned relative to a first peripheral area of the substrate for formation of a peripheral NMOS transistor, a second gate line being positioned relative to a second peripheral area of the substrate for formation of a peripheral PMOS transistor, a third gate line being positioned relative to a memory array area of the substrate for formation of a memory array NMOS transistor;
>
> [0016] masking the second gate line, the second peripheral PMOS substrate area, the third gate line and the memory array NMOS substrate area while conducting a p-type halo ion implant into the first peripheral NMOS substrate area adjacent the first gate line, the p-type halo ion implant being conducted at a first energy level to provide a p-type first impurity concentration at a first depth within the first peripheral NMOS substrate area; and
>
> [0017] in a common step, blanket ion implanting phosphorus into the first peripheral NMOS substrate area, the second peripheral PMOS substrate area and the memory array NMOS substrate area adjacent the first, the second and the third gate lines to form peripheral NMOS transistor LDD regions, peripheral PMOS transistor n-type halo regions and memory array NMOS transistor source/drain diffusion regions, respectively, the phosphorus implant being conducted at a second energy level to provide an n-type second impurity concentration at a second depth within the first, the second and the memory array substrate areas, the first energy level and the first depth being greater than the second energy level and the second depth, respectively.

[0018] In accordance with another aspect of the invention, a method of forming CMOS integrated circuitry comprises the following steps:

> [0019] providing a series of gate lines over a semiconductor substrate, a first gate line being positioned relative to an area of the substrate for formation of an NMOS transistor, a second gate line being positioned relative to an area of the substrate for formation of a PMOS transistor;

[0020] masking the second gate line and the PMOS substrate area while conducting a p-type halo ion implant into the NMOS substrate area adjacent the first gate line, the p-type halo ion implant being conducted at a first energy level to provide a p-type first impurity concentration at a first depth within the NMOS substrate area; and

[0021] in a common step, blanket ion implanting phosphorus into both the NMOS substrate area and the PMOS substrate area adjacent the first and the second gate lines to form both NMOS LDD regions and PMOS n-type halo regions, respectively, the phosphorus implant being conducted at a second energy level to provide an n-type second impurity concentration at a second depth within both the PMOS substrate area and the NMOS substrate area, the first energy level and the first depth being greater than the second energy level and the second depth, respectively.

[0022] More particularly, **FIG. 1** illustrates portions of a semiconductor wafer fragment in process indicated generally with reference numeral **10**. Such comprises a bulk silicon substrate **12** which is intrinsically p-doped, with a portion **14** thereof being subsequently n-doped to define an n-well. A series of gate lines are provided over semiconductor substrate **12**. The discussion proceeds with reference to preferred formation of CMOS memory integrated circuitry, with some of the gate lines comprising memory array gate lines and other of the gate lines constituting peripheral circuitry gate lines.

[0023] Specifically, a first gate line **16** is positioned relative to a first peripheral area **18** of substrate **12** for formation of a peripheral NMOS transistor. A second gate line **20** is positioned relative to a second peripheral area **22** of substrate **12** and n-well **14** for formation of a peripheral PMOS transistor. A third gate line **24** is positioned relative to a memory array area **26** for formation of a memory array NMOS transistor. Typical preferred present day cross sectional widths for gates **24, 16** and **20** are 0.40 micron, 0.42 micron, and 0.55 micron, respectively. In otherwords, the desired relationships are that the cross sectional widths of the n-channel periphery gates be greater than or equal to the memory array n-channel gates, with the p-channel peripheral gates being wider than both. The respective gate lines include a gate oxide layer **28**, a conductive polysilicon layer **30**, an overlying WSi_x layer **32**, an overlying novellus oxide layer **34**, and a Si_3N_4 capping layer **36**.

[0024] Referring to **FIG. 2, a** photoresist masking layer **38** is provided over second gate line **20**, second peripheral PMOS substrate area **22**, third gate line **24**, and memory array NMOS substrate area **26**. An n-type LDD implant **42**, preferably As, is then provided into the exposed first peripheral NMOS substrate area **18** adjacent first gate line **16**. An example and preferred average concentration of As for regions **42** is 8×10^{18} ions/cm^3. An example depth for the peak concentration is 400 Angstroms.

[0025] A p-type halo ion implant is subsequently conducted into the exposed first peripheral NMOS substrate area **18** adjacent first gate line **16**, thus producing p-type halo ion implant regions **44**. The p-type halo ion implant is conducted at a first energy level to provide a p-type first impurity concentration at a first depth within first peripheral NMOS substrate area **18**. The depth is preferably conducted to be deeper than the maximum concentration depth of As LDD regions **42**. An example and preferred p-type implant material is boron. An example and preferred implant dose is 7×10^{12} ions/cm^2-1.5×10^{13} ions/cm^2 to provide an example average dopant concentration of from 1×10^{16} ions/cm^3 to 1×10^{18} ions/cm^3, with about 1×10^{17} ions/cm^3 being preferred. An example preferred implant energy is from 60 KeV to 100 KeV (70 KeV preferred) to provide a peak concentration implant depth of 2000 Angstroms. Most preferably, the p-type halo implant is conducted as a series of implants angled from 0°, with an angle of about 30° from vertical (i.e., from 0°) being an example preferred angle. For example, a series of four 30° angled implants at 70 KeV at 90° wafer orientations using respective doses of 1.0×10^{12} ions/cm^2 is a preferred implant sequence. Such provides an advantage of desirably driving a portion of the halo implant beneath the gate.

[0026] Referring to **FIG. 3**, masking layer **38** is removed and wafer fragment **10** is subjected to oxidizing conditions to form oxidized sidewalls **46** about the illustrated gate lines, and to form oxide **48** over exposed peripheral NMOS area **18**, peripheral PMOS area **22**, and memory array NMOS area **26**.

[0027] Thereafter and in a common step, phosphorous is blanket ion implanted into exposed first peripheral NMOS substrate area **18**, second peripheral PMOS substrate area **22**, and memory array NMOS substrate area **26** adjacent the first, the second, and the third gate lines, respectively. This forms peripheral NMOS transistor LDD regions **50**, peripheral PMOS transistor n-type halo regions **52**, and memory array NMOS transistor source/drain diffusion regions **54**. The phosphorous implant is conducted at a second energy level to provide respective n-type second impurity concentrations at a second depth within the first, the second and the memory array substrate areas. The first energy level and the first depth of implants **44** are chosen to be greater than the second energy level and the second depth, respectively, of the blanket phosphorus implant. Most preferably, the implant energy difference between the p-type halo implant and the n-type blanket implant is greater than or equal to 10 KeV to provide the peak concentration of regions **44** at 1000 Angstroms below that of regions **50**. An example energy level for the phosphorous implant is from 30 Kev to 60 KeV, with 30 KeV being preferred. An example and desired dose is from 7×10^{12} ions/cm^2-1.5×10^{13} ions/cm^2 to provide an example average dopant concentration of diffusion regions **50, 52** and **54** of from 1×10^{17} ions/cm^3 to 1×10^{19} ions/cm^3, with about 8×10^{17} ions/cm^3 being preferred.

[0028] The above described sequence is the preferred order by which the respective implants occur. The subject orders could be changed without departing from the principals and scope of the invention which is intended to be limited only by the accompanying claims appropriately interpreted in accordance the Doctrine of Equivalents. Most preferably, the As LDD implant is conducted before the sidewall and substrate oxidations. The p-type halo implant is preferably conducted either before or after such oxidations. And, the greatest success was achieved where the blanket phosphorous implant is conducted after the sidewall and substrate oxidations.

[0029] Referring to **FIG. 4**, oxide or nitride sidewall spacers **60** are provided about the illustrated respective gate lines. Thereafter, a photoresist masking layer **62** is provided and patterned to expose peripheral NMOS transistor area **18** and mask the illustrated array and p-channel periphery areas **22** and **26**. An n-type implant is thereafter conducted to provide n-type diffusion regions **64** for the peripheral NMOS transistors to essentially complete formation thereof.

[0030] Referring to **FIG. 5**, the n-channel transistors are masked with a photoresist layer **66**, and ion implantation is conducted with a p-type material (i.e., boron) into the peripheral PMOS transistor to form desired p-type source/drain diffusion regions **68**.

[0031] Most preferably, additional doping in the memory array area relative to source/drain diffusion regions **54** is not required or conducted.

[0032] P-type halo implant **44** is provided principally for improving/eliminating short channel effects in the peripheral n-channel transistors. Accordingly with respect to the above described preferred embodiment, the single masking step of **FIG. 2** provides several advantageous functions. The initial **FIG. 2** doping enables provision of desired p-type n-channel halo implants **44**. The subsequent blanket phosphorous implant provides the combination of a p-channel halo, a source/drain diffusion implant for the array, and reduction of n-channel periphery LDD resistance which is much more desirable for the NMOS peripheral transistors than for the NMOS array transistors. All **FIGS. 2 and 3** implants are preferably conducted with the single **FIG. 2** masking, whereas prior art methods use multiple masks to achieve the same implants.

[0033] The above described embodiment was described principally with reference to formation of memory devices, such as DRAMs, that preferably utilized two different types of NMOS transistors and one type of PMOS transistors. The artisan will as well appreciate that the invention has application to non-memory devices including formation of three different transistor types. Further, the artisan will also appreciate applicability of the invention to formation of CMOS circuitry only incorporating one type of NMOS transistor and one type of PMOS transistor.

[0034] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

1. A method of forming CMOS integrated circuitry comprising the following steps:

providing a series of gate lines over a semiconductor substrate, a first gate line being positioned relative to an area of the substrate for formation of an NMOS transistor, a second gate line being positioned relative to an area of the substrate for formation of a PMOS transistor;

masking the second gate line and the PMOS substrate area while conducting a p-type halo ion implant into the NMOS substrate area adjacent the first gate line, the p-type halo ion implant being conducted at a first energy level to provide a p-type first impurity concentration at a first depth within the NMOS substrate area; and

in a common step, blanket ion implanting phosphorus into both the NMOS substrate area and the PMOS substrate area adjacent the first and the second gate lines to form both NMOS LDD regions and PMOS n-type halo regions, respectively, the phosphorus implant being conducted at a second energy level to provide an n-type second impurity concentration at a second depth within both the PMOS substrate area and the NMOS substrate area, the first energy level and the first depth being greater than the second energy level and the second depth, respectively.

2. The method of forming CMOS integrated circuitry of claim 1 wherein the p-type halo implant is conducted as a series of angled implants.

3. The method of forming CMOS integrated circuitry of claim 1 wherein the p-type halo implant is conducted as a series of angled implants, the angled implants being conducted at about 30° from vertical.

4. The method of forming CMOS integrated circuitry of claim 1 further comprising oxidizing sidewalls of the first gate line and the second gate line, and oxidizing the NMOS substrate area and the PMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate area and PMOS substrate area oxidations.

5. The method of forming CMOS integrated circuitry of claim 1 wherein the p-type halo implanting step is conducted before the blanket ion implanting step.

6. The method of forming CMOS integrated circuitry of claim 1 further comprising oxidizing sidewalls of the first gate line and the second gate line, and oxidizing the NMOS substrate area and the PMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate area and PMOS substrate area oxidations; and the p-type halo implanting step being conducted before the blanket ion implanting step.

7. The method of forming CMOS integrated circuitry of claim 1 further comprising oxidizing sidewalls of the first gate line and the second gate line, and oxidizing the NMOS substrate area and the PMOS substrate area; the p-type halo implanting step being conducted before the sidewall, NMOS substrate area and PMOS substrate area oxidation; and the blanket ion implanting step being conducted after the sidewall, NMOS substrate area and PMOS substrate area oxidations.

8. The method of forming CMOS integrated circuitry of claim 1 wherein the p-type halo implant is conducted as a series of angled implants, and

the p-type halo implanting step is conducted before the blanket ion implanting step.

9. The method of forming CMOS integrated circuitry of claim 1 wherein the p-type halo implant is conducted as a series of angled implants, and

the method further comprising oxidizing sidewalls of the first gate line and the second gate line, and oxidizing the NMOS substrate area and the PMOS substrate area; the step of blanket ion implanting being conducted after

the sidewall, NMOS substrate area and PMOS substrate area oxidations; and the p-type halo implanting step being conducted before the blanket ion implanting step.

10. The method of forming CMOS integrated circuitry of claim 1 wherein the p-type halo implant is conducted as a series of angled implants, and

the method further comprising oxidizing sidewalls of the first gate line and the second gate line, and oxidizing the NMOS substrate area and the PMOS substrate area; the p-type halo implanting step being conducted before the sidewall, NMOS substrate area and PMOS substrate area oxidation; and the blanket ion implanting step being conducted after the sidewall, NMOS substrate area and PMOS substrate area oxidations.

11. CMOS integrated circuitry produced according to the process of claim 1.

12. A method of forming CMOS integrated circuitry comprising the following steps:

providing a series of gate lines over a semiconductor substrate, a first gate line being positioned relative to a first area of the substrate for formation of a first NMOS transistor, a second gate line being positioned relative to a second area of the substrate for formation of a PMOS transistor, a third gate line being positioned relative to a third area of the substrate for formation of a second NMOS transistor;

masking the second gate line, the second PMOS substrate area, the third gate line and the third NMOS substrate area while conducting a p-type halo ion implant into the first NMOS substrate area adjacent the first gate line, the p-type halo ion implant being conducted at a first energy level to provide a p-type first impurity concentration at a first depth within the first NMOS substrate area; and

in a common step, blanket ion implanting phosphorus into the first NMOS substrate area, the second PMOS substrate area and the third NMOS substrate area adjacent the first, the second and the third gate lines to form first NMOS transistor LDD regions, second PMOS transistor n-type halo regions and second NMOS transistor source/drain diffusion regions, respectively, the phosphorus implant being conducted at a second energy level to provide an n-type second impurity concentration at a second depth within the first, the second and the third substrate areas, the first energy level and the first depth being greater than the second energy level and the second depth, respectively.

13. The method of forming CMOS integrated circuitry of claim 12 wherein the p-type halo implant is conducted as a series of angled implants.

14. The method of forming CMOS integrated circuitry of claim 12 wherein the p-type halo implant is conducted as a series of angled implants, the angled implants being conducted at about 30° from vertical.

15. The method of forming CMOS integrated circuitry of claim 12 further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first and third NMOS substrate areas and the second PMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations.

16. The method of forming CMOS integrated circuitry of claim 12 wherein the p-type halo implanting step is conducted before the blanket ion implanting step.

17. The method of forming CMOS integrated circuitry of claim 12 further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first and third NMOS substrate areas and the second PMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations; and the p-type halo implanting step being conducted before the blanket ion implanting step.

18. The method of forming CMOS integrated circuitry of claim 12 further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first and third NMOS substrate areas and the second PMOS substrate area; the p-type halo implanting step being conducted before the sidewall, NMOS substrate areas and PMOS substrate area oxidations; and the blanket ion implanting step being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations.

19. The method of forming CMOS integrated circuitry of claim 12 wherein the p-type halo implant is conducted as a series of angled implants, and

the p-type halo implanting step is conducted before the blanket ion implanting step.

20. The method of forming CMOS integrated circuitry of claim 12 wherein the p-type halo implant is conducted as a series of angled implants, and

the method further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first and third NMOS substrate areas and the second PMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations; and the p-type halo implanting step being conducted before the blanket ion implanting step.

21. The method of forming CMOS integrated circuitry of claim 12 wherein the p-type halo implant is conducted as a series of angled implants, and

the method further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first and third NMOS substrate areas and the second PMOS substrate area; the p-type halo implanting step being conducted before the sidewall, NMOS substrate areas and PMOS substrate area oxidations; and the blanket ion implanting step being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations.

22. CMOS integrated circuitry produced according to the process of claim 12.

23. A method of forming CMOS memory integrated circuitry comprising the following steps:

providing a series of gate lines over a semiconductor substrate, the gate lines comprising memory array gate lines and peripheral circuitry gate lines, a first gate line being positioned relative to a first peripheral area of the substrate for formation of a peripheral NMOS transistor, a second gate line being positioned relative to a second peripheral area of the substrate for formation of a peripheral PMOS transistor, a third gate line being positioned relative to a memory array area of the substrate for formation of a memory array NMOS transistor;

masking the second gate line, the second peripheral PMOS substrate area, the third gate line and the memory array NMOS substrate area while conducting a p-type halo ion implant into the first peripheral NMOS substrate area adjacent the first gate line, the p-type halo ion implant being conducted at a first energy level to provide a p-type first impurity concentration at a first depth within the first peripheral NMOS substrate area; and

in a common step, blanket ion implanting phosphorus into the first peripheral NMOS substrate area, the second peripheral PMOS substrate area and the memory array NMOS substrate area adjacent the first, the second and the third gate lines to form peripheral NMOS transistor LDD regions, peripheral PMOS transistor n-type halo regions and memory array NMOS transistor source/drain diffusion regions, respectively, the phosphorus implant being conducted at a second energy level to provide an n-type second impurity concentration at a second depth within the first, the second and the memory array substrate areas, the first energy level and the first depth being greater than the second energy level and the second depth, respectively.

24. The method of forming CMOS memory integrated circuitry of claim 23 wherein the p-type halo implant is conducted as a series of angled implants.

25. The method of forming CMOS memory integrated circuitry of claim 23 wherein the p-type halo implant is conducted as a series of angled implants, the angled implants being conducted at about 30° from vertical.

26. The method of forming CMOS memory integrated circuitry of claim 23 further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first peripheral NMOS substrate area, the peripheral PMOS substrate area, and the memory array NMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations.

27. The method of forming CMOS memory integrated circuitry of claim 23 wherein the p-type halo implanting step is conducted before the blanket ion implanting step.

28. The method of forming CMOS memory integrated circuitry of claim 23 further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first peripheral NMOS substrate area, the peripheral PMOS substrate area, and the memory array NMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations; and the p-type halo implanting step being conducted before the blanket ion implanting step.

29. The method of forming CMOS memory integrated circuitry of claim 23 further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first peripheral NMOS substrate area, the peripheral PMOS substrate area, and the memory array NMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations; and the blanket ion implanting step being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations.

30. The method of forming CMOS memory integrated circuitry of claim 23 wherein the p-type halo implant is conducted as a series of angled implants, and

the p-type halo implanting step is conducted before the blanket ion implanting step.

31. The method of forming CMOS memory integrated circuitry of claim 23 wherein the p-type halo implant is conducted as a series of angled implants, and

the method further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first peripheral NMOS substrate area, the peripheral PMOS substrate area, and the memory array NMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations; and the p-type halo implanting step being conducted before the blanket ion implanting step.

32. The method of forming CMOS memory integrated circuitry of claim 23 wherein the p-type halo implant is conducted as a series of angled implants, and

the method further comprising oxidizing sidewalls of the first, second and third gate lines, and oxidizing the first peripheral NMOS substrate area, the peripheral PMOS substrate area, and the memory array NMOS substrate area; the step of blanket ion implanting being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations; and the blanket ion implanting step being conducted after the sidewall, NMOS substrate areas and PMOS substrate area oxidations.

33. CMOS integrated circuitry produced according to the process of claim 23.

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