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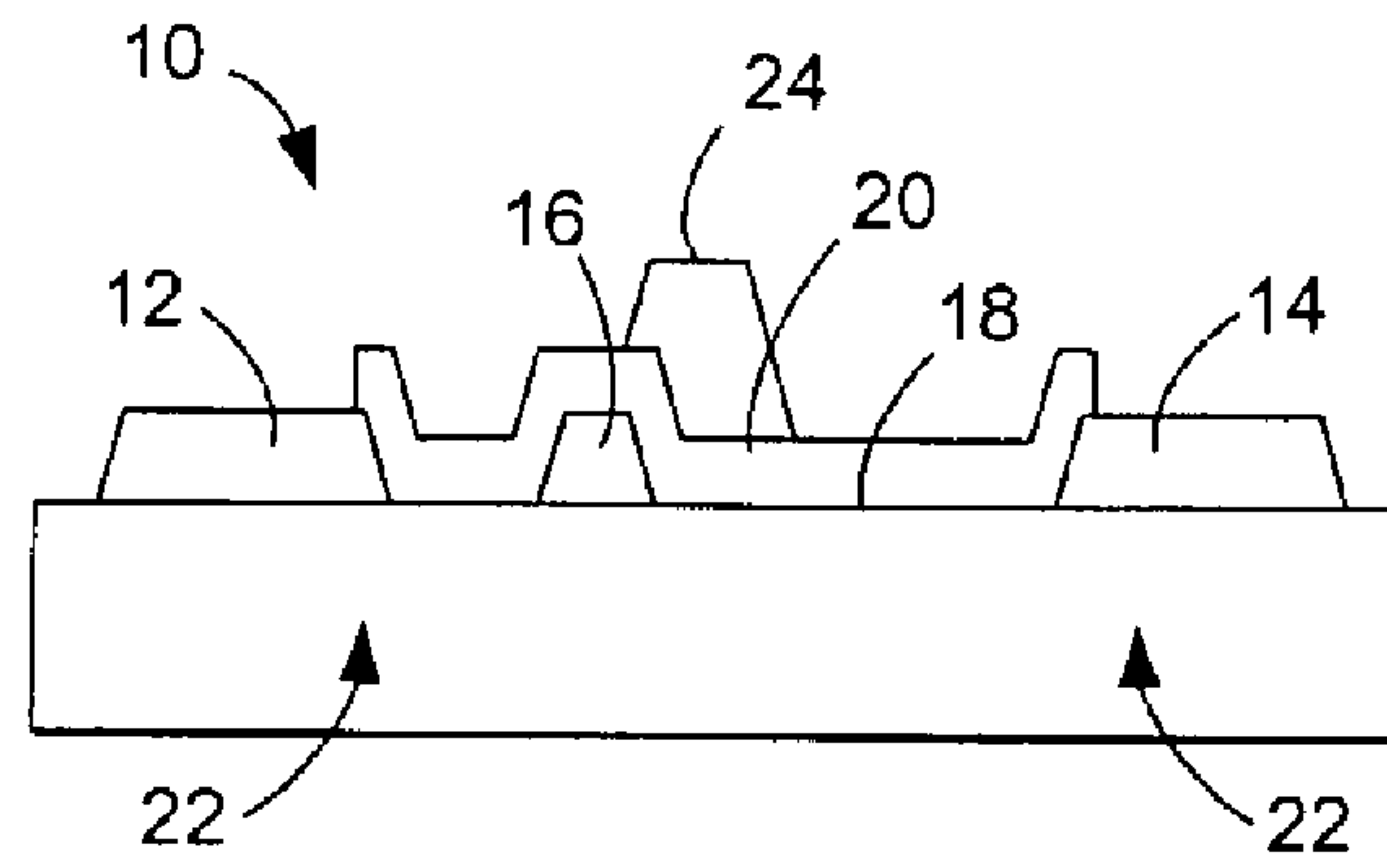
(54) **Titre : FABRICATION DE PLAQUES MULTIPLES OU UNIQUES A EFFET DE CHAMP GRILLE**
(54) **Title: FABRICATION OF SINGLE OR MULTIPLE GATE FIELD PLATES**



(57) **Abrégé/Abstract:**
A process for fabricating single or multiple gate field plates using consecutive steps of dielectric material deposition/growth, dielectric material etch and metal evaporation on the surface of a field effect transistors. This fabrication process permits a tight control on the field plate operation since dielectric material deposition/growth is typically a well controllable process. Moreover, the dielectric material deposited on the device surface does not need to be removed from the device intrinsic regions: this essentially enables the realization of field-plated devices without the need of low-damage dielectric material dry/wet etches. Using multiple gate field plates also reduces gate resistance by multiple connections, thus improving performances of large periphery and/or sub-micron gate devices.

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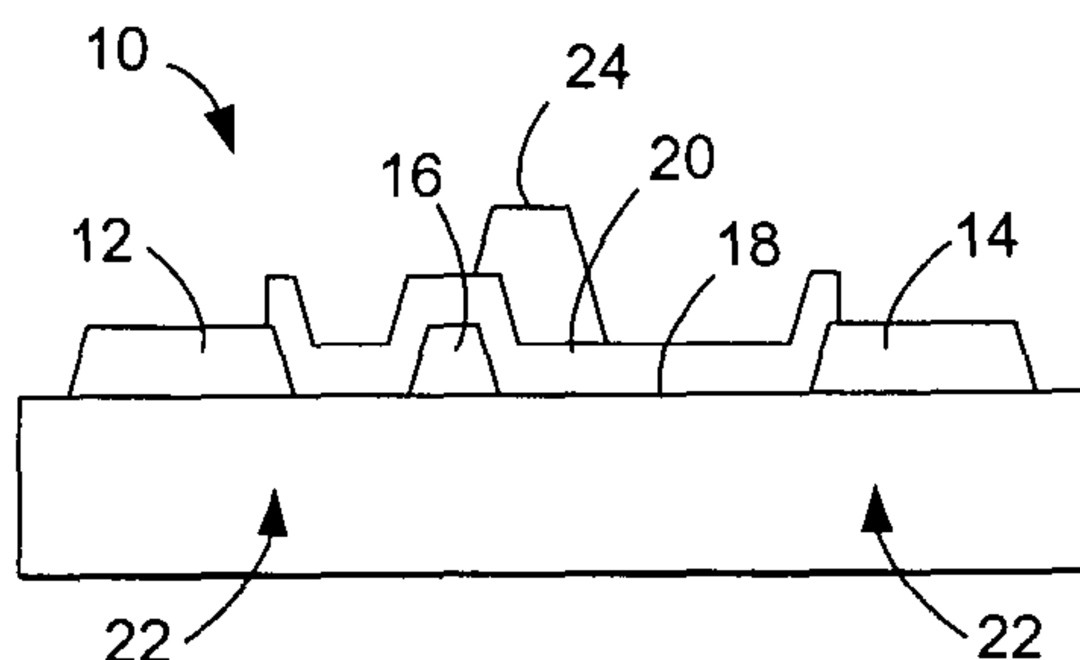
(54) Title: FABRICATION OF SINGLE OR MULTIPLE GATE FIELD PLATES



(57) Abstract: A process for fabricating single or multiple gate field plates using consecutive steps of dielectric material deposition/growth, dielectric material etch and metal evaporation on the surface of a field effect transistors. This fabrication process permits a tight control on the field plate operation since dielectric material deposition/growth is typically a well controllable process. Moreover, the dielectric material deposited on the device surface does not need to be removed from the device intrinsic regions: this essentially enables the realization of field-plated devices without the need of low-damage dielectric material dry/wet etches. Using multiple gate field plates also reduces gate resistance by multiple connections, thus improving performances of large periphery and/or sub-micron gate devices.

FABRICATION OF SINGLE OR MULTIPLE GATE FIELD PLATES

BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to semiconductor devices, and more particularly, to the
5 fabrication of single or multiple gate field plates.

2. Description of the Related Art.

(Note: This application references to various publications as indicated in the specification by reference numbers enclosed in brackets, e.g., [x]. A list of these publications ordered according to these reference numbers can be found below in the section
10 entitled "References.")

In a semiconductor-based field effect transistor (FET), a large electric field arises during normal operation in the gate-drain access region. Field plating is a well-known technique for improving device performance under high electric field operation as well as alleviating surface traps phenomena [1], [2]. For example, field plating has been an effective and well-known technique in order to alleviate all the detrimental effects (breakdown voltages, trapping effects, reliability) that take places in devices operating at high electric field.

The basic concept of field plating relies on the vertical depletion of the device active region, thus enabling larger extensions of the horizontal depletion region. This results in a lower electric field in the device active region for a given bias voltage, alleviating all the detrimental effects (low breakdown, trapping phenomena, poor reliability) that take place whenever a device is operated at a high electric field. Moreover, a field plate positioned in the gate drain access region has also the capability of modulating the device active region, resulting in a decrease of surface traps effects that prevent proper device operation under large radio frequency (RF) signals

What is needed, however, are improved methods of fabricating single or multiple gate field plates as well as improved structures incorporating single or multiple gate field plates.

SUMMARY OF THE INVENTION

Embodiments of the present invention provide improved methods of fabricating single and multiple gate field plates. A fabrication process according to the invention uses consecutive steps of dielectric material deposition or growth, dielectric material etch and metal evaporation on the surface of field effect transistors. The advantages of the fabrication process include tight control of the dielectric material thickness, and the absence of any exposure of the surface of the device active region to any dry or wet etch process that may induce damage in the semiconductor material forming the field effect transistor. Moreover, the dielectric material deposited

on the device surface does not need to be removed from the device intrinsic regions, which enables the realization of field-plated devices without damage caused by the dry or wet etch processes. Using multiple gate field plates reduces gate resistance through the use of multiple connections, thus improving performances of large periphery and/or sub-micron
5 gate devices. Finally, by properly adjusting the thickness of the dielectric material, parallel gate contacts can be deposited on top of the dielectric material, in order to significantly reduce gate resistance by electrically connecting the parallel gate contacts on device extrinsic regions.

According to another aspect, there is provided a method of fabricating one or more
10 gate field plates, comprising:

providing a dielectric material on an active region and a gate of a device;

etching the dielectric material; and

evaporating metal onto the dielectric material to create at least one field plate wherein:

15 (i) no dielectric material provided on the active region of the device is removed to expose the active region,

(ii) the at least one field plate is created on the dielectric material, and

(iii) the gate is directly on the active region.

According to another aspect, there is provided a method of fabricating gate field
20 plates, comprising:

(a) depositing or growing the dielectric material on intrinsic and extrinsic regions of the device;

(b) patterning the dielectric material, so that the dielectric material remains principally on an active region of the device; and

25 (c) creating a field plate on the patterned dielectric material, wherein gate and field plate contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween.

According to a further aspect, there is provided a high electron mobility transistor (HEMT), comprising:

30 a barrier layer formed on a channel layer;

a spacer layer grown on the barrier layer; and

source and drain electrodes formed making ohmic contacts through the barrier layer such that an electric current flows between the source and drain electrodes when a gate electrode is biased at an appropriate level;

wherein the spacer layer is etched and the gate electrode is deposited such that at least a portion of the gate electrode is on a surface of barrier layer, and

wherein a portion of the gate electrode is patterned to extend across the spacer layer so that the gate electrode forms a field plate extending a distance away from the
5 gate electrode towards the drain electrode, or

wherein a field plate is formed above a dielectric layer formed on the gate electrode, such that the field plate and the gate electrode overlap.

According to another aspect, there is provided a method of fabricating a gated device, comprising:

10 (a) providing a spacer layer or dielectric material on an active region of a device;

(b) providing an opening in the spacer layer or dielectric material for depositing a gate on the device;

(c) providing a gate in the opening; and

(d) providing metal onto the dielectric material or spacer layer to create at least one
15 field plate on the spacer layer or the dielectric material, wherein no material provided on the active region is removed to expose the active region except at a location of the opening for the gate

According to a further aspect, there is provided a gated device, comprising:

a spacer layer on an active region of a device;

20 an opening in the spacer layer for a gate;

a gate in the opening; and

a field plate on the spacer layer, wherein the spacer layer is not removed to expose the active region except at a location of the opening for the gate.

According to another aspect, there is provided a method of fabricating one or more
25 gate field plates, comprising:

providing a dielectric material on an active region of a device; and

providing metal onto the dielectric material to create at least one field plate, wherein a gate and at least one field plate of the device are electrically connected at least in an extrinsic region of the device.

30 According to another aspect, there is provided a method of fabricating gate field plates, comprising:

(a) depositing or growing dielectric material on intrinsic and extrinsic regions of a device;

(b) patterning the dielectric material, so that the dielectric material remains
35 principally on an active region of the device; and

(c) creating a field plate on the patterned dielectric material, wherein the gate and the field plate are electrically shorted and overlap at least outside a lateral boundary of the active region, providing a low resistance connection therebetween.

According to a further aspect, there is provided a transistor, comprising:

5 a semiconductor layer, wherein the semiconductor layer confines a conducting channel in the transistor;

a spacer layer on the semiconductor layer, wherein the spacer layer does not significantly induce a charge in the conducting channel;

a gate electrode deposited in an opening in the spacer layer, wherein at least a 10 bottom-most portion of the gate electrode is on the semiconductor layer;

source and drain electrodes making ohmic contacts such that an electric current flows in the conducting channel between the source and drain electrodes when the gate electrode is biased at an appropriate level;

a field plate extending across at least a portion of the spacer layer; and

15 wherein the spacer layer is removed to expose the semiconductor layer only at the opening for the gate electrode.

According to another aspect, there is provided a method of fabricating a gated device, comprising:

(a) providing a spacer layer or dielectric material on a semiconductor layer of a 20 device, wherein the semiconductor layer confines a conducting channel in the device;

(b) providing an opening in the spacer layer or dielectric material for depositing a gate on the device;

(c) providing a gate in the opening; and

(d) providing metal onto the dielectric material or spacer layer to create at least one 25 field plate on the spacer layer or the dielectric material, wherein no material provided on the semiconductor layer is removed to expose the semiconductor layer except at the opening for the gate.

According to a further aspect, there is provided a gated device, comprising:

a spacer layer on a semiconductor layer of a device, wherein the semiconductor 30 layer confines a conducting channel in the device;

an opening in the spacer layer for a gate;

a gate in the opening; and

a field plate on the spacer layer, wherein the spacer layer is not removed to expose the semiconductor layer except at the opening for the gate.

According to another aspect, there is provided a method of fabricating one or more gate field plates, comprising:

providing a dielectric material on an active region of a device; and

providing metal onto the dielectric material to create at least one field plate, wherein
5 a gate and at least one field plate of the device are electrically connected and overlap at least outside a lateral boundary of the active region.

According to a further aspect, there is provided a method of fabricating one or more gate field plates, comprising:

(a) providing a dielectric material on a semiconductor layer of a device, wherein the
10 semiconductor layer confines a conducting channel in the device;

(b) providing an opening in the dielectric material for depositing a gate on the device; and

(c) providing metal onto the dielectric material to create at least one field plate, wherein no material provided on the semiconductor layer is removed to expose the active
15 region except at the opening for the gate.

According to another aspect, there is provided a method of fabricating a gated device, comprising:

providing a spacer layer on an active region of a device, wherein the spacer layer is not part of a structure that forms the active region;

20 providing an opening in the spacer layer for a gate;

depositing a gate in the opening; and

creating a field plate on the spacer layer, wherein no layer provided on the active region of the device is removed to expose the active region except at the opening for the gate, and wherein the field plate is electrically connected to the gate.

25 According to a further aspect, there is provided a method of fabricating a transistor, comprising:

providing a spacer layer on a semiconductor layer, wherein:

the semiconductor layer confines a conducting channel in the transistor; and

the spacer layer does not significantly induce a charge in the conducting
30 channel;

removing the spacer layer to expose the semiconductor layer only at an opening for a gate electrode;

depositing the gate electrode in the opening, wherein at least a bottom-most portion of the gate electrode is on a surface of the semiconductor layer;

35 depositing source and drain electrodes making ohmic contacts such that an electric

current flows in the conducting channel between the source and drain electrodes when the gate electrode is biased at an appropriate level; and

depositing a field plate extending across at least a portion of the spacer layer.

According to another aspect, there is provided a transistor, comprising:

5 a semiconductor layer confining a conducting channel in the transistor;

a gate on or above the semiconductor layer;

dielectric material on the semiconductor layer and the gate of a device; and

one or more field plates on the dielectric material, wherein the dielectric material is not removed to expose the semiconductor layer.

10 According to a further aspect, there is provided a high electron mobility transistor (HEMT), comprising:

a nucleation layer;

a channel layer on the nucleation layer;

a barrier layer on the channel layer;

15 a spacer layer on the barrier layer; and

source and drain electrodes making ohmic contacts through the barrier layer such that an electric current flows between the source and drain electrodes when a gate electrode is biased at an appropriate level;

wherein the spacer layer is etched to expose the barrier layer and the gate electrode

20 is deposited such that at least a bottom portion of the gate electrode is on a surface of barrier layer,

wherein a top portion of the gate electrode is patterned to extend across the spacer layer so that the top portion of the gate electrode forms a field plate extending a distance away from the gate electrode towards the drain electrode; and

25 wherein a passivation layer covers both the gate electrode and at least a portion of the spacer layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

30 FIG. 1A is a cross-sectional and FIG. 1B is a top view of a field effect transistor (FET);

FIG. 2A is a device cross-section and FIG. 2B is a device top view illustrating dielectric material deposition/growth;

FIG. 3A is a device cross-section and FIG. 3B is a device top view illustrating dielectric material being removed from device extrinsic regions;

FIG. 4A is a device cross-section and FIG. 4B is a device top view illustrating evaporation of gate field plate;

5 FIG. 5A is a device cross-section and FIG. 5B is a device top view illustrating an example of multiple field plate structure;

FIG. 6 is a graph of simulation of f_{max} dependence vs. gate finger width;

FIG. 7A is a device cross-section, FIG. 7B is a device top view and FIG. 7C is a device cross-section illustrating a multiple field plate device for reduced gate resistance;

10 FIG. 8 is a schematic cross-section of a unit cell of a nitride-based HEMT (High Electron Mobility Transistor) device;

FIG. 9 is a schematic cross-section of a unit cell of a nitride-based HEMT device having a different configuration from the device illustrated in FIG. 8; and

FIG. 10 is a graph that illustrates the effect of field plate distance on device performance.

5

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to
10 be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Overview

The present invention describes a simple fabrication process for the realization
15 of single or multiple gate field plate structures for field effect transistors (FETs). The present invention uses simple and typically well-controlled consecutive processing steps of dielectric material deposition or growth, dielectric material etch and metal evaporation.

20 ### Fabrication Process

FIGS. 1A, 1B, 2A, 2B, 3A, 3C, 4A, and 4B illustrate the steps of one possible realization of the fabrication process according an embodiment of the invention, wherein the fabrication process comprises a method of fabricating gate field plates.

FIG. 1A is a cross-sectional and FIG. 1B is a top view of a field effect
25 transistor (FET) 10 that includes source and drain ohmic contacts 12 and 14, a gate contact 16 and an active region 18. The steps of the fabrication process are applied on the field effect transistor 10 or other device. The method generally comprises performing consecutive steps of dielectric material deposition or growth, dielectric material etch and metal evaporation to create one or more field plates on a surface of

the device, wherein the steps permit a tight control on field plate operation and wherein the dielectric material deposited on the surface does not need to be removed from the active region 18, thereby enabling realization of a field-plated device without using a low-damage dielectric material dry or wet etch process. The performing step further comprises the steps of: (1) depositing or growing the dielectric material on the intrinsic and extrinsic regions of the device, wherein the dielectric material thickness is controlled in order to achieve proper operation of the device; (2) patterning the dielectric material by the dry or wet etch process or by a lift-off process, so that the dielectric material remains principally on an active region of the device; and (3) evaporating a field plate on the patterned dielectric material, wherein gate and field plate contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween. These steps are described in more detail below in conjunction with FIGS. 2A, 2B, 3A, 3B, 4A and 4B.

FIG. 2A is a device cross-section and FIG. 2B is a device top view illustrating the first step of the fabrication process, which comprises depositing or growing the dielectric material 20 on intrinsic and extrinsic regions of the device 10. The dielectric material 20 thickness is the critical parameter to be controlled in order to achieve proper operation of the finished device 10. However, this is usually a well controlled process in most deposition/growth techniques, e.g., PECVD (Plasma Enhanced Chemical Vapor Deposition). Typical materials are silicon nitrides and oxides, but others can be used, as long as they can be patterned by dry or wet etching or by lift-off.

FIG. 3A is a device cross-section and FIG. 3B is a device top view illustrating the second step of the fabrication process, which comprises patterning the dielectric material 20, by etch or removal from device extrinsic regions 22, so that the dielectric material 20 remains principally on an active region 18 of the device 10. In the case where the pattern is formed by etching, it should be stressed that the device 10 surface will be protected during this step, preventing any exposure of the surface of the active region 18 to any dry or wet etch process that may induce damage in the

semiconductor material forming the device. After this step, ohmic contacts 12, 14 are electrically accessible, as well as the gate portion 16 that resides in the device extrinsic region 22.

FIG. 4A is a device cross-section and FIG. 4B is a device top view illustrating
5 the third step of the fabrication process, which comprises creating a field plate 24 on the patterned dielectric material 20, wherein gate 16 and field plate 24 contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween. Preferably, metal evaporation is used to form the field plate 24, wherein the field plate 24 comprised of a metal stripe or contact. The
10 field plate 24 is positioned in a gate 16 drain access region, thereby providing a capability of modulating the active region 18, resulting in a decrease of surface traps effect that prevent proper device operation under large RF signals. The field plate 24 is connected to both sides of the device intrinsic region, and the gate 16 and field plate 24 are electrically shorted at least at one side of the extrinsic region 22, providing a
15 low resistance connection between the two metal lines thereof. The offset and length of the field plate 24 are optimized with respect to the targeted device performance, i.e., breakdown voltage, RF performance, etc.

If a multiple field plate structure is required, the three steps of dielectric material deposition/growth, dielectric material etch and metal evaporation described
20 in FIGS. 2A, 2B, 3A, 3B, 4A and 4B can be repeated.

FIG. 5A is a device cross-section and FIG. 5B is a device top view illustrating an example of creating multiple connections using multiple gate field plates in order to reduce gate resistance, thereby improving the performance of a large periphery device and/or sub-micron gate device. This example is a two field plate structure,
25 which includes another layer of dielectric material 26 and another field plate 28 comprised of a metal stripe or contact. Dielectric material 26 thickness, field plate 28 length and offset with respect to the gate 16 and other field plates 24, and the number of field plates 24, 28 introduced, comprise fabrication process parameters. Using

multiple field plates 24, 28 allows more freedom in device 10 design, and has a significant impact in the realization of high voltage devices 10.

Another advantage of the present invention is the possibility of alleviating the decrease in RF performance induced by gate resistance in a large periphery device.
5 Typically, the frequency of maximum oscillation (f_{max}) decreases at the increasing of the gate finger width due to the increase in gate resistance.

FIG. 6 is a graph of simulation of f_{max} dependence vs. gate finger width. As indicated in the graph, the introduction of a field plate structure shorted on both ends of the active region can improve f_{max} performances of devices with large finger width.
10 Using a field plate with a resistance Rf equivalent to the gate resistance Rg and connected to both sides of the active region significantly improves f_{max} performance. Further improvement can be achieved by lowering field plate resistance. It should be stressed that this decrease will be observed only if the parasitic capacitances added by the field plate structure are negligible compared to those of the intrinsic device. This
15 can be achieved by proper choice of dielectric material and its thickness, and has to be considered as an optimization process.

Multiple connections between the gate and field plate also results in a significant decrease in the gate resistance. In order to achieve this multiple connection without severely degrading RF operation, a small portion of the active region is
20 etched prior to gate deposition to create the multiple connections between the gate and the field plates without degrading the device's RF operation.

In this region, the gate and field plates can be connected without introducing any additional parasitic capacitance to the device. Again, device performance improves only if the introduced parasitic capacitance is small as compared to those of
25 the intrinsic device. Furthermore, the spacing between individual active regions is used to engineer the thermal impedance of the device more effectively than a device with a conventional topology.

Critical parameters are the choice of dielectric material, the thickness of the dielectric material, and the length of the field plates. These critical parameters have to be considered as optimization steps of the proposed fabrication process.

Using this method allows the fabrication of large periphery devices with a reduced number of air bridges. Moreover, the fabrication of sub-micron devices can take advantage of the present invention. Typically, sub-micron gates are fabricated using a T-shape process, since the T-shape reduces gate resistance as compared to a standard gate shape. Low gate resistance can be achieved even with sub-micron gates by creating the multiple connections without a T-shape process.

In addition, a parallel gate contact can be deposited on top of the dielectric material by properly adjusting the material dielectric thickness, in order to significantly reduce gate resistance by creating multiple connections using the parallel field plates on the device extrinsic regions. The low resistance path is provided by the parallel field plates, through a proper choice of the width at which the connection between the gate and field plates occurs.

FIG. 7A is a device cross-section, FIG. 7B is a device top view and FIG. 7C is a device cross-section illustrating examples of multiple field plate structures for reduced gate resistance. Moreover, having a field plate covering the gate source access region, such as shown in FIGS. 7A, 7B and 7C, is also used for of modulating source access resistance for improving device linearity performance.

Gallium Nitride-Based High Electron Mobility Transistor with Field Plates

GaN based transistors including AlGaN/GaN High Electron Mobility Transistors (HEMTs) are capable of very high voltage and high power operation at RF, microwave and millimeter-wave frequencies. However, electron trapping and the ensuing difference between DC and RF characteristics has limited the performance of these devices. SiN passivation has been successfully employed to alleviate this trapping problem, resulting in high performance devices with power densities over 10 W/mm at 10 GHz. For example, [3] discloses methods and structures for reducing the

trapping effect in GaN transistors. However, due to the high electric fields existing in these structures, charge trapping is still an issue.

The present invention has been successfully utilized for improving the performance of AlGaN/GaN HEMT power devices. At 4 GHz operation, power
5 densities of 12W/mm and 18.8W/mm have been achieved for devices on sapphire and silicon carbide substrate, respectively. Due to the simplicity of the processing step involved in the field plate fabrication, the present invention can be used in the development of A1GaN/GaN HEMTs technology and other semiconductor devices. Using properly designed multiple field plates greatly improves both breakdown and
10 large RF signal performance in such devices.

A GaN-based HEMT includes a channel layer and a barrier layer on the channel layer. Metal source and drain ohmic contacts are formed in contact with the barrier layer. A gate contact is formed on the barrier layer between the source and drain contacts and a spacer layer is formed above the barrier layer. The spacer layer
15 may be formed before or after formation of the gate contact. The spacer layer may comprise a dielectric layer, a layer of undoped or depleted $Al_xGa_{1-x}N$ ($0<=x<=1$) material, or a combination thereof. A conductive field plate is formed above the spacer layer and extends a distance Lf (field plate distance) from the edge of the gate contact towards the drain contact. The field plate may be electrically connected to
20 the gate contact. In some embodiments, the field plate is formed during the same deposition step as an extension of the gate contact. In other embodiments, the field plate and gate contact are formed during separate deposition steps. This arrangement may reduce the peak electric field in the device resulting in increased breakdown voltage and reduced trapping. The reduction of the electric field may also yield other
25 benefits such as reduced leakage currents and enhanced reliability.

An embodiment of the invention is illustrated in FIG. 8, which is a schematic cross-section of a unit cell 30 of a nitride-based HEMT device. Specifically, the device 30 includes a substrate 32, which may comprise silicon carbide, sapphire, spinel, ZnO, silicon or any other material capable of supporting growth of Group III-

nitride materials. An $Al_zGa_{1-z}N$ ($0<=z<=1$) nucleation layer 34 is grown on the substrate 32 via an epitaxial crystal growth method, such as MOCVD (Metalorganic Chemical Vapor Deposition), HVPE (Hydride Vapor Phase Epitaxy) or MBE (Molecular Beam Epitaxy). The formation of nucleation layer 34 may depend on the
5 material of substrate 32. For example, methods of forming nucleation layer 34 on various substrates are taught in [4] and [5]. Methods of forming nucleation layers on silicon carbide substrates are disclosed in [6], [7] and [8].

A high resistivity Group III-nitride channel layer 36 is formed on the nucleation layer 34. Channel layer 36 may comprise $Al_xGa_yIn_{(1-x-y)}N$ ($0<=x<=1$,
10 $0<=y<=1$, $x+y<=1$). Next, an $Al_xGa_{1-x}N$ ($0<=x<=1$) barrier layer 38 is formed on the channel layer 36. Each of the channel layer 36 and barrier layer 38 may comprise sub-layers that may comprise doped or undoped layers of Group III-nitride materials. Exemplary structures are illustrated in [3], [9], [10], [11] and [12]. Other nitride-based HEMT structures are illustrated in [13] and [14].

15 In the embodiment illustrated in FIG. 8, a Group III-nitride semiconductor spacer layer 40 is grown on the $Al_xGa_{1-x}N$ barrier layer 28. Spacer layer 40 may have a uniform or graded composition. Spacer layer 40 may be undoped and/or may be designed to be fully depleted as grown.

Source 42 and drain 44 electrodes are formed making ohmic contacts through
20 the barrier layer 38 such that an electric current flows between the source and drain electrodes 42, 44 via a two-dimensional electron gas (2DEG) induced at the heterointerface between the channel layer 36 and barrier layer 38 when a gate electrode 46 is biased at an appropriate level. The formation of source and drain electrodes 42, 44 is described in detail in the patents and publications referenced
25 above.

The spacer layer 40 may be etched and the gate electrode 46 deposited such that the bottom of the gate electrode 46 is on the surface of barrier layer 38. The metal forming the gate electrode 46 may be patterned to extend across spacer layer 40 so that the top of the gate 46 forms a field plate structure 48 extending a distance Lf

away from the edge of gate 46 towards drain 44. Stated differently, the part of the gate 46 metal resting on the spacer layer 40 forms an epitaxial field plate 48. Finally, the structure is covered with a dielectric passivation layer 50 such as silicon nitride. Methods of forming the dielectric passivation 50 are described in detail in the patents
5 and publications referenced above.

Other embodiments of the invention are illustrated in FIG. 9, which is a schematic cross-section of a unit cell 30 of a nitride-based HEMT device having a different configuration from the device illustrated in FIG. 8. The substrate 32, nucleation layer 34, channel layer 36 and barrier layer 38 in the device 30 illustrated
10 in FIG. 9 are similar to the corresponding layers illustrated in FIG. 8. In some embodiments, the substrate 32 comprises semi-insulating 4H-SiC commercially available from Cree, Inc. of Durham, N.C., the nucleation layer 34 is formed of AlN, and the channel layer 36 comprises a 2 μm thick layer of GaN:Fe, while barrier layer 38 comprises 0.8 nm of AlN and 22.5 nm of $Al_xGa_{1-x}N$, wherein $x = 0.195$, as
15 measured by PL (photoluminescence).

The gate electrode 46 is formed after formation of barrier layer 38 and passivation layer 50 is deposited on the device. A field plate 48 is then formed on the passivation layer 50 overlapping the gate 46 and extending a distance Lf in the gate-drain region. In the embodiment illustrated in FIG. 9, passivation layer 50 serves as a
20 spacer layer for the field plate 48. The overlap of the field plate 48 above the gate 46 and the amount of extension in the gate-drain region may be varied for optimum results. Field plate 48 and gate 46 may be electrically connected with a via or other connection (not shown).

In some embodiments, the field plate 48 may extend a distance Lf of 0.2 to 1
25 μm. In some embodiments, the field plate 48 may extend a distance Lf of 0.5 to 0.9 μm. In preferred embodiments, the field plate 48 may extend a distance Lf of 0.7 μm.

A GaN-based HEMT structure in accordance with the embodiment of FIG. 9 was constructed and tested. The device achieved a power density of 32 W/mm with 55% Power Added Efficiency (PAE) operating at 120 V and 4GHz.

The effect of field plate distance (Lf) on device performance was tested. Devices were fabricated generally in accordance with the embodiment of FIG. 9 except that the field plate length Lf was varied from a distance of 0 to 0.9 μm. The PAE of the resulting devices was then measured. As illustrated in FIG. 10, the PAE showed improvement once the field plate length was extended to 0.5 μm, with an optimum length of about 0.7 μm. However, the optimum length may depend on the specific device design as well as operating voltage and frequency.

References

The following references are incorporated by reference herein:

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[3] U.S. Patent No. 6,586,781, issued July 1, 2003, to Wu, et al., entitled "Group III nitride based FETs and HEMTs with reduced trapping and method for producing the same."

[4] U.S. Patent No. 5,290,393, issued March 1, 1994, to Nakamura, entitled "Crystal growth method for gallium nitride-based compound semiconductor."

[5] U.S. Patent No. 5,686,738, issued November 11, 1997, to Moustakas, entitled "Highly insulating monocrystalline gallium nitride thin films."

[6] U.S. Patent No. 5,393,993, issued February 28, 1995, to Edmond, et al., entitled "Buffer structure between silicon carbide and gallium nitride and resulting semiconductor devices."

[7] U.S. Patent No. 5,523,589, issued June 4, 1996, to Edmond, et al., entitled "Vertical geometry light emitting diode with group III nitride active layer and extended lifetime."

[8] U.S. Patent No. 5,739,554, issued April 14, 1998, to Edmond, et al., entitled "Double heterojunction light emitting diode with gallium nitride active layer."

[9] U.S. Patent No. 6,316,793, issued November 13, 2001, to Sheppard, et al., entitled "Nitride based transistors on semi-insulating silicon carbide substrates."

5 [10] U.S. Patent No. 6,548,333, issued April 15, 2003, to Smith, entitled "Aluminum gallium nitride/gallium nitride high electron mobility transistors having a gate contact on a gallium nitride based cap segment."

[11] U.S. Patent Application Publication No. 2002/0167023, published November 14, 2002, by Chavarkar, Prashant; et al., entitled "Group-III nitride based
10 high electron mobility transistor (HEMT) with barrier/spacer layer."

[12] U.S. Patent Application Publication No. 2003/0020092, published January 30, 2003, by Parikh, Primit, et al., entitled "Insulating gate AlGaN/GaN HEMT."

[13] U.S. Patent No. 5,192,987, issued March 9, 1993, to Khan, et al., entitled
15 "High electron mobility transistor with GaN/$Al_xGa_{1-x}N$ heterojunctions."

[14] U.S. Patent No. 5,296,395, issued March 22, 1994, to Khan, et al., entitled "Method of making a high electron mobility transistor."

[15] Y.-F. Wu, A. Saxler, M. Moore, R.P. Smith, S. Sheppard, P.M. Chavarkar, T. Wisleder, U.K. Mishra, P. Parikh, "30 W/mm GaN HEMTs by field
20 plate optimization", IEEE EDL, Vol. 25, No.3, pp. 117-119, March 2004.

[16] S. Karmalkar, U.K. Mishra, Very high voltage AlGaN-GaN HEMT using a field plate deposited on a stepped insulator, Solid State Electronics, 45 (2001) 1645-1652.

Conclusion

This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended
5 to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A method of fabricating one or more gate field plates, comprising:
providing a dielectric material on an active region and a gate of a device;
5 etching the dielectric material; and
evaporating metal onto the dielectric material to create at least one field plate wherein:
(i) no dielectric material provided on the active region of the device is removed to expose the active region,
(ii) the at least one field plate is created on the dielectric material, and
10 (iii) the gate is directly on the active region.

2. The method of claim 1, wherein each of the steps vary one or more parameters comprising the field plate's offset with respect to the gate and other field plates, the number of the field plates, the field plate's length, the dielectric material's thickness, and the electrical
15 connection between the field plates and the gate, in order to permit control on field plate's operation and achieve a desired breakdown voltage or radio frequency (RF) performance.

3. The method of claim 1, further comprising creating multiple connections using multiple field plates in order to reduce gate resistance.

20

4. The method of claim 1, wherein the at least one field plate is positioned in a gate drain access region, thereby providing a capability of modulating the active region, resulting in a decrease of surface traps effect that prevent proper device operation under larger radio frequency (RF) signals.

25

5. The method of claim 1, further comprising preventing any exposure of the surface of the active region to the dry or wet etch process that may induce damage in the device.

6. The method of claim 1, further comprising depositing parallel field plates on top of the
30 dielectric material by properly adjusting the dielectric material's thickness, in order to significantly reduce gate resistance by electrically connecting at least two parallel field plates on extrinsic regions, wherein the dielectric material's thickness is selected to ensure parasitic capacitances added by the field plates are negligible compared to those of an intrinsic device.

35 7. The method of claim 1, wherein the device is a field effect transistor that includes source and drain ohmic contacts, the gate and the active region.

8. The method of claim 1, wherein:

(1) the providing step comprises depositing or growing the dielectric material on intrinsic and extrinsic regions of the device;

5 (2) the etching step comprises patterning the dielectric material, so that the dielectric material remains principally on the active region of the device; and

(3) the evaporating step comprises creating the at least one field plate on the patterned dielectric material, wherein the gate and the at least one field plate contacts are electrically connected at least at one side of, or in, the device's extrinsic region, providing a low resistance

10 connection therebetween.

9. The method of claim 8, further comprising controlling the dielectric material's thickness between the field plates in order to achieve proper radio frequency (RF) operation of the device.

15

10. The method of claim 8, wherein the patterning step (2) comprises patterning the dielectric material by a dry or wet etch process or by a lift-off process.

11. The method of claim 8, wherein the creating step (3) comprises evaporating the at least

20 one field plate on the patterned dielectric material before the gate and the at least one field plate contacts are electrically shorted.

12. The method of claim 8, wherein steps (1)-(3) are repeated to create a plurality of the field plates.

25

13. The method of claim 8, wherein the at least one field plate has a resistance Rf that is equivalent to a gate resistance Rg.

14. The method of claim 8, wherein the at least one field plate is connected to both sides of

30 the device intrinsic region.

15. The method of claim 8, further comprising creating multiple connections between the gate and the at least one field plate to decrease gate resistance.

16. The method of claim 15, wherein the creating multiple connections step comprises etching a portion of the active region prior to deposition of the gate to create the multiple connections between the gate and the at least one field plate.

5 17. The method of claim 15, further comprising dividing the active region into a plurality of active regions and spacing between the active regions to engineer a thermal impedance of the device.

18. The method of claim 15, wherein the device comprises a larger periphery device with a
10 reduced number of air bridges as compared to a device without multiple connections, without the dielectric material remaining principally on the active region, and without the electrically shorted gate and at least one field plate contacts.

19. The method of claim 15, wherein the creating multiple connections step comprises
15 creating the multiple connections without a T-shape in order to lower gate resistance.

20. The method of claim 15, wherein the creating multiple connections step comprises creating the multiple connections using parallel field plates.

20 21. The method of claim 20, wherein the creating multiple connections step comprises creating the field plate covering the gate source access region in order to modulate source access resistance for improving device linearity performance.

22. A device fabricated using the method of claim 1.

25

23. A method of fabricating gate field plates, comprising:

(a) depositing or growing dielectric material on intrinsic and extrinsic regions of a device;

(b) patterning the dielectric material, so that the dielectric material remains principally
30 on an active region of the device; and

(c) creating a field plate on the patterned dielectric material, wherein the gate and the field plate are electrically shorted and overlap at least outside a lateral boundary of the active region, providing a low resistance connection therebetween.

35 24. The method of claim 23, wherein the dielectric material thickness is controlled in order to achieve proper operation of the device.

25. The method of claim 23, wherein the patterning step (b) comprises patterning the dielectric material by a dry or wet etch process or by a lift-off process.

5 26. The method of claim 23, wherein the creating step (c) comprises evaporating a field plate on the patterned dielectric material.

27. The method of claim 23, wherein steps (a)-(b) are repeated to create a plurality of the field plates.

10

28. A transistor , comprising:

a semiconductor layer, wherein the semiconductor layer confines a conducting channel in the transistor;

a spacer layer on the semiconductor layer, wherein the spacer layer does not
15 significantly induce a charge in the conducting channel;

a gate electrode deposited in an opening in the spacer layer, wherein at least a bottom-most portion of the gate electrode is on the semiconductor layer;

source and drain electrodes making ohmic contacts such that an electric current flows in the conducting channel between the source and drain electrodes when the gate electrode is
20 biased at an appropriate level;

a field plate extending across at least a portion of the spacer layer; and

wherein the spacer layer is removed to expose the semiconductor layer only at the opening for the gate electrode.

25 29. The transistor of claim 28, wherein:

the transistor is a High Electron Mobility Transistor (HEMT);

the semiconductor layer is a barrier layer inducing the conducting channel, comprising a two dimensional electron gas (2DEG), in a channel layer; and

the electric current flows between the source and drain electrodes via the two-
30 dimensional electron gas (2DEG) induced at a heterointerface between the channel layer and barrier layer when the gate electrode is biased at the appropriate level.

30. The transistor of claim 28, wherein a portion of the gate electrode on the spacer layer forms the field plate.

35

31. The transistor of claim 28, further comprising a dielectric that is a passivation layer on the both the gate electrode and at least a portion of the spacer layer.

32. The transistor of claim 28, wherein the spacer layer comprises a dielectric layer, a layer of undoped or depleted $Al_xGa_{1-x}N$ ($0<=x<=1$) material, or a combination thereof.

33. The transistor of claim 28, wherein the field plate is formed above the spacer layer and extends a distance Lf (field plate distance) from the edge of the gate electrode towards the drain electrode.

34. The transistor of claim 28, wherein the field plate is electrically connected to the gate electrode.

35. The transistor of claim 28, wherein the field plate is formed during the same deposition step as an extension of the gate electrode.

36. The transistor of claim 28, wherein the field plate and gate electrode are formed during separate deposition steps.

37. The transistor of claim 29, wherein the channel layer is formed on or above a substrate comprising silicon carbide, sapphire, spinel, zinc oxide, silicon or any other material capable of supporting growth of Group III-nitride materials.

38. The transistor of claim 29, wherein the channel layer is formed on or above a nucleation layer that is an $Al_zGa_{1-z}N$ ($0<=z<=1$) nucleation layer.

39. The transistor of claim 38, wherein the nucleation layer is an AIN nucleation layer.

40. The transistor of claim 29, wherein the channel layer is a high resistivity Group III-nitride channel layer.

41. The transistor of claim 29, wherein the channel layer comprises $Al_xGa_yIn_{(1-x-y)}N$ ($0<=x<=1$, $0<=y<=1$, $x+y<=1$).

42. The transistor of claim 41, wherein the channel layer comprises GaN:Fe.

43. The transistor of claim 29, wherein the barrier layer comprises $Al_xGa_{1-x}N$ $(0<=x<=1)$.

44. The transistor of claim 29, wherein the barrier layer comprises AlN and AlGaN.

45. The transistor of claim 29, wherein each of the channel layer and barrier layer comprise sub-layers that are doped or undoped layers of Group III-nitride materials.

46. The transistor of claim 29, wherein the spacer layer is a Group III-nitride semiconductor spacer layer is grown on an $Al_xGa_{1-x}N$ barrier layer.

47. The transistor of claim 28, wherein the spacer layer has a uniform composition.

48. The transistor of claim 28, wherein the spacer layer has a graded composition.

49. The transistor of claim 28, wherein the spacer layer is undoped.

50. The transistor of claim 28, wherein the spacer layer is fully depleted as grown.

51. The transistor of claim 29, wherein:

the gate electrode is formed after formation of the barrier layer;

a passivation layer is deposited on the device;

the field plate is then formed on the passivation layer overlapping the gate and extending a distance Lf in the gate-drain region; and

the passivation layer serves as a spacer layer for the field plate.

52. The transistor of claim 28, wherein the transistor is a III-nitride based HEMT and the conducting channel comprises a two dimensional electron gas (2DEG).

53. The transistor of claim 29, wherein the channel is GaN and the barrier layer is AlGaN.

54. The transistor of claim 28, wherein the transistor is formed on a substrate.

55. The transistor of claim 28, wherein the field plate extends a distance away from the gate electrode towards the drain electrode.

56. The transistor of claim 29, wherein the field plate is positioned and dimensioned such that the HEMT operates at Gigahertz frequencies with a power density of at least 12 W/mm.

57. The method of claim 1, wherein the providing step comprises depositing or growing
5 the dielectric material on intrinsic and extrinsic regions of the device, wherein:

the etching step exposes a portion of, or electrical contact to, the gate;

the evaporating step evaporates metal onto the dielectric material, and onto the portion of the gate or the electrical contact to the gate, to create the at least one field plate electrically connected to the gate; and

10 the dielectric material remains principally on the active region of the device.

58. The method of claim 1, wherein the device is a III-nitride based High Electron Mobility Transistor (HEMT).

15 59. The method of claim 1, wherein the device is a III-nitride based field effect transistor.

60. The method of claim 1, wherein a gate and the field plates are only electrically connected at one or more sides of an extrinsic region of the device, and gate resistance is reduced by controlling a width at which a connection between a gate and the field plates occurs.

20

61. The method of claim 1, wherein the field plate enables device operation under larger radio frequency (RF) signals as compared to a device without the field plate positioned in the gate drain access region.

25 62. The method of claim 1, wherein the device is a field effect transistor that includes source and drain ohmic contacts, the gate and the active region, and wherein:

the source and drain ohmic contacts are formed prior to creation of the at least one field plate;

above the active region, the at least one field plate at least partially overlies the gate;
30 and

the gate and the at least one field plate are electrically connected at least in an extrinsic region of the device.

63. A method of fabricating a gated device, comprising:

35 (a) providing a spacer layer or dielectric material on a semiconductor layer of a device, wherein the semiconductor layer confines a conducting channel in the device;

(b) providing an opening in the spacer layer or dielectric material for depositing a gate on the device;

(c) providing a gate in the opening; and

(d) providing metal onto the dielectric material or spacer layer to create at least one field plate on the spacer layer or the dielectric material, wherein no material provided on the semiconductor layer is removed to expose the semiconductor layer except at the opening for the gate.

64. The method of claim 63, wherein the spacer layer is not removed to expose the semiconductor layer after formation of the gate.

65. The method of claim 63, wherein at least part of the field plate is above the gate.

66. The method of claim 63, wherein the field plate is integrated with the gate, and formed as an extension of the gate during a same deposition step as the gate.

67. The method of claim 63, wherein the field plate is not electrically connected to the gate, above the gate.

68. The method of claim 63, further comprising providing multiple electrical connections between the field plate and the gate.

69. The method of claim 63, wherein the gate and the field plate are electrically connected at least in an extrinsic region of the device.

70. The method of claim 63, wherein the device is a III-nitride based device.

71. The method of claim 63, wherein the gate is directly on the semiconductor layer .

72. The method of claim 63, wherein the device is a field effect transistor that includes source and drain ohmic contacts, the gate, and the active region.

73. The method of claim 63, wherein the device is a High Electron Mobility Transistor.

74. The method of claim 63, wherein the spacer layer comprises a dielectric, a layer of undoped or depleted $Al_xGa_{1-x}N$ (0<=x<=1) material, or a combination thereof.

75. The method of claim 63, wherein the spacer layer comprises a material and a thickness suitable for Gigahertz operation of the device.

5 76. The method of claim 63, wherein:

the device is a High Electron Mobility Transistor (HEMT) wherein the semiconductor layer is a barrier layer on a channel layer;

the spacer layer is etched to expose the barrier layer and the gate is deposited such that at least a bottom portion of the gate is on a surface of barrier layer;

10 the field plate extends across at least a portion of the spacer layer; and

a passivation layer is on both the gate and at least a portion of the spacer layer.

77. The method of claim 76, wherein the field plate is formed above the spacer layer and extends a distance Lf (field plate distance) from an edge of the gate towards the drain electrode.

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78. The method of claim 63, further comprising creating one or more additional field plates on the device, wherein each field plate is created by:

(a) providing dielectric material on intrinsic and extrinsic regions of the device;

(b) patterning the dielectric material, so that the dielectric material remains principally

20 on the semiconductor layer of the device; and

(c) creating the additional field plates on the patterned dielectric material.

79. The method of claim 78, wherein steps (a)-(c) are repeated to create a plurality of the field plates.

25

80. The method of claim 78, wherein the field plate has a resistance Rf that is equivalent to a gate resistance Rg.

81. A gated device, comprising:

30 a spacer layer on a semiconductor layer of a device, wherein the semiconductor layer confines a conducting channel in the device;

an opening in the spacer layer for a gate;

a gate in the opening; and

a field plate on the spacer layer, wherein the spacer layer is not removed to expose the

35 semiconductor layer except at the opening for the gate.

82. The device of claim 81, wherein at least part of the field plate is above the gate.

83. The device of claim 81, wherein the field plate is integrated with the gate.

5 84. The device of claim 81, wherein the field plate is not electrically connected to the gate, above the gate.

85. The device of claim 81, further comprising providing multiple electrical connections between the field plate and the gate.

10

86. The device of claim 81, wherein the gate and the field plate are electrically connected at least in an extrinsic region of the device.

87. The device of claim 81, wherein the device is a III-nitride based device.

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88. The device of claim 81, wherein the gate is directly on the semiconductor layer.

89. The device of claim 81, wherein the device is a field effect transistor that includes source and drain ohmic contacts, the gate, and the semiconductor layer.

20

90. The device of claim 81, wherein the device is a High Electron Mobility Transistor.

91. The device of claim 81, wherein the spacer layer comprises a dielectric.

25 92. The device of claim 81, wherein the spacer layer comprises a material and a thickness suitable for Gigahertz operation of the device.

93. The device of claim 81, further comprising:

(a) patterned dielectric material on intrinsic and extrinsic regions of the device, so that
30 the dielectric material remains principally on the semiconductor layer; and

(b) one or more additional field plates on the patterned dielectric material.

94. The device of claim 81, wherein the field plate has a resistance Rf that is equivalent to a gate resistance Rg.

35

95. The device of claim 81, wherein:

the device is a High Electron Mobility Transistor (HEMT) wherein the semiconductor layer is a barrier layer on a channel layer;

the spacer layer is etched to expose the barrier layer and the gate is deposited such that
5 at least a bottom portion of the gate is on a surface of barrier layer;

the field plate extends across at least a portion of the spacer layer; and

a passivation layer is on both the gate and at least a portion of the spacer layer.

96. The device of claim 95, wherein the field plate is formed above the spacer layer and
10 extends a distance Lf (field plate distance) from an edge of the gate towards the drain electrode.

97 The method of claim 63, further comprising a plurality of the at least one field plate, and controlling the dielectric material's thickness between the field plates in order to achieve proper radio frequency (RF) operation of the device.

15

98. The method of claim 63, wherein steps (a) and (c) are repeated to create a plurality of the at least one field plate.

99. The method of claim 63, wherein the gate is directly on the semiconductor layer .

20

100. The method of claim 63, wherein the gate and the at least one field plate of the device are electrically connected and overlap at least outside a lateral boundary of the semiconductor layer as viewed from a top of the device.

25 101. The method of claim 63, wherein the device is a group III nitride field effect transistor.

102. The method of claim 63, further comprising etching the spacer layer to provide the opening for the gate.

30 103. The method of claim 63, wherein:

the at least one field plate is not electrically connected to the gate, above the gate, and the gate and the at least one field plate of the device are electrically connected and overlap at least outside a lateral boundary of the semiconductor layer, as viewed from a top of the device.

35 104. A method of fabricating one or more gate field plates, comprising:

providing a dielectric material on an active region of a device; and

providing metal onto the dielectric material to create at least one field plate, wherein a gate and at least one field plate of the device are electrically connected and overlap at least outside a lateral boundary of the active region.

5 105. The method of claim 104, wherein the gate is directly on the active region.

106. The method of claim 104, further comprising providing the dielectric material on the gate prior to creating the at least one field plate.

10 107. The method of claim 104, further comprising varying one or more parameters comprising the field plate's offset with respect to the gate and other field plates, the number of the field plates, the field plate's length, the dielectric material's thickness, and the electrical connection between the field plates and the gate, in order to permit control on field plate's operation and achieve a desired breakdown voltage or radio frequency (RF) performance.

15

108. The method of claim 104, further comprising creating multiple connections using multiple field plates in order to reduce gate resistance.

109. The method of claim 104, wherein the field plate is positioned in a gate drain access
20 region, thereby providing a capability of modulating the active region, resulting in a decrease of surface traps effect that prevent proper device operation under large radio frequency (RF) signals.

110. The method of claim 104, further comprising preventing any exposure of the surface of
25 the active region to the dry or wet etch process that may induce damage in the device.

111. The method of claim 104, further comprising depositing parallel field plates on top of the dielectric material by properly adjusting the dielectric material's thickness, in order to significantly reduce gate resistance by electrically connecting at least two parallel field plates
30 outside a lateral boundary of the active region, wherein the dielectric material's thickness is selected to ensure parasitic capacitances added by the field plates are negligible compared to those of an intrinsic device.

112. The method of claim 104, wherein the device is a field effect transistor that includes
35 source and drain ohmic contacts, the gate and the active region.

113. The method of claim 63, further comprising depositing or growing the dielectric material on intrinsic and extrinsic regions of the device, the method further comprising etching the dielectric material, so that the dielectric material remains principally on the semiconductor layer .

5

114. The method of claim 113, further comprising controlling the dielectric material's thickness between the field plates in order to achieve proper radio frequency (RF) operation of the device.

10 115. The method of claim 114, wherein the etching step comprises patterning the dielectric material by a dry or wet etch process or by a lift-off process.

116. The method of claim 114, wherein field plate is evaporated on the patterned dielectric material before the gate and field plate contacts are electrically connected.

15

117. The method of claim 114 wherein the steps are repeated to create a plurality of the field plates.

118. The method of claim 114, wherein the field plate has a resistance Rf that is equivalent
20 to a gate resistance Rg.

119. The method of claim 114, wherein the field plate is connected to both sides of the device intrinsic region.

25 120. The method of claim 114, further comprising creating multiple connections between the gate and the field plate to decrease gate resistance.

121. The method of claim 120, wherein the creating multiple connections step comprises etching a portion of the semiconductor layer prior to deposition of the gate to create a
30 connection between the gate and the field plate above the portion of the semiconductor layer without degrading a Radio Frequency operation of the device.

122. The method of claim 120, further comprising dividing the semiconductor layer and conducting channel to form a plurality of active regions and spacing between the active regions
35 to engineer a thermal impedance of the device.

123. The method of claim 120, wherein the device comprises a larger periphery device with a reduced number of air bridges as compared to a device without multiple connections, without the dielectric material remaining principally on the semiconductor layer, and without the electrically shorted gate and field plate.

5

124. The method of claim 120, wherein the creating multiple connections step comprises creating the multiple connections without a T-shape in order to lower gate resistance.

125. The method of claim 120, wherein the creating multiple connections step comprises

10 creating the multiple connections using parallel field plates.

126. The method of claim 125, wherein the creating multiple connections step comprises creating the field plate covering the gate source access region in order to modulate source access resistance for improving device linearity performance.

15

127. The method of claim 104, the dielectric material deposited on the active region of the device is not removed to expose the active region.

128. The method of claim 104, wherein the device is a nitride based High Electron Mobility

20 Transistor (HEMT).

129. The transistor of claim 28, wherein a portion of the gate electrode is patterned to extend across the spacer layer so that the gate electrode forms a field plate extending a distance away from the gate electrode towards the drain electrode.

25

130. The transistor of claim 28, wherein the field plate is formed above a dielectric layer formed on the gate electrode, such that the field plate and the gate electrode overlap.

131. The transistor of claim 29, further comprising a substrate, a nucleation layer on the

30 substrate, and the channel layer on the nucleation layer, wherein the barrier layer is on the channel layer.

132. The transistor of claim 28, wherein:

the transistor is a high electron mobility transistor (HEMT);

the semiconductor layer comprises Aluminum, Gallium, and Nitrogen and induces the conducting channel, comprising a two dimensional electron gas (2DEG) in the channel layer comprising Gallium Nitride; and

the field plate extends a distance across the spacer layer, such that the HEMT produces a power density of at least 32 W/mm with at least 55% Power Added Efficiency, when operating at 120 V and 4 GHz.

133. The transistor of claim 28, wherein:

the transistor is a high electron mobility transistor (HEMT);

the semiconductor layer comprises Aluminum, Gallium, and Nitrogen and induces the conducting channel, comprising a two dimensional electron gas (2DEG), in the channel layer comprising Gallium Nitride; and

the field plate extends a distance across the spacer layer, such that the HEMT has a power added efficiency of 52-60% and an output power including a 3dB power of 8 W/mm.

134. The transistor of claims 132, wherein the field plate extends the distance of 0.5 – 1 micrometers in a gate drain access region.

135. The transistor of claims 133, wherein the field plate extends the distance of 0.5 – 1 micrometers in a gate drain access region.

136. The transistor of claim 28, wherein a passivation layer is on both the gate electrode and at least a portion of the spacer layer.

137. The transistor of claim 28, wherein the spacer layer is a dielectric layer.

138. The transistor of claim 28, wherein the spacer layer is a layer of undoped or depleted $Al_xGa_{1-x}N$ ($0<=x<=1$) material.

139. The method of claim 63, wherein:

the device is a High Electron Mobility Transistor (HEMT) structured to achieve a power density of at least 32 W/mm with at least 55% Power Added Efficiency, when operating at 120 V and 4 GHz; and

the semiconductor layer confines a two dimensional electron gas in the HEMT.

140. The method of claim 139, wherein:

the semiconductor layer comprises a barrier layer on a channel layer; and

the conducting channel comprises a two dimensional electron gas confined in the channel layer.

5 141. The method of claim 63, wherein:

the semiconductor layer comprises a barrier layer on a channel layer; and

the conducting channel comprises a two dimensional electron gas confined in the channel layer.

10 142. The device of claim 81, wherein:

the device is a High Electron Mobility Transistor (HEMT) structured to achieve a power density of at least 32 W/mm with at least 55% Power Added Efficiency, when operating at 120 V and 4 GHz; and

the semiconductor layer confines the conducting channel comprising a two dimensional

15 electron gas in the HEMT.

143. The device of claim 142, wherein:

the semiconductor layer comprises a barrier layer on a channel layer; and

the conducting channel comprises a two dimensional electron gas is confined in the

20 channel layer.

144. The device of claim 81, wherein:

the semiconductor layer comprises a barrier layer on a channel layer; and

the conducting channel comprises a two dimensional electron gas is confined in the

25 channel layer.

145. A method of fabricating one or more gate field plates, comprising:

(a) providing a dielectric material on a semiconductor layer of a device, wherein the semiconductor layer confines a conducting channel in the device;

30 (b) providing an opening in the dielectric material for depositing a gate on the device; and

(c) providing metal onto the dielectric material to create at least one field plate, wherein no material provided on the semiconductor layer is removed to expose the active region except at the opening for the gate.

35

146. The method of claim 145, further comprising a plurality of the at least one field plate, and controlling the dielectric material's thickness between the field plates in order to achieve proper radio frequency (RF) operation of the device.

5 147. The method of claim 145, wherein steps (a)-(b) are repeated to create a plurality of the at least one field plate.

148. The method of claim 145, wherein the device is a transistor and the gate is directly on the semiconductor layer.

10

149. The method of claim 145, wherein the gate and the at least one field plate of the device are electrically connected and overlap with each other at least outside a lateral boundary of the semiconductor layer, as viewed from a top of the device.

15 150. The method of claim 145, wherein the gate and the at least one field plate are only electrically connected at one or more sides of an extrinsic region of the device, and gate resistance is reduced by controlling a width at which a connection between a gate and the field plates occurs.

20 151. The method of claim 145, wherein the device is a group III-nitride field effect transistor.

152. The method of claim 145, wherein:

the device is a High Electron Mobility Transistor (HEMT) structured to achieve a
25 power density of at least 32 W/mm with at least 55% Power Added Efficiency, when operating at 120 V and 4 GHz; and

the semiconductor layer comprises a barrier layer on a channel layer, wherein a two dimensional electron gas is confined in the channel layer.

30 153. A method of fabricating a gated device, comprising:

providing a spacer layer on an active region of a device, wherein the spacer layer is not part of a structure that forms the active region;

providing an opening in the spacer layer for a gate;

depositing a gate in the opening; and

creating a field plate on the spacer layer, wherein no layer provided on the active region of the device is removed to expose the active region except at the opening for the gate, and wherein the field plate is electrically connected to the gate.

5 154. The method of claim 154, wherein the device is a group III-nitride field effect transistor.

155. The method of claim 1, wherein the device is a group III-nitride field effect transistor and the active region comprises a barrier layer on a channel layer such that a two dimensional
10 electron gas is confined in the channel layer.

156. The method of claim 1, wherein the gate and the at least one field plate are only electrically connected at one or more sides of an extrinsic region of the device, and gate resistance is reduced by controlling a width at which a connection between a gate and the field
15 plates occurs.

157. A method of fabricating a transistor, comprising:

providing a spacer layer on a semiconductor layer, wherein:

the semiconductor layer confines a conducting channel in the transistor; and
20 the spacer layer does not significantly induce a charge in the conducting channel;

removing the spacer layer to expose the semiconductor layer only at an opening for a gate electrode;

depositing the gate electrode in the opening, wherein at least a bottom-most portion of
25 the gate electrode is on a surface of the semiconductor layer;

depositing source and drain electrodes making ohmic contacts such that an electric current flows in the conducting channel between the source and drain electrodes when the gate electrode is biased at an appropriate level; and

depositing a field plate extending across at least a portion of the spacer layer.

30

158. A transistor, comprising:

a semiconductor layer confining a conducting channel in the transistor;

a gate on or above the semiconductor layer;

dielectric material on the semiconductor layer and the gate of a device; and
35 one or more field plates on the dielectric material, wherein the dielectric material is not removed to expose the semiconductor layer.

159. The transistor of claim 158, wherein:
the transistor is a field effect transistor, and
one or more offsets of one or more of the field plates with respect to the gate, a number
5 of the field plates, one or more lengths of one or more of the field plates, one or more thicknesses of the dielectric material, or one or more electrical connections between the gate and one or more of the field plates, are such that the transistor's frequency of maximum oscillation is reduced by 0-0.5% for a gate finger width in a range of 0-100 micrometers.

10 160. The transistor of claim 158, wherein:
the transistor is a field effect transistor, and
one or more offsets of one or more of the field plates with respect to the gate, a number of the field plates, one or more lengths of one or more of the field plates, one or more thicknesses of the dielectric material, or one or more electrical connections between the gate
15 and one or more of the field plates, are such that the transistor density produces a power density of at least 32 W/mm with at least 55% Power Added Efficiency, when operating at 120 V and 4 GHz.

161. The transistor of claim 158, wherein:
20 the transistor is a field effect transistor, and
one or more offsets of one or more of the field plates with respect to the gate, a number of the field plates, one or more lengths of one or more of the field plates, one or more thicknesses of the dielectric material, or one or more electrical connections between the gate and one or more of the field plates, are such that the transistor has a power added efficiency of 52-60% and an
25 output power including a 3dB power of 8 W/mm.

162. The transistor of claim 161, wherein one or more of the field plates extend a distance of 0.5 – 1 micrometers in a gate drain access region.

30 163. The transistor of claim 158, further comprising multiple field plates and multiple connections between field plates and the gate.

164. The transistor of claim 163, wherein:
the multiple field plates include parallel field plates on top of the dielectric material,
35 at least two of the parallel field plates are electrically connected on extrinsic regions of the device, and

one or more thicknesses of the dielectric material are such that parasitic capacitances added by the field plates are negligible compared to those of an intrinsic transistor.

165. The transistor of claim 158, wherein:

5 (1) the dielectric material is on intrinsic and extrinsic regions of the transistor;

(2) the dielectric material remains principally on the semiconductor layer; and

(3) the gate and one or more of the field plates are electrically connected at least at one side of the transistor's extrinsic region.

10 166. The transistor of claim 165, wherein the electrical connection includes an electrical short.

167. The transistor of claim 165, wherein one or more of the field plates have a resistance Rf that is equivalent to a gate resistance Rg.

15

168. The transistor of claim 165, wherein one or more of the field plates are connected to both sides of the transistor's intrinsic region.

169. The transistor of claim 166, further comprising multiple connections between the gate

20 and one or more of the field plates.

170. The transistor of claim 169, further comprising an active region, wherein a portion of the active region comprising the semiconductor layer is etched to create the multiple connections between the gate and one or more of the field plates.

25

171. The transistor of claim 170, further comprising an active region comprising the semiconductor layer, wherein the active region is divided into a plurality of active regions and spacing between the active regions engineers a thermal impedance of the transistor.

30 172. The transistor of claim 170, wherein the transistor has a reduced number of air bridges as compared to a transistor without the multiple connections, without the dielectric material remaining principally on the semiconductor layer, and without the electrical short.

173. The transistor of claim 170, without a T-shape connection.

35

174. The transistor of claim 170, wherein one or more of the field plates cover a gate source access region.

175. The transistor of claim 158, wherein the transistor is a nitride based High Electron Mobility Transistor (HEMT) and the conducting channel is a two dimensional electron gas.

176. The transistor of claim 158, wherein the gate and one or more of the field plates are electrically connected at least in an extrinsic region of the transistor.

177. The transistor of claim 158, wherein the gate is directly on the semiconductor layer.

178. The transistor of claim 158, wherein the gate and one or more of the field plates are only electrically connected at one or more sides of an extrinsic region of the transistor.

179. The transistor of claim 158, wherein the transistor is a high electron mobility transistor (HEMT) and the semiconductor layer is part of an active region forming a conductive channel of the HEMT.

180. The transistor of claim 158, wherein the transistor's source contact and one or more of the field plates are electrically connected.

181. The transistor of claim 158, wherein the transistor is a group III-nitride field effect transistor and the semiconductor layer comprises a barrier layer on a channel layer such that a two dimensional electron gas is confined in the channel layer.

182. The transistor of claim 181, wherein the barrier is AlGaN and the channel is GaN.

183. The transistor of claim 158, further comprising multiple field plates and additional dielectric material between the field plates.

184. The transistor of claim 158, wherein the transistor is a high electron mobility transistor.

185. The transistor of claim 158, wherein the one or more field plates are on etched dielectric material.

186. The transistor of claim 158, wherein at least one of the field plates is electrically connected to the gate.

187. The transistor of claim 158, further comprising a source contact connected to one or more of the field plates, wherein the one or more of the field plates electrically connected to the source contact are not electrically connected to the gate.

188. A high electron mobility transistor (HEMT), comprising:

a nucleation layer;

a channel layer on the nucleation layer;

a barrier layer on the channel layer;

a spacer layer on the barrier layer; and

source and drain electrodes making ohmic contacts through the barrier layer such that an electric current flows between the source and drain electrodes when a gate electrode is biased at an appropriate level;

wherein the spacer layer is etched to expose the barrier layer and the gate electrode is deposited such that at least a bottom portion of the gate electrode is on a surface of barrier layer,

wherein a top portion of the gate electrode is patterned to extend across the spacer layer so that the top portion of the gate electrode forms a field plate extending a distance away from the gate electrode towards the drain electrode; and

wherein a passivation layer covers both the gate electrode and at least a portion of the spacer layer.

189. The HEMT of claim 188, wherein the electric current flows between the source and drain electrodes via a two-dimensional electron gas (2DEG) induced at a heterointerface between the channel layer and barrier layer when the gate electrode is biased at the appropriate level.

190. The HEMT of claim 188, wherein the portion of the gate electrode on the spacer layer forms an epitaxial field plate.

191. The HEMT of claim 188, wherein the spacer layer comprises a dielectric layer, a layer of undoped or depleted AlxGa1-xN (0<=x<=1) material, or a combination thereof.

192. The HEMT of claim 188, wherein the field plate is formed above the spacer layer and extends a distance Lf (field plate distance) from an edge of the gate electrode towards the drain electrode.

193. The HEMT of claim 188, wherein the field plate is electrically connected to the gate electrode.

194. The HEMT of claim 188, wherein the field plate is formed during the same deposition step as an extension of the gate electrode.

195. The HEMT of claim 188, wherein the field plate and gate electrode are formed during separate deposition steps.

196. The HEMT of claim 188, wherein the substrate comprises silicon carbide, sapphire, spinel, zinc oxide, silicon or any other material capable of supporting growth of Group III-nitride materials.

197. The HEMT of claim 188, wherein the nucleation layer is an AlzGa1-zN (0<=z<=1) nucleation layer.

198. The HEMT of claim 188, wherein the nucleation layer is an AlN nucleation layer.

199. The HEMT of claim 188, wherein the channel layer is a high resistivity Group III-nitride channel layer.

200. The HEMT of claim 188, wherein the channel layer comprises AlxGayIn(1-x-y)N (0<=x<=1, 0<=y<=1, x+y<=1).

201. The HEMT of claim 188, wherein the channel layer comprises GaN:Fe.

202. The HEMT of claim 188, wherein the barrier layer comprises AlxGa1-xN (0<=x<=1).

203. The HEMT of claim 188, wherein the barrier layer comprises AlN and AlGaN.

204. The HEMT of claim 188, wherein each of the channel layer and barrier layer comprise sub-layers that are doped or undoped layers of Group III-nitride materials.

205. The HEMT of claim 188, wherein the spacer layer is a Group III-nitride semiconductor spacer layer grown on the barrier layer that is an AlxGa1-xN barrier layer.

5 206. The HEMT of claim 188, wherein the spacer layer has a uniform composition.

207. The HEMT of claim 188, wherein the spacer layer has a graded composition.

208. The HEMT of claim 188, wherein the spacer layer is undoped.

10

209. The HEMT of claim 188, wherein the spacer layer is fully depleted as grown.

210. The HEMT of claim 188, wherein the gate electrode is formed after formation of the barrier layer, a passivation layer is deposited on the device, and the field plate is then formed on

15 the passivation layer overlapping the gate and extending a distance Lf in a gate-drain region, and the passivation layer serves as the spacer layer for the field plate.

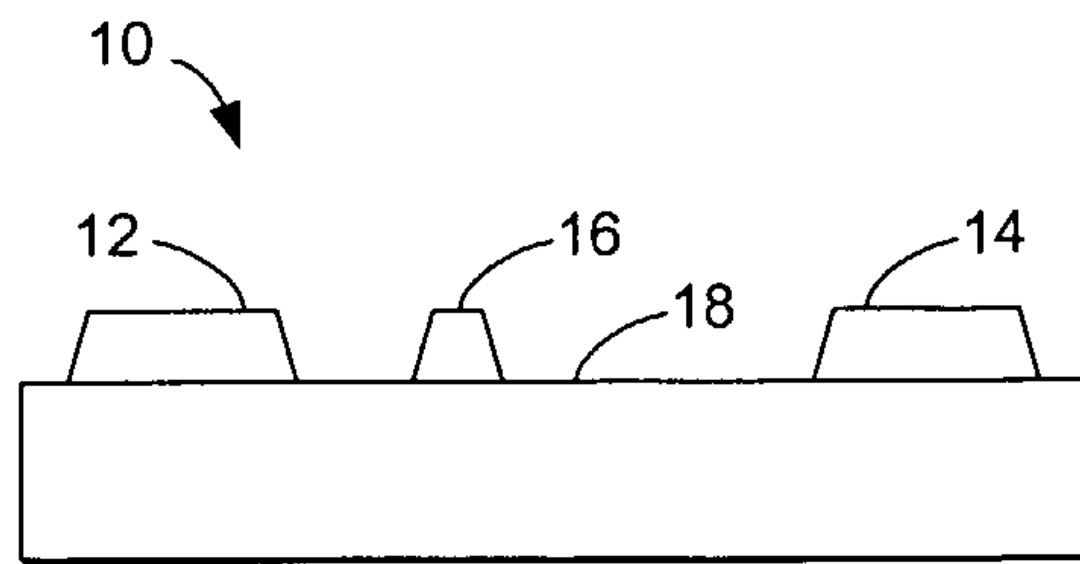


FIG. 1A

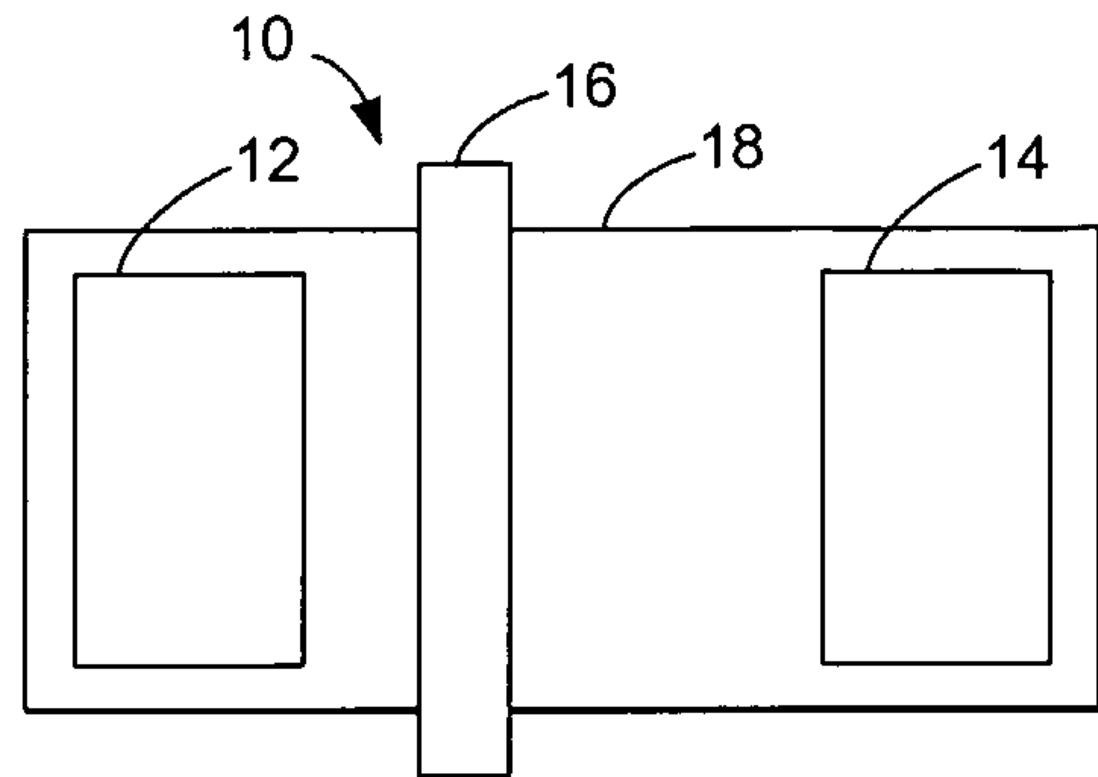


FIG. 1B

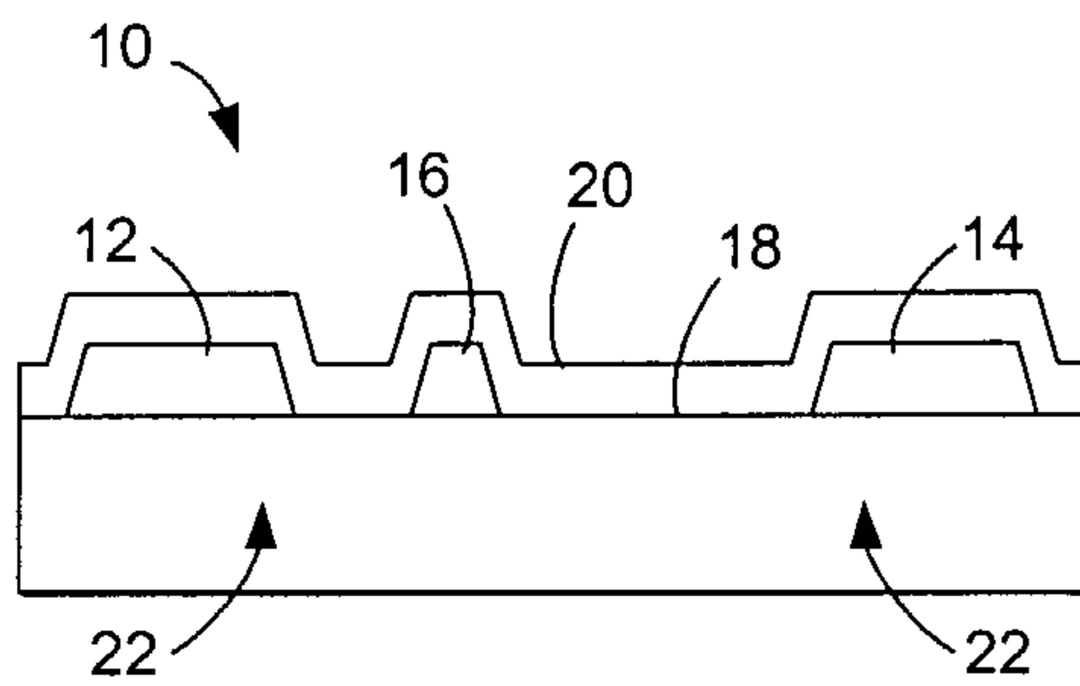


FIG. 2A

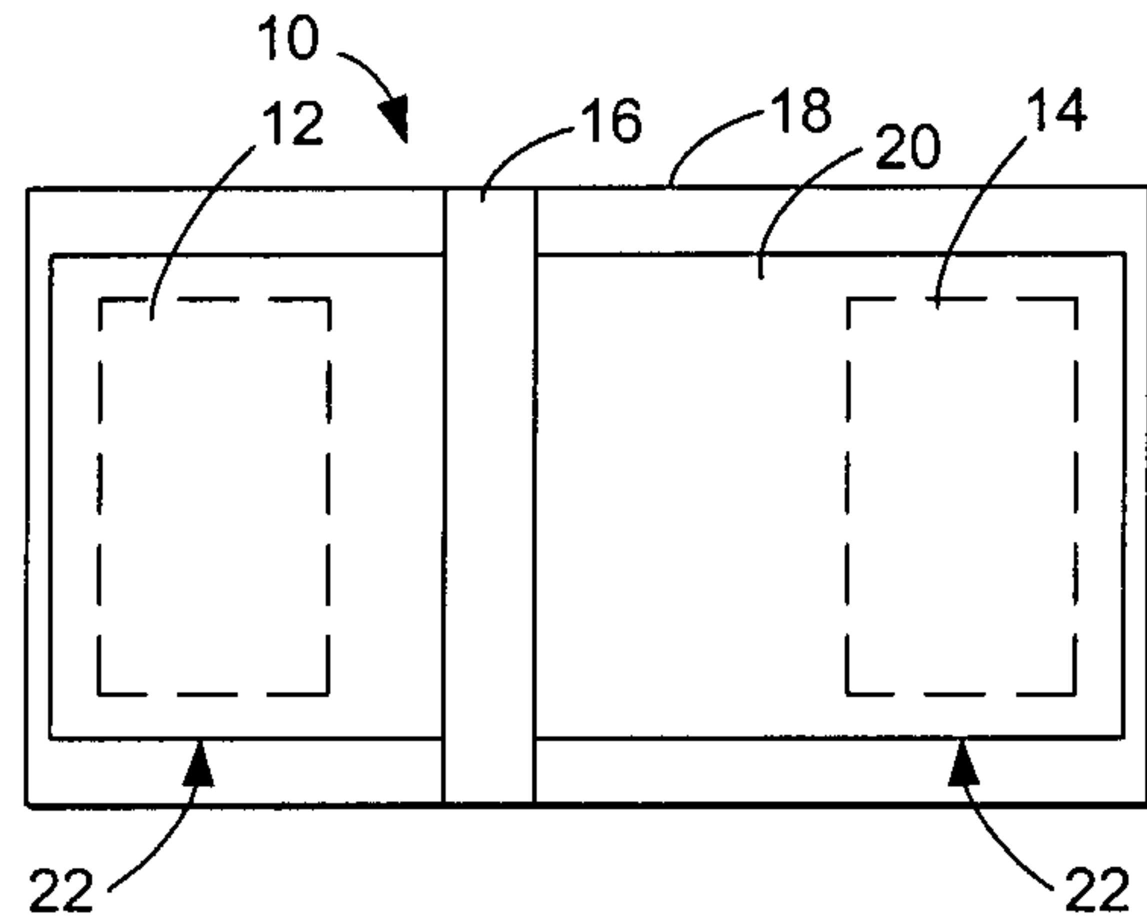


FIG. 2B

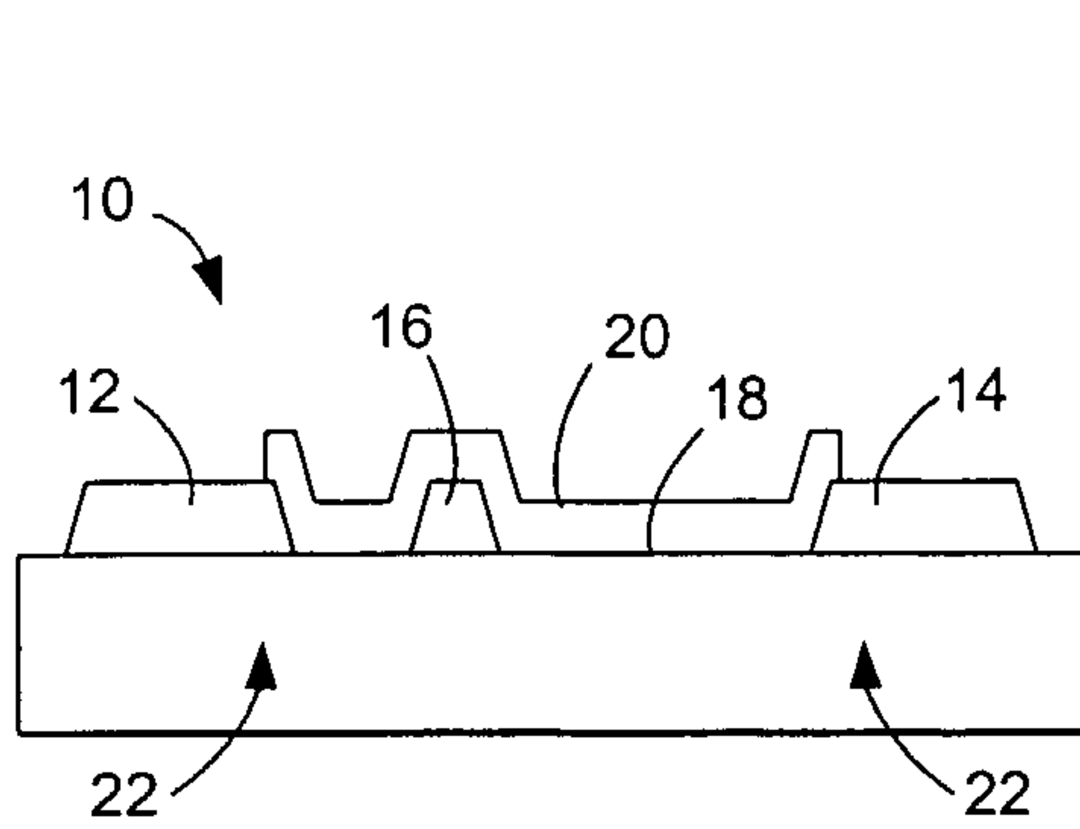


FIG. 3A

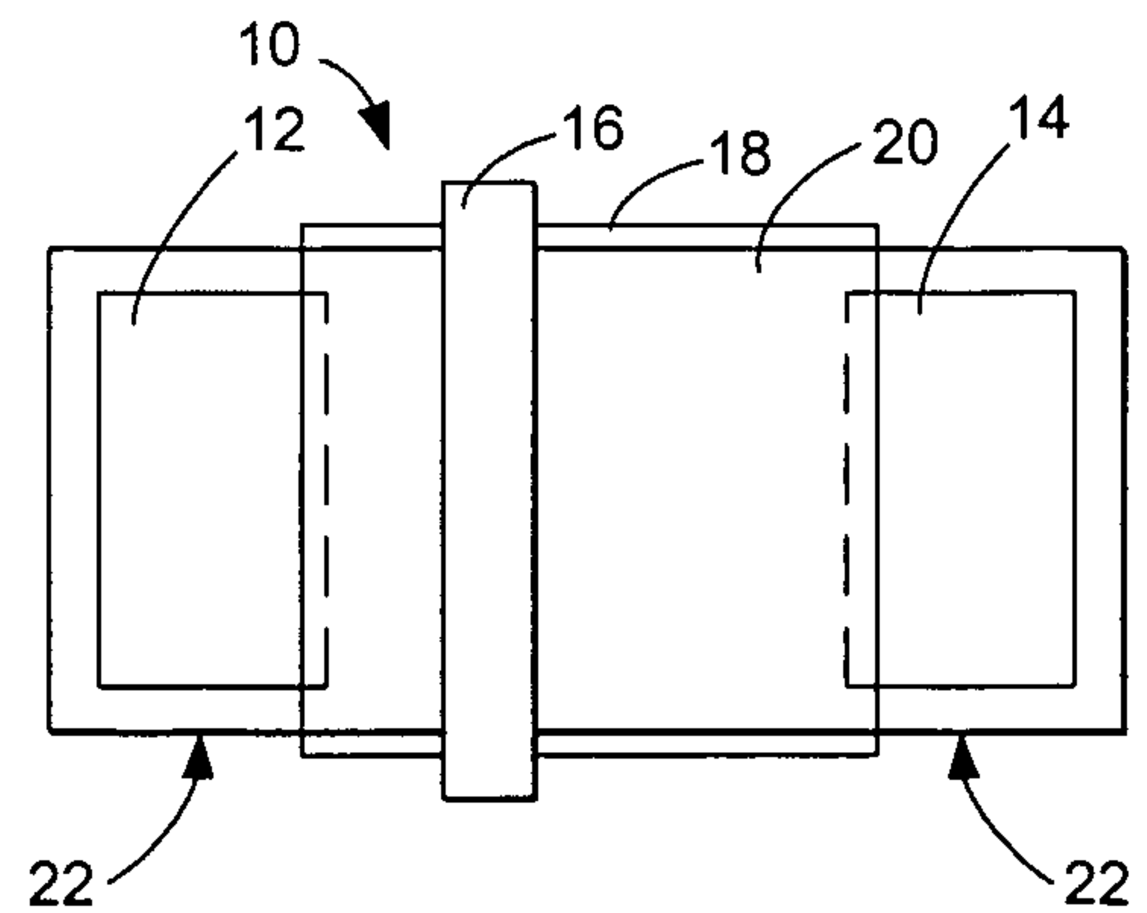


FIG. 3B

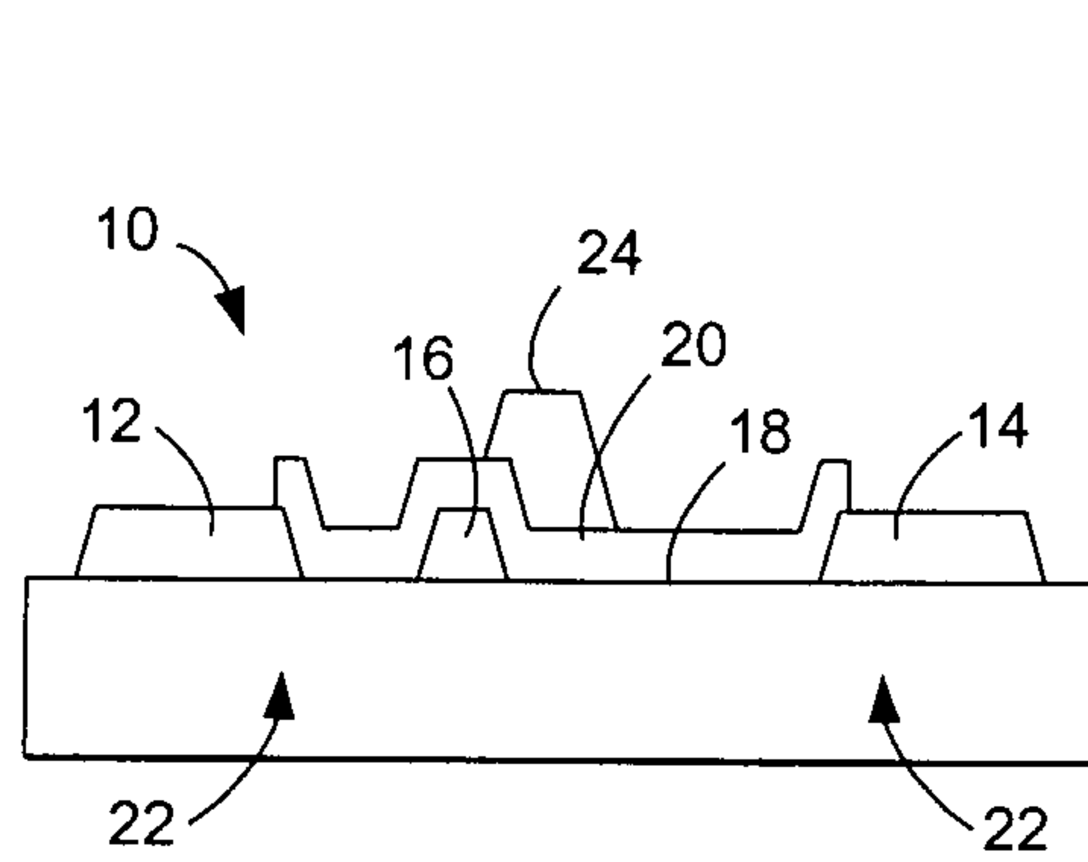


FIG. 4A

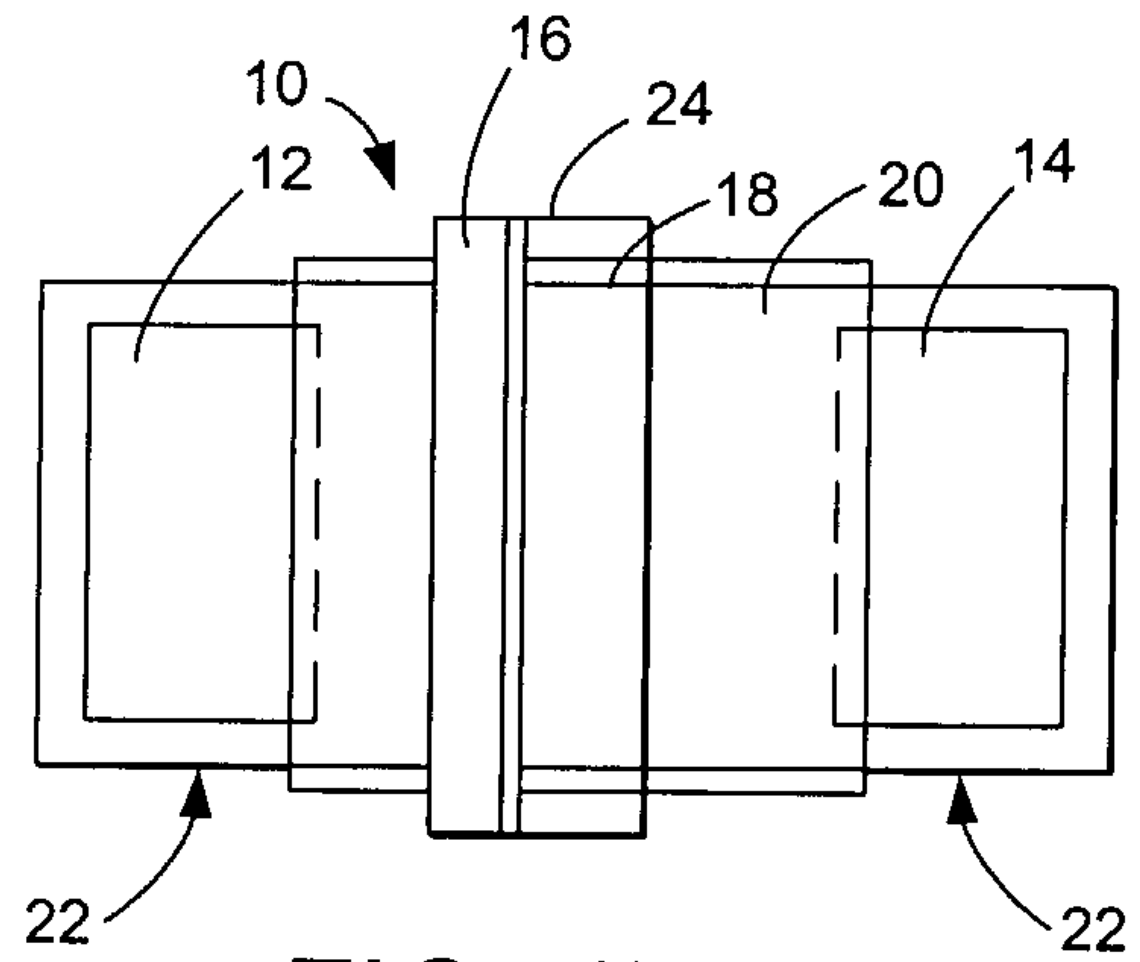


FIG. 4B

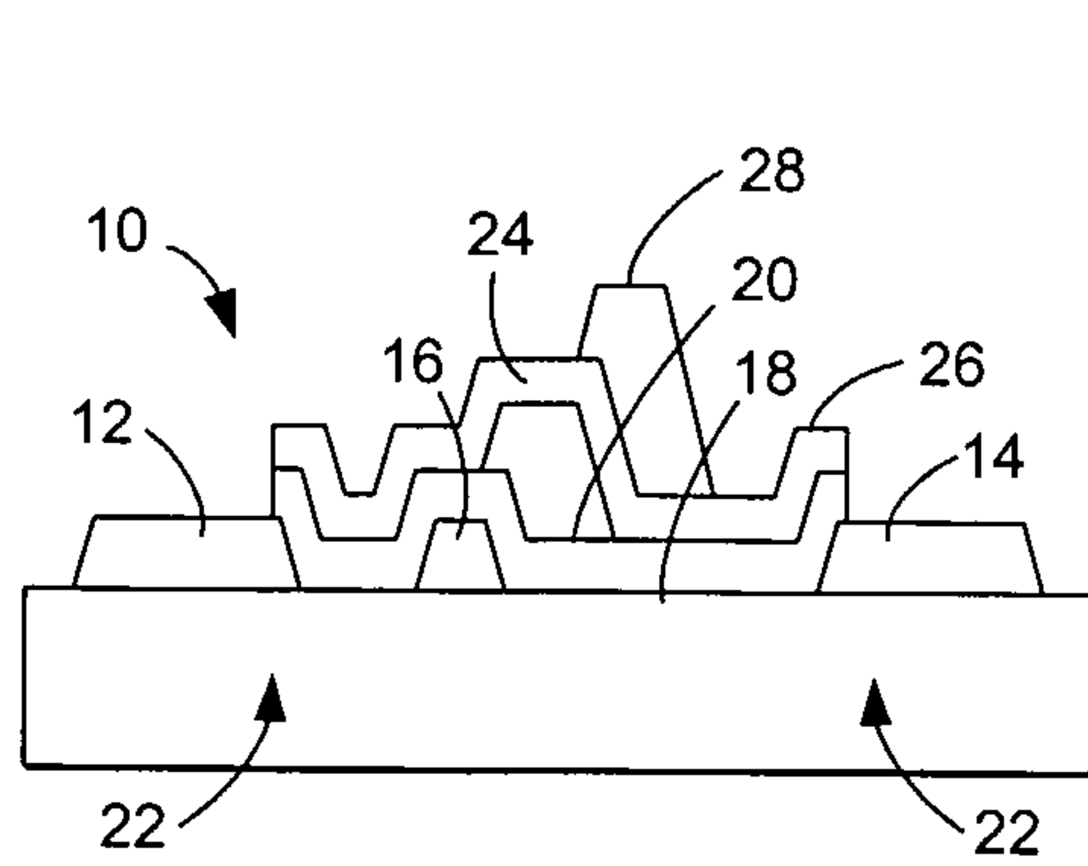


FIG. 5A

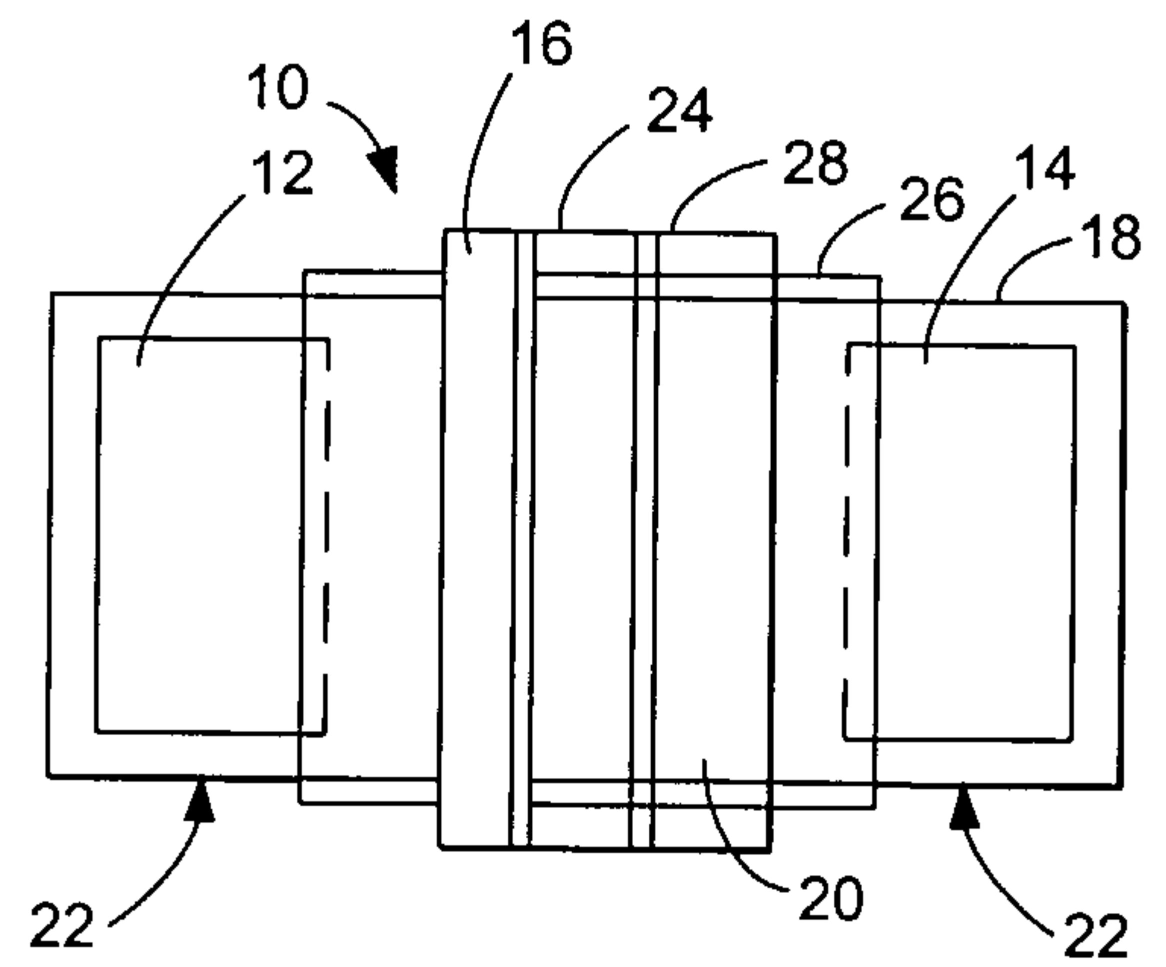


FIG. 5B

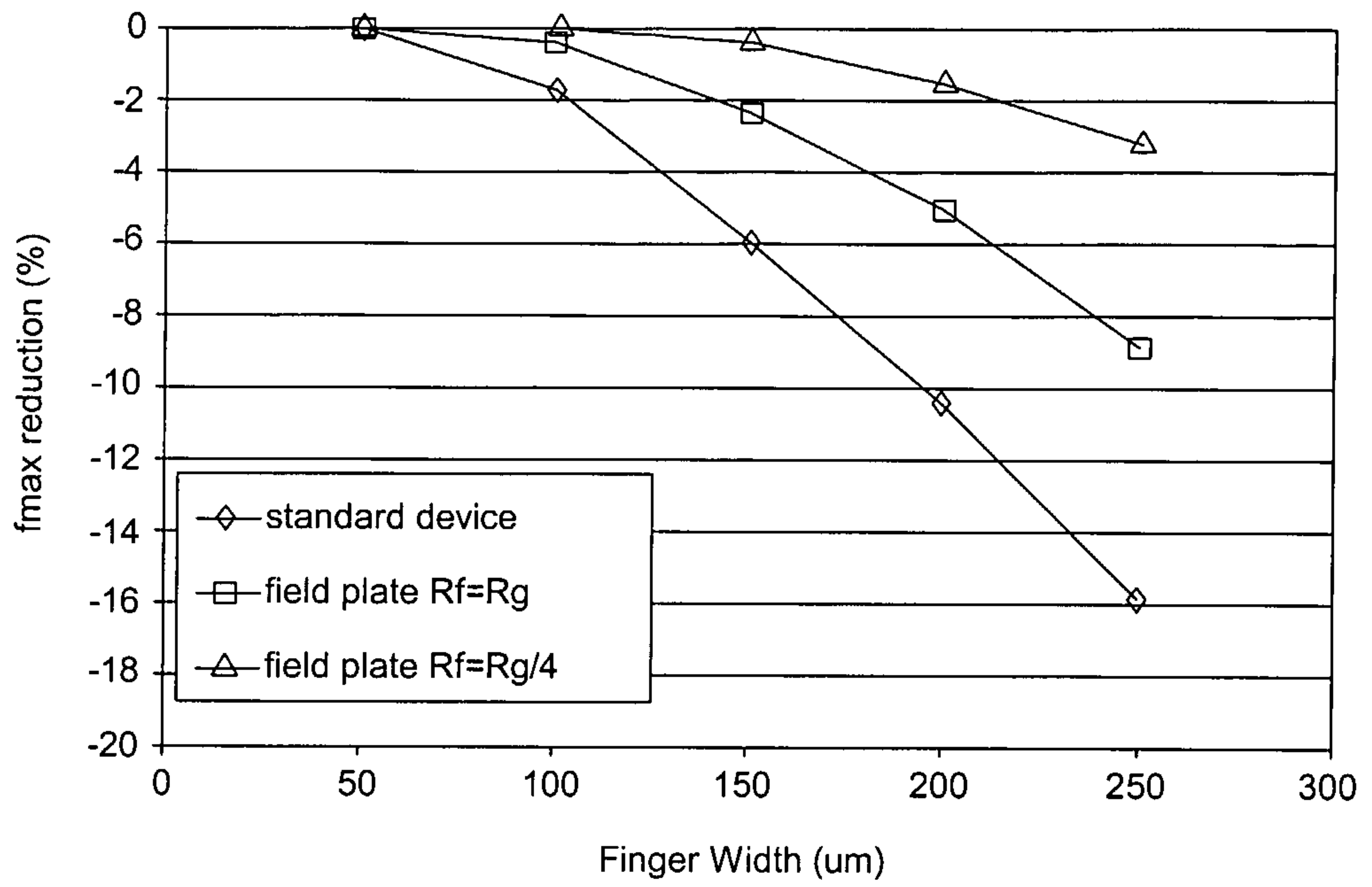


FIG. 6

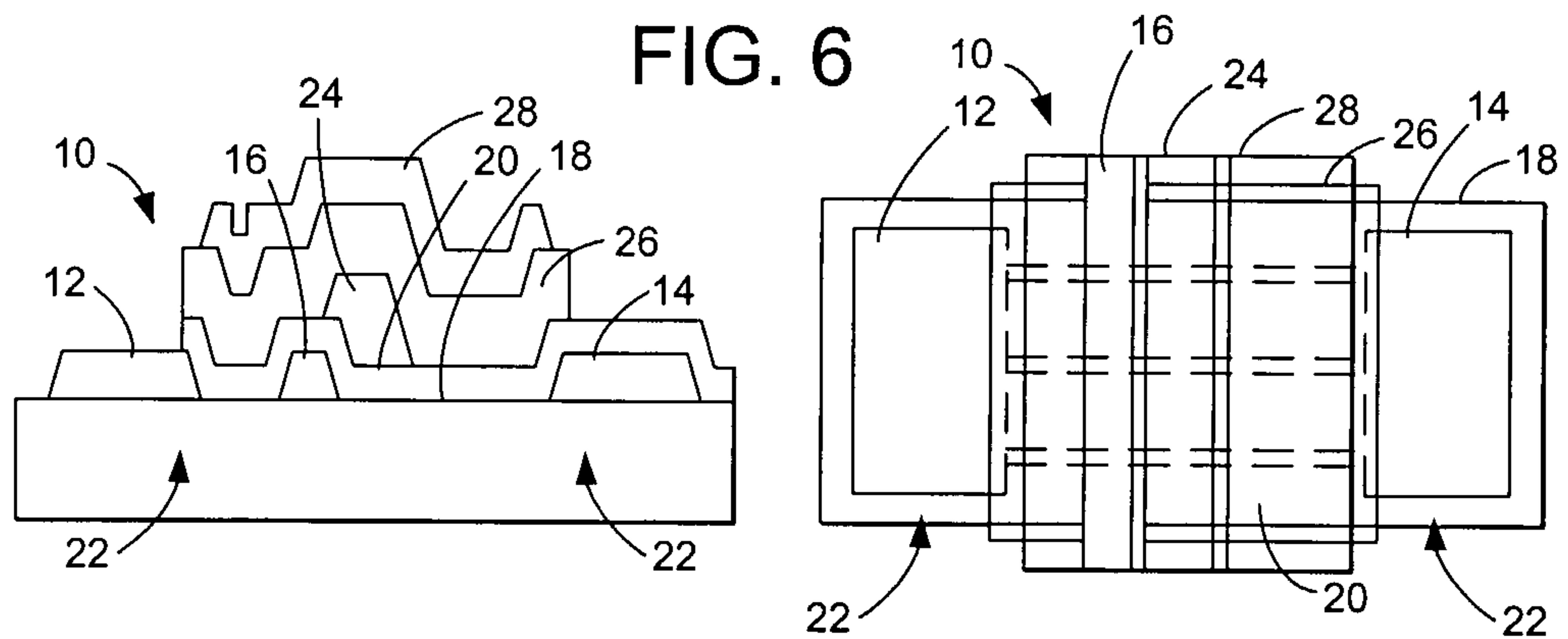


FIG. 7A

FIG. 7B

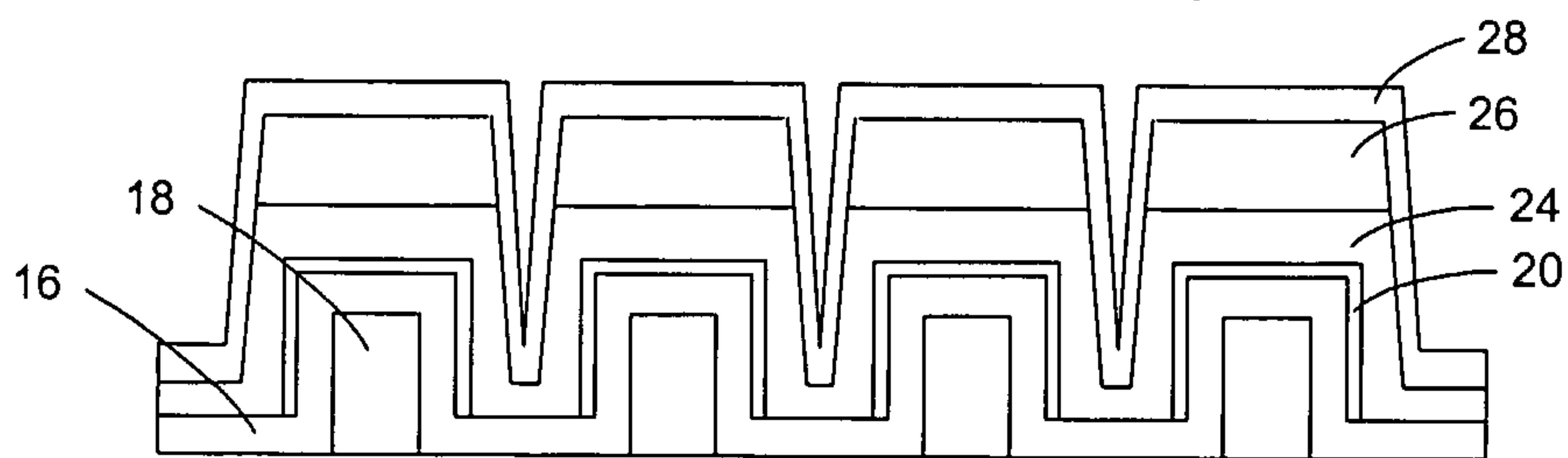


FIG. 7C

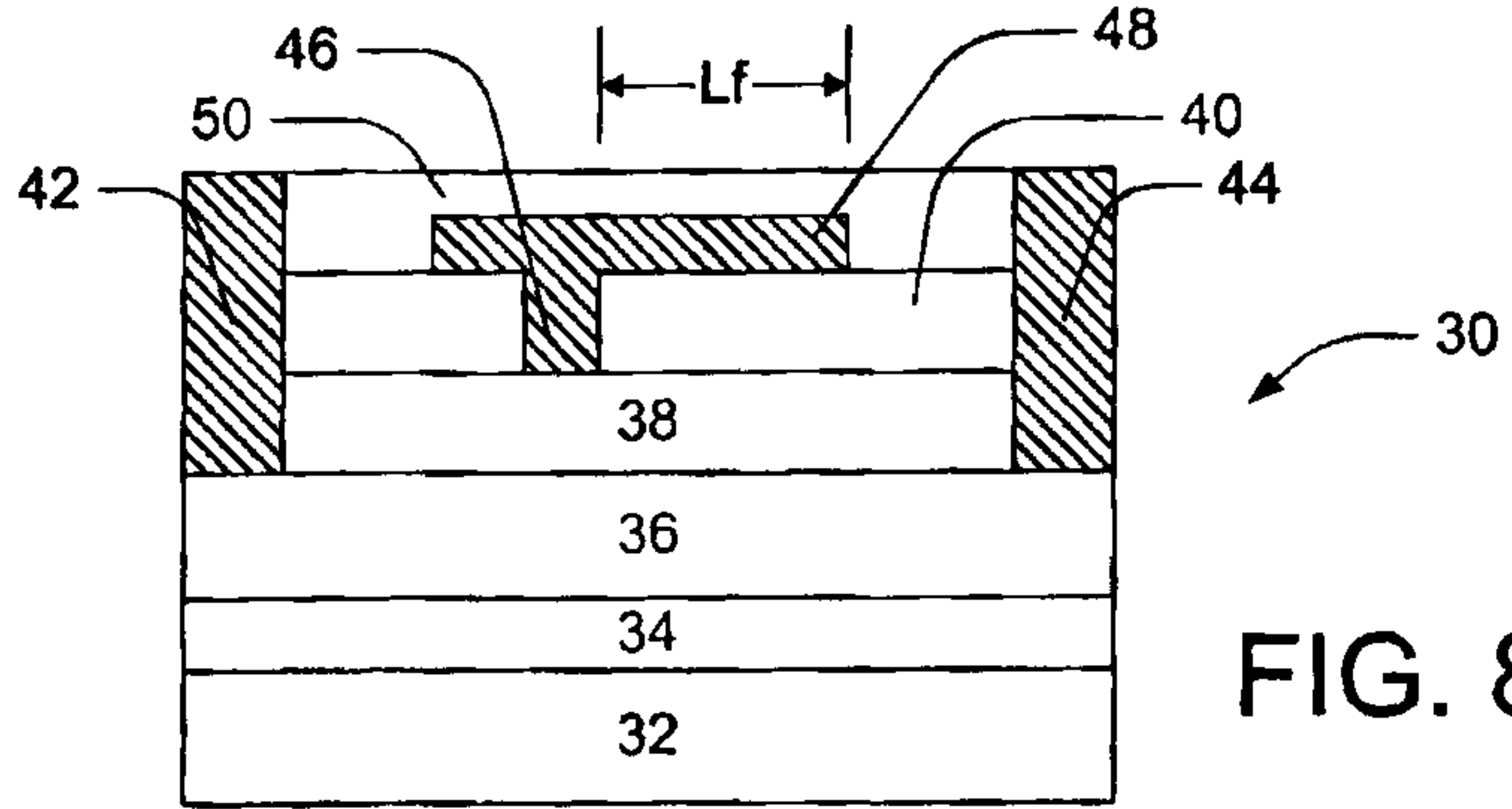


FIG. 8

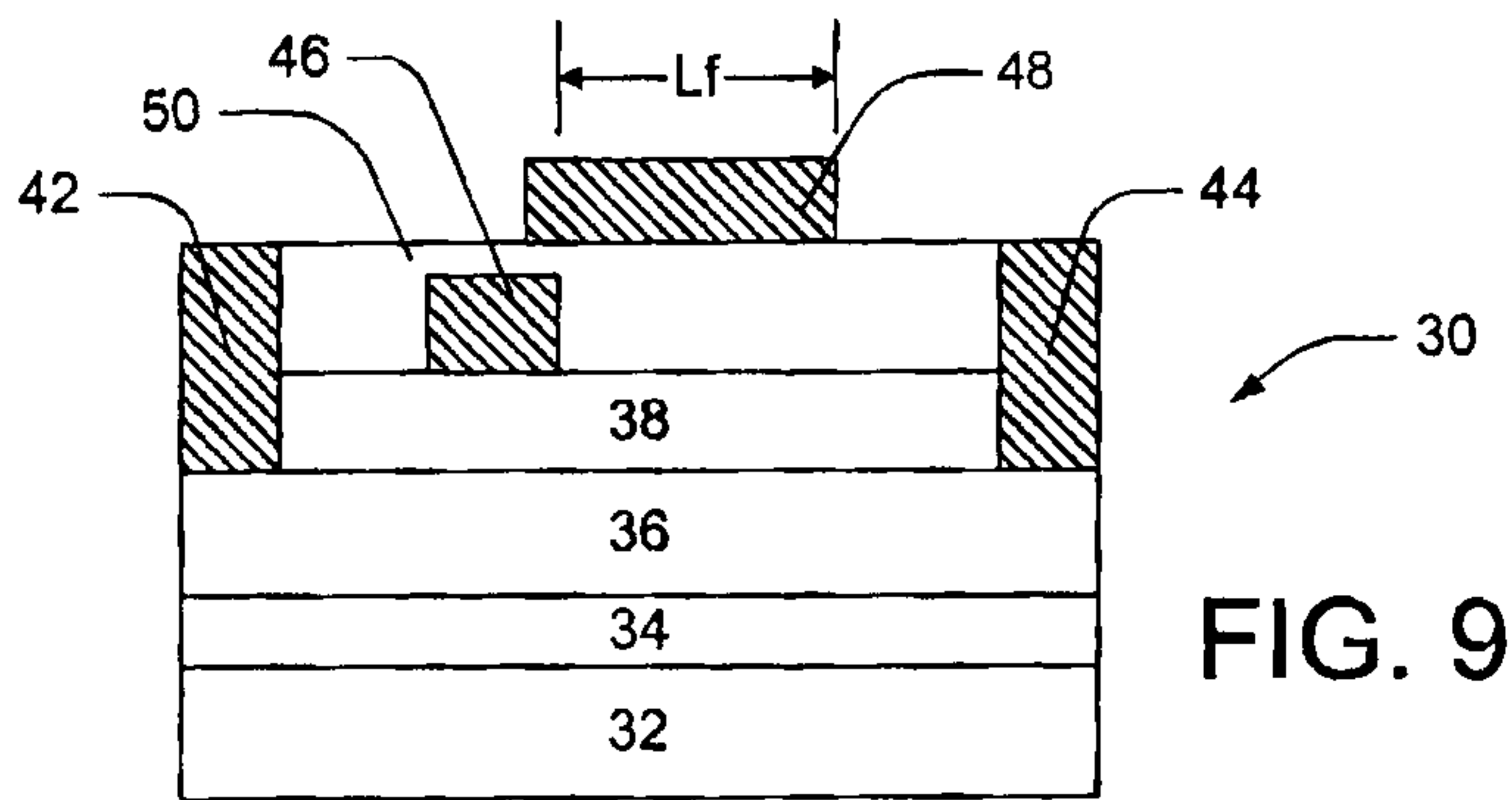


FIG. 9

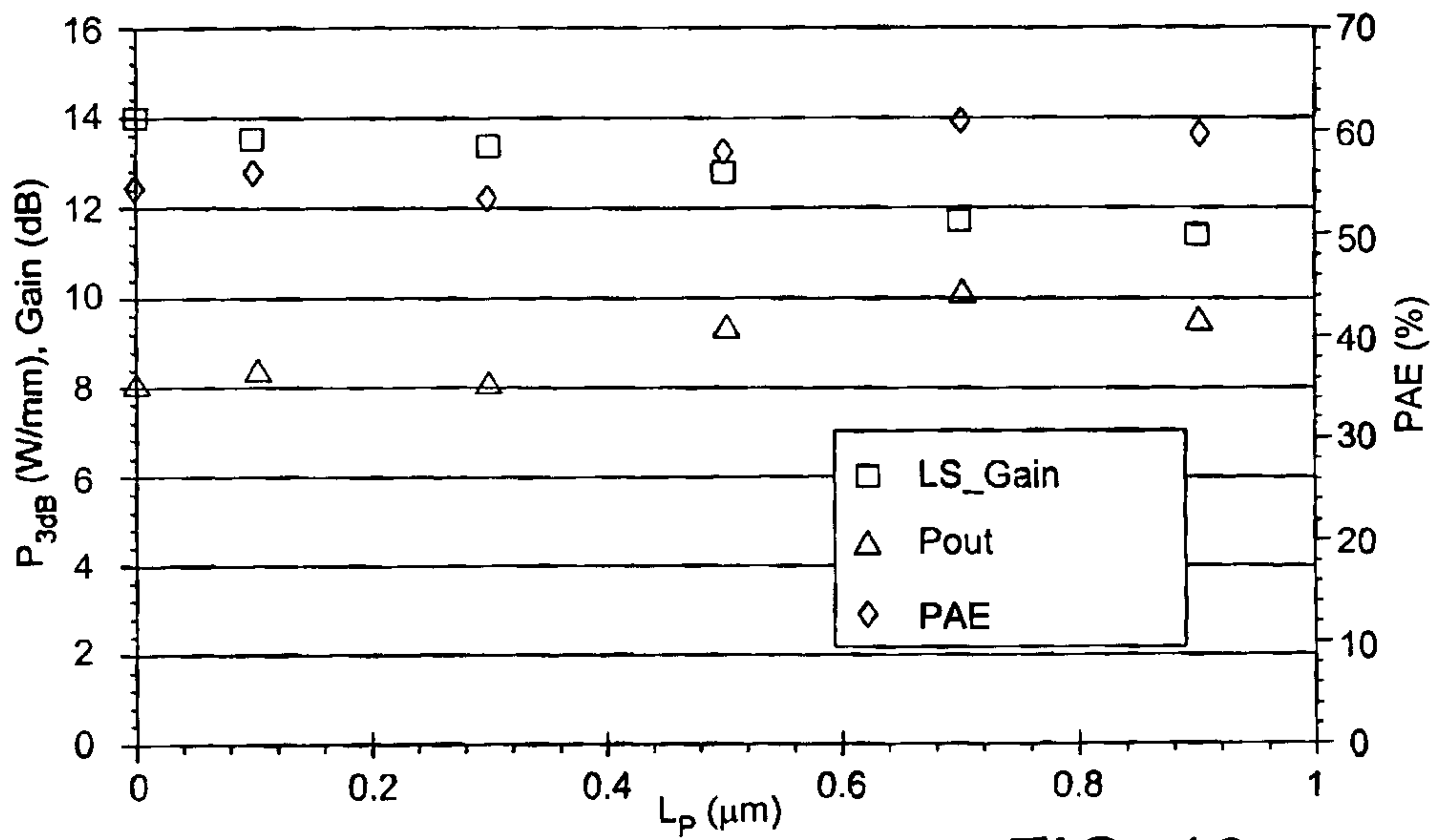
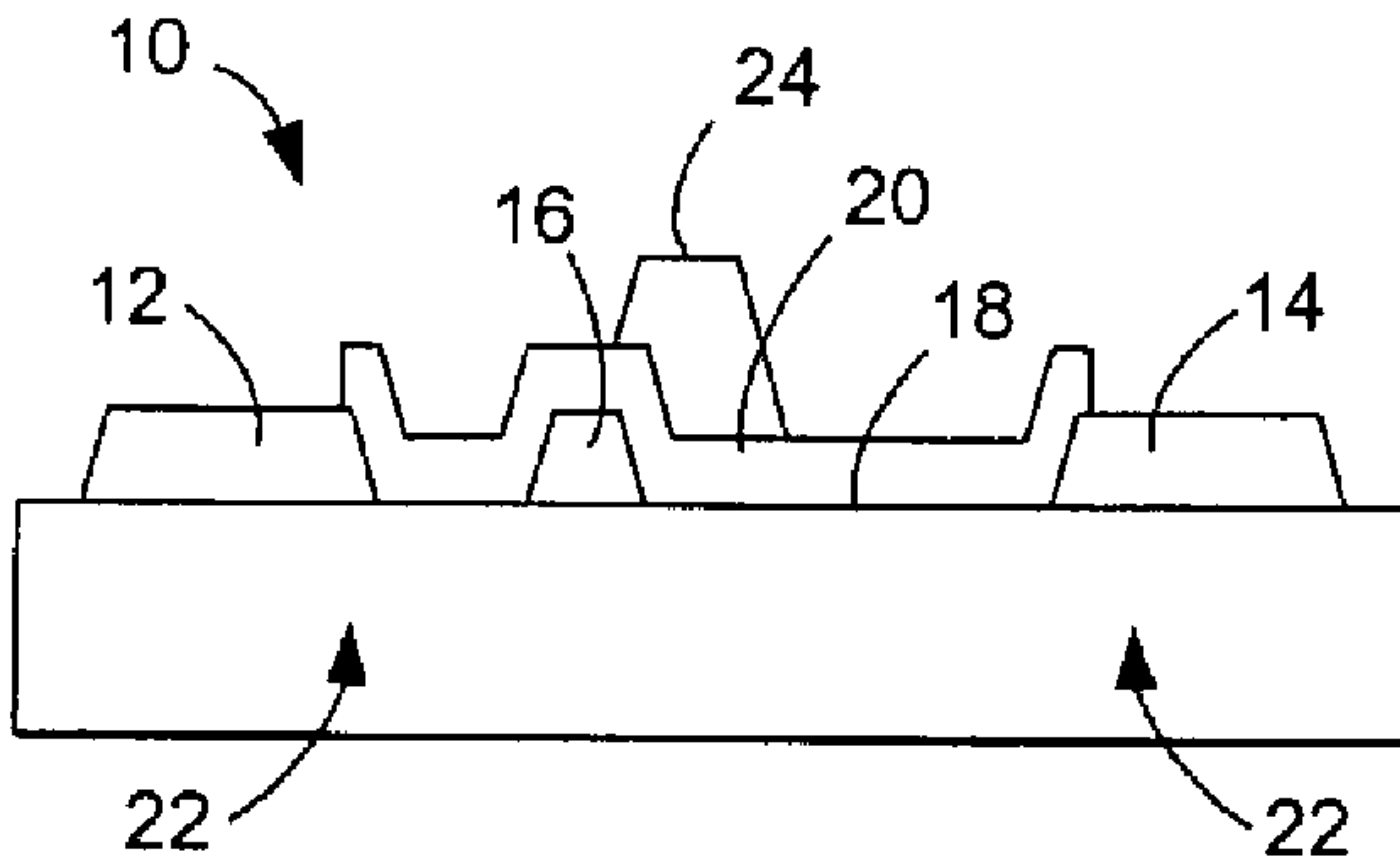


FIG. 10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