(54) Title: APPARATUS FOR TRANSMITTING BROADCAST SIGNALS, APPARATUS FOR RECEIVING BROADCAST SIGNALS, METHOD FOR TRANSMITTING BROADCAST SIGNALS AND METHOD FOR RECEIVING BROADCAST SIGNALS

(57) Abstract: A method and an apparatus for transmitting broadcast signals thereof are disclosed. The apparatus for transmitting broadcast signals comprises an encoder for encoding service data, a mapper for mapping the encoded service data into a plurality of OFDM symbols to build at least one signal frame, a modulator for modulating data in the built at least one signal frame by an OFDM (Orthogonal Frequency Division Multiplex) scheme and a transmitter for transmitting the broadcast signals having the modulated data.

Description

Title of Invention: APPARATUS FOR TRANSMITTING BROADCAST SIGNALS, APPARATUS FOR RECEIVING BROADCAST SIGNALS, METHOD FOR TRANSMITTING BROADCAST SIGNALS AND METHOD FOR RECEIVING BROADCAST SIGNALS

Technical Field

[1]   The present invention relates to an apparatus for transmitting broadcast signals, an apparatus for receiving broadcast signals and methods for transmitting and receiving broadcast signals.

Background Art

[2]   As analog broadcast signal transmission comes to an end, various technologies for transmitting/receiving digital broadcast signals are being developed. A digital broadcast signal may include a larger amount of video/audio data than an analog broadcast signal and further include various types of additional data in addition to the video/audio data.

Disclosure of Invention

Technical Problem

[3]   That is, a digital broadcast system can provide HD (high definition) images, multi-channel audio and various additional services. However, data transmission efficiency for transmission of large amounts of data, robustness of transmission/reception networks and network flexibility in consideration of mobile reception equipment need to be improved for digital broadcast.

Solution to Problem

[4]   To achieve the object and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method for transmitting broadcast signals comprises encoding service data, building at least one signal frame including the encoded service data, wherein the at least one signal frame includes a plurality of OFDM symbols,modulating data in the built at least one signal frame by an OFDM (Orthogonal Frequency Division Multiplex) scheme and transmitting the broadcast signals having the modulated data.

Advantageous Effects of Invention

[5]   The present invention can process data according to service characteristics to control QoS for each service or service component, thereby providing various broadcast

services.

[6]   The present invention can achieve transmission flexibility by transmitting various broadcast services through the same RF signal bandwidth.

[7]   The present invention can improve data transmission efficiency and increase robustness of transmission/reception of broadcast signals using a MIMO system.

[8]   According to the present invention, it is possible to provide broadcast signal transmission and reception methods and apparatus capable of receiving digital broadcast signals without error even with mobile reception equipment or in an indoor environment.

Brief Description of Drawings

[9]   FIG. 1 illustrates a structure of an apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention.

[10]   FIG. 2 illustrates an input formatting module according to an embodiment of the present invention.

[11]   FIG. 3 illustrates an input formatting module according to another embodiment of the present invention.

[12]   FIG. 4 illustrates an input formatting module according to another embodiment of the present invention.

[13]   FIG. 5 illustrates a coding & modulation module according to an embodiment of the present invention.

[14]   FIG. 6 illustrates a frame structure module according to an embodiment of the present invention.

[15]   FIG. 7 illustrates a waveform generation module according to an embodiment of the present invention.

[16]   FIG. 8 illustrates a structure of an apparatus for receiving broadcast signals for future broadcast services according to an embodiment of the present invention.

[17]   FIG. 9 illustrates a synchronization & demodulation module according to an embodiment of the present invention.

[18]   FIG. 10 illustrates a frame parsing module according to an embodiment of the present invention.

[19]   FIG. 11 illustrates a demapping & decoding module according to an embodiment of the present invention.

[20]   FIG. 12 illustrates an output processor according to an embodiment of the present invention.

[21]   FIG. 13 illustrates an output processor according to another embodiment of the present invention.

[22]   FIG. 14 illustrates a coding & modulation module according to another embodiment

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[38]   FIG. 30 is a view illustrating logical composition of a 32K FFT mode random main-seed generator according to an embodiment of the present invention.

[39]   FIG. 31 is a view illustrating an output signal of a time interleaver according to another embodiment of the present invention.

[40]   FIG. 32 is a view illustrating a 32K FFT mode quasi-random main interleaving-seed generator according to an embodiment of the present invention.

[41]   FIG. 33 is expressions representing operations of 32K FFT mode bit shuffling and 32K FFT mode quasi-random main interleaving-seed generator according to an embodiment of the present invention.

[42]   FIG. 34 is a view illustrating logical composition of a 32K FFT mode quasi-random main interleaving-seed generator according to an embodiment of the present invention.

[43]   FIG. 35 is a view illustrating single-memory deinterleaving for input sequential OFDM symbols.

[44]   FIG. 36 is a flowchart illustrating a method for transmitting broadcast signals according to an embodiment of the present invention.

[45]   FIG. 37 is a flowchart illustrating a method for receiving broadcast signals according to an embodiment of the present invention.

Best Mode for Carrying out the Invention

[46]   Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. The detailed description, which will be given below with reference to the accompanying drawings, is intended to explain exemplary embodiments of the present invention, rather than to show the only embodiments that can be implemented according to the present invention. The following detailed description includes specific details in order to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced without such specific details.

[47]   Although most terms used in the present invention have been selected from general ones widely used in the art, some terms have been arbitrarily selected by the applicant and their meanings are explained in detail in the following description as needed. Thus, the present invention should be understood based upon the intended meanings of the terms rather than their simple names or meanings.

[48]   The present invention provides apparatuses and methods for transmitting and receiving broadcast signals for future broadcast services. Future broadcast services according to an embodiment of the present invention include a terrestrial broadcast service, a mobile broadcast service, a UHDTV service, etc. The apparatuses and methods for transmitting according to an embodiment of the present invention may be

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categorized into a base profile for the terrestrial broadcast service, a handheld profile for the mobile broadcast service and an advanced profile for the UHDTV service. In this case, the base profile can be used as a profile for both the terrestrial broadcast service and the mobile broadcast service. That is, the base profile can be used to define a concept of a profile which includes the mobile profile. This can be changed according to intention of the designer.

[49]   The present invention may process broadcast signals for the future broadcast services through non-MIMO (Multiple Input Multiple Output) or MIMO according to one embodiment. A non-MIMO scheme according to an embodiment of the present invention may include a MISO (Multiple Input Single Output) scheme, a SISO (Single Input Single Output) scheme, etc.

[50]   While MISO or MIMO uses two antennas in the following for convenience of description, the present invention is applicable to systems using two or more antennas.

[51]   FIG. 1 illustrates a structure of an apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention.

[52]   The apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention can include an input formatting module 1000, a coding & modulation module 1100, a frame structure module 1200, a waveform generation module 1300 and a signaling generation module 1400. A description will be given of the operation of each module of the apparatus for transmitting broadcast signals.

[53]   Referring to FIG. 1, the apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention can receive MPEG-TSs, IP streams (v4/v6) and generic streams (GSs) as an input signal. In addition, the apparatus for transmitting broadcast signals can receive management information about the configuration of each stream constituting the input signal and generate a final physical layer signal with reference to the received management information.

[54]   The input formatting module 1000 according to an embodiment of the present invention can classify the input streams on the basis of a standard for coding and modulation or services or service components and output the input streams as a plurality of logical data pipes (or data pipes or DP data). The data pipe is a logical channel in the physical layer that carries service data or related metadata, which may carry one or multiple service(s) or service component(s). In addition, data transmitted through each data pipe may be called DP data.

[55]

[56]   *In addition, the input formatting module 1000 according to an embodiment of the present invention can divide each data pipe into blocks necessary to perform coding

and modulation and carry out processes necessary to increase transmission efficiency or to perform scheduling. Details of operations of the input formatting module 1000 will be described later.

[57]   The coding & modulation module 1100 according to an embodiment of the present invention can perform forward error correction (FEC) encoding on each data pipe received from the input formatting module 1000 such that an apparatus for receiving broadcast signals can correct an error that may be generated on a transmission channel. In addition, the coding & modulation module 1100 according to an embodiment of the present invention can convert FEC output bit data to symbol data and interleave the symbol data to correct burst error caused by a channel. As shown in FIG. 1, the coding & modulation module 1100 according to an embodiment of the present invention can divide the processed data such that the divided data can be output through data paths for respective antenna outputs in order to transmit the data through two or more Tx antennas.

[58]   The frame structure module 1200 according to an embodiment of the present invention can map the data output from the coding & modulation module 1100 to signal frames. The frame structure module 1200 according to an embodiment of the present invention can perform mapping using scheduling information output from the input formatting module 1000 and interleave data in the signal frames in order to obtain additional diversity gain.

[59]   The waveform generation module 1300 according to an embodiment of the present invention can convert the signal frames output from the frame structure module 1200 into a signal for transmission. In this case, the waveform generation module 1300 according to an embodiment of the present invention can insert a preamble signal (or preamble) into the signal for detection of the transmission apparatus and insert a reference signal for estimating a transmission channel to compensate for distortion into the signal. In addition, the waveform generation module 1300 according to an em- bodiment of the present invention can provide a guard interval and insert a specific sequence into the same in order to offset the influence of channel delay spread due to multi-path reception. Additionally, the waveform generation module 1300 according to an embodiment of the present invention can perform a procedure necessary for efficient transmission in consideration of signal characteristics such as a peak- to-average power ratio of the output signal.

[60]   The signaling generation module 1400 according to an embodiment of the present invention generates final physical layer signaling information using the input management information and information generated by the input formatting module 1000, coding & modulation module 1100 and frame structure module 1200. Ac- cordingly, a reception apparatus according to an embodiment of the present invention

can decode a received signal by decoding the signaling information.

[61]   As described above, the apparatus for transmitting broadcast signals for future broadcast services according to one embodiment of the present invention can provide terrestrial broadcast service, mobile broadcast service, UHDTV service, etc. Accordingly, the apparatus for transmitting broadcast signals for future broadcast services according to one embodiment of the present invention can multiplex signals for different services in the time domain and transmit the same.

[62]   FIGS. 2, 3 and 4 illustrate the input formatting module 1000 according to embodiments of the present invention. A description will be given of each figure.

[63]   FIG. 2 illustrates an input formatting module according to one embodiment of the present invention. FIG. 2 shows an input formatting module when the input signal is a single input stream.

[64]   Referring to FIG. 2, the input formatting module according to one embodiment of the present invention can include a mode adaptation module 2000 and a stream adaptation module 2100.

[65]   As shown in FIG. 2, the mode adaptation module 2000 can include an input interface block 2010, a CRC-8 encoder block 2020 and a BB header insertion block 2030. Description will be given of each block of the mode adaptation module 2000.

[66]   The input interface block 2010 can divide the single input stream input thereto into data pieces each having the length of a baseband (BB) frame used for FEC (BCH/LDPC) which will be performed later and output the data pieces.

[67]   The CRC-8 encoder block 2020 can perform CRC encoding on BB frame data to add redundancy data thereto.

[68]   The BB header insertion block 2030 can insert, into the BB frame data, a header including information such as mode adaptation type (TS/GS/IP), a user packet length, a data field length, user packet sync byte, start address of user packet sync byte in data field, a high efficiency mode indicator, an input stream synchronization field, etc.

[69]   As shown in FIG. 2, the stream adaptation module 2100 can include a padding insertion block 2110 and a BB scrambler block 2120. Description will be given of each block of the stream adaptation module 2100.

[70]   If data received from the mode adaptation module 2000 has a length shorter than an input data length necessary for FEC encoding, the padding insertion block 2110 can insert a padding bit into the data such that the data has the input data length and output the data including the padding bit.

[71]   The BB scrambler block 2120 can randomize the input bit stream by performing an XOR operation on the input bit stream and a pseudo random binary sequence (PRBS).

[72]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions.

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[73]   As shown in FIG. 2, the input formatting module can finally output data pipes to the coding & modulation module.

[74]   FIG. 3 illustrates an input formatting module according to another embodiment of the present invention. FIG. 3 shows a mode adaptation module 3000 of the input formatting module when the input signal corresponds to multiple input streams.

[75]   The mode adaptation module 3000 of the input formatting module for processing the multiple input streams can independently process the multiple input streams.

[76]   Referring to FIG. 3, the mode adaptation module 3000 for respectively processing the multiple input streams can include input interface blocks, input stream syn-chronizer blocks 3100, compensating delay blocks 3200, null packet deletion blocks 3300, CRC-8 encoder blocks and BB header insertion blocks. Description will be given of each block of the mode adaptation module 3000.

[77]   Operations of the input interface block, CRC-8 encoder block and BB header insertion block correspond to those of the input interface block, CRC-8 encoder block and BB header insertion block described with reference to FIG. 2 and thus description thereof is omitted.

[78]   The input stream synchronizer block 3100 can transmit input stream clock reference (ISCR) information to generate timing information necessary for the apparatus for receiving broadcast signals to restore the TSs or GSs.

[79]   The compensating delay block 3200 can delay input data and output the delayed input data such that the apparatus for receiving broadcast signals can synchronize the input data if a delay is generated between data pipes according to processing of data including the timing information by the transmission apparatus.

[80]   The null packet deletion block 3300 can delete unnecessarily transmitted input null packets from the input data, insert the number of deleted null packets into the input data based on positions in which the null packets are deleted and transmit the input data.

[81]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions.

[82]   FIG. 4 illustrates an input formatting module according to another embodiment of the present invention.

[83]   Specifically, FIG. 4 illustrates a stream adaptation module of the input formatting module when the input signal corresponds to multiple input streams.

[84]   The stream adaptation module of the input formatting module when the input signal corresponds to multiple input streams can include a scheduler 4000, a 1-frame delay block 4100, an in-band signaling or padding insertion block 4200, a physical layer signaling generation block 4300 and a BB scrambler block 4400. Description will be given of each block of the stream adaptation module.

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[85]   The scheduler 4000 can perform scheduling for a MIMO system using multiple antennas having dual polarity. In addition, the scheduler 4000 can generate parameters for use in signal processing blocks for antenna paths, such as a bit-to-cell demux block, a cell interleaver block, a time interleaver block, etc. included in the coding & modulation module illustrated in FIG. 1.

[86]   The 1-frame delay block 4100 can delay the input data by one transmission frame such that scheduling information about the next frame can be transmitted through the current frame for in-band signaling information to be inserted into the data pipes.

[87]   The in-band signaling or padding insertion block 4200 can insert undelayed physical layer signaling (PLS)-dynamic signaling information into the data delayed by one transmission frame. In this case, the in-band signaling or padding insertion block 4200 can insert a padding bit when a space for padding is present or insert in-band signaling information into the padding space. In addition, the scheduler 4000 can output physical layer signaling-dynamic signaling information about the current frame separately from in-band signaling information. Accordingly, a cell mapper, which will be described later, can map input cells according to scheduling information output from the scheduler 4000.

[88]   The physical layer signaling generation block 4300 can generate physical layer signaling data which will be transmitted through a preamble symbol of a transmission frame or spread and transmitted through a data symbol other than the in-band signaling information. In this case, the physical layer signaling data according to an embodiment of the present invention can be referred to as signaling information. Furthermore, the physical layer signaling data according to an embodiment of the present invention can be divided into PLS-pre information and PLS-post information. The PLS-pre in- formation can include parameters necessary to encode the PLS-post information and static PLS signaling data and the PLS-post information can include parameters necessary to encode the data pipes. The parameters necessary to encode the data pipes can be classified into static PLS signaling data and dynamic PLS signaling data. The static PLS signaling data is a parameter commonly applicable to all frames included in a super-frame and can be changed on a super-frame basis. The dynamic PLS signaling data is a parameter differently applicable to respective frames included in a super- frame and can be changed on a frame-by-frame basis. Accordingly, the reception apparatus can acquire the PLS-post information by decoding the PLS-pre information and decode desired data pipes by decoding the PLS-post information.

[89]   The BB scrambler block 4400 can generate a pseudo-random binary sequence (PRBS) and perform an XOR operation on the PRBS and the input bit streams to decrease the peak-to-average power ratio (PAPR) of the output signal of the waveform generation block. As shown in FIG. 4, scrambling of the BB scrambler block 4400 is

applicable to both data pipes and physical layer signaling information.

[90]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to designer.

[91]   As shown in FIG. 4, the stream adaptation module can finally output the data pipes to the coding & modulation module.

[92]   FIG. 5 illustrates a coding & modulation module according to an embodiment of the present invention.

[93]   The coding & modulation module shown in FIG. 5 corresponds to an embodiment of the coding & modulation module illustrated in FIG. 1.

[94]   As described above, the apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention can provide a terrestrial broadcast service, mobile broadcast service, UHDTV service, etc.

[95]   Since QoS (quality of service) depends on characteristics of a service provided by the apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention, data corresponding to respective services needs to be processed through different schemes. Accordingly, the coding & modulation module according to an embodiment of the present invention can independently process data pipes input thereto by independently applying SISO, MISO and MIMO schemes to the data pipes respectively corresponding to data paths. Consequently, the apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention can control QoS for each service or service component transmitted through each data pipe.

[96]   Accordingly, the coding & modulation module according to an embodiment of the present invention can include a first block 5000 for SISO, a second block 5100 for MISO, a third block 5200 for MIMO and a fourth block 5300 for processing the PLS-pre/PLS-post information. The coding & modulation module illustrated in FIG. 5 is an exemplary and may include only the first block 5000 and the fourth block 5300, the second block 5100 and the fourth block 5300 or the third block 5200 and the fourth block 5300 according to design. That is, the coding & modulation module can include blocks for processing data pipes equally or differently according to design.

[97]   A description will be given of each block of the coding & modulation module.

[98]   The first block 5000 processes an input data pipe according to SISO and can include an FEC encoder block 5010, a bit interleaver block 5020, a bit-to-cell demux block 5030, a constellation mapper block 5040, a cell interleaver block 5050 and a time interleaver block 5060.

[99]   The FEC encoder block 5010 can perform BCH encoding and LDPC encoding on the input data pipe to add redundancy thereto such that the reception apparatus can correct an error generated on a transmission channel.

[100]   The bit interleaver block 5020 can interleave bit streams of the FEC-encoded data pipe according to an interleaving rule such that the bit streams have robustness against burst error that may be generated on the transmission channel. Accordingly, when deep fading or erasure is applied to QAM symbols, errors can be prevented from being generated in consecutive bits from among all codeword bits since interleaved bits are mapped to the QAM symbols.

[101]   The bit-to-cell demux block 5030 can determine the order of input bit streams such that each bit in an FEC block can be transmitted with appropriate robustness in consideration of both the order of input bit streams and a constellation mapping rule.

[102]   In addition, the bit interleaver block 5020 is located between the FEC encoder block 5010 and the constellation mapper block 5040 and can connect output bits of LDPC encoding performed by the FEC encoder block 5010 to bit positions having different reliability values and optimal values of the constellation mapper in consideration of LDPC decoding of the apparatus for receiving broadcast signals. Accordingly, the bit-to-cell demux block 5030 can be replaced by a block having a similar or equal function.

[103]   The constellation mapper block 5040 can map a bit word input thereto to one constellation. In this case, the constellation mapper block 5040 can additionally perform rotation & Q-delay. That is, the constellation mapper block 5040 can rotate input constellations according to a rotation angle, divide the constellations into an in-phase component and a quadrature-phase component and delay only the quadrature-phase component by an arbitrary value. Then, the constellation mapper block 5040 can remap the constellations to new constellations using a paired in-phase component and quadrature-phase component.

[104]   In addition, the constellation mapper block 5040 can move constellation points on a two-dimensional plane in order to find optimal constellation points. Through this process, capacity of the coding & modulation module 1100 can be optimized. Furthermore, the constellation mapper block 5040 can perform the above-described operation using IQ-balanced constellation points and rotation. The constellation mapper block 5040 can be replaced by a block having a similar or equal function.

[105]   The cell interleaver block 5050 can randomly interleave cells corresponding to one FEC block and output the interleaved cells such that cells corresponding to respective FEC blocks can be output in different orders.

[106]   The time interleaver block 5060 can interleave cells belonging to a plurality of FEC blocks and output the interleaved cells. Accordingly, the cells corresponding to the FEC blocks are dispersed and transmitted in a period corresponding to a time interleaving depth and thus diversity gain can be obtained.

[107]   The second block 5100 processes an input data pipe according to MISO and can

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include the FEC encoder block, bit interleaver block, bit-to-cell demux block, constellation mapper block, cell interleaver block and time interleaver block in the same manner as the first block 5000. However, the second block 5100 is distinguished from the first block 5000 in that the second block 5100 further includes a MISO processing block 5110. The second block 5100 performs the same procedure including the input operation to the time interleaver operation as those of the first block 5000 and thus description of the corresponding blocks is omitted.

[108]   The MISO processing block 5110 can encode input cells according to a MISO encoding matrix providing transmit diversity and output MISO-processed data through two paths. MISO processing according to one embodiment of the present invention can include OSTBC (orthogonal space time block coding)/OSFBC (orthogonal space frequency block coding, Alamouti coding).

[109]   The third block 5200 processes an input data pipe according to MIMO and can include the FEC encoder block, bit interleaver block, bit-to-cell demux block, constellation mapper block, cell interleaver block and time interleaver block in the same manner as the second block 5100, as shown in FIG. 5. However, the data processing procedure of the third block 5200 is different from that of the second block 5100 since the third block 5200 includes a MIMO processing block 5220.

[110]   That is, in the third block 5200, basic roles of the FEC encoder block and the bit interleaver block are identical to those of the first and second blocks 5000 and 5100 although functions thereof may be different from those of the first and second blocks 5000 and 5100.

[111]   The bit-to-cell demux block 5210 can generate as many output bit streams as input bit streams of MIMO processing and output the output bit streams through MIMO paths for MIMO processing. In this case, the bit-to-cell demux block 5210 can be designed to optimize the decoding performance of the reception apparatus in consideration of characteristics of LDPC and MIMO processing.

[112]   Basic roles of the constellation mapper block, cell interleaver block and time interleaver block are identical to those of the first and second blocks 5000 and 5100 although functions thereof may be different from those of the first and second blocks 5000 and 5100. As shown in FIG. 5, as many constellation mapper blocks, cell interleaver blocks and time interleaver blocks as the number of MIMO paths for MIMO processing can be present. In this case, the constellation mapper blocks, cell interleaver blocks and time interleaver blocks can operate equally or independently for data input through the respective paths.

[113]   The MIMO processing block 5220 can perform MIMO processing on two input cells using a MIMO encoding matrix and output the MIMO-processed data through two paths. The MIMO encoding matrix according to an embodiment of the present

invention can include spatial multiplexing, Golden code, full-rate full diversity code, linear dispersion code, etc.

[114]   The fourth block 5300 processes the PLS-pre/PLS-post information and can perform SISO or MISO processing.

[115]   The basic roles of the bit interleaver block, bit-to-cell demux block, constellation mapper block, cell interleaver block, time interleaver block and MISO processing block included in the fourth block 5300 correspond to those of the second block 5100 although functions thereof may be different from those of the second block 5100.

[116]   A shortened/punctured FEC encoder block 5310 included in the fourth block 5300 can process PLS data using an FEC encoding scheme for a PLS path provided for a case in which the length of input data is shorter than a length necessary to perform FEC encoding. Specifically, the shortened/punctured FEC encoder block 5310 can perform BCH encoding on input bit streams, pad 0s corresponding to a desired input bit stream length necessary for normal LDPC encoding, carry out LDPC encoding and then remove the padded 0s to puncture parity bits such that an effective code rate becomes equal to or lower than the data pipe rate.

[117]   The blocks included in the first block 5000 to fourth block 5300 may be omitted or replaced by blocks having similar or identical functions according to design.

[118]   As illustrated in FIG. 5, the coding & modulation module can output the data pipes (or DP data), PLS-pre information and PLS-post information processed for the respective paths to the frame structure module.

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[120]   *FIG. 6 illustrates a frame structure module according to one embodiment of the present invention.

[121]   The frame structure module shown in FIG. 6 corresponds to an embodiment of the frame structure module 1200 illustrated in FIG. 1.

[122]   The frame structure module according to one embodiment of the present invention can include at least one cell-mapper 6000, at least one delay compensation module 6100 and at least one block interleaver 6200. The number of cell mappers 6000, delay compensation modules 6100 and block interleavers 6200 can be changed. A description will be given of each module of the frame structure block.

[123]   The cell-mapper 6000 can allocate cells corresponding to SISO-, MISO- or MIMO-processed data pipes output from the coding & modulation module, cells corresponding to common data commonly applicable to the data pipes and cells corresponding to the PLS-pre/PLS-post information to signal frames according to scheduling information. The common data refers to signaling information commonly applied to all or some data pipes and can be transmitted through a specific data pipe. The data pipe through which the common data is transmitted can be referred to as a

common data pipe and can be changed according to design.

[124]   When the apparatus for transmitting broadcast signals according to an embodiment of the present invention uses two output antennas and Alamouti coding is used for MISO processing, the cell-mapper 6000 can perform pair-wise cell mapping in order to maintain orthogonality according to Alamouti encoding. That is, the cell-mapper 6000 can process two consecutive cells of the input cells as one unit and map the unit to a frame. Accordingly, paired cells in an input path corresponding to an output path of each antenna can be allocated to neighboring positions in a transmission frame.

[125]   The delay compensation block 6100 can obtain PLS data corresponding to the current transmission frame by delaying input PLS data cells for the next transmission frame by one frame. In this case, the PLS data corresponding to the current frame can be transmitted through a preamble part in the current signal frame and PLS data corresponding to the next signal frame can be transmitted through a preamble part in the current signal frame or in-band signaling in each data pipe of the current signal frame. This can be changed by the designer.

[126]   The block interleaver 6200 can obtain additional diversity gain by interleaving cells in a transport block corresponding to the unit of a signal frame. In addition, the block interleaver 6200 can perform interleaving by processing two consecutive cells of the input cells as one unit when the above-described pair-wise cell mapping is performed. Accordingly, cells output from the block interleaver 6200 can be two consecutive identical cells.

[127]   When pair-wise mapping and pair-wise interleaving are performed, at least one cell mapper and at least one block interleaver can operate equally or independently for data input through the paths.

[128]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[129]   As illustrated in FIG. 6, the frame structure module can output at least one signal frame to the waveform generation module.

[130]   FIG. 7 illustrates a waveform generation module according to an embodiment of the present invention.

[131]   The waveform generation module illustrated in FIG. 7 corresponds to an embodiment of the waveform generation module 1300 described with reference to FIG. 1.

[132]   The waveform generation module according to an embodiment of the present invention can modulate and transmit as many signal frames as the number of antennas for receiving and outputting signal frames output from the frame structure module illustrated in FIG. 6.

[133]   Specifically, the waveform generation module illustrated in FIG. 7 is an embodiment of a waveform generation module of an apparatus for transmitting broadcast signals

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using m Tx antennas and can include m processing blocks for modulating and outputting frames corresponding to m paths. The m processing blocks can perform the same processing procedure. A description will be given of operation of the first processing block 7000 from among the m processing blocks.

[134]   The first processing block 7000 can include a reference signal & PAPR reduction block 7100, an inverse waveform transform block 7200, a PAPR reduction in time block 7300, a guard sequence insertion block 7400, a preamble insertion block 7500, a waveform processing block 7600, other system insertion block 7700 and a DAC (digital analog converter) block 7800.

[135]   The reference signal insertion & PAPR reduction block 7100 can insert a reference signal into a predetermined position of each signal block and apply a PAPR reduction scheme to reduce a PAPR in the time domain. If a broadcast transmission/reception system according to an embodiment of the present invention corresponds to an OFDM system, the reference signal insertion & PAPR reduction block 7100 can use a method of reserving some active subcarriers rather than using the same. In addition, the reference signal insertion & PAPR reduction block 7100 may not use the PAPR reduction scheme as an optional feature according to broadcast transmission/reception system.

[136]   The inverse waveform transform block 7200 can transform an input signal in a manner of improving transmission efficiency and flexibility in consideration of transmission channel characteristics and system architecture. If the broadcast transmission/reception system according to an embodiment of the present invention corresponds to an OFDM system, the inverse waveform transform block 7200 can employ a method of transforming a frequency domain signal into a time domain signal through inverse FFT operation. If the broadcast transmission/reception system according to an embodiment of the present invention corresponds to a single carrier system, the inverse waveform transform block 7200 may not be used in the waveform generation module.

[137]   The PAPR reduction in time block 7300 can use a method for reducing PAPR of an input signal in the time domain. If the broadcast transmission/reception system according to an embodiment of the present invention corresponds to an OFDM system, the PAPR reduction in time block 7300 may use a method of simply clipping peak amplitude. Furthermore, the PAPR reduction in time block 7300 may not be used in the broadcast transmission/reception system according to an embodiment of the present invention since it is an optional feature.

[138]   The guard sequence insertion block 7400 can provide a guard interval between neighboring signal blocks and insert a specific sequence into the guard interval as necessary in order to minimize the influence of delay spread of a transmission channel.

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Accordingly, the reception apparatus can easily perform synchronization or channel estimation. If the broadcast transmission/reception system according to an embodiment of the present invention corresponds to an OFDM system, the guard sequence insertion block 7400 may insert a cyclic prefix into a guard interval of an OFDM symbol.

[139]   The preamble insertion block 7500 can insert a signal of a known type (e.g. the preamble or preamble symbol) agreed upon between the transmission apparatus and the reception apparatus into a transmission signal such that the reception apparatus can rapidly and efficiently detect a target system signal. If the broadcast transmission/ reception system according to an embodiment of the present invention corresponds to an OFDM system, the preamble insertion block 7500 can define a signal frame composed of a plurality of OFDM symbols and insert a preamble symbol into the beginning of each signal frame. That is, the preamble carries basic PLS data and is located in the beginning of a signal frame.

[140]   The waveform processing block 7600 can perform waveform processing on an input baseband signal such that the input baseband signal meets channel transmission characteristics. The waveform processing block 7600 may use a method of performing square-root-raised cosine (SRRC) filtering to obtain a standard for out-of-band emission of a transmission signal. If the broadcast transmission/reception system according to an embodiment of the present invention corresponds to a multi-carrier system, the waveform processing block 7600 may not be used.

[141]   The other system insertion block 7700 can multiplex signals of a plurality of broadcast transmission/reception systems in the time domain such that data of two or more different broadcast transmission/reception systems providing broadcast services can be simultaneously transmitted in the same RF signal bandwidth. In this case, the two or more different broadcast transmission/reception systems refer to systems providing different broadcast services. The different broadcast services may refer to a terrestrial broadcast service, mobile broadcast service, etc. Data related to respective broadcast services can be transmitted through different frames.

[142]   The DAC block 7800 can convert an input digital signal into an analog signal and output the analog signal. The signal output from the DAC block 7800 can be transmitted through m output antennas. A Tx antenna according to an embodiment of the present invention can have vertical or horizontal polarity.

[143]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[144]   FIG. 8 illustrates a structure of an apparatus for receiving broadcast signals for future broadcast services according to an embodiment of the present invention.

[145]   The apparatus for receiving broadcast signals for future broadcast services according to an embodiment of the present invention can correspond to the apparatus for

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transmitting broadcast signals for future broadcast services, described with reference to FIG. 1. The apparatus for receiving broadcast signals for future broadcast services according to an embodiment of the present invention can include a synchronization & demodulation module 8000, a frame parsing module 8100, a demapping & decoding module 8200, an output processor 8300 and a signaling decoding module 8400. A de- scription will be given of operation of each module of the apparatus for receiving broadcast signals.

[146]   The synchronization & demodulation module 8000 can receive input signals through m Rx antennas, perform signal detection and synchronization with respect to a system corresponding to the apparatus for receiving broadcast signals and carry out de- modulation corresponding to a reverse procedure of the procedure performed by the apparatus for transmitting broadcast signals.

[147]   The frame parsing module 8100 can parse input signal frames and extract data through which a service selected by a user is transmitted. If the apparatus for transmitting broadcast signals performs interleaving, the frame parsing module 8100 can carry out deinterleaving corresponding to a reverse procedure of interleaving. In this case, the positions of a signal and data that need to be extracted can be obtained by decoding data output from the signaling decoding module 8400 to restore scheduling information generated by the apparatus for transmitting broadcast signals.

[148]   The demapping & decoding module 8200 can convert the input signals into bit domain data and then deinterleave the same as necessary. The demapping & decoding module 8200 can perform demapping for mapping applied for transmission efficiency and correct an error generated on a transmission channel through decoding. In this case, the demapping & decoding module 8200 can obtain transmission parameters necessary for demapping and decoding by decoding the data output from the signaling decoding module 8400.

[149]   The output processor 8300 can perform reverse procedures of various compression/ signal processing procedures which are applied by the apparatus for transmitting broadcast signals to improve transmission efficiency. In this case, the output processor 8300 can acquire necessary control information from data output from the signaling decoding module 8400. The output of the output processor 8300 corresponds to a signal input to the apparatus for transmitting broadcast signals and may be MPEG-TSs, IP streams (v4 or v6) and generic streams.

[150]   The signaling decoding module 8400 can obtain PLS information from the signal de- modulated by the synchronization & demodulation module 8000. As described above, the frame parsing module 8100, demapping & decoding module 8200 and output processor 8300 can execute functions thereof using the data output from the signaling decoding module 8400.

[151]   FIG. 9 illustrates a synchronization & demodulation module according to an embodiment of the present invention.

[152]   The synchronization & demodulation module shown in FIG. 9 corresponds to an embodiment of the synchronization & demodulation module described with reference to FIG. 8. The synchronization & demodulation module shown in FIG. 9 can perform a reverse operation of the operation of the waveform generation module illustrated in FIG. 7.

[153]   As shown in FIG. 9, the synchronization & demodulation module according to an embodiment of the present invention corresponds to a synchronization & demodulation module of an apparatus for receiving broadcast signals using m Rx antennas and can include m processing blocks for demodulating signals respectively input through m paths. The m processing blocks can perform the same processing procedure. A description will be given of operation of the first processing block 9000 from among the m processing blocks.

[154]   The first processing block 9000 can include a tuner 9100, an ADC block 9200, a preamble detector 9300, a guard sequence detector 9400, a waveform transform block 9500, a time/frequency synchronization block 9600, a reference signal detector 9700, a channel equalizer 9800 and an inverse waveform transform block 9900.

[155]   The tuner 9100 can select a desired frequency band, compensate for the magnitude of a received signal and output the compensated signal to the ADC block 9200.

[156]   The ADC block 9200 can convert the signal output from the tuner 9100 into a digital signal.

[157]   The preamble detector 9300 can detect a preamble (or preamble signal or preamble symbol) in order to check whether or not the digital signal is a signal of the system corresponding to the apparatus for receiving broadcast signals. In this case, the preamble detector 9300 can decode basic transmission parameters received through the preamble.

[158]   The guard sequence detector 9400 can detect a guard sequence in the digital signal. The time/frequency synchronization block 9600 can perform time/frequency synchronization using the detected guard sequence and the channel equalizer 9800 can estimate a channel through a received/restored sequence using the detected guard sequence.

[159]   The waveform transform block 9500 can perform a reverse operation of inverse waveform transform when the apparatus for transmitting broadcast signals has performed inverse waveform transform. When the broadcast transmission/reception system according to one embodiment of the present invention is a multi-carrier system, the waveform transform block 9500 can perform FFT. Furthermore, when the broadcast transmission/reception system according to an embodiment of the present

invention is a single carrier system, the waveform transform block 9500 may not be used if a received time domain signal is processed in the frequency domain or processed in the time domain.

[160]   The time/frequency synchronization block 9600 can receive output data of the preamble detector 9300, guard sequence detector 9400 and reference signal detector 9700 and perform time synchronization and carrier frequency synchronization including guard sequence detection and block window positioning on a detected signal. Here, the time/frequency synchronization block 9600 can feed back the output signal of the waveform transform block 9500 for frequency synchronization.

[161]   The reference signal detector 9700 can detect a received reference signal. Accordingly, the apparatus for receiving broadcast signals according to an embodiment of the present invention can perform synchronization or channel estimation.

[162]   The channel equalizer 9800 can estimate a transmission channel from each Tx antenna to each Rx antenna from the guard sequence or reference signal and perform channel equalization for received data using the estimated channel.

[163]   The inverse waveform transform block 9900 may restore the original received data domain when the waveform transform block 9500 performs waveform transform for efficient synchronization and channel estimation/equalization. If the broadcast transmission/reception system according to an embodiment of the present invention is a single carrier system, the waveform transform block 9500 can perform FFT in order to carry out synchronization/channel estimation/equalization in the frequency domain and the inverse waveform transform block 9900 can perform IFFT on the channel-equalized signal to restore transmitted data symbols. If the broadcast transmission/ reception system according to an embodiment of the present invention is a multi-carrier system, the inverse waveform transform block 9900 may not be used.

[164]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[165]   FIG. 10 illustrates a frame parsing module according to an embodiment of the present invention.

[166]   The frame parsing module illustrated in FIG. 10 corresponds to an embodiment of the frame parsing module described with reference to FIG. 8. The frame parsing module shown in FIG. 10 can perform a reverse operation of the operation of the frame structure module illustrated in FIG. 6.

[167]   As shown in FIG. 10, the frame parsing module according to an embodiment of the present invention can include at least one block deinterleaver 10000 and at least one cell demapper 10100.

[168]   The block deinterleaver 10000 can deinterleave data input through data paths of the m Rx antennas and processed by the synchronization & demodulation module on a

signal block basis. In this case, if the apparatus for transmitting broadcast signals performs pair-wise interleaving as illustrated in FIG. 8, the block deinterleaver 10000 can process two consecutive pieces of data as a pair for each input path. Accordingly, the block interleaver 10000 can output two consecutive pieces of data even when deinterleaving has been performed. Furthermore, the block deinterleaver 10000 can perform a reverse operation of the interleaving operation performed by the apparatus for transmitting broadcast signals to output data in the original order.

[169]   The cell demapper 10100 can extract cells corresponding to common data, cells corresponding to data pipes and cells corresponding to PLS data from received signal frames. The cell demapper 10100 can merge data distributed and transmitted and output the same as a stream as necessary. When two consecutive pieces of cell input data are processed as a pair and mapped in the apparatus for transmitting broadcast signals, as shown in FIG. 6, the cell demapper 10100 can perform pair-wise cell demapping for processing two consecutive input cells as one unit as a reverse procedure of the mapping operation of the apparatus for transmitting broadcast signals.

[170]   In addition, the cell demapper 10100 can extract PLS signaling data received through the current frame as PLS-pre & PLS-post data and output the PLS-pre & PLS-post data.

[171]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[172]   FIG. 11 illustrates a demapping & decoding module according to an embodiment of the present invention.

[173]   The demapping & decoding module shown in FIG. 11 corresponds to an embodiment of the demapping & decoding module illustrated in FIG. 8. The demapping & decoding module shown in FIG. 11 can perform a reverse operation of the operation of the coding & modulation module illustrated in FIG. 5.

[174]   The coding & modulation module of the apparatus for transmitting broadcast signals according to an embodiment of the present invention can process input data pipes by independently applying SISO, MISO and MIMO thereto for respective paths, as described above. Accordingly, the demapping & decoding module illustrated in FIG. 11 can include blocks for processing data output from the frame parsing module according to SISO, MISO and MIMO in response to the apparatus for transmitting broadcast signals.

[175]   As shown in FIG. 11, the demapping & decoding module according to an embodiment of the present invention can include a first block 11000 for SISO, a second block 11100 for MISO, a third block 11200 for MIMO and a fourth block 11300 for processing the PLS-pre/PLS-post information. The demapping & decoding module shown in FIG. 11 is exemplary and may include only the first block 11000 and the

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fourth block 11300, only the second block 11100 and the fourth block 11300 or only the third block 11200 and the fourth block 11300 according to design. That is, the demapping & decoding module can include blocks for processing data pipes equally or differently according to design.

[176]   A description will be given of each block of the demapping & decoding module.

[177]   The first block 11000 processes an input data pipe according to SISO and can include a time deinterleaver block 11010, a cell deinterleaver block 11020, a constellation demapper block 11030, a cell-to-bit mux block 11040, a bit deinterleaver block 11050 and an FEC decoder block 11060.

[178]   The time deinterleaver block 11010 can perform a reverse process of the process performed by the time interleaver block 5060 illustrated in FIG. 5. That is, the time deinterleaver block 11010 can deinterleave input symbols interleaved in the time domain into original positions thereof.

[179]   The cell deinterleaver block 11020 can perform a reverse process of the process performed by the cell interleaver block 5050 illustrated in FIG. 5. That is, the cell dein-terleaver block 11020 can deinterleave positions of cells spread in one FEC block into original positions thereof.

[180]   The constellation demapper block 11030 can perform a reverse process of the process performed by the constellation mapper block 5040 illustrated in FIG. 5. That is, the constellation demapper block 11030 can demap a symbol domain input signal to bit domain data. In addition, the constellation demapper block 11030 may perform hard decision and output decided bit data. Furthermore, the constellation demapper block 11030 may output a log-likelihood ratio (LLR) of each bit, which corresponds to a soft decision value or probability value. If the apparatus for transmitting broadcast signals applies a rotated constellation in order to obtain additional diversity gain, the constellation demapper block 11030 can perform 2-dimensional LLR demapping cor-responding to the rotated constellation. Here, the constellation demapper block 11030 can calculate the LLR such that a delay applied by the apparatus for transmitting broadcast signals to the I or Q component can be compensated.

[181]   The cell-to-bit mux block 11040 can perform a reverse process of the process performed by the bit-to-cell demux block 5030 illustrated in FIG. 5. That is, the cell-to-bit mux block 11040 can restore bit data mapped by the bit-to-cell demux block 5030 to the original bit streams.

[182]   The bit deinterleaver block 11050 can perform a reverse process of the process performed by the bit interleaver 5020 illustrated in FIG. 5. That is, the bit deinterleaver block 11050 can deinterleave the bit streams output from the cell-to-bit mux block 11040 in the original order.

[183]   The FEC decoder block 11060 can perform a reverse process of the process

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performed by the FEC encoder block 5010 illustrated in FIG. 5. That is, the FEC decoder block 11060 can correct an error generated on a transmission channel by performing LDPC decoding and BCH decoding.

[184]   The second block 11100 processes an input data pipe according to MISO and can include the time deinterleaver block, cell deinterleaver block, constellation demapper block, cell-to-bit mux block, bit deinterleaver block and FEC decoder block in the same manner as the first block 11000, as shown in FIG. 11. However, the second block 11100 is distinguished from the first block 11000 in that the second block 11100 further includes a MISO decoding block 11110. The second block 11100 performs the same procedure including time deinterleaving operation to outputting operation as the first block 11000 and thus description of the corresponding blocks is omitted.

[185]   The MISO decoding block 11110 can perform a reverse operation of the operation of the MISO processing block 5110 illustrated in FIG. 5. If the broadcast transmission/ reception system according to an embodiment of the present invention uses STBC, the MISO decoding block 11110 can perform Alamouti decoding.

[186]   The third block 11200 processes an input data pipe according to MIMO and can include the time deinterleaver block, cell deinterleaver block, constellation demapper block, cell-to-bit mux block, bit deinterleaver block and FEC decoder block in the same manner as the second block 11100, as shown in FIG. 11. However, the third block 11200 is distinguished from the second block 11100 in that the third block 11200 further includes a MIMO decoding block 11210. The basic roles of the time deinterleaver block, cell deinterleaver block, constellation demapper block, cell-to-bit mux block and bit deinterleaver block included in the third block 11200 are identical to those of the corresponding blocks included in the first and second blocks 11000 and 11100 although functions thereof may be different from the first and second blocks 11000 and 11100.

[187]   The MIMO decoding block 11210 can receive output data of the cell deinterleaver for input signals of the m Rx antennas and perform MIMO decoding as a reverse operation of the operation of the MIMO processing block 5220 illustrated in FIG. 5. The MIMO decoding block 11210 can perform maximum likelihood decoding to obtain optimal decoding performance or carry out sphere decoding with reduced complexity. Otherwise, the MIMO decoding block 11210 can achieve improved decoding performance by performing MMSE detection or carrying out iterative decoding with MMSE detection.

[188]   The fourth block 11300 processes the PLS-pre/PLS-post information and can perform SISO or MISO decoding. The fourth block 11300 can carry out a reverse process of the process performed by the fourth block 5300 described with reference to FIG. 5.

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[189]   The basic roles of the time deinterleaver block, cell deinterleaver block, constellation demapper block, cell-to-bit mux block and bit deinterleaver block included in the fourth block 11300 are identical to those of the corresponding blocks of the first, second and third blocks 11000, 11100 and 11200 although functions thereof may be different from the first, second and third blocks 11000, 11100 and 11200.

[190]   The shortened/punctured FEC decoder 11310 included in the fourth block 11300 can perform a reverse process of the process performed by the shortened/punctured FEC encoder block 5310 described with reference to FIG. 5. That is, the shortened/punctured FEC decoder 11310 can perform de-shortening and de-puncturing on data shortened/punctured according to PLS data length and then carry out FEC decoding thereon. In this case, the FEC decoder used for data pipes can also be used for PLS. Accordingly, additional FEC decoder hardware for the PLS only is not needed and thus system design is simplified and efficient coding is achieved.

[191]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[192]   The demapping & decoding module according to an embodiment of the present invention can output data pipes and PLS information processed for the respective paths to the output processor, as illustrated in FIG. 11.

[193]   FIGS. 12 and 13 illustrate output processors according to embodiments of the present invention.

[194]   FIG. 12 illustrates an output processor according to an embodiment of the present invention. The output processor illustrated in FIG. 12 corresponds to an embodiment of the output processor illustrated in FIG. 8. The output processor illustrated in FIG. 12 receives a single data pipe output from the demapping & decoding module and outputs a single output stream. The output processor can perform a reverse operation of the operation of the input formatting module illustrated in FIG. 2.

[195]   The output processor shown in FIG. 12 can include a BB scrambler block 12000, a padding removal block 12100, a CRC-8 decoder block 12200 and a BB frame processor block 12300.

[196]   The BB scrambler block 12000 can descramble an input bit stream by generating the same PRBS as that used in the apparatus for transmitting broadcast signals for the input bit stream and carrying out an XOR operation on the PRBS and the bit stream.

[197]   The padding removal block 12100 can remove padding bits inserted by the apparatus for transmitting broadcast signals as necessary.

[198]   The CRC-8 decoder block 12200 can check a block error by performing CRC decoding on the bit stream received from the padding removal block 12100.

[199]   The BB frame processor block 12300 can decode information transmitted through a BB frame header and restore MPEG-TSs, IP streams (v4 or v6) or generic streams

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using the decoded information.

[200]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[201]   FIG. 13 illustrates an output processor according to another embodiment of the present invention. The output processor shown in FIG. 13 corresponds to an embodiment of the output processor illustrated in FIG. 8. The output processor shown in FIG. 13 receives multiple data pipes output from the demapping & decoding module. Decoding multiple data pipes can include a process of merging common data commonly applicable to a plurality of data pipes and data pipes related thereto and decoding the same or a process of simultaneously decoding a plurality of services or service components (including a scalable video service) by the apparatus for receiving broadcast signals.

[202]   The output processor shown in FIG. 13 can include a BB descrambler block, a padding removal block, a CRC-8 decoder block and a BB frame processor block as the output processor illustrated in FIG. 12. The basic roles of these blocks correspond to those of the blocks described with reference to FIG. 12 although operations thereof may differ from those of the blocks illustrated in FIG. 12.

[203]   A de-jitter buffer block 13000 included in the output processor shown in FIG. 13 can compensate for a delay, inserted by the apparatus for transmitting broadcast signals for synchronization of multiple data pipes, according to a restored TTO (time to output) parameter.

[204]   A null packet insertion block 13100 can restore a null packet removed from a stream with reference to a restored DNP (deleted null packet) and output common data.

[205]   A TS clock regeneration block 13200 can restore time synchronization of output packets based on ISCR (input stream time reference) information.

[206]   A TS recombining block 13300 can recombine the common data and data pipes related thereto, output from the null packet insertion block 13100, to restore the original MPEG-TSs, IP streams (v4 or v6) or generic streams. The TTO, DNT and ISCR information can be obtained through the BB frame header.

[207]   An in-band signaling decoding block 13400 can decode and output in-band physical layer signaling information transmitted through a padding bit field in each FEC frame of a data pipe.

[208]   The output processor shown in FIG. 13 can BB-descramble the PLS-pre information and PLS-post information respectively input through a PLS-pre path and a PLS-post path and decode the descrambled data to restore the original PLS data. The restored PLS data is delivered to a system controller included in the apparatus for receiving broadcast signals. The system controller can provide parameters necessary for the synchronization & demodulation module, frame parsing module, demapping & decoding

module and output processor module of the apparatus for receiving broadcast signals.

[209]   The above-described blocks may be omitted or replaced by blocks having similar r identical functions according to design.

[210]   FIG. 14 illustrates a coding & modulation module according to another embodiment of the present invention.

[211]   The coding & modulation module shown in FIG. 14 corresponds to another embodiment of the coding & modulation module illustrated in FIGS. 1 to 5.

[212]   To control QoS for each service or service component transmitted through each data pipe, as described above with reference to FIG. 5, the coding & modulation module shown in FIG. 14 can include a first block 14000 for SISO, a second block 14100 for MISO, a third block 14200 for MIMO and a fourth block 14300 for processing the PLS-pre/PLS-post information. In addition, the coding & modulation module can include blocks for processing data pipes equally or differently according to the design. The first to fourth blocks 14000 to 14300 shown in FIG. 14 are similar to the first to fourth blocks 5000 to 5300 illustrated in FIG. 5.

[213]   However, the first to fourth blocks 14000 to 14300 shown in FIG. 14 are distinguished from the first to fourth blocks 5000 to 5300 illustrated in FIG. 5 in that a constellation mapper 14010 included in the first to fourth blocks 14000 to 14300 has a function different from the first to fourth blocks 5000 to 5300 illustrated in FIG. 5, a rotation & I/Q interleaver block 14020 is present between the cell interleaver and the time interleaver of the first to fourth blocks 14000 to 14300 illustrated in FIG. 14 and the third block 14200 for MIMO has a configuration different from the third block 5200 for MIMO illustrated in FIG. 5. The following description focuses on these differences between the first to fourth blocks 14000 to 14300 shown in FIG. 14 and the first to fourth blocks 5000 to 5300 illustrated in FIG. 5.

[214]   The constellation mapper block 14010 shown in FIG. 14 can map an input bit word to a complex symbol. However, the constellation mapper block 14010 may not perform constellation rotation, differently from the constellation mapper block shown in FIG. 5. The constellation mapper block 14010 shown in FIG. 14 is commonly applicable to the first, second and third blocks 14000, 14100 and 14200, as described above.

[215]   The rotation & I/Q interleaver block 14020 can independently interleave in-phase and quadrature-phase components of each complex symbol of cell-interleaved data output from the cell interleaver and output the in-phase and quadrature-phase components on a symbol-by-symbol basis. The number of number of input data pieces and output data pieces of the rotation & I/Q interleaver block 14020 is two or more which can be changed by the designer. In addition, the rotation & I/Q interleaver block 14020 may not interleave the in-phase component.

[216]   The rotation & I/Q interleaver block 14020 is commonly applicable to the first to fourth blocks 14000 to 14300, as described above. In this case, whether or not the rotation & I/Q interleaver block 14020 is applied to the fourth block 14300 for processing the PLS-pre/post information can be signaled through the above-described preamble.

[217]   The third block 14200 for MIMO can include a Q-block interleaver block 14210 and a complex symbol generator block 14220, as illustrated in FIG. 14.

[218]   The Q-block interleaver block 14210 can permute a parity part of an FEC-encoded FEC block received from the FEC encoder. Accordingly, a parity part of an LDPC H matrix can be made into a cyclic structure like an information part. The Q-block interleaver block 14210 can permute the order of output bit blocks having Q size of the LDPC H matrix and then perform row-column block interleaving to generate final bit streams.

[219]   The complex symbol generator block 14220 receives the bit streams output from the Q-block interleaver block 14210, maps the bit streams to complex symbols and outputs the complex symbols. In this case, the complex symbol generator block 14220 can output the complex symbols through at least two paths. This can be modified by the designer.

[220]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[221]   The coding & modulation module according to another embodiment of the present invention, illustrated in FIG. 14, can output data pipes, PLS-pre information and PLS-post information processed for respective paths to the frame structure module.

[222]   FIG. 15 illustrates a demapping & decoding module according to another embodiment of the present invention.

[223]   The demapping & decoding module shown in FIG. 15 corresponds to another embodiment of the demapping & decoding module illustrated in FIG. 11. The demapping & decoding module shown in FIG. 15 can perform a reverse operation of the operation of the coding & modulation module illustrated in FIG. 14.

[224]   As shown in FIG. 15, the demapping & decoding module according to another embodiment of the present invention can include a first block 15000 for SISO, a second block 11100 for MISO, a third block 15200 for MIMO and a fourth block 14300 for processing the PLS-pre/PLS-post information. In addition, the demapping & decoding module can include blocks for processing data pipes equally or differently according to design. The first to fourth blocks 15000 to 15300 shown in FIG. 15 are similar to the first to fourth blocks 11000 to 11300 illustrated in FIG. 11.

[225]   However, the first to fourth blocks 15000 to 15300 shown in FIG. 15 are distinguished from the first to fourth blocks 11000 to 11300 illustrated in FIG. 11 in that

an I/Q deinterleaver and derotation block 15010 is present between the time interleaver and the cell deinterleaver of the first to fourth blocks 15000 to 15300, a constellation mapper 15010 included in the first to fourth blocks 15000 to 15300 has a function different from the first to fourth blocks 11000 to 11300 illustrated in FIG. 11 and the third block 15200 for MIMO has a configuration different from the third block 11200 for MIMO illustrated in FIG. 11. The following description focuses on these differences between the first to fourth blocks 15000 to 15300 shown in FIG. 15 and the first to fourth blocks 11000 to 11300 illustrated in FIG. 11.

[226]   The I/Q deinterleaver & derotation block 15010 can perform a reverse process of the process performed by the rotation & I/Q interleaver block 14020 illustrated in FIG. 14. That is, the I/Q deinterleaver & derotation block 15010 can deinterleave I and Q components I/Q-interleaved and transmitted by the apparatus for transmitting broadcast signals and derotate complex symbols having the restored I and Q components.

[227]   The I/Q deinterleaver & derotation block 15010 is commonly applicable to the first to fourth blocks 15000 to 15300, as described above. In this case, whether or not the I/Q deinterleaver & derotation block 15010 is applied to the fourth block 15300 for processing the PLS-pre/post information can be signaled through the above-described preamble.

[228]   The constellation demapper block 15020 can perform a reverse process of the process performed by the constellation mapper block 14010 illustrated in FIG. 14. That is, the constellation demapper block 15020 can demap cell-deinterleaved data without performing derotation.

[229]   The third block 15200 for MIMO can include a complex symbol parsing block 15210 and a Q-block deinterleaver block 15220, as shown in FIG. 15.

[230]   The complex symbol parsing block 15210 can perform a reverse process of the process performed by the complex symbol generator block 14220 illustrated in FIG. 14. That is, the complex symbol parsing block 15210 can parse complex data symbols and demap the same to bit data. In this case, the complex symbol parsing block 15210 can receive complex data symbols through at least two paths.

[231]   The Q-block deinterleaver block 15220 can perform a reverse process of the process carried out by the Q-block interleaver block 14210 illustrated in FIG. 14. That is, the Q-block deinterleaver block 15220 can restore Q size blocks according to row-column deinterleaving, restore the order of permuted blocks to the original order and then restore positions of parity bits to original positions according to parity deinterleaving.

[232]   The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[233]   As illustrated in FIG. 15, the demapping & decoding module according to another

embodiment of the present invention can output data pipes and PLS information processed for respective paths to the output processor.

[234]   As described above, the apparatus and method for transmitting broadcast signals according to an embodiment of the present invention can multiplex signals of different broadcast transmission/reception systems within the same RF channel and transmit the multiplexed signals and the apparatus and method for receiving broadcast signals according to an embodiment of the present invention can process the signals in response to the broadcast signal transmission operation. Accordingly, it is possible to provide a flexible broadcast transmission and reception system.

[235]   Hereinafter, a frequency interleaving procedure according to an embodiment of the present invention will be described.

[236]   The purpose of the block interleaver 6200 in the present invention, which operates on a single OFDM symbol, is to provide frequency diversity by randomly interleaving data cells received from the frame structure module 1200. In order to get maximum interleaving gain in a single signal frame (or frame), a different interleaving-seed is used for every OFDM symbol pair comprised of two sequential OFDM symbols.

[237]   The block interleaver 6200 may interleave cells in a transport block as a unit of a signal frame to acquire additional diversity gain. The block interleaver 6200 according to an embodiment of the present invention may be referred to as a frequency interleaver, which can be changed according to a designer's intention. According to an embodiment of the present invention, the block interleaver 6200 may apply different interleaving seeds to at least one OFDM sysmbol or apply different interleaving seeds to a frame including a plurality of OFDM symbols.

[238]   In the present invention, the aforementioned frequency interleaving method may be referred to as random frequency interleaving (random FI).

[239]   In addition, according to an embodiment of the present invention, the random FI may be applied to a super-frame structure including a plurality of signal frames with a plurality of OFDM symbols.

[240]   As described above, a broadcast signal transmitting apparatus or a frequency interleaver therein according to an embodiment of the present invention may apply different interleaving seeds (or interleaving patterns) for at least one OFDM symbol, that is, for each OFDM symbol or each of pair-wise OFDM symbols and perform the random FI, thereby acquiring frequency diversity. In addition, the frequency interleaver according to an embodiment of the present invention may apply different interleaving seed for each respective signal frame and perform the random FI, thereby acquiring additional frequency diversity.

[241]   Accordingly, a broadcast transmitting apparatus or a frequency interleaver according to an embodiment of the present invention may have a ping-pong frequency interleaver

structure that perform frequency interleaving in units of one pair of consecutive OFDM symbols (pair-wise OFDM symbol) using two memory banks. Hereinafter, an interleaving operation of the frequency interleaver according to an embodiment of the present invention may be referred to as pair-wise symbol FI (or pair-wise FI) or ping-pong FI (ping-pong interleaving). The aforementioned interleaving operation corresponds to an embodiment of the random FI, which can be changed according to a designer's intention.

[242]   Even-indexed pair-wise OFDM symbols and odd pair-wise OFDM symbols may be intermittently interleaved via different FI memory banks. In addition, the frequency interleaver according to an embodiment of the present invention may simultaneously perform reading and writing operations on one pair of consecutive OFDM symbols input to each memory bank using an arbitrary interleaving seed. A detailed operation will be described below.

[243]   In addition, according to an embodiment of the present invention, as a logical frequency interleaving operation for logically and effectively interleaving all OFDM symbols in a super-frame, an interleaving seed is basically changed in units of one pair of OFDM symbols.

[244]   In this case, according to an embodiment of the present invention, the interleaving seed may be generated by an arbitrary random generator or a random generator formed by a combination of various random generators. In addition, according to an embodiment of the present invention, various interleaving seeds may be generated by cyclic-shifting one main interleaving seed in order to effectively change an interleaving seed. In this case, a cyclic-shifting rule may be hierarchically defined in consideration of OFDM symbol and signal frame units. This can be changed according to a designer's intention, which will be described in detail.

[245]   A broadcast signal receiving apparatus according to an embodiment of the present invention may perform an inverse procedure of the aforementioned random frequency interleaving. In this case, the broadcast signal receiving apparatus or a frequency deinterleaver thereof according to an embodiment of the present invention may not use a ping-pong structure using a double-memory and may perform deinterleaving on consecutive input OFDM symbols via a single-memory. Accordingly, memory use efficiency can be enhanced. In addition, reading and writing operations are still required, which is called as a single-memory deinterleaving operation. Such a deinterleaving scheme is very efficient in a memory-use aspect.

[246]   FIG. 16 is a view illustrating an operation of a frequency interleaver according to an embodiment of the present invention.

[247]   FIG. 16 illustrates the basic operation of the frequency interleaver using two memory banks at the transmitter, which enables a single-memory deinterleaving at the receiver.

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[248]   As described above, the frequency interleaver according to an embodiment of the present invention may perform a ping-pong interleaving operation.

[249]   Typically, ping-pong interleaving operation is accomplished by means of two memory banks. In the proposed FI operation, two memory banks are for each pair-wise OFDM symbol.

[250]   The maximum memory ROM (Read Only Memory) size for interleaving is approximately two times to a maximum FFT size. At a transmit side, the ROM size increase is rather less critical, compared to a receiver side.

[251]   As described above, odd pair-wise OFDM symbols and odd pair-wise OFDM symbols may be intermittently interleaved via different FI memory-banks. That is, the second (odd-indexed) pair-wise OFDM symbol is interleaved in the second bank, while the first (even-indexed) pair-wise OFDM symbol is interleaved in the first bank and so on. For each pair-wise OFDM symbol, a single interleaving seed is used. Based on the interleaving seed and reading-writing (or writing-reading) operation, two OFDM symbols are sequentially interleaved.

[252]   Reading-writing operations according to an embodiment of the present invention are simultaneously accomplished without a collision. Writing-reading operations according to an embodiment of the present invention are simultaneously accomplished without a collision.

[253]   FIG. 16 illustrates an operation of the aforementioned frequency interleaver. As illustrated in FIG. 16, the frequency interleaver may include a demux 16000, two memory banks, a memory bank-A 16100 and a memory bank-B 16200, and a demux 16300.

[254]   First, the frequency interleaver according to an embodiment of the present invention may perform a demultiplexing processing to the input sequential OFDM symbols for the pair-wise OFDM symbol FI. Then the frequency interleaver according to an embodiment of the present invention performs a reading-writing FI operation in each memory bank A and B with a single interleaving seed. As shown in FIG. 16, two memory banks are used for each OFDM symbol pair. Operationally, the first (even-indexed) OFDM symbol pair is interleaved in memory bank-A, while the second (odd-indexed) OFDM symbol pair is interleaved in memory bank-B and so on, alternating between A and B.

[255]   Then the frequency interleaver according to an embodiment of the present invention may perform a multiplexing processing to ping-pong FI outputs for sequential OFDM symbol transmission.

[256]   FIG. 17 illustrates a basic switch model for MUX and DEMUX procedures according to an embodiment of the present invention.

[257]   FIG. 17 illustrates simple operations the DEMUX and MUX applied input and output

of memory-bank-A/-B in the aforementioned ping-pong FI structure.

[258]   The DEMUX and MUX may control the input sequential OFDM symbols to be in-
terleaved, and the output OFDM symbol pair to be transmitted, respectively. Different
interleaving seeds are used for every OFDM symbol pair.

[259]   Hereinafter, reading-writing operations of frequency interleaving according to an em-
bodiment of the present invention will be described.

[260]   A frequency interleaver according to an embodiment of the present invention may
select or use a single interleaving see and use the interleaving seed in writing and
reading operations for the first and second OFDM symbols, respectively. That is, the
frequency interleaver according to an embodiment of the present invention may use the
one selected arbitrary interleaving seed in an operation of writing a first OFDM
symbol of a pair-wise OFDM symbol, and use a second OFDM symbol in a reading
operation, thereby achieving effective interleaving. Virtually, it seems like that two
different interleaving seeds are applied to two OFDM symbols, respectively.

[261]   Details of the reading-writing operation according to an embodiment of the present
invention are as follows:

[262]   For the first OFDM symbol, the frequency interleaver according to an embodiment
of the present invention may perform random writing into memory (according to an in-
terleaving seed) and perform then linear reading. For the second OFDM symbol, the
frequency interleaver according to an embodiment of the present invention may
perform linear writing into memory, (affected by the linear reading operation for the
first OFDM symbol), simultaneously. Also, the frequency interleaver according to an
embodiment of the present invention may perform then random reading (according to
an interleaving seed).

[263]   As described above, the broadcast signal receiving apparatus according to an em-
bodiment of the present invention may continuously transmit a plurality of frames on
the time axis. In the present invention, a set of signal frames transmitted for a prede-
termined period of time may be referred to as a super-frame. Accordingly, one super-
frame may include N signal frames and each signal frame may include a plurality of
OFDM symbols.

[264]   FIG. 18 is a view illustrating a concept of frequency interleaving applied to a single
super-frame according to an embodiment of the present invention.

[265]   A frequency interleaver according to an embodiment of the present invention may
change interleaving seed every pair-wise OFDM symbol in a single signal frame
(symbol index reset) and change interleaving seed to be used in a single signal frame
by every frame (frame index reset). Consequently, the frequency interleaver according
to an embodiment of the present invention may change interleaving seed in a super-
frame (super-frame index reset).

[266]   Accordingly, the frequency interleaver according to an embodiment of the present may logically and effectively interleave all OFDM symbols in a super-frame.

[267]   FIG. 19 is a view illustrating logical operation mechanism of frequency interleaving applied to a single super-frame according to an embodiment of the present invention.

[268]   FIG. 19 illustrates logical operation mechanism of a frequency interleaver and related parameter thereof, for effectively changing interleaving seeds to be used the one super-frame described with reference to FIG. 18.

[269]   As described above, in the present invention, various interleaving seeds may be effectively generated by cyclic-shifting one main interleaving seed by as much as an arbitrary offset. As illustrated in FIG. 19, according to an embodiment of the present invention, the aforementioned offset may be differently generated for each frame and each of pair-wise OFDM symbol to generate different interleaving seeds. Hereinafter, the logical operation mechanism will be described.

[270]   As illustrated in a lower block of FIG. 19, a frequency interleaver according to an embodiment of the present invention may randomly generate a frame offset for each signal frame using an input frame index. The frame offset according to an embodiment of the present invention may be generated by a frame offset generator included in a frequency interleaver. In this case, when super-frame index is reset, a frame offset applied to each frame is generated for each signal frame in each super-frame identified according to a super-frame index.

[271]   As illustrated in a middle block of FIG. 19, a frequency interleaver according to an embodiment of the present invention may randomly generate a symbol offset to be applied to each OFDM symbol included in each signal frame using an input symbol index. The symbol offset according to an embodiment of the present invention may be generated by a symbol offset generator included in a frequency interleaver. In this case, when a frame index is reset, a symbol offset for each symbol is generated for symbols in each signal frame identified according to a frame index. In addition, the frequency interleaver according to an embodiment of the present invention may generate various interleaving seeds by cyclic-shifting a main interleaving seed on each OFDM symbol by as much as a symbol offset.

[272]   Then, as illustrated in an upper block of FIG. 19, a frequency interleaver according to an embodiment of the present invention may perform random FI on cells included in each OFDM symbol using an input cell index. A random FI parameter according to an embodiment of the present invention may be generated by a random FI generator included in the frequency interleaver.

[273]   FIG. 20 illustrates math figures of logical operation mechanism of frequency interleaving applied to a single super-frame according to an embodiment of the present invention.

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[274]   In detail, FIG. 20 illustrates a correlation of the aforementioned frame offset parameter, symbol offset, parameter, and random FI applied to a cell included in each OFDM. As illustrated in FIG. 20, an offset to be used in an OFDM symbol may be generated through a hierarchical structure of the aforementioned frame offset generator and the aforementioned symbol offset generator. In this case, the frame offset generator and the symbol offset generator may be designed using a arbitrary random generator.

[275]   FIG. 21 illustrates an operation of a memory bank according to an embodiment of the present invention.

[276]   As described above, two memory banks according to an embodiment of the present invention may apply an arbitrary interleaving seed generated via the aforementioned procedure to each pair-wise OFDM symbol. In addition, each memory bank may change interleaving seed every pair-wise OFDM symbol.

[277]   FIG. 22 illustrates a frequency deinterleaving procedure according to an embodiment of the present invention.

[278]   A broadcast signal receiving apparatus according to an embodiment of the present invention may perform an inverse procedure of the aforementioned frequency interleaving procedure. FIG. 22 illustrates single-memory deinterleaving (FDI) for input sequential OFDM symbols.

[279]   Basically, frequency deinterleaving operation follows to the inverse processing of frequency interleaving operation. For a single-memory use, no further processing is required.

[280]   When pair-wise OFDM symbols illustrated in a left portion of FIG. 22 are input, the broadcast signal receiving apparatus according to an embodiment of the present invention may perform the aforementioned reading and writing operation using a single memory, as illustrated in a right portion of FIG. 22. In this case, the broadcast signal receiving apparatus according to an embodiment of the present invention may generate a memory-index and perform frequency deinterleaving (reading and writing) corresponding to an inverse procedure of frequency interleaving (writing and reading) performed by a broadcast signal transmitting apparatus. The benefit is inherently caused by the proposed pair-wise ping-pong interleaving architecture.

[281]   The following math figures show a change procedure of interleaving seed in each of the aforementioned memory banks.

[282]   MathFigure 1

[Math.1]

$$for \quad j = 0, 1, \ldots, N_{sym} \quad and \quad for \quad k = 0, 1, \ldots, N_{data},$$

$$F_j(C_j(k)) = X_j(k)$$

$$where \quad C_j(k) = (T(k) + S_{\lfloor j/2 \rfloor}) \bmod N_{data}$$

$T(k)$ *is a main* interleaving *seed generated by a random generator, used in the main FI*

$S_{\lfloor j/2 \rfloor}$ *is a random symbol offset generated by a random generator, used in the jth pair − wise OFDM symbol*

[283]   MathFigure 2

[Math.2]

$$for \quad j = 0, 1, \ldots, N_{sym} \quad and \quad k = 0, 1, \ldots, N_{data}$$

$$F_j(k) = X_j(C_j(k))$$

$$where \quad C_j(k) \ is \ the \ same \ random \ seed$$

$$used \ for \ the \ first \ symbol$$

[284]   The above expression 1 is for the first OFDM symbol, i.e., (j mod 2) = 0 of the ith pair-wise OFDM symbol and the above expression 2 is for the second OFDM symbol, i.e., (j mod 2) = 1 of the ith pair-wise OFDM symbol.emory banks.

[285]   As described above, a waveform transform block 9500 may perform FFT trans-formation on input data. According to an embodiment of the present invention, an FFT size may be 4K, 8K, 16K, 32K, or the like, and an FFT mode indicating the FFT size may be defined. The aforementioned FFT mode may be signaled via a preamble (or a preamble signal, a preamble symbol) in a signal frame or signal via PLS-pre or PLS-prost. The FFT size may be changed according to a designer's intention.

[286]   A frequency interleaver or an interleaving seed generator included therein according to an embodiment of the present invention may perform an operation according to the aforementioned FFT mode. In addition, an interleaving seed generator according to an embodiment of the present invention may include a random seed generator and a quasi-random interleaving seed generator. Hereinafter, an operation of the interleaving seed generator according to each FFT mode is divided into an operation of the random seed generator and an operation of the quasi-random interleaving seed generator and

will be described.

[287]   Hereinafter, the random seed generator for a 32K FFT mode will be described.

[288]   As described above, the random seed generator according to an embodiment of the present invention may apply different interleaving seeds to respective OFDM symbols to acquire frequency diversity. Logical composition of the random seed generator may include a random main-seed generator (Cj(K)) for interleaving cells in a single OFDM symbol and a random symbol-offset generator (

$$S_{\lfloor j/2 \rfloor}$$

) for changing a symbol offset.

[289]   The random main-seed generator may generate the aforementioned random FI parameter. That is, the random main-seed generator may generate seed for interleaving cells in a single OFDM symbol.

[290]   The random main-seed generator according to an embodiment of the present invention may include a spreader and a randomizer and perform rendering a full randomness in frequency-domain. According to an embodiment of the present invention, in the case of 32K FFT mode, the random main-seed generator may include a 1 bit spreader and an 14 bit-randomizer. The randomizer according to an embodiment of the present invention may a main-PRBS generator which is defined based on the 14-bit binary word sequence (or binary sequence).

[291]   The random symbol-offset generator according to an embodiment of the present invention may change a symbol offset of each OFDM symbol. That is, the random symbol-offset generator may generate the aforementioned symbol offset. The random symbol-offset generator according to an embodiment of the present invention may include k bits-spreader and (X-k) bits-randomizer and perform rendering a spreading as much as 2k cases, in time-domain. X may be differently set for the respective FFT modes. According to an embodiment of the present invention, in the case of 32K FFT mode, a (15-k) bit-randomizer may be used. The (X-k) bits-randomizer according to an embodiment of the present invention may a sub-PRBS generator which is defined based on (15-k) bit binary word sequence (or binary sequence).

[292]   The aforementioned spreader and randomizer may be used to achieve spreading and random effects during generation of the interleaving seed.

[293]   FIG. 23 is a view illustrating an output signal of a time interleaver according to an embodiment of the present invention.

[294]   The time interleaver according to an embodiment of the present invention may perform a column-wise writing operation and a row-wise reading operation on one FEC block, as illustrated in a left portion of FIG. 23. A right block of FIG. 23 indicates an output signal of the time interleaver and the output signal is input to a frequency in-

terleaver according to an embodiment of the present invention.

[295]   Thus, one FEC block is periodically spread in each FI block. Accordingly, in order to increase the robustness of a channel with strong periodic properties, the afore-mentioned random interleaving seed generator may be used.

[296]   FIG. 24 is a view of a 32K FFT mode random main-seed generator according to an embodiment of the present invention.

[297]   The 32K FFT mode random main-seed generator according to an embodiment of the present invention may include a spreader (1-bit toggling), a randomizer, a memory-index check, a random symbol-offset generator, and a modulo operator. As described above, the random main-seed generator may include a spreader and a randomizer. Hereinafter, an operation of each block will be described.

[298]   The (cell) spreader may be operated using an upper portion of n-bit of total 15-bit and may function as a multiplexer based on a look-up table. In the case of 32K FFT mode, the (cell) spreader may be a 1-bit multiplexer (or toggling).

[299]   The randomizer may be operated via a PN generator and may provide full randomness during interleaving. As described above, in the case of 32K FFT mode, the randomizer may be a PN generator that considers 14-bit. This can be changed according to a designer's intention. Also the spreader and the randomizer are operated through multiplexer and PN generator, respectively.

[300]   The memory-index check may not use seed when a memory-index generated by the spreader and the randomizer is greater than Ndata and may repeatedly operate the spreader and the randomizer to adjust the output memory-index such that the output memory-index does not exceed Ndata. The Ndata according to the embodiment of the present invention is equal to the number of the data cells.

[301]   The random symbol-offset generator may generate a symbol-offset for cyclic-shifting main interleaving-seed generated by the main-interleaving seed generator for each pair-wise OFDM symbol. A detailed operation will be described below.

[302]   The modulo operator may be operated when a result value, obtained by adding a symbol-offset output by the random symbol-offset generator for each pair-wise OFDM symbol to the memory-index output by the memory-index check, exceeds Ndata. Locations of the illustrated memory-index check and modulo operator can be changed according to a designer's intention.

[303]   FIG. 25 illustrates math figures representing an operation of a 32K FFT mode random main-seed generator according to an embodiment of the present invention.

[304]   The math figures illustrated in an upper portion of FIG. 25 show initial value setting and primitive polynomial of a randomizer. In this case, the primitive polynomial may be 14th primitive polynomial and the initial value may be changed by arbitrary values.

[305]   The math figures illustrated in a lower portion of FIG. 25 show procedures of cal-

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culating and outputting main-interleaving seed for an output signal of the spreader and the randomizer. As illustrated in the math figure, one random symbol-offset may be applied to each pair-wise OFDM in the same way.

[306]   FIG. 26 is a view illustrating a 32K FFT mode random symbol-offset generator according to an embodiment of the present invention.

[307]   As above described, the random symbol-offset generator according to an embodiment of the present invention may include k bits-spreader and (X-k) bits-randomizer.

[308]   Hereinafter, each block will be described.

[309]   The k bits-spreader may be operated through a 2k multiplexer and may be optimally designed to maximize inter-symbol spreading properties (or to minimize correlation properties).

[310]   The randomizer may be operated through a N bits-PN generator and designed to provide randomness.

[311]   The 32K FFT mode random symbol-offset generator may include a 0/1/2 bits-spreader and a 15/14/13 bits-random generator (or a PN generator). Details will be described below.

[312]   FIG. 27 illustrates math figures showing operations of a random symbol-offset generator and a random Symbol-offset generator for 32K FFT mode including a 0 bits-spreader and a 15 bits-PN generator according to an embodiment of the present invention.

[313]   (a) illustrates a random symbol-offset generator including a 0 bits-spreader and a 15 bits-PN generator. (b) illustrates an operation of a 32K FFT mode random Symbol-offset generator.

[314]   The random symbol-offset generator illustrated in (a) may be operated for each pair-wise OFDM symbol.

[315]   A math figure illustrated in an upper portion of (b) shows initial value setting and primitive polynomial of the randomizer. In this case, the primitive polynomial may be 12th primitive polynomial and the initial value may be changed by arbitrary values.

[316]   A math figure illustrated in a lower portion of (b) shows a procedure for calculating and outputting a symbol-offset for output signals of a spreader and a randomizer. As illustrated in the math figure, the random symbol-offset generator may be operated for each pair-wise OFDM symbol. Accordingly, the length of an entire output offset may correspond to half of the length of an entire OFDM symbol.

[317]   FIG. 28 illustrates math figures illustrating operations of a random symbol-offset generator and a random Symbol-offset generator for 32K FFT mode including a 1 bits-spreader and an 14 bits-PN generator according to an embodiment of the present invention.

[318]   (a) shows the random symbol-offset generator including a 1 bits-spreader and an 14
          bits-PN generator. (b) shows a math figure representing an operation of a 32K FFT
          mode random symbol-offset generator.

[319]   The random symbol-offset generator illustrated in (a) may be operated for each pair-
          wise OFDM symbol.

[320]   A math figure illustrated in an upper portion of (b) shows initial value setting and
          primitive polynomial of a randomizer. In this case, the primitive polynomial may be
          14th primitive polynomial and the initial value may be changed by arbitrary values.

[321]   A math figure illustrated in a lower portion of (b) shows a procedure of calculating
          and outputting a symbol-offset for an output signal of the spreader and the randomizer.
          As illustrated in the math figure, the random symbol-offset generator may be operated
          for each pair-wise OFDM symbol. Accordingly, the length of an entire output offset
          may correspond to half of the length of an entire OFDM symbol.

[322]   FIG. 29 illustrates math figures illustrating operations of a random symbol-offset
          generator and a random Symbol-offset generator for 32K FFT mode including a 2 bits-
          spreader and a 13 bits-PN generator according to an embodiment of the present
          invention.

[323]   (a) shows the random Symbol-offset generator including a 2 bits-spreader and a 13
          bits-PN generator. (b) shows a math figure representing an operation of a 32K FFT
          mode random symbol-offset generator.

[324]   The random symbol-offset generator illustrated in (a) may be operated for each pair-
          wise OFDM symbol.

[325]   A math figure illustrated in an upper portion of (b) shows initial value setting and
          primitive polynomial of a randomizer. In this case, the primitive polynomial may be
          13th primitive polynomial and the initial value may include arbitrary values.

[326]   A math figure illustrated in a lower portion of (b) shows a procedure of calculating
          and outputting a symbol-offset for an output signal of the spreader and the randomizer.
          As illustrated in the math figure, the random symbol-offset generator may be operated
          for each pair-wise OFDM symbol. Accordingly, the length of an entire output offset
          may correspond to half of the length of an entire OFDM symbol.

[327]

[328]   FIG. 30 is a view illustrating logical composition of a 32K FFT mode random main-
          seed generator according to an embodiment of the present invention.

[329]   As described above, the 32K FFT mode random main-seed generator according to an
          embodiment of the present invention may include a random main interleaving-seed
          generator, a random symbol-offset generator, a memory index check, and a modulo
          operator.

[330]   FIG. 30 illustrates the logical composition of a 32K FFT mode random main-seed

generator formed by combining a random main interleaving-seed generator and a random symbol-offset generator. FIG. 34 illustrates an embodiment of the random main interleaving-seed generator including a 1 bit-spreader and an 14 bits-randomizer, and an embodiment of the random symbol-offset generator including a 2 bits-spreader and a 13 bits-randomizer. Details thereof have been described above and thus will be omitted here.

[331]   Hereinafter, a quasi-random interleaving seed generator for 32K FFT mode will be described.

[332]   As described above, the quasi-random interleaving seed generator according to an embodiment of the present invention may apply different interleaving seeds to respective OFDM symbols to acquire frequency diversity. The logical composition of the quasi-random interleaving seed generator may include a main quasi-random seed generator (Cj(K)) for interleaving cells in a single OFDM symbol and a random symbol-offset generator (

$$S_{\lfloor j/2 \rfloor}$$

) for changing a symbol offset.

[333]   The main quasi-random seed generator may generate the aforementioned random FI parameter. That is, the main quasi-random seed generator may generate seed for interleaving cells in a single OFDM symbol.

[334]   The main quasi-random seed generator according to an embodiment of the present invention may include a spreader and a randomizer and perform rendering a full randomness in frequency-domain. According to an embodiment of the present invention, in the case of 32K FFT mode, the main quasi-random seed generator may include a 3 bit spreader and a 9 bit-randomizer. The randomizer according to an embodiment of the present invention may a main-PRBS generator which is defined based on the 12-bit binary word sequence (or binary sequence).

[335]   The random symbol-offset generator according to an embodiment of the present invention may change a symbol offset for each OFDM symbol. That is, the random symbol-offset generator may generate the aforementioned symbol offset. The random symbol-offset generator according to an embodiment of the present invention may include k bits-spreader and (X-k) bits-randomizer and perform rendering a spreading as much as 2k cases, in time-domain. X may be differently set for respective FFT modes. According to an embodiment of the present invention, in the case of 32K FFT mode, a (15-k) bits-randomizer may be used. The (X-k) bits-randomizer according to an embodiment of the present invention may a sub-PRBS generator which is defined based on (15-k) bit binary word sequence (or binary sequence).

[336]   The main roles of the spreader and the randomizer are as follows.

[337]   Spreader: rendering a spreading effect to frequency interleaving (FI)

[338]   Randomizer: rendering a random effect to FI

[339]   FIG. 31 is a view illustrating an output signal of a time interleaver according to
another embodiment of the present invention.

[340]   The time interleaver according to an embodiment of the present invention may
perform a column-wise writing operation and a row-wise reading operation on each
FEC block with a size of 5, as illustrated in a left portion of FIG. 31. A right block of
FIG. 31 indicates an output signal of the time interleaver and the output signal is input
to a frequency interleaver according to an embodiment of the present invention.

[341]   Thus, one FEC block has a length of 5 in each FI block and agglomerate in a burst
form. Thus, in order to increase the robustness of a channel with strong burst error
properties, interleaving seed having high spreading properties as well as high
randomness is required. Accordingly, the aforementioned quasi-random interleaving
seed generator may be used.

[342]   FIG. 32 is a view illustrating a 32K FFT mode quasi-random main interleaving-seed
generator according to an embodiment of the present invention.

[343]   The 32K FFT mode quasi-random main interleaving-seed generator according to an
embodiment of the present invention may include a spreader (3-bit toggling), a
randomizer, a memory-index check, a random symbol-offset generator, and a modulo
operator. As described above, the random main-seed generator may include a spreader
and a randomizer. Hereinafter, an operation of each block will be described.

[344]   The spreader may be operated through an n-bit multiplexer and may maximize (or
minimize inter-cell correlation) inter-cell spreading. In the case of 32K FFT mode, the
spreader may use a look-up table that considers 3-bit.

[345]   The randomizer may be operated as a (15-n) bits-PN generator and may provide
randomness (or correlation properties). The randomizer according to an embodiment of
the present invention may include bit shuffling. The bit shuffling optimizes spreading
properties or random properties and is designed in consideration of Ndata. In the case
of 32K FFT mode, the bit shuffling may use a 9-bit PN generator, which can be
changed.

[346]   The memory-index check may not use seed when a memory-index generated by the
spreader and the randomizer is greater than Ndata and may repeatedly operate the
spreader and the randomizer to adjust the output memory-index such that the output
memory-index does not exceed Ndata.

[347]   The random symbol-offset generator may generate a symbol-offset for cyclic-shifting
main interleaving-seed generated by the main-interleaving seed generator for each
pair-wise OFDM symbol. A detailed operation has been described with regard to the

32K FFT mode random main-seed generator and is not described again here.

[348]   The modulo operator may be operated when a result value, obtained by adding a symbol-offset output by the random symbol-offset generator for each pair-wise OFDM symbol to the memory-index output by the memory-index check, exceeds Ndata. Locations of the illustrated memory-index check and modulo operator can be changed according to a designer's intention.

[349]   FIG. 33 is math figures representing operations of 32K FFT mode bit shuffling and 32K FFT mode quasi-random main interleaving-seed generator according to an embodiment of the present invention.

[350]   (a) illustrates a math figure representing an operation of the 32K FFT mode bit shuffling and (b) illustrates a math figure representing an operation of the 32K FFT mode quasi-random main interleaving-seed generator.

[351]   As illustrated in (a), the 32K FFT mode bit shuffling may mix bits of registers of a PN generator during calculation of a memory-index.

[352]   A math figure illustrated in an upper portion of (b) shows initial value setting and primitive polynomial of a randomizer. In this case, the primitive polynomial may be 12th primitive polynomial and the initial value may be changed by arbitrary values.

[353]   A math figure illustrated in a lower portion of (b) shows a procedure of calculating and outputting main-interleaving seed for an output signal of the spreader and the randomizer. As illustrated in the math figure, one random symbol-offset may be applied to each pair-wise OFDM symbol in the same way.

[354]   FIG. 34 is a view illustrating logical composition of a 32K FFT mode quasi-random main interleaving-seed generator according to an embodiment of the present invention.

[355]   As described above, the 32K FFT mode quasi-random main interleaving-seed generator according to an embodiment of the present invention may include a quasi-random main interleaving-seed generator, a random symbol-offset generator, a memory index check, and a modulo operator.

[356]   FIG. 34 illustrates the logical composition of a 32K FFT mode quasi-random main interleaving-seed generator formed by combining a quasi-random main interleaving-seed generator and a random symbol-offset generator. FIG. 34 illustrates an embodiment of the random main interleaving-seed generator including a 3 bit-spreader and a 12 bits-randomizer and an embodiment of the random symbol-offset generator including a 2 bits-spreader and a 13 bits-randomizer. Details thereof have been described above and thus will be omitted here.

[357]   FIG. 35 is a view illustrating single-memory deinterleaving for input sequential OFDM symbols.

[358]   FIG. 35 is a view illustrating concept of a broadcast signal receiving apparatus or a frequency deinterleaver thereof, for applying interleaving seed used in a broadcast

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signal transmitting apparatus (or a frequency interleaver) to each pair-wise OFDM symbol to perform deinterleaving.

[359]   As described above, the broadcast signal receiving apparatus according to an embodiment of the present invention may perform an inverse procedure of the aforementioned frequency interleaving procedure using a single memory. FIG. 35 illustrates an operation of the broadcast signal receiving apparatus for processing single-memory deinterleaving (FDI) for input sequential OFDM symbols.

[360]   The broadcast signal receiving apparatus according to an embodiment of the present invention may perform an inverse procedure of the aforementioned operation of a frequency interleaver. Thus, deinterleaving seeds correspond to the aforementioned interleaving seed.

[361]   FIG. 36 is a flowchart illustrating a method for transmitting broadcast signals according to an embodiment of the present invention.

[362]   The apparatus for transmitting broadcast signals according to an embodiment of the present invention can encode service data (S36000). As described above, service data is transmitted through a data pipe which is a logical channel in the physical layer that carries service data or related metadata, which may carry one or multiple service(s) or service component(s). Data carried on a data pipe can be referred to as the DP data or the service data. The detailed process of step S36000 is as described in FIG. 1 or 5.

[363]   The apparatus for transmitting broadcast signals according to an embodiment of the present invention can build at least one signal frame including the encoded service data (S36010). The detailed process of this step is as described in FIG. 6.

[364]   Then, the apparatus for transmitting broadcast signals according to an embodiment of the present invention can map the encoded service data into OFDM symbols of the signal frame and frequency interleave the mapped service data. As above described, the basic function of the cell mapper 3700 is to map data cells for each of the DPs, PLS data, if any, into arrays of active OFDM cells corresponding to each of the OFDM symbols within a signal frame. Then, the block interleaver 6200 may operate on a single OFDM symbol basis, provide frequency diversity by randomly interleaving the cells received from the cell mapper 3700. The purpose of the block interleaver 6200 in the present invention, which operates on a single OFDM symbol, is to provide frequency diversity by randomly interleaving data cells received from the frame structure module 1200. In order to get maximum interleaving gain in a single signal frame (or frame), a different interleaving-seed is used for every OFDM symbol pair comprised of two sequential OFDM symbols. The detailed process of the frequency interleaving is as described in FIG. 16 to 35.

[365]   Subsequently, the apparatus for transmitting broadcast signals according to an embodiment of the present invention can modulate data in the built at least one signal

frame by an OFDM (Orthogonal Frequency Division Multiplexing) scheme (S36020). The detailed process of this step is as described in FIG. 1 or 7.

[366]   The apparatus for transmitting broadcast signals according to an embodiment of the present invention can transmit the broadcast signals including the modulated data (S36030). The detailed process of this step is as described in FIG. 1 or 7.

[367]   FIG. 37 is a flowchart illustrating a method for receiving broadcast signals according to an embodiment of the present invention.

[368]   The flowchart shown in FIG. 37 corresponds to a reverse process of the broadcast signal transmission method according to an embodiment of the present invention, described with reference to FIG. 36.

[369]   The apparatus for receiving broadcast signals according to an embodiment of the present invention can receive broadcast signals (S37000). The apparatus for receiving broadcast signals according to an embodiment of the present invention can demodulate the received broadcast signals using an OFDM (Othogonal Frequency Division Multiplexing) scheme (S37010). Details are as described in FIG. 8 or 9.

[370]   The apparatus for receiving broadcast signals according to an embodiment of the present invention can parse at least one signal frame from the demodulated broadcast signals (S37020). Details are as described in FIG. 8 or 10. In this case, the apparatus for receiving broadcast signals according to an embodiment of the present invention can perform frequency de-interleaving corresponds to a reverse process of the frequency interleaving as shown in the above. The detailed process of the frequency interleaving is as described in FIG. 16 to 35.

[371]   Subsequently, the apparatus for receiving broadcast signals according to an embodiment of the present invention can decode data in the parsed at least one signal frame to output service data (S37030). Details are as described in FIG. 8 or 11 and FIG. 15.

[372]   As described above, service data is transmitted through a data pipe which is a logical channel in the physical layer that carries service data or related metadata, which may carry one or multiple service(s) or service component(s). Data carried on a data pipe can be referred to as the DP data or the service data.

[373]   It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Mode for the Invention

[374]   Various embodiments have been described in the best mode for carrying out the

invention.

Industrial Applicability

[375]   The present invention is available in a series of broadcast signal provision fields.

[376]   It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

[Claim 1]   A method for transmitting broadcast signals, the method comprising:

encoding service data;

building at least one signal frame including the encoded service data, wherein the at least one signal frame includes a plurality of OFDM symbols;

modulating data in the built at least one signal frame by an OFDM (Orthogonal Frequency Division Multiplex) scheme; and

transmitting the broadcast signals having the modulated data.

[Claim 2]   The method of claim 1, wherein the method further includes:

frequency interleaving data in the at least one signal frame by using a different interleaving-seed which is used for every OFDM symbol pair comprised of two sequential OFDM symbols.

[Claim 3]   An apparatus for transmitting broadcast signals, the apparatus comprising:

an encoder for encoding service data;

a mapper for mapping the encoded service data into a plurality of OFDM symbols to build at least one signal frame;

a modulator for modulating data in the built at least one signal frame by an OFDM (Orthogonal Frequency Division Multiplex) scheme; and

a transmitter for transmitting the broadcast signals having the modulated data.

[Claim 4]   The apparatus of claim 7, wherein a frequency interleaver for frequency interleaving data in the at least one signal frame by using a different interleaving-seed which is used for every OFDM symbol pair comprised of two sequential OFDM symbols.

[Claim 5]   A method for receiving broadcast signals, the method comprising:

receiving the broadcast signals;

demodulating the received broadcast signals by an OFDM (Orthogonal Frequency Division Multiplex) scheme;

parsing at least one signal frame from the demodulated broadcast signals; and

decoding data in the parsed at least one signal frame to output service data.

[Claim 6]   The method of claim 5, wherein the method includes:

frequency de-interleaving the demodulated broadcast signals by using a different de-interleaving-seed which is used for every OFDM symbol

pair comprised of two sequential OFDM symbols.

[Claim 7]   An apparatus for receiving broadcast signals, the apparatus comprising:

a receiver for receiving the broadcast signals;

a demodulator for demodulating the received broadcast signals by an OFDM (Orthogonal Frequency Division Multiplex) scheme;

a demapper for demapping service data from at least one signal frame in the demodulated broadcast signals; and

a decoder for decoding the service data in the at least one signal frame.

[Claim 8]   The apparatus of claim 7, the apparatus further include;

a frequency de-interleaver for frequency de-interleaving the demodulated broadcast signals by using a different de-interleaving-seed which is used for every OFDM symbol pair comprised of two sequential OFDM symbols.

[Fig. 1]
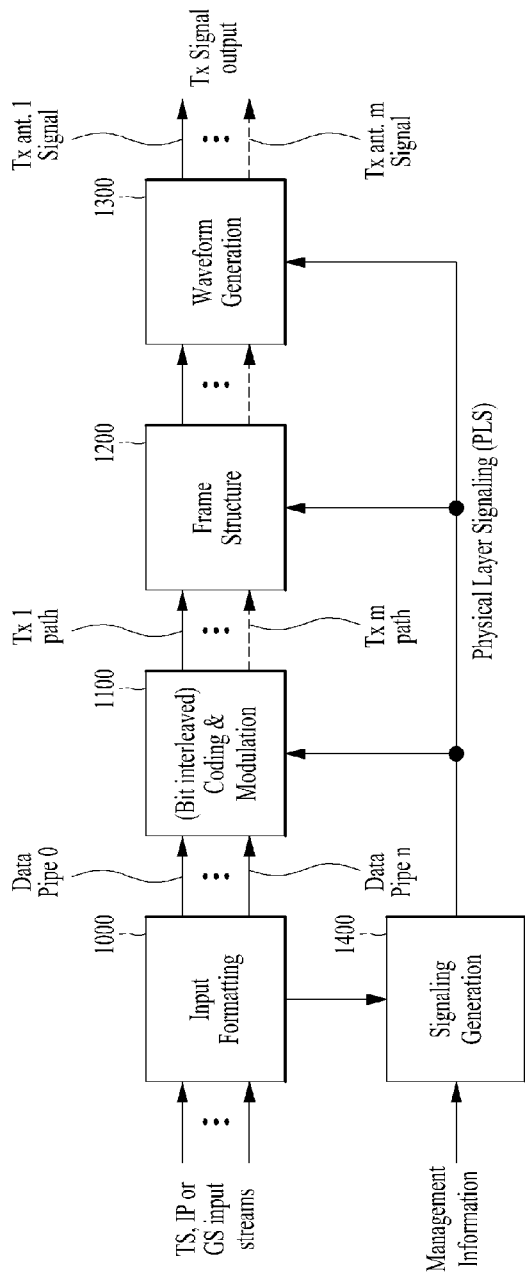
[Fig. 2]
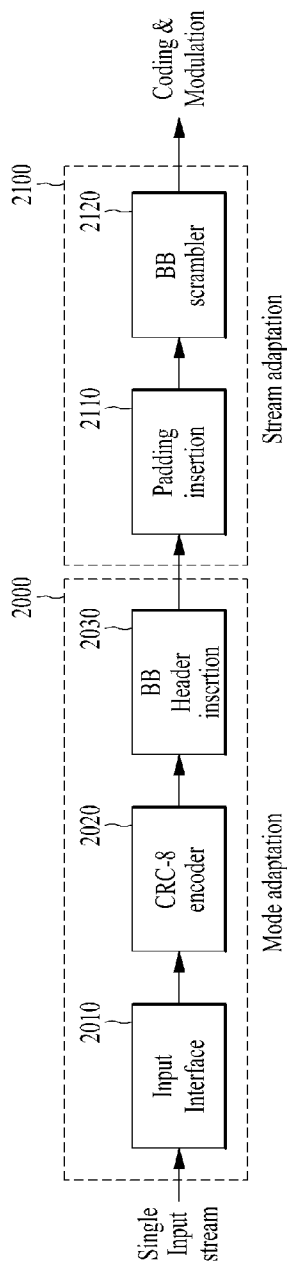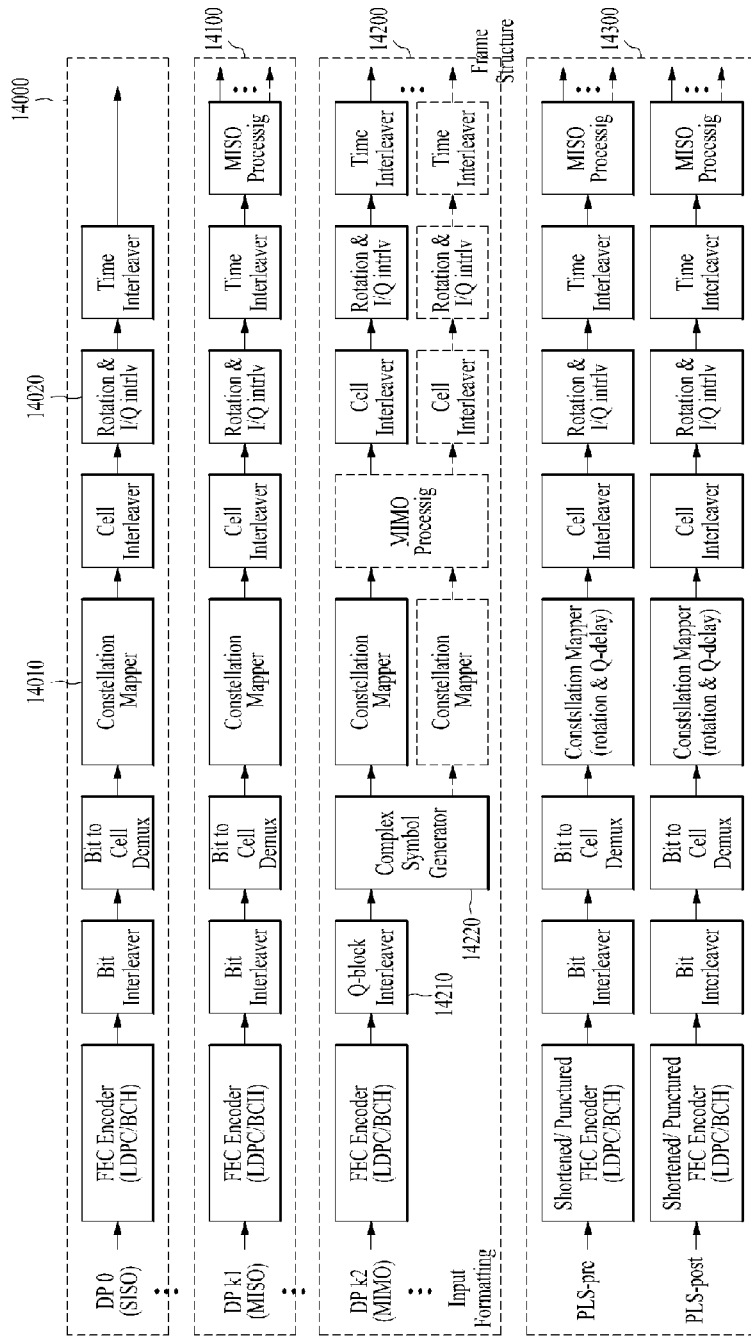
[Fig. 3]
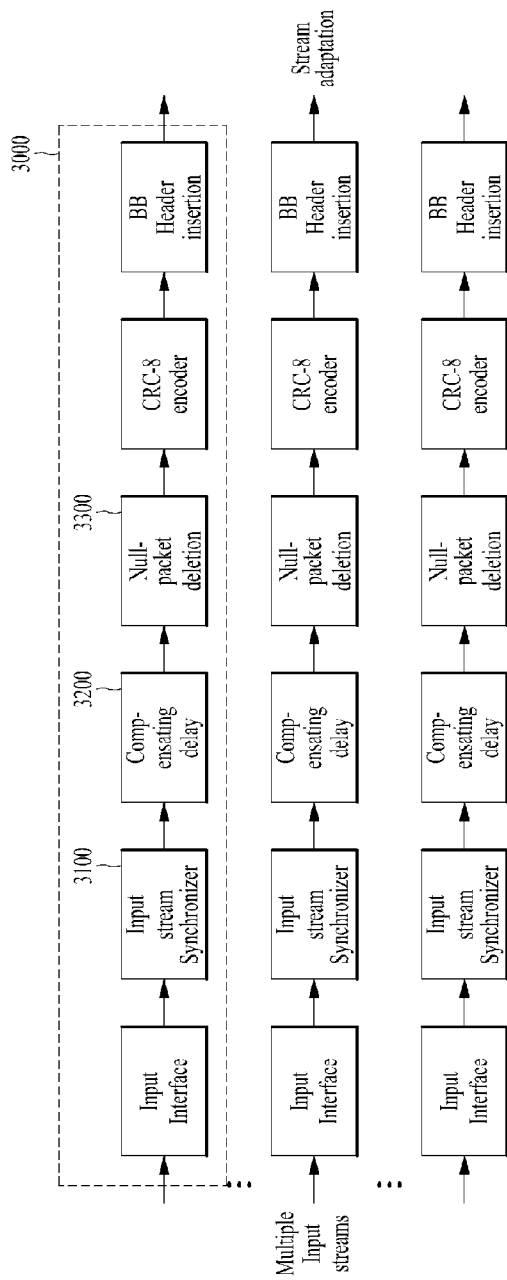
[Fig. 4]
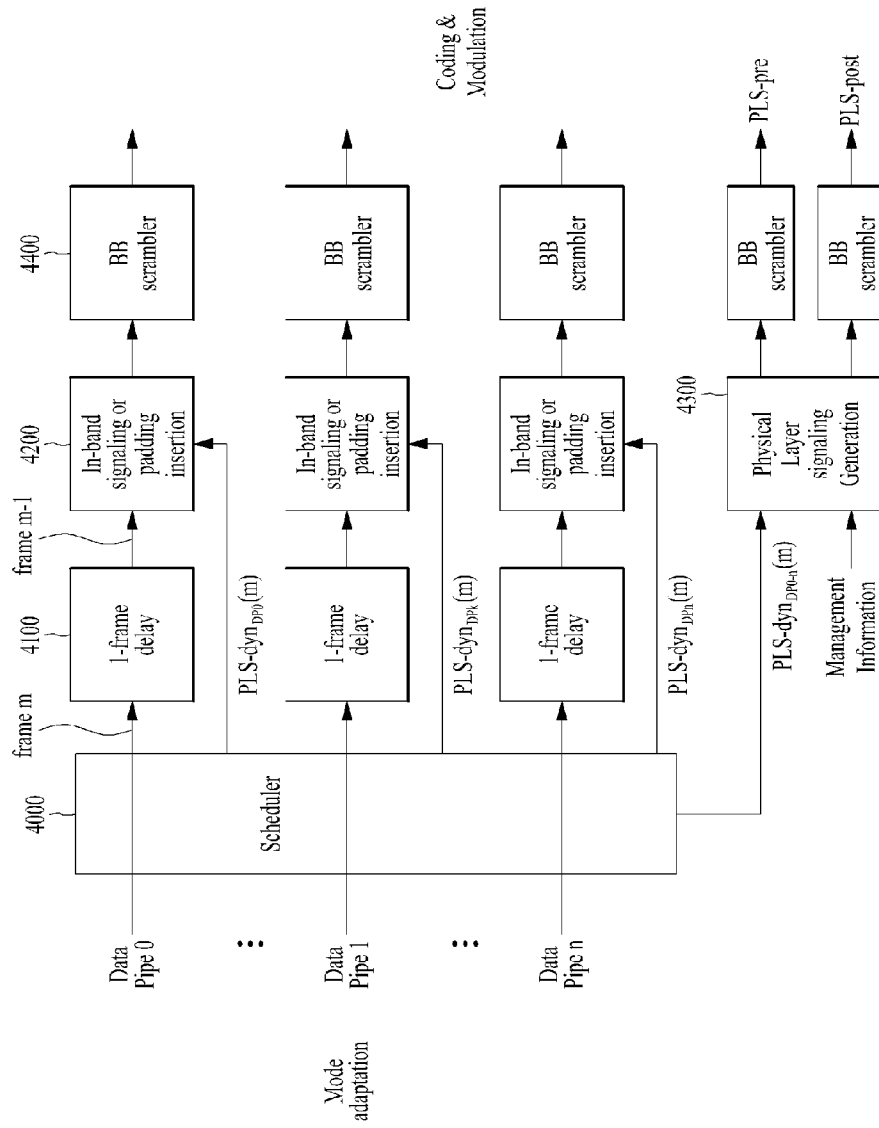
[Fig. 5]
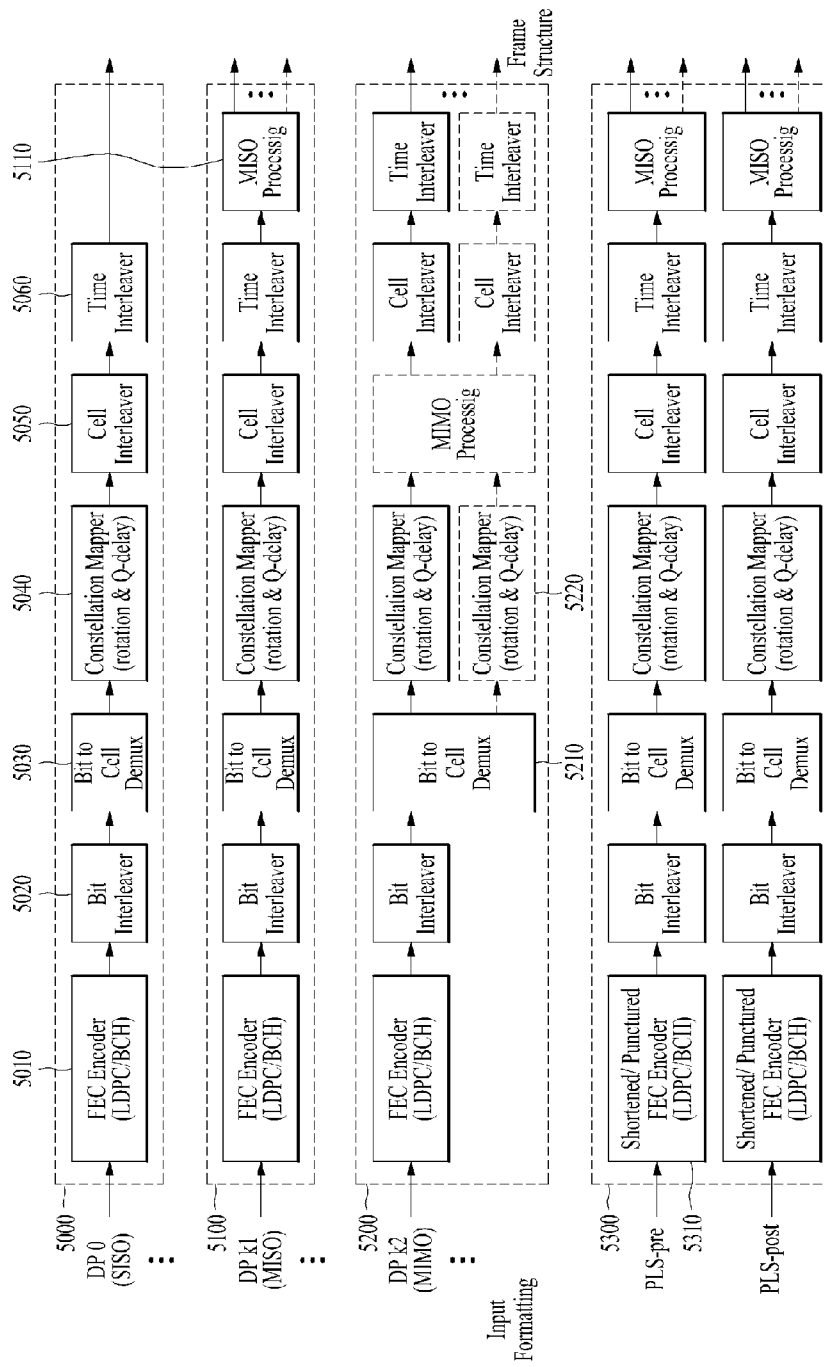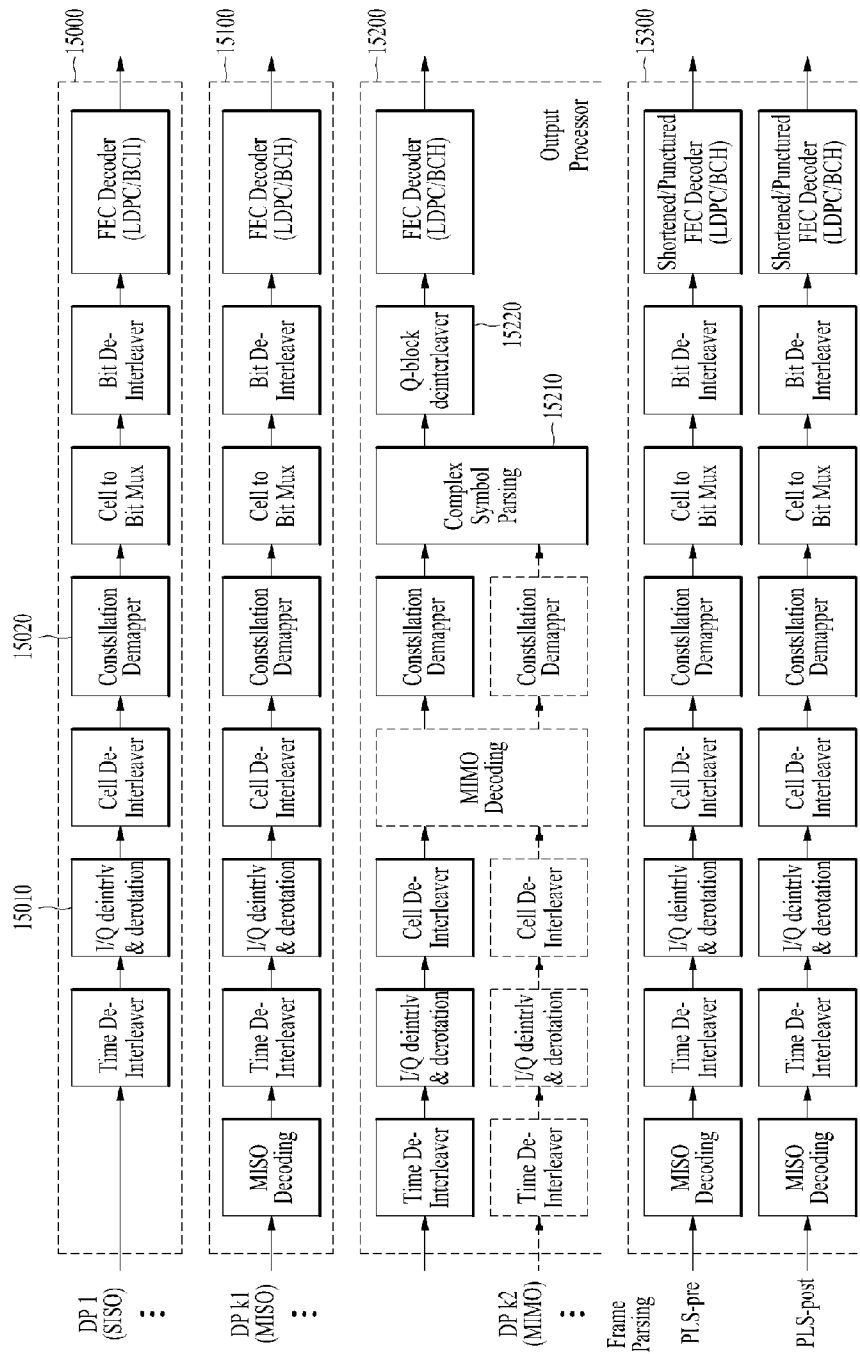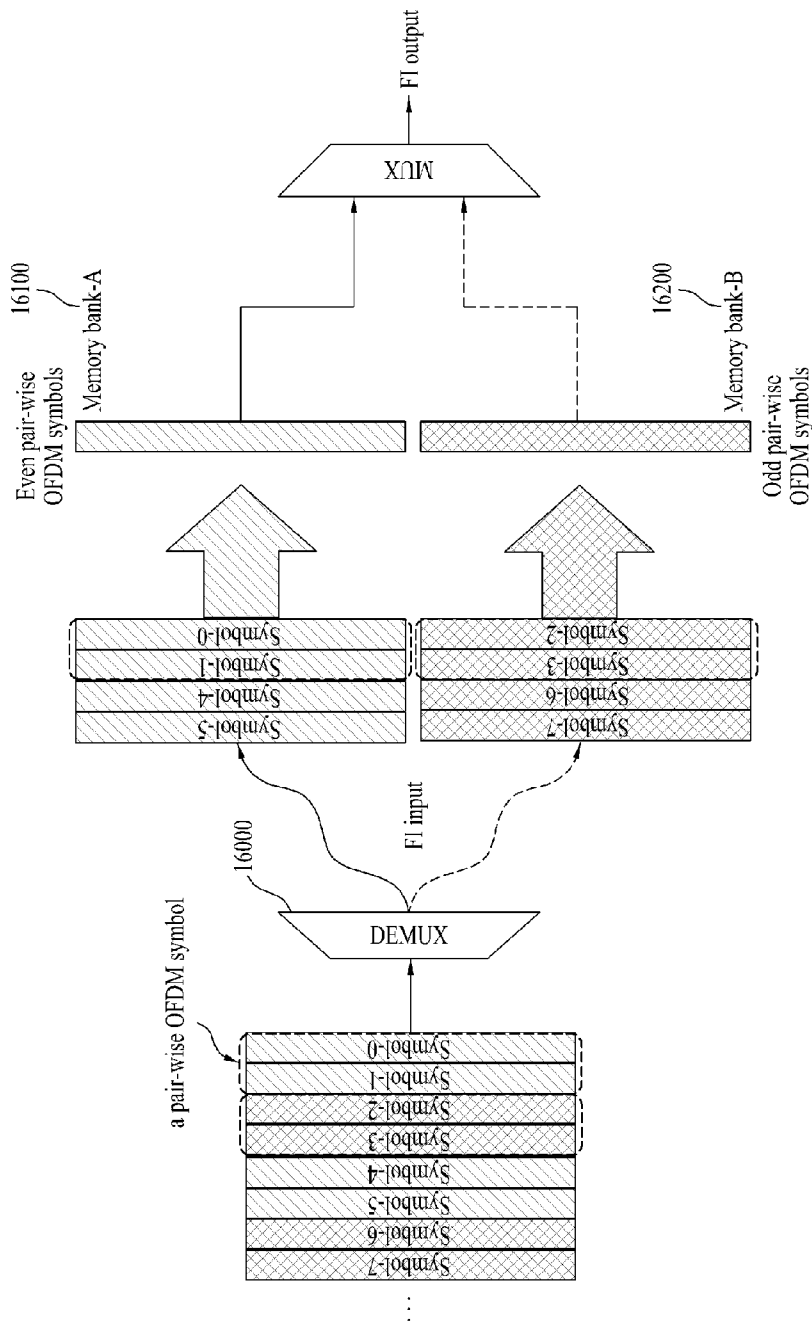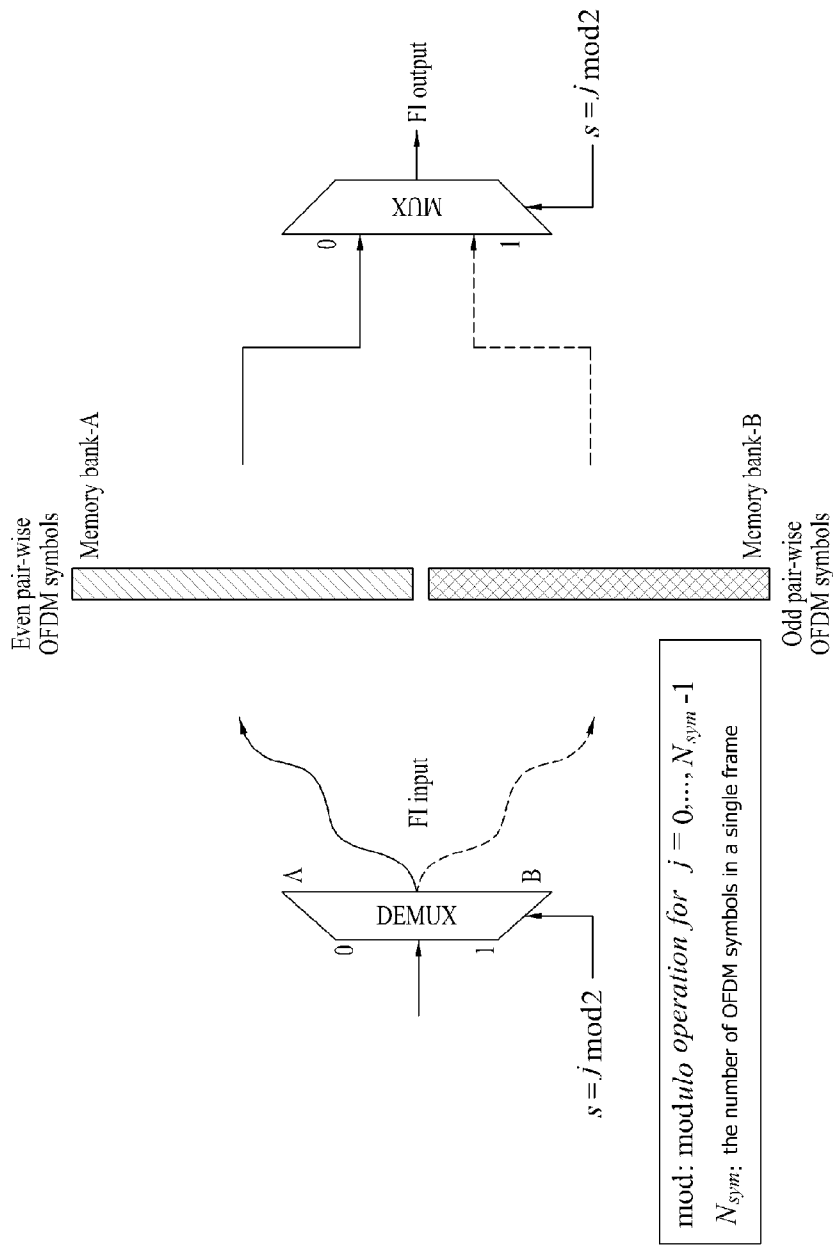
[Fig. 6]
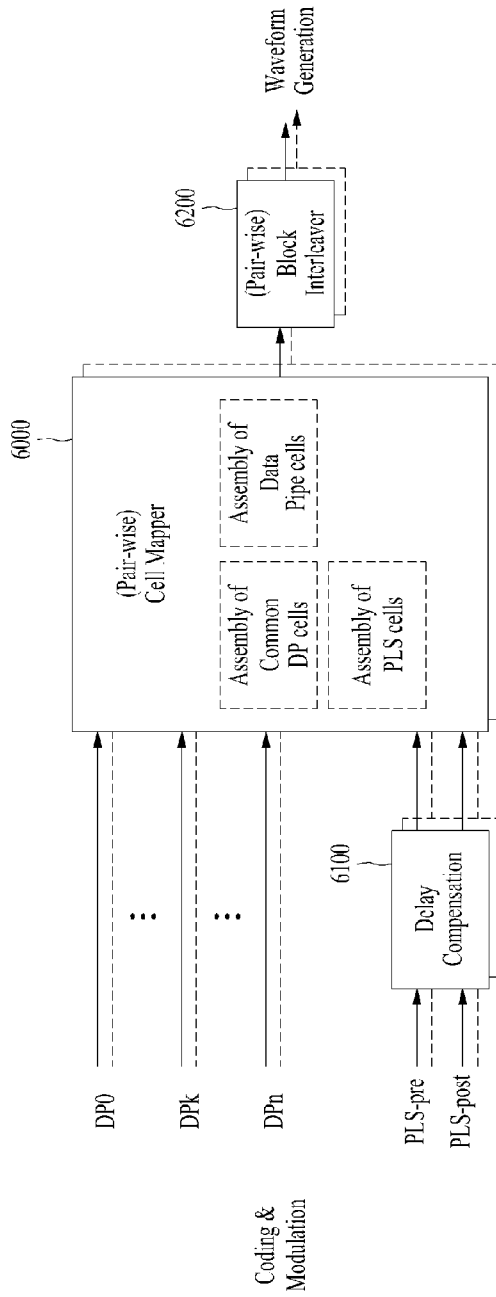
[Fig. 7]
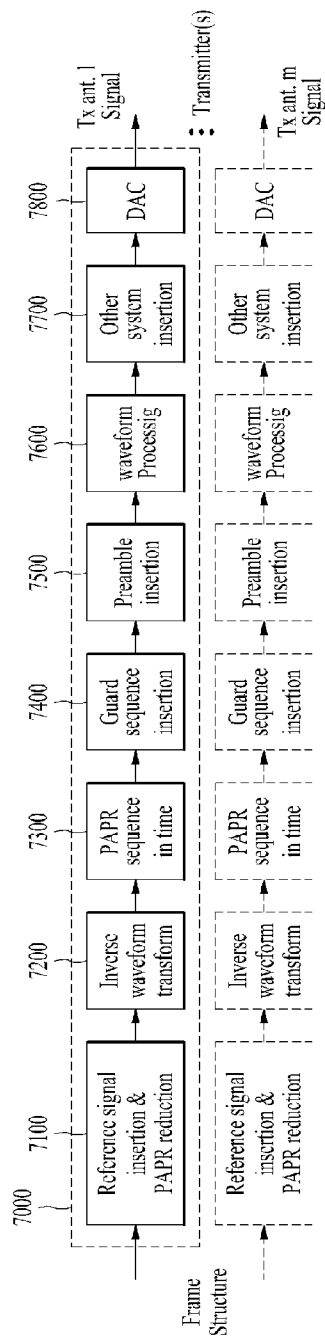
[Fig. 8]
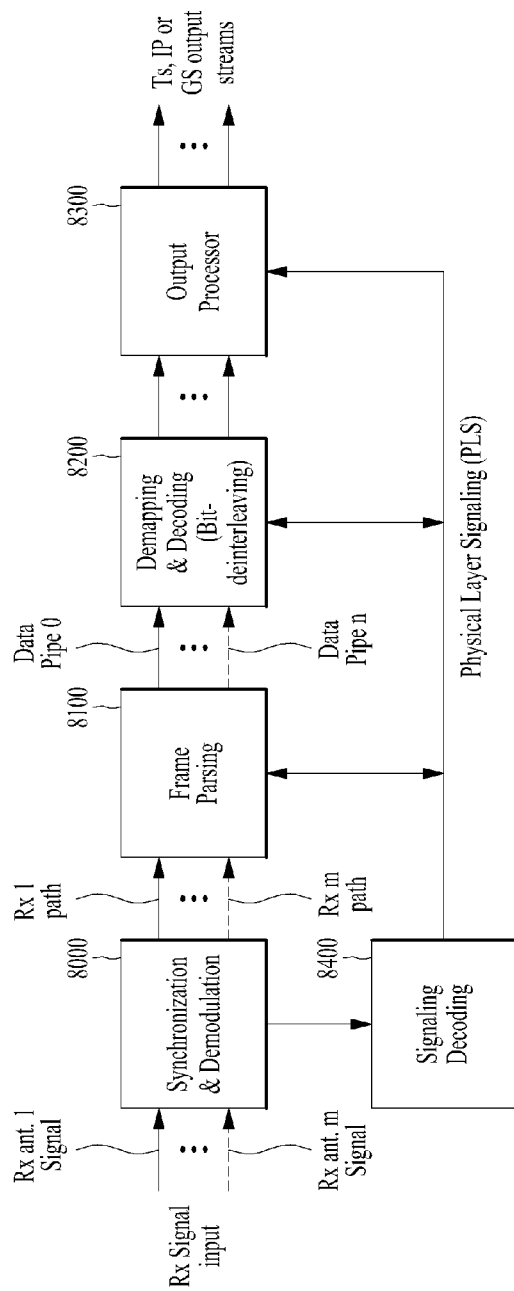
[Fig. 9]
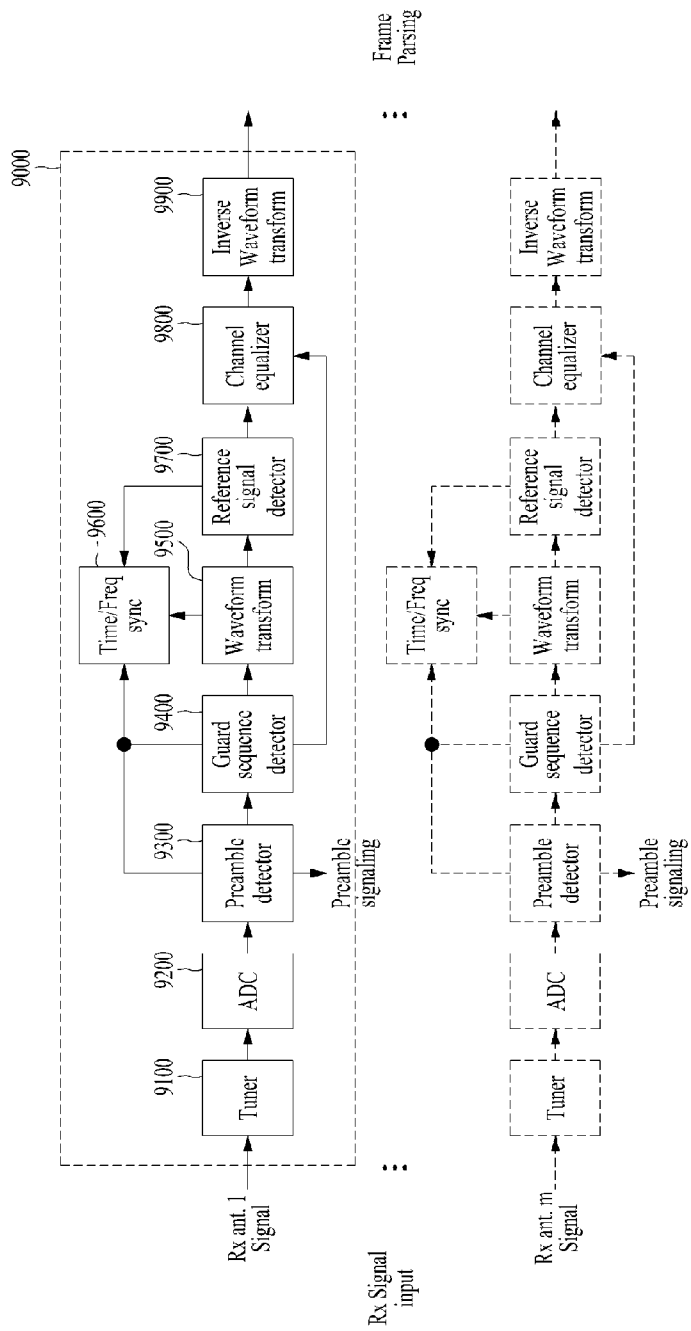
[Fig. 10]
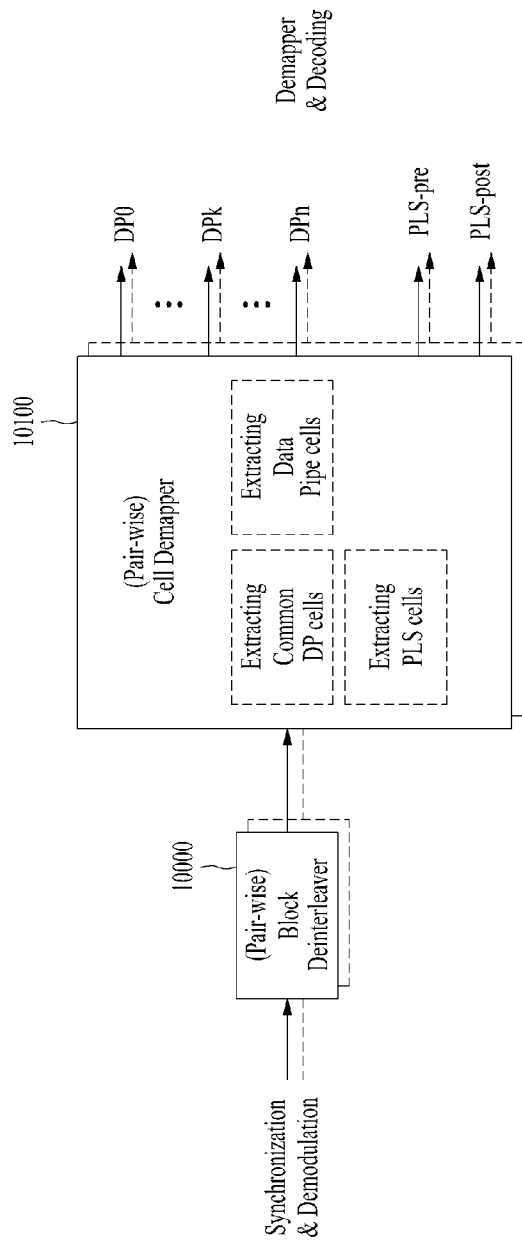
[Fig. 11]
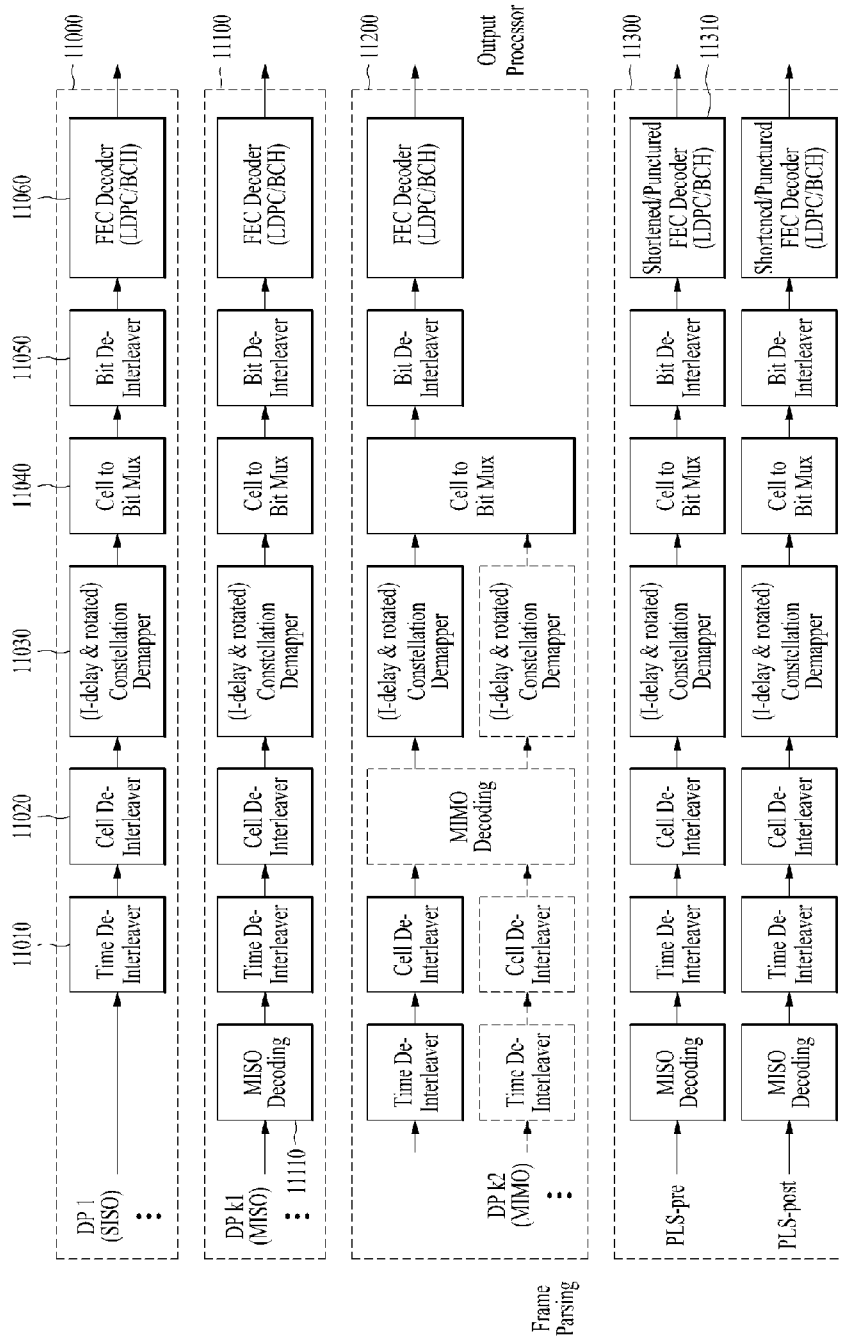
[Fig. 12]
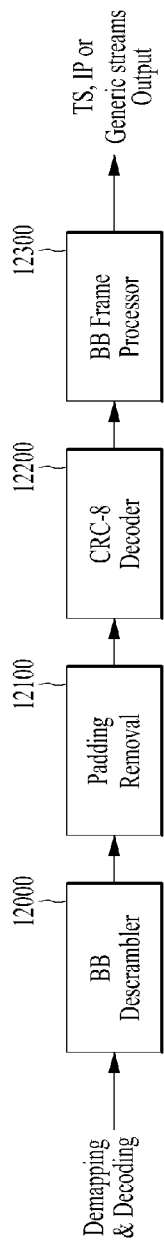
[Fig. 13]

[Fig. 14]

[Fig. 15]
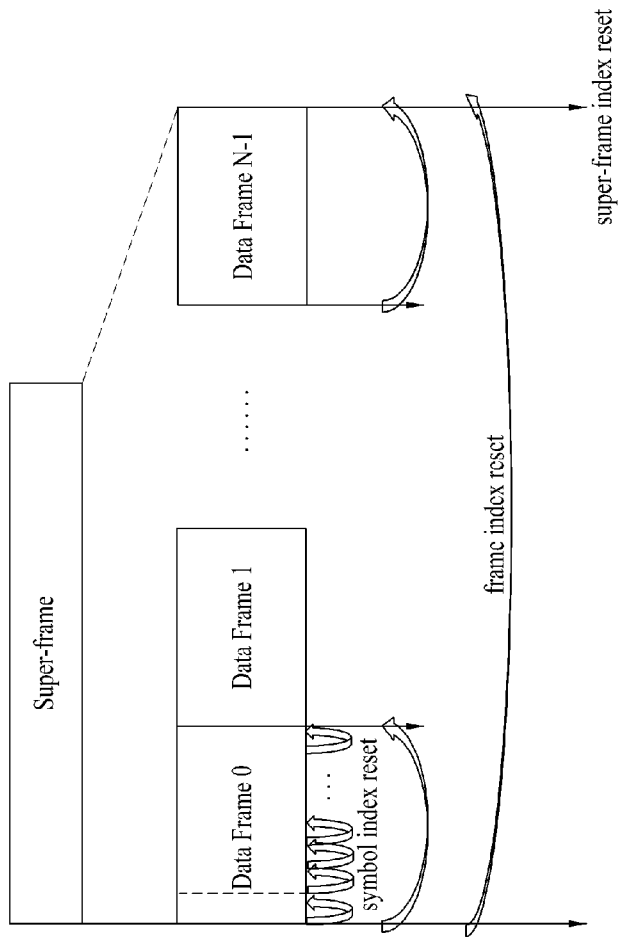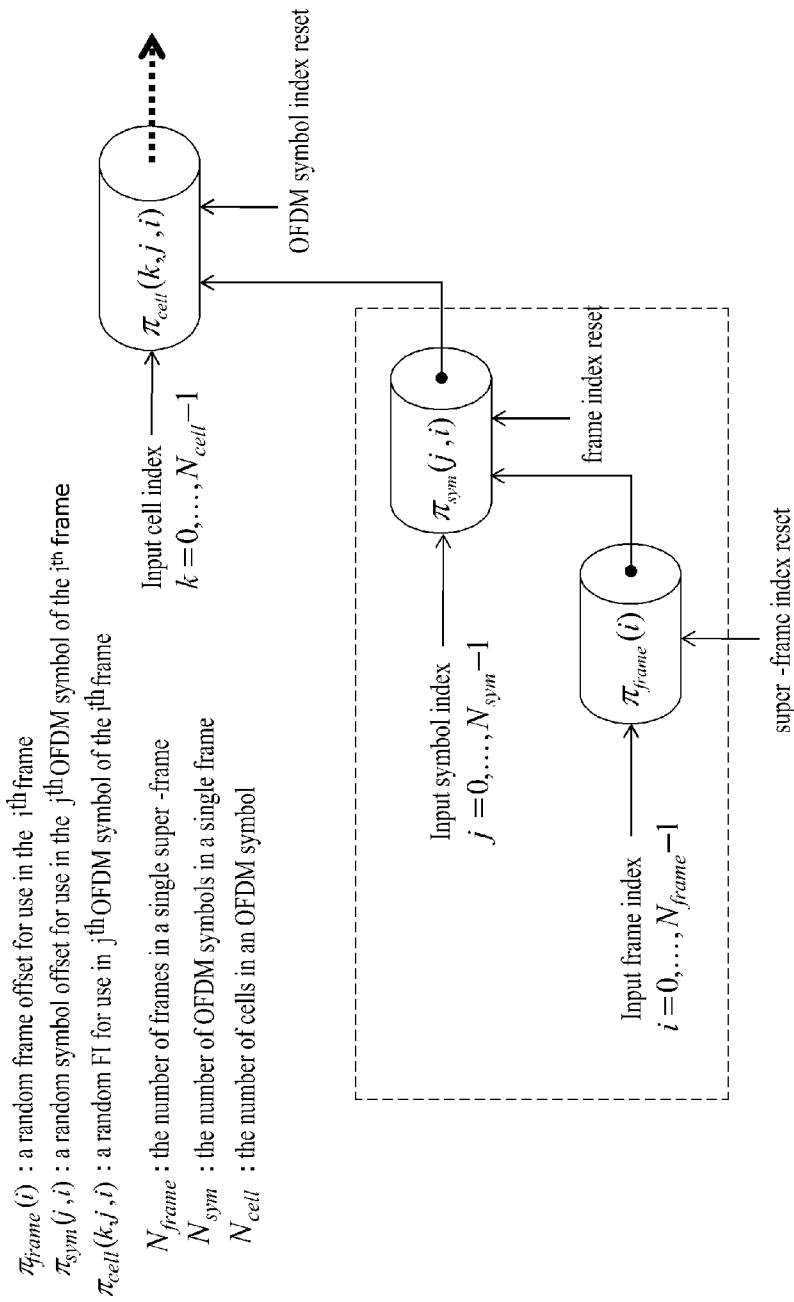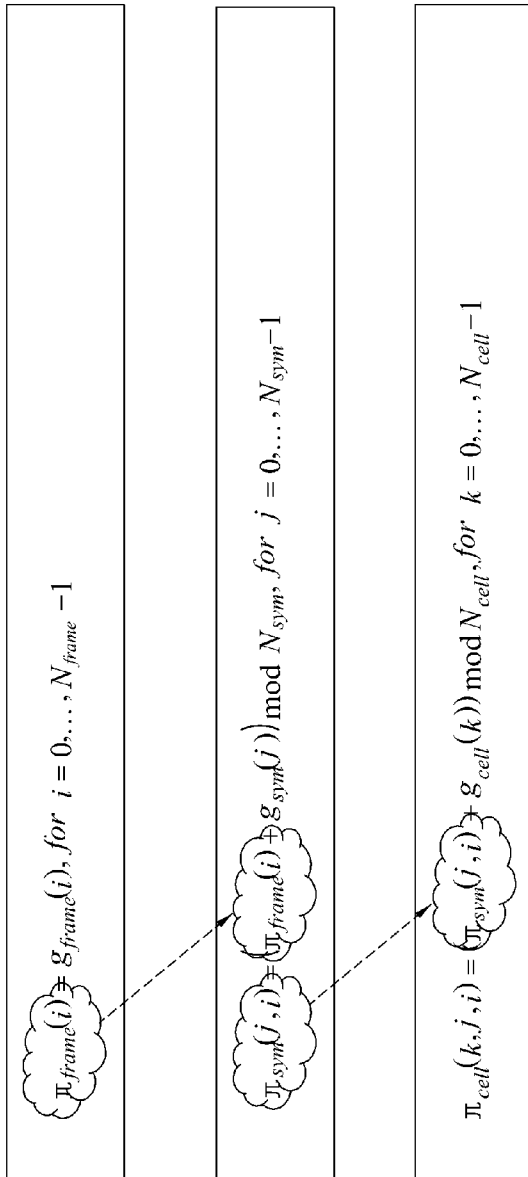
[Fig. 16]

[Fig. 17]

mod: modulo operation for $j = 0, ..., N_{sym} - 1$

N_{sym}: the number of OFDM symbols in a single frame

[Fig. 18]

[Fig. 19]

$\pi_{frame}(i)$: a random frame offset for use in the ith frame

$\pi_{sym}(j,i)$: a random symbol offset for use in the jth OFDM symbol of the ith frame

$\pi_{cell}(k,j,i)$: a random FI for use in j^{th} OFDM symbol of the ith frame

N_{frame} : the number of frames in a single super -frame

N_{sym} : the number of OFDM symbols in a single frame

N_{cell} : the number of cells in an OFDM symbol

[Fig. 20]

$$\pi_{frame}(i) = g_{frame}(i), \; for \; i = 0,\ldots, N_{frame} - 1$$

$$\pi_{sym}(j, i) = (\pi_{frame}(i) + g_{sym}(j)) \bmod N_{sym}, \; for \; j = 0,\ldots, N_{sym} - 1$$

$$\pi_{cell}(k, j, i) = (\pi_{sym}(j, i) + g_{cell}(k)) \bmod N_{cell}, \; for \; k = 0,\ldots, N_{cell} - 1$$
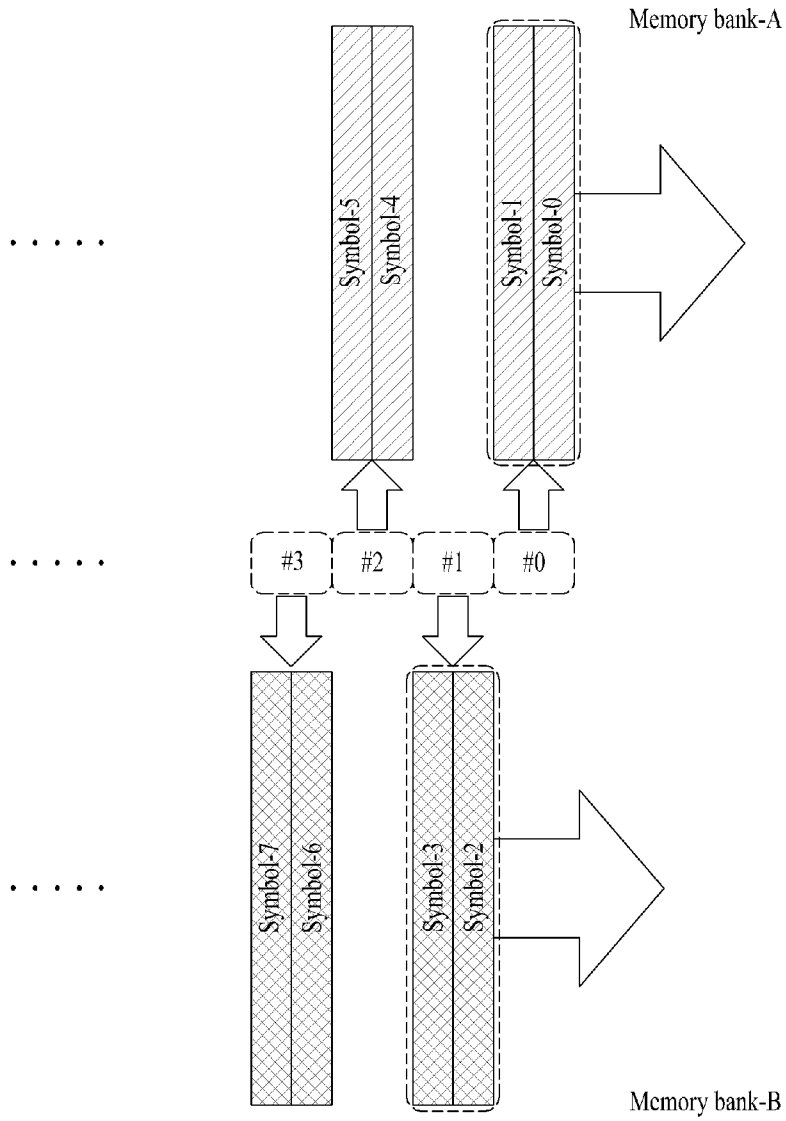
g_{frame} : a random frame offset generator for used in frame interleaver
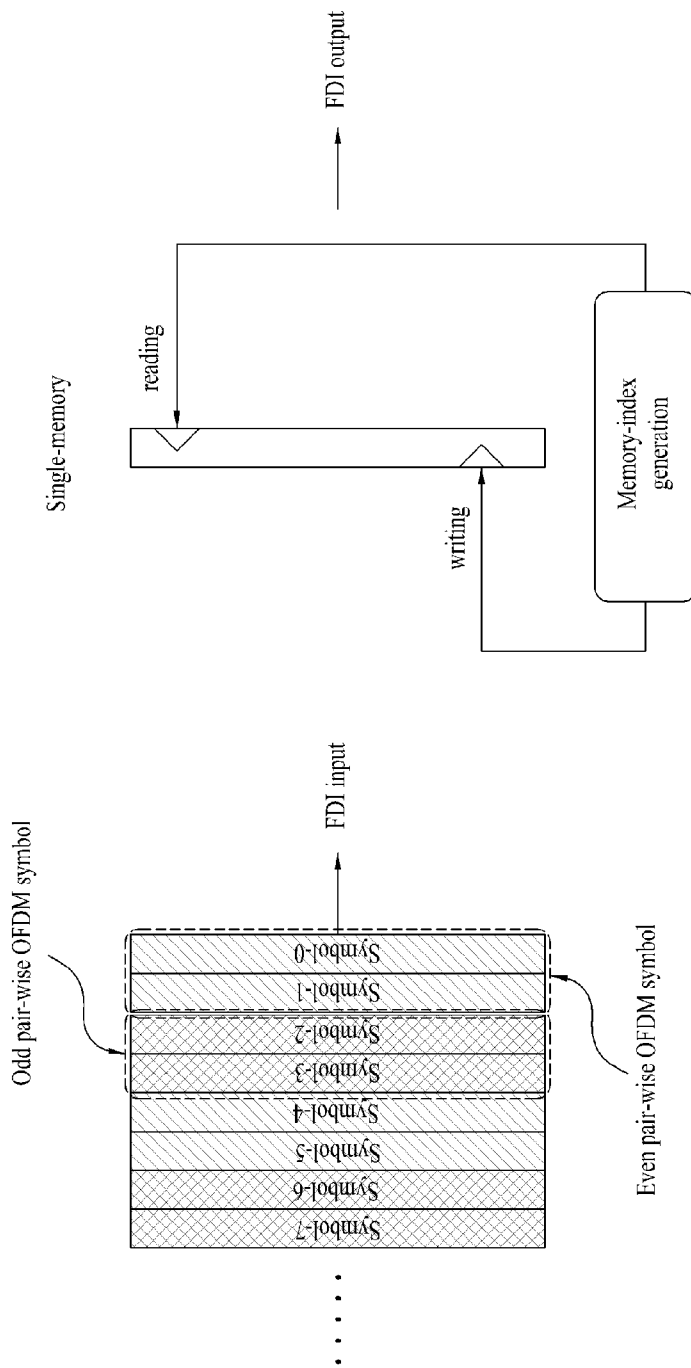
g_{sym} : a random symbol offset generator for used in symbol interleaver

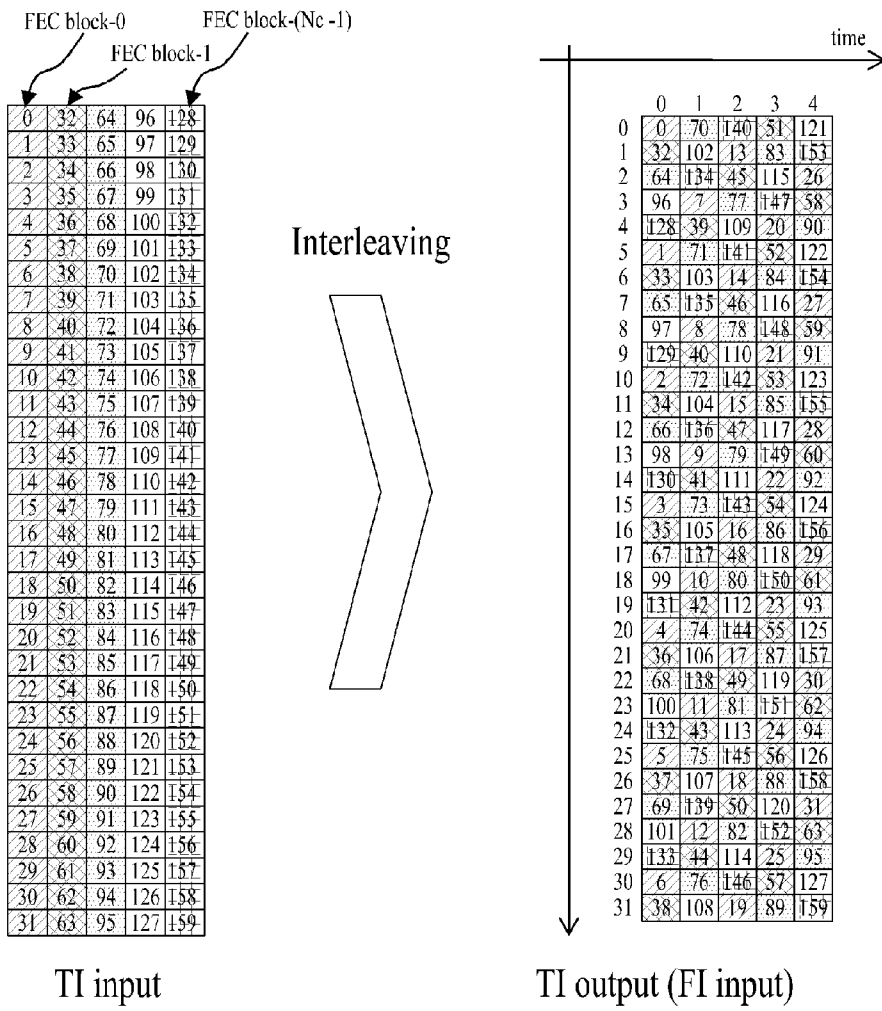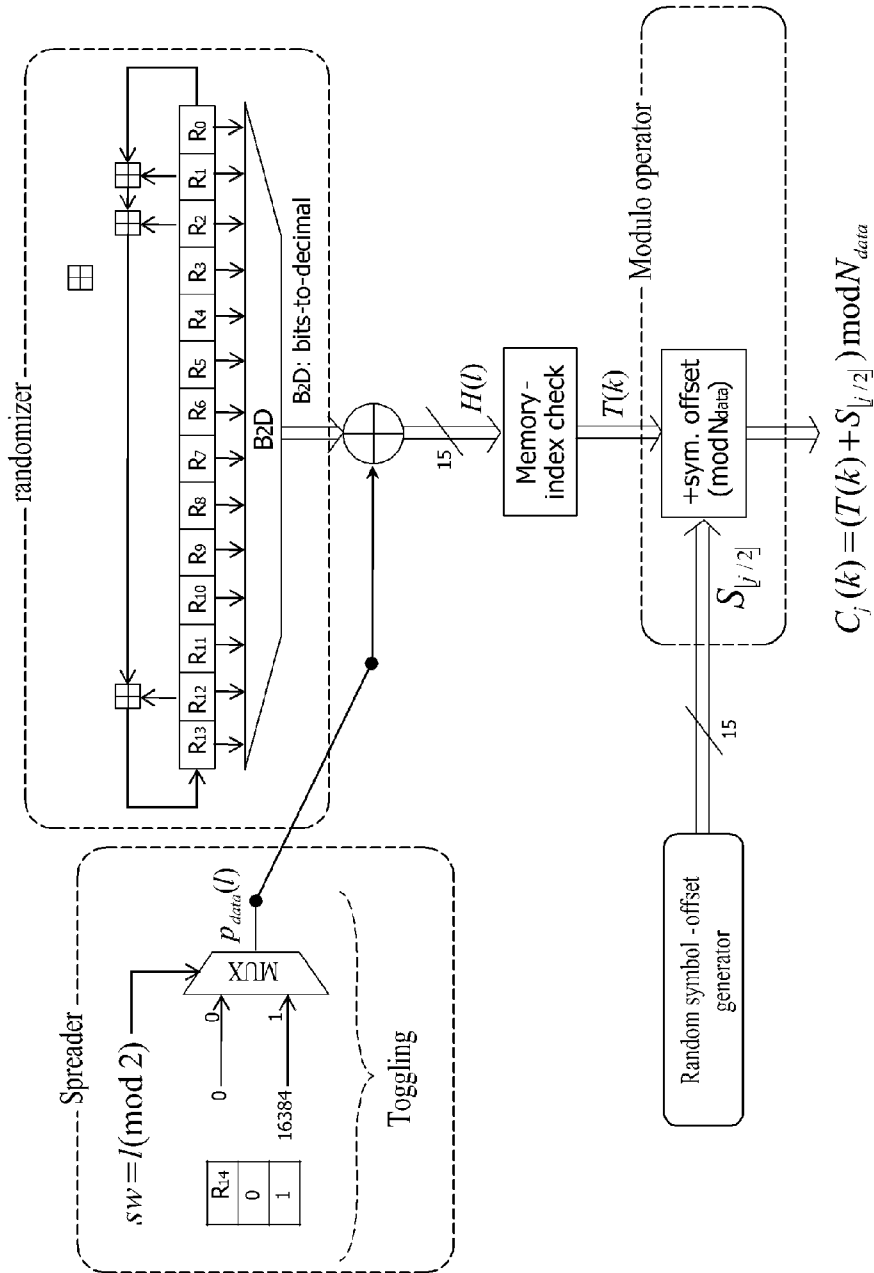g_{cell} : a random generator for used in cell interleaver

[Fig. 21]

[Fig. 22]

[Fig. 23]

FEC block-0   FEC block-(Nc -1)
        FEC block-1

TI input

Interleaving

TI output (FI input)

[Fig. 24]

$$C_j(k) = (T(k) + S_{\lfloor j/2 \rfloor}) \bmod N_{data}$$

[Fig. 25]

The associated 14th polynomial, $f(x)=1+x^2+x^{12}+x^{13}+x^{14}$

Operation of the PN generator for $0 \leq 1 < N_{max} (32768)$

$$0 \leq l < 2$$

$$R^l_{[13,12,11,10,9,8,7,6,5,4,3,2,1,0]} = 0,0,0,0,0,0,0,0,0,0,0,0,0,0$$

$$l = 2$$

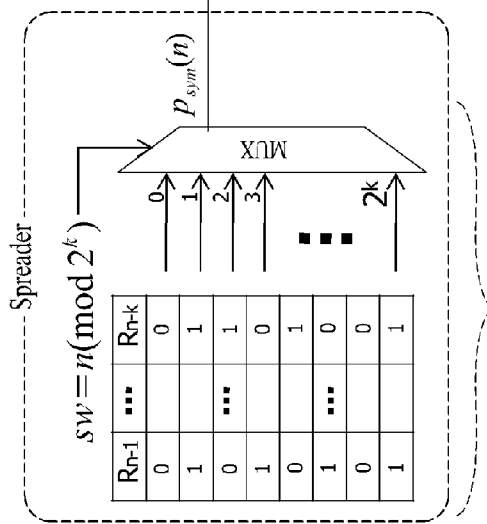$$R^2_{[13,12,11,10,9,8,7,6,5,4,3,2,1,0]} = 0,0,1,0,0,0,0,0,0,0,0,1,1,1$$
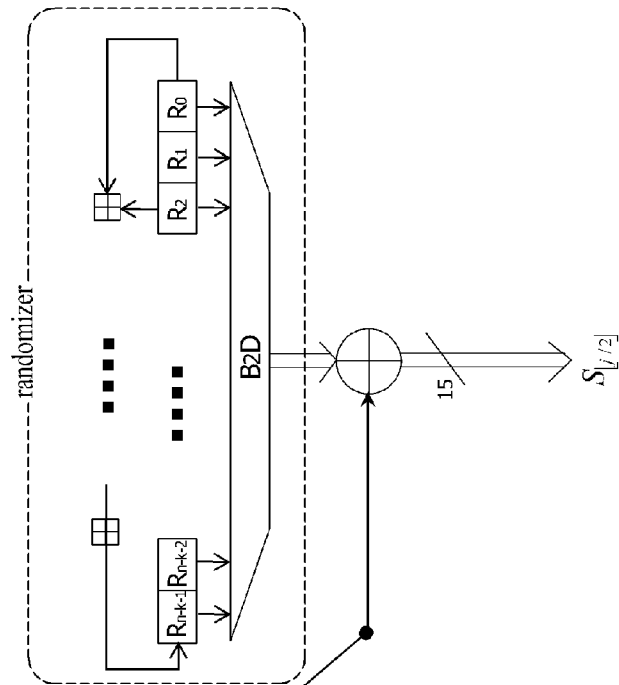
$$2 < l < N_{max}$$

$$R^l_{[11,10,9,8,7,6,5,4,3,2,1,0]} = R^{l-1}_{[13,12,11,10,9,8,7,6,5,4,3,2,1]}$$

$$R^l_{13} = R^{l-1}_0 \oplus R^{l-1}_1 \oplus R^{l-1}_2 \oplus R^{l-1}_{12}$$

$$k = 0;$$

$$for \quad (l=0; l < N_{max}; l = l+1)$$

$$\{$$

$$\quad H(l) = P_{data}(l) + \sum_{n=0}^{12} (2^n \times R^l_n);$$

$$\quad if \ H(l) < N_{data}$$

$$\quad\quad \{$$

$$\quad\quad\quad T(k) = H(l);$$

$$\quad\quad\quad C_j(k) = (T(k) + S_{\lfloor j/2 \rfloor}) \bmod N_{data};$$

$$\quad\quad\quad k = k+1;$$

$$\quad\quad \}$$

$$\}$$

[Fig. 26]

[Fig. 27]

The associated 15th primitive polynomial, $f(x)=1+x^{14}+x^{15}$
Operation of the PN generator for $0 \leq n < \left\lfloor N_{sym}/2 \right\rfloor$

$n=0$

$R^0_{[14,13,12,11,10,9,8,7,6,5,4,3,2,1,0]} = 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0$

$n=1$

$R^1_{[14,13,12,11,10,9,8,7,6,5,4,3,2,1,0]} = 1,1,1,1,1,1,1,1,1,1,1,1,1,1,1$

$1 < n < \left\lfloor N_{sym}/2 \right\rfloor$

$R^n_{[13,12,11,10,9,8,7,6,5,4,3,2,1,0]} = R^{n-1}_{[14,13,12,11,10,9,8,7,6,5,4,3,2,1]}$

$R^n_{14} = R^{n-1}_0 \oplus R^{n-1}_1$

(a)

$for \ (n=0; n < \left\lfloor \dfrac{N_{sym}}{2} \right\rfloor ; n=n+1)$

$\{$

$\quad S_n = \sum_{m=0}^{14} (2^m \times R^n_m);$

$\}$

(b)

[Fig. 28]

(a)

(b)

[Fig. 29]

(a)

(b)

The associated 13th primitive polynomial, $f(x)=1+x^2+x^4+x^8+x^9+x^{12}+x^{13}$

Operation of the PN generator for $0 \le n < \lfloor Nsym/2 \rfloor$

[Fig. 30]

$$C_j(k) = (T(k) + S\rfloor_{\lfloor j/2 \rfloor}) \bmod N_{data}$$
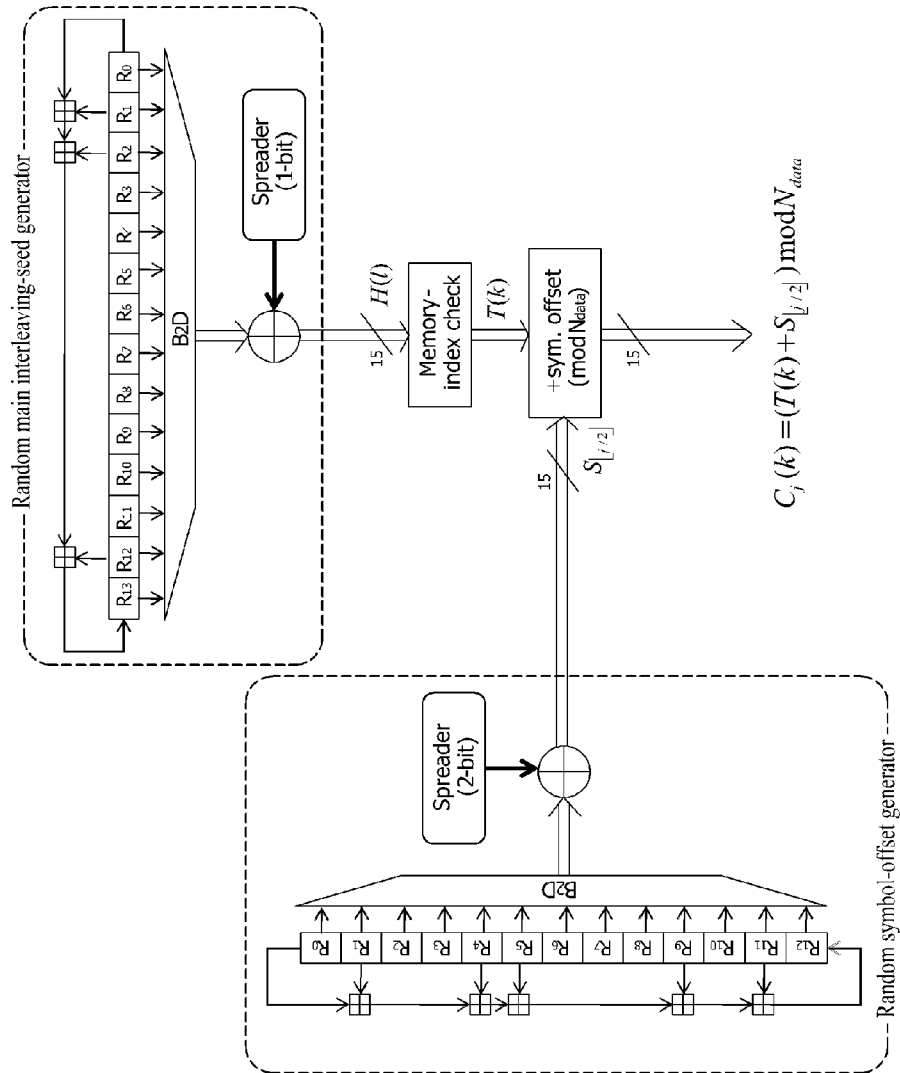
[Fig. 31]
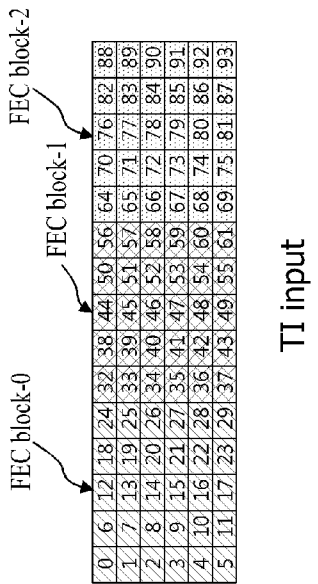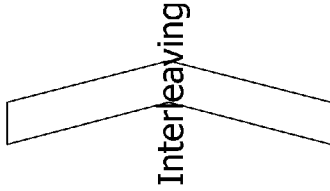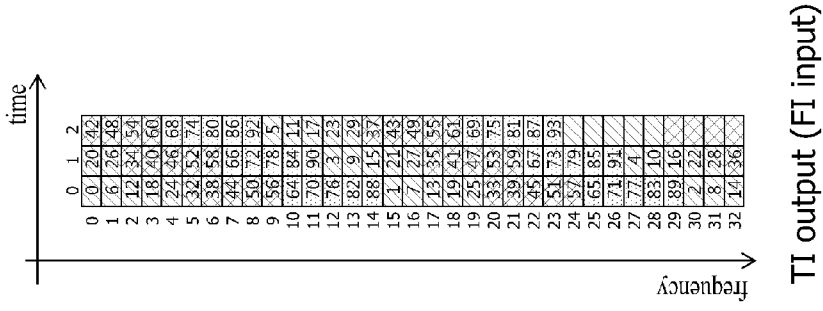
[Fig. 32]
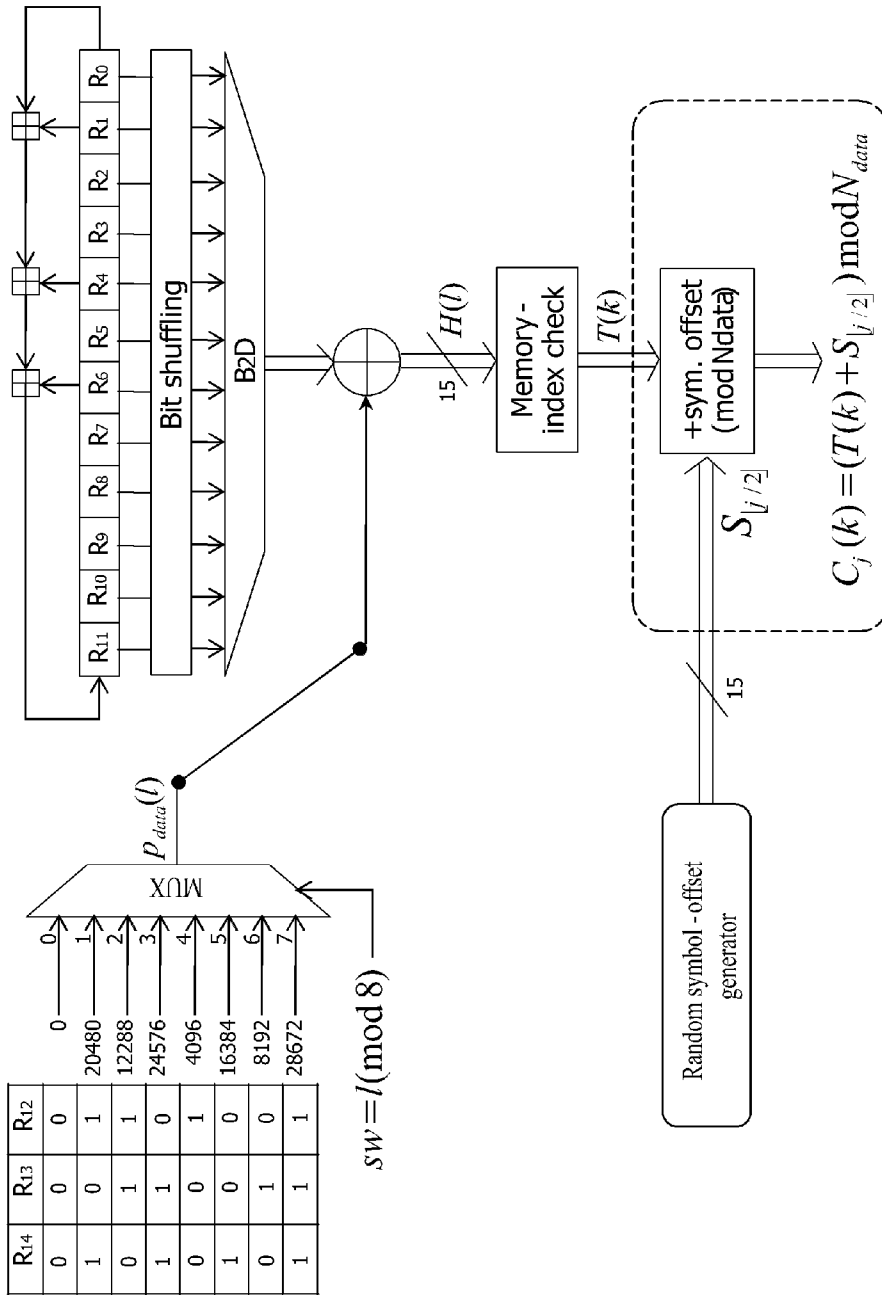
[Fig. 33]

The associated 12th primitive polynomial, $f(x)=1+x^6+x^8+x^{11}-x^{12}$
Operation of the PN generator for $0 \le l < N_{max}$

$0 \le l < 8$

$R^l_{[11,10,9,8,7,6,5,4,3,2,1,0]} = 0,0,0,0,0,0,0,0,0,0,0,0$

$l = 8$

$R^8_{[11,10,9,8,7,6,5,4,3,2,1,0]} = 0,0,0,0,0,0,0,0,0,0,0,1$

$8 < l < N_{max}$

$R^l_{[10,9,8,7,6,5,4,3,2,1,0]} = R^{l-1}_{[11,10,9,8,7,6,5,4,3,2,1]}$

$R^l_{11} = R^{l-1}_0 \oplus R^{l-1}_1 \oplus R^{l-1}_4 \oplus R^{l-1}_6$

$k = 0;\ \vec{R}_r,\ \leftarrow R^l_n\ (bit\ shuffling)$
$for\ (l=0; l<N_{max}; l=l+1)$
{
$\quad H(l) = P_{data}(l) + \sum_{r=0}^{11}(2^n \times \vec{R}^l_n);$
$\quad if\ H(l) < N_{data}$
$\quad${
$\quad\quad T(k) = H(l);$
$\quad\quad C_j(k) = (T(k) + S_{[j/2]}) \bmod N_{data};$
$\quad\quad k = k+1;$
$\quad$}
}

(b)

Bit shuffling

(a)
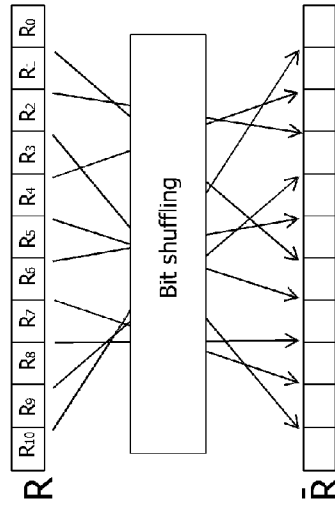
[Fig. 34]
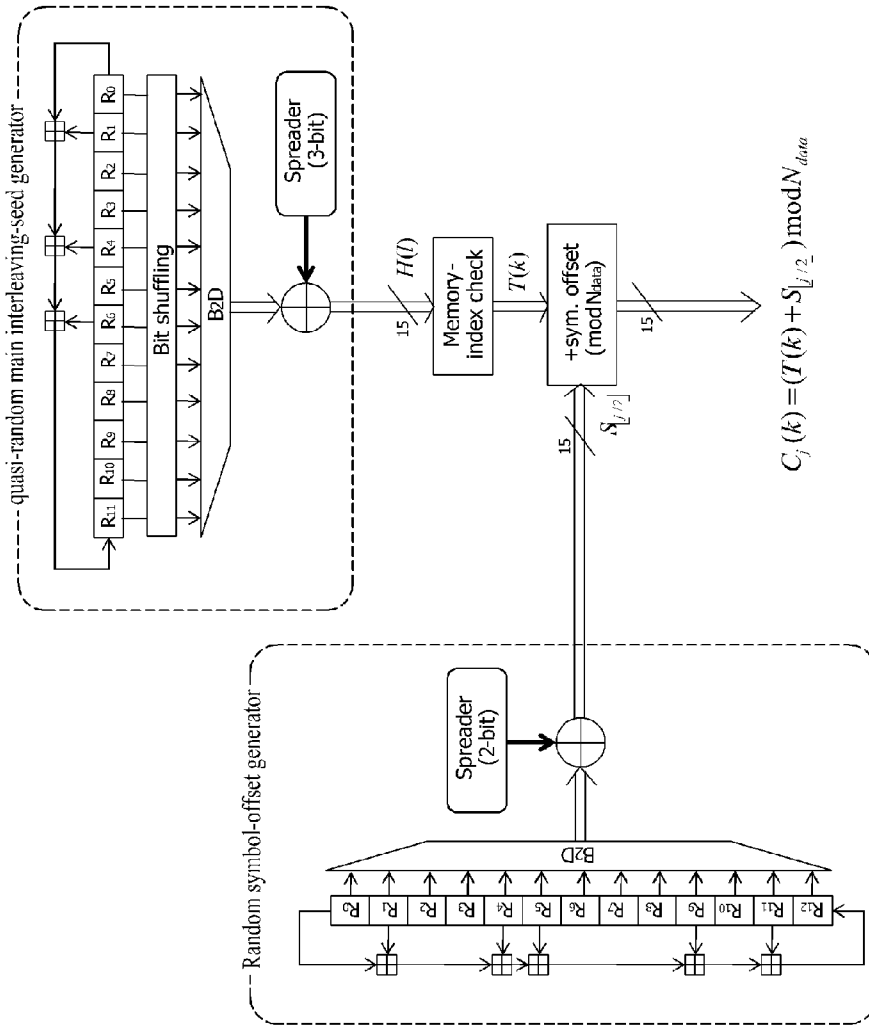
[Fig. 35]
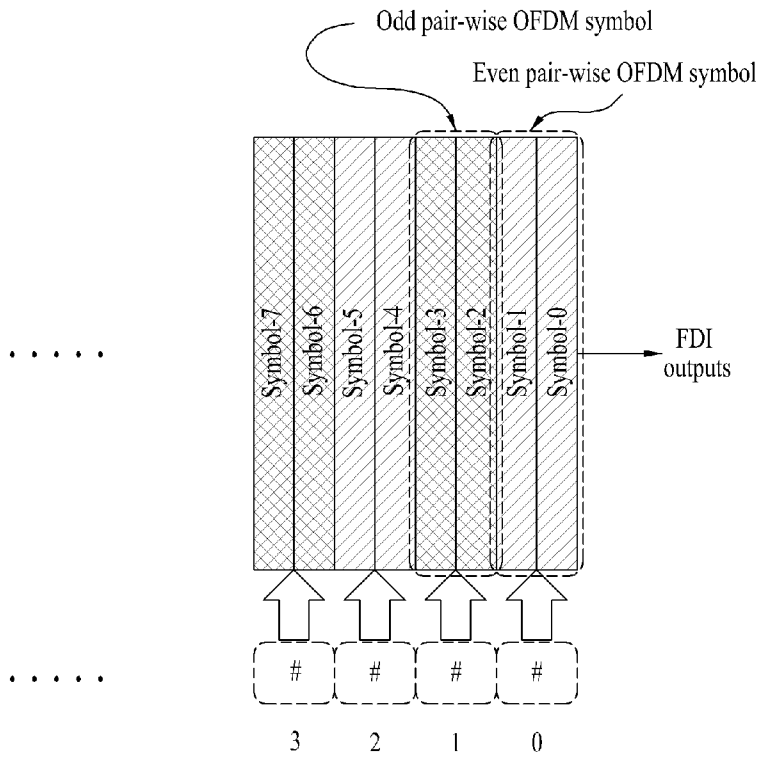
Deinterleaving seeds corresponding to interleaving seeds

[Fig. 36]
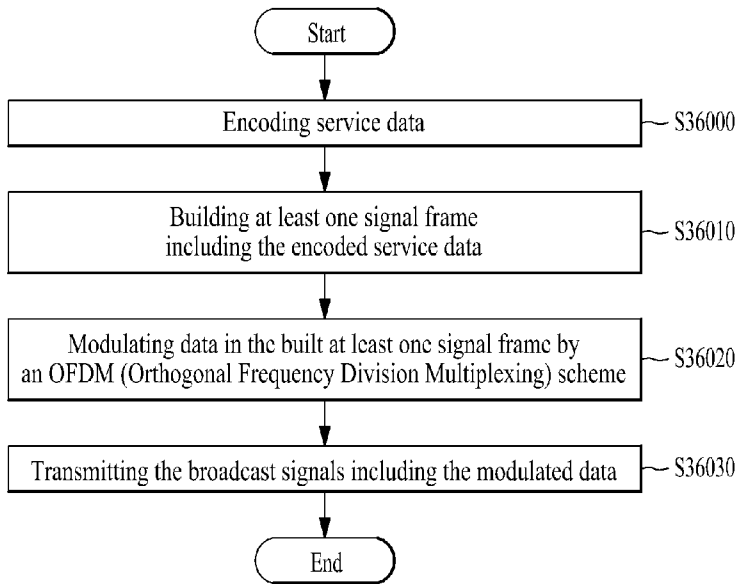
[Fig. 37]
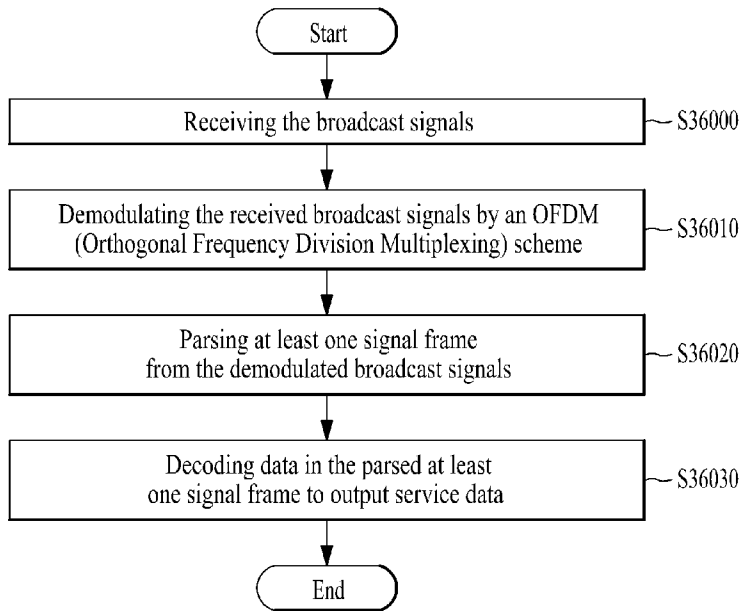
A.   CLASSIFICATION OF SUBJECT MATTER

H04N 7/08(2006.01)i, H04N 21/234(2011.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B.   FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N 7/08; H04L 27/28; H04W 72/04; H04N 21/234

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: interleaving, pair, different

C.   DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0296593 A1 (SAMUEL ASANBENG ATUNGSIRI et al.) 25 November 2010 See abstract, paragraphs [0029], [0033], [0038], [0070]-[0072], claims 2, 7-15 and figures 1, 7.	1,3,5,7
Y		2,4,6,8
Y	US 2009-0296840 A1 (SAMUEL ASANBENG ATUNGSIRI et al.) 03 December 2009 See paragraphs [0008], [0119] and figure 4.	2,4,6,8
A	US 2010-0290425 A1 (ZION HADAD) 18 November 2010 See paragraph [0021], claim 12 and figure 1.	1-8
A	US 2012-0327879 A1 (LOTHAR STADELMEIER et al.) 27 December 2012 See paragraphs [0104]-[0110], [0125], [0203]-[0204] and figure 6A.	1-8
A	US 2013-0064314 A1 (WOO SUK KO et al.) 14 March 2013 See paragraphs [0134], [0278]-[0281] and figures 7, 40.	1-8

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

*	Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	
"E"	earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	
"P"	document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 November 2014 (24.11.2014)	**05 December 2014 (05.12.2014)**

Name and mailing address of the ISA/KR	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea	KIM, Seong Woo
Facsimile No. +82-42-472-7140	Telephone No. +82-42-481-3348

Form PCT/ISA/210 (second sheet) (July 2009)

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0296593 A1	25/11/2010	AU 2008-229928 A1	14/05/2009
		AU 2008-230048 A1	14/05/2009
		AU 2008-230049 A1	14/05/2009
		AU 2008-237590 A1	14/05/2009
		AU 2008-237593 A1	14/05/2009
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