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Edwards

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[54] **NIGHT DEPOSITORY LINE SECURITY**

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[51] **Int. Cl.** **G08c 15,** H04q 9/00

[58] **Field of Search** ..... 340/408 R, 409 R, 151 R

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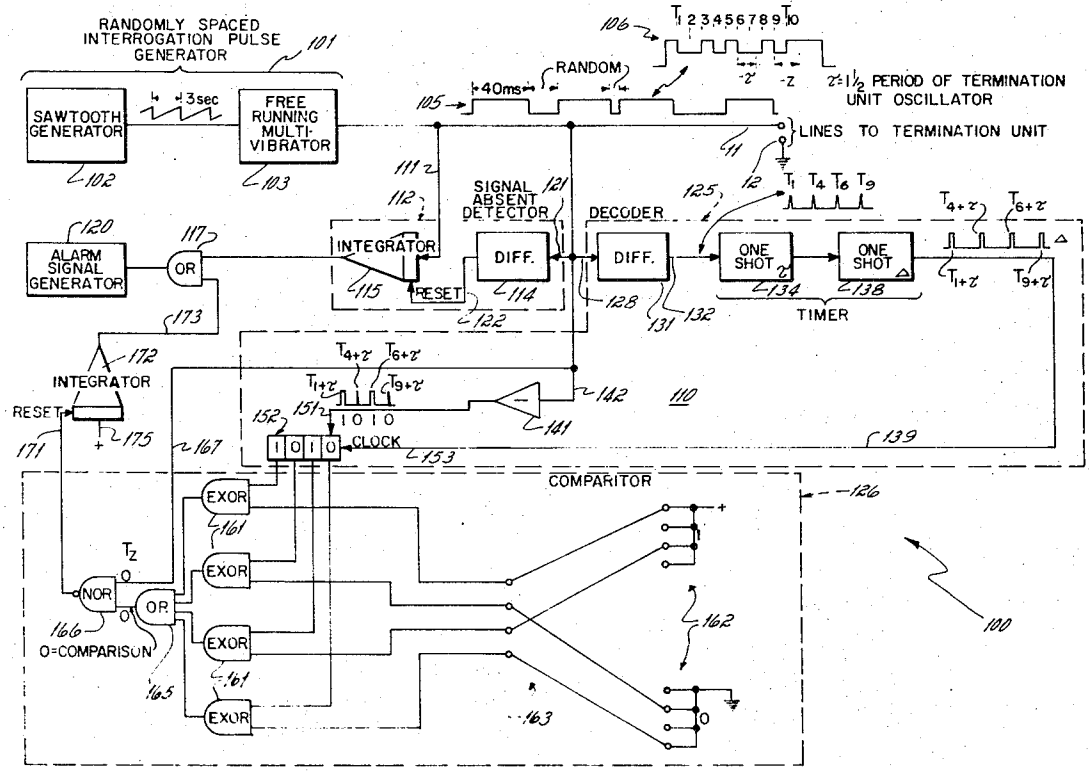
[57] **ABSTRACT**

A line security system for use in intruder alarms for bank night depositories and the like. A termination unit at the secured premise responds to randomly spaced interrogation signals sent over lines from a central unit to generate return signals synchronized to the random signals. The termination unit includes an oscillator driven counter which sequentially emits pulses coded by the plugboard. An inhibit circuit stops the oscillator at the end of each response signal cycle. The termination of the interrogation pulse resets the counter to insure that it remains synchronized with a decoder at the central unit, and also disables the inhibit circuit so that the next interrogation pulse may restart the oscillator. The termination unit is powered by energy derived from the interrogation pulses and stored in a capacitor. The central unit sounds an alarm when no response signal occurs or after receipt of several successive response signals of improper or unsynchronized code.

17 Claims, 2 Drawing Figures



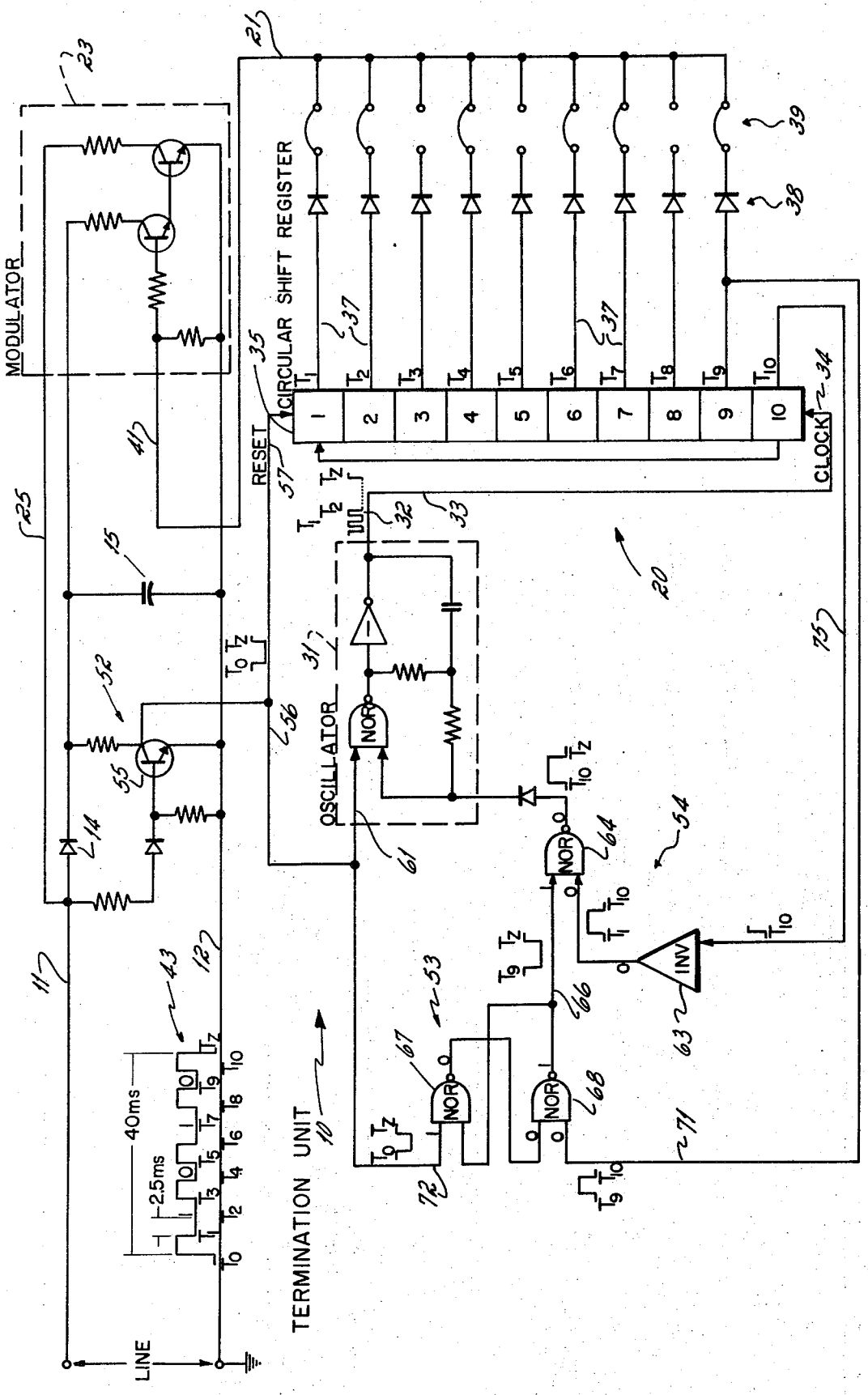
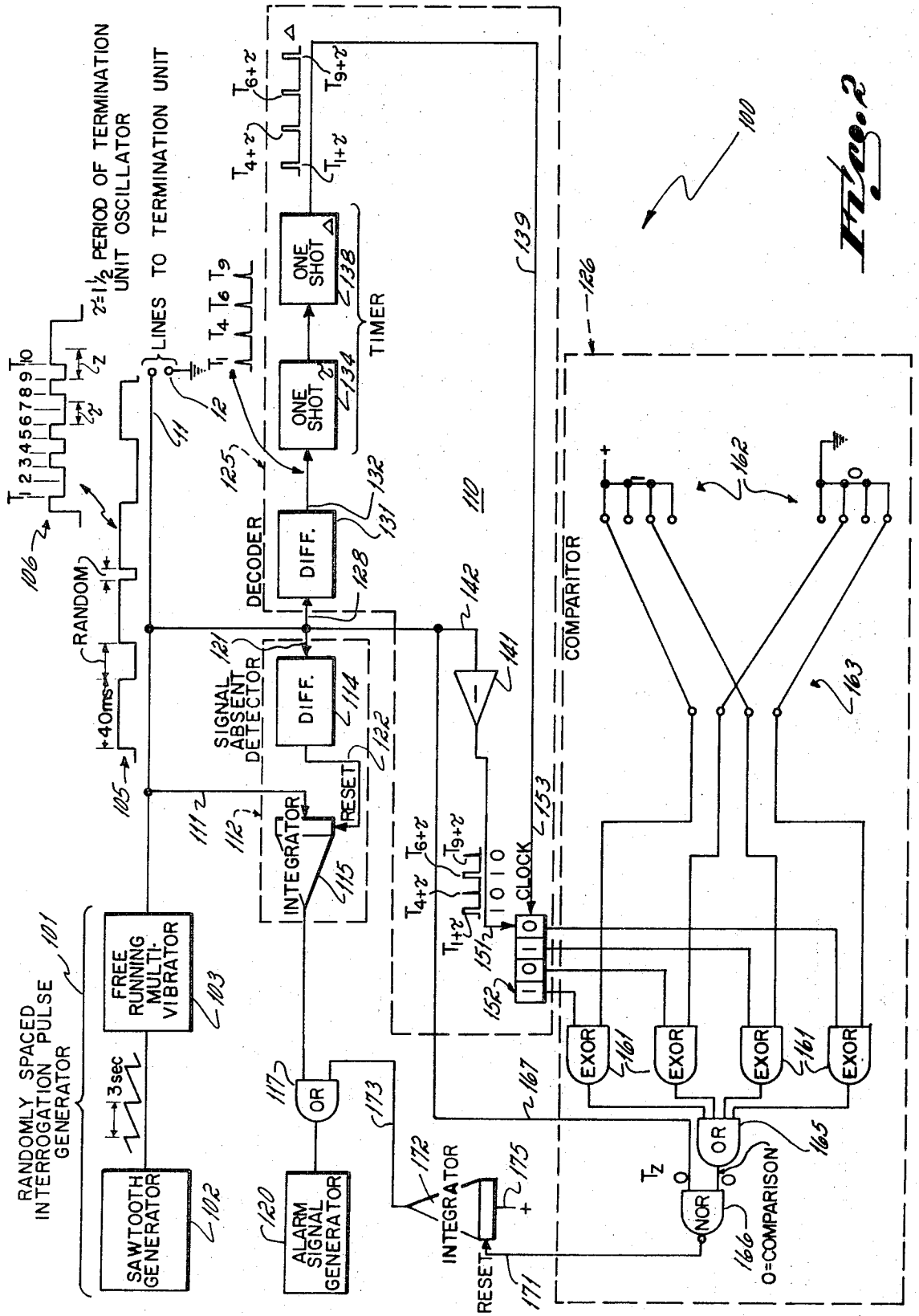

MODULATOR
CIRCULAR SHIFT REGISTER
RESET
CLOCK
OSCILLATOR
NOR
INV
TERMINATION UNIT
LINE
40ms
2.5ms

Fig. 1


RANDOMLY SPACED INTERROGATION PULSE GENERATOR
SAWTOOTH GENERATOR
FREE RUNNING MULTI-VIBRATOR
3sec
RANDOM
+40ms
INTEGRATOR
RESET
SIGNAL ABSENT DETECTOR
DIFF.
DECODER
ONE SHOT
TIMER
LINES TO TERMINATION UNIT
τ=1½ PERIOD OF TERMINATION UNIT OSCILLATOR
ALARM SIGNAL GENERATOR
OR
CLOCK
COMPARITOR
EXOR
NOR
0=COMPARISON

NIGHT DEPOSITORY LINE SECURITY

The present invention relates to intrusion alarm line security systems, and more particularly, to a system wherein a premise unit located at a protected area, such as at a bank night depository, transmits coded response signals to a central unit in response to random interrogation signals on the connecting lines.

Intruder alarm systems are in common use for protecting premises against unauthorized intrusions. These systems normally employ some sort of alarm condition sensor which responds to an abnormal condition at the protected area. Commonly, these alarm sensors transmit a signal indicating this alarm condition over lines which connect the sensor at the premise area with the central alarm unit. It is important in such systems that, for additional security, measures be taken to detect any tampering which may occur with the connecting lines. In the simpler alarm systems, the alarm condition may be indicated by a switch connected in the lines which will be opened or closed upon the opening of a door or window or the like. Attempts are sometimes made by intruders to short circuit the lines across the switch or cut the lines to defeat the alarm. In somewhat more sophisticated devices, an impedance or signal generator is connected across the lines so that a simple opening or shortening of the leads can be detected at the central unit through a change in the impedance or removal of the return signal. Devices employing signal generators may include transmitters which operate independently or continuously to generate signals or may include devices which respond when interrogated from the central unit.

The impedance termination systems can be defeated by substituting the correct impedance on the lines. With the signal generator type of systems, it is sometimes encountered that an intruder might attempt to breach the security of the system by recording the return signals on the lines and then retransmitting the recorded signal on the lines and back to the central unit so that he might thereafter proceed to break the lines to the alarm sensor. The likelihood of attempts such as this being successful can be substantially reduced by employing a random interrogation system. With such systems, it is much more difficult for the intruder to synthesize a proper return signal on the lines. The system of this type, however, does require a degree of synchronization between the interrogation signal and the return signal which responds to it so that lack of synchronization can be used to distinguish the synthesized signal from a proper response.

It is a primary objective of the present invention to provide such a random interrogation line security system in which the response signal is at all times precisely synchronized to the random interrogation pulses.

One of the undesirable properties of random interrogation systems in general is that they frequently require extremely large and complex premise units to generate the required response signals.

It is a further objective of the present invention to provide such a system in which the premise unit is small, simple, and extremely compact, and which derives its power primarily from the lines connecting it with the central unit.

The present invention is predicated in part upon the concept of providing a line security system having a premise unit which generates a response signal synchronized to randomly spaced interrogation pulses, and which premise unit includes a transmitter which employs a counter which generates a series of signals in response to an interrogation pulse and which counter is automatically reset by the interrogation pulse so that the return in interrogation signals are maintained in synchronism.

The specific embodiment of the present invention disclosed below provides a premise unit employing an oscillator driven counter or shift register. The shift register has ten outputs which are energized sequentially as the oscillator generates clock pulses to the register. The outputs of the shift register are selectively connectable through a patch panel to a transmitter output so that a binary code is generated in accordance with the setting of the patch panel. In the specific code employed, two consecutive connections designate a one-bit and a single connection designates a zero-bit, open connections providing the spacers between the bits.

The oscillator is normally held in an OFF condition and the shift register is held in a RESET condition both through a reset circuit connected across the lines which is responsive to the absence of an interrogation pulse on the lines. The occurrance of an interrogation signal on the lines will remove the shift register reset signal and allow the oscillator to begin generating clock pulses to the shift register. After the clock starts, a flip-flop is set which enables a clock inhibit circuit to automatically stop the clock when the shift register has completed its scan. Upon termination of the interrogation pulse, the shift register is automatically reset and the inhibit circuit is disabled so that the clock can be restarted when the next interrogation pulse occurs on the lines.

The central unit is provided with a randomly spaced constant pulse width interrogation pulse generator and a receiver both connected to the lines. The receiver actuates an alarm when either of two conditions occurs. The first and most common condition is that of total absence of a response signal to an interrogation pulse on the lines. This condition will immediately sound the alarm. The second condition is the presence of a return signal on the lines but in a form which does not correspond to the proper code or which is not properly synchronized with the interrogation signal. When this condition occurs, an alarm trigger circuit begins to integrate a signal which will sound an alarm if several such occurances occur in sequence. This detects line tampering but will ignore a certain amount of error in the return signal as a result of noise on the lines or in the system.

The termination unit is powered entirely by power derived from the interrogation pulse. This energy is stored in a capacitor, thus, providing a compact premise unit.

Additionally, the termination unit may be provided with means which allow recycling of the shift register and code selecting means, such as a flip-flop, and another plugboard so that other information such as a termination unit identification code may be added.

The advantages of the system reside in the ability to provide the line security system employing a random interrogation pulse responsive premise unit which is highly compact, simple, and effective in detecting a breach of security on the system lines. The system is capable of micropower circuit construction.

These and other objectives and advantages of the present invention will be more readily apparent from the following detailed description of the drawings illustrating one preferred form of an alarm system embodying principals of the present invention.

FIG. 1 is a logic and schematic diagram of a termination unit of a line security system according to the present invention;

FIG. 2 is a schematic and logic diagram of a central unit of a line security system according to the present invention.

The termination unit of FIG. 1 is normally employed in a burglar alarm system. This termination unit **10** is located at a premise to be protected. The termination unit **10** is connected through a pair of lines **11** and **12** to a central unit **100** (FIG. 2). The central unit will enunciate an alarm condition at the premises protected by the termination unit. A typical alarm condition results from the breaking of a closure as, for example, the unauthorized opening of a door. This condition is normally detected by a switch connected in series with the lines **11** and **12.** The switch opens upon the breaking of the closure to cause a condition which would be detected by the central unit to enunciate the alarm condition.

The termination unit **10** is powered by electrical energy transmitted over the lines **11** and **12** from the central unit. The unit **10** responds to interrogation pulses on the lines **11** and **12** to return over the lines **11** and **12** a signal representative of a secure condition. If the lines are broken, the absence of the return signal will be detected by the central unit and, thus, an alarm condition will be indicated.

The termination unit **10** has no power supply of its own, but instead it relies entirely upon energy supplied over the lines **11** and **12** of the central unit. In this interrogation type system, in a normal state, there is no power transmitted over the lines **11** and **12.** Instead, all of the energy to power the termination unit **10** is derived from the interrogation pulse. This pulse takes the form of a voltage on line **11** which is positive with respect to the line **12** which is grounded. The energy from the central unit passes through a diode **14** from line **11** to charge a storage capacitor **15.** The capacitor **15** will be charged to the interrogation pulse voltage which may be typically **12** volts. The interrogation pulse, upon its occurrence on the lines **11** and **12,** actuates a signal generator **20** which generates a secure condition signal on lines **21.** This signal is communicated to a transmitter or modulator circuit **23** in the form of a series of negative pulses which are impressed by way of the line **25** on the line **11** upstream of the diode **14.** The diode **14** prevents a discharge of the capacitor **15** by the superimposition of the negative signal pulses from line **25.** The signal from line **25** represents coded information which is identical to a reference code stored at the central unit. This signal is decoded by the central unit and compared with the reference signal to detect the presence or absence of a secure condition on the lines **11** and **12.** If the lines **11** or **12** are broken, the interrogation pulse will not cause the return of any signal and this condition when detected by the central unit will indicate the alarm state.

To reduce the likelihood of the success of more sophisticated attempts to violate the line security, the interrogation pulses from the central unit are randomly spaced. This makes it more difficult for an intruder to synthesize the interrogation pulse response and to feed it back along the lines **11** and **12** when the circuit is broken. This might be attempted, for example, by recording the pulse response and transmitting it back to the central unit. Random interrogation makes it more difficult to properly time the response. Such a system, however, must be able to synchronize the return signal with a reference signal in the decoder. The present invention does this by synchronizing both with the interrogation pulse. It provides a counter in the premise or termination unit which is started and reset by the interrogation pulse. This is provided by circuitry described below.

The signal generator **20** of the termination unit **10** includes an oscillator **31** which generates clock pulses **32** along line **33** to the clock input **34** of the shift register **35.** The shift register **35** is a circular shift register having **10** stages. The outputs of nine of these stages are connected through blocking diodes **38** to a plugboard **39.** As the shift register is clocked, output signals appear successively on the output lines **37.** The plugboard **39** allows the selective connection of each of the outputs **37** of the shift register **35** to the input **41** of the modulator circuit **23.** The outputs **37** of the shift register **35,** which are energized in sequence, are each representative of a specific time in the signal cycle. The connections made by the plugboard **39** result in the imposition of a low-voltage signal during the time controlled by the respective position of the shift register **35** on output line **21.** The plugboard connection shown in FIG. 1 will result in a signal having the form of signal **43.** The coding selected in the present circuit is such that a negative-going pulse of only one time period in width will represent a zero while a pulse having a two time period width will represent a one, thus giving a binary coded serial data transmission. The coded signal represented as **43** in the drawing will thus have the form of a digital number 1-0-1-0. This code is determined by the setting of the patch panel **39** connecting outputs **37** representing signals of one clock pulse width beginning at times T_1, T_2, T_4, T_6, T_7 and T_9 to line **21** to the modulator **23.** Time periods beginning at times T_3, T_5 and T_8 denote space intervals.

The signal generator synchronizing circuit includes an interrogation pulse-responsive start and reset circuit **52,** an oscillator starting circuit **53** and an oscillator stopping or inhibiting circuit **54.** The circuit **53** serves as an oscillator starting circuit by disabling the inhibiting circuit **54.**

The circuit **52** includes a transistor **55** connected between the lines **11** and **12** downstream of the diode **14.** The base of the transistor **55** is connected through a resistor/diode network from the line **11** upstream of diode **14.** The collector of the transistor **55** is connected to a reset line **56** connected to the reset input **57** of the shift register **35.** In the intervals between interrogation pulses, the transistor **55** is nonconductive and the signal on reset line **56** is positive, by virtue of the charge on the capacitor **15.** This positive signal on line **56** holds the shift register **35** in reset condition during this interval between interrogation pulses. The reset condition of the register **35** is one wherein the bit positions **1** through **9** of the shift register contains zeros and the bit position **10** contains a one.

Line **56** is also connected to the input **61** of the oscillator **31** to disable the oscillator during the interval between interrogation pulses. This bit position **10** of the

shift register **35** has its output connected to an input of an inverter **63** of the circuit **54.** The OFF state of the inverter **63** denotes the oscillator inhibit signal. This inhibit signal is disabled, during this interval by the ONE-state output from line **66** of the circuit **53.** The circuit **53** includes a pair of NOR-gates **67** and **68** connected in an R-S flip-flop circuit arrangement. This flip-flop is illustrated in an ON condition. It has a set input **71** connected to the ninth position of the shift register **35** and a reset input **72** connected to the reset line **56.**

In its initial stand-by position, the termination unit **10** will have a zero signal appearing at the input lines **11** and **12.** A position reset signal will be present on line **56** holding the shift register **35** in its reset condition. The shift register **35** will thus have a ONE in the tenth position and a zero in its other nine positions. The oscillator will be inhibited only by the negative signal from the reset line **56** at its input **61.** The flip-flop of the inhibit disable circuit **53** will be set giving a positive signal on line **66,** while the flip-flop **63** of inhibit circuit **54** will be reset to zero.

At the beginning of the interrogation pulse, at time T_0, the signal on line **11** will go positive causing the transistor **55** of circuit **52** to conduct, thus removing the reset signal from line **56.** This will cause a zero signal to appear at the input **61** of the oscillator **31** which allows the oscillator to start generating sequential output pulses to the clock input **34** of the shift register **35.** This will cause the bit to be transferred from the tenth position to the first position of the shift register **35** as the first pulse is emitted from the oscillator at time T_1. As each subsequent pulse is emitted from the oscillator **31** along line **33,** the bit will progress through the shift register successively causing it to transmit output signals along the line **21** whenever the respective outputs **37** from the respective position of the shift register **35** is connected by patch panel **39** thereto. As the bit progresses through the shift register **35** toward bit position **10,** it is necessary to at some time reset the flip-flop of the inhibit disable circuit **53** so as to permit the bit from position **10** to pass through the NOR-gate **64** to stop or inhibit the oscillator **31.** This is provided by the output of bit position **9** which is connected to the set input **71** of the flip-flop circuit **53.** When the bit enters this ninth position, the flip-flop **53** is set causing its output to assume a zero state enabling the inhibit circuit **54.** Thus, when the bit enters position **10** of the register **35,** it is transmitted along the output line **75** to the reset input of the inverter **63,** causing the inverter to turn on, thus causing the output of the NOR-gate **64** to go positive inhibiting the oscillator **31.** At some time thereafter the interrogation pulse will cease at time T_2 and the positive signal on line **56** will reset the flip-flop of circuit **53** so that the presence of the bit in the tenth position of the shift register **35** will not prevent the restarting of the oscillator **31.** The positive pulse on line **56** also holds the shift register in a reset condition so that in the event that the shift register has erroneously stopped in some other than the reset condition, due perhaps to the incidence of noise, the register will be assured of being synchronized to its reset condition for the beginning of the next interrogation cycle. The positive pulse or signal on line **56** also holds the oscillator **31** in a disabled condition.

Referring now to FIG. **2,** the central unit **100** is illustrated. This unit includes a randomly spaced but constant width interrogation pulse generator **101** which includes a sawtooth generator **102** and a free-running multi-vibrator **103.** The multi-vibrator is set to switch ON for 40 milliseconds and OFF for a time which may be **40** milliseconds or less. The variable pulse spacing is achieved by the saw-tooth generator **102** which is connected to the multi-vibrator **103** in such a manner that its output affects the initial charge condition on the capacitor which determines the OFF time of the multi-vibrator. Thus, a quasi-random spacing between the positive pulses is achieved. The output of the saw-tooth generator **102** is of low frequency having a period of approximately three seconds. Thus, the intervals between interrogation pulses will progressively decrease for a period of three seconds and then abruptly increase toward a maximum of approximately 40 milliseconds.

The general wave form of the interrogation pulses is represented by a curve **105** in FIG. **2.** The output of the multi-vibrator **103** is connected to the line **11** while the line **12** is connected to ground. These lines **11** and **12** connect to the termination unit **10.** The returned signal on the lines **11** and **12** is superimposed on the interrogation pulse and is represented by the curve **106** in FIG. **6.**

An alarm circuit illustrated generally at **110** comprises the rest of the circuit shown in FIG. **2.** This circuit includes an input **111** which is connected from the line **11** to a signal at detector **112.** The signal absence detector **112** includes a differentiator and detector circuit **114** and an intergrator **115.** The input **111** from the line **11** is connected to the input of the integrator **115.** The output of the integrator is connected through an OR-gate **117** to an alarm signal generator **120.** An interrogation signal, if allowed to accumulate in the integrator **115,** will cause the alarm signal generator **120** to actuate. The signal absence detector **112** has a second input **121** connected also to the line **11.** This input is transmitted through a differentiator and detector circuit **114** which extracts from the pulse signal **105** the received information **106** on the line **11.** If this information is present in any form, whether in the proper code or not, a signal is emitted from the output **122** of the differentiator **114** to a reset input of the integrator **115** to reset the integrator, thus preventing the occurence of the alarm signal indication. In the case that a pulse passes with the total absence of any return signal, such as will occur if the line is broken, the integrator **115** will not be reset and the alarm condition will be indicated.

If information is present upon the line **111,** but is not in the proper coded form, this condition will be detected by the decoder circuit **125** in combination with the comparator circuit **126.** This decoder circuit **125** has an input **128** also connected from the line **11.** The decoder circuit **125** includes a differentiator **131** having its input connected from the decoder input **128.** This differentiator responds to the trailing edges of the wave form **106.** If the proper signal is present, pulses will be emitted at the output **132** of the differentiator **131** at times T_1, T_4, T_6 and T_9. These pulses are transmitted to a one-shot multi-vibrator **134** which operates as a time delay for a period τ which is equal to approximately 1-½ times the normal spacing between the clock pulse outputs from the oscillator **31** in the termination unit **12** (FIG. **1**). Thus, the output from the one-shot multi-vibrator **134** will coincide with a negative pulse of the signal **106** only when that pulse is at least two

time increments long. A pulse of a single time increment in length will not coincide with the delayed signal from the output of the one-shot multi-vibrator **134.** Thus, this information provides a means for distinguishing between the longer pulses indicating a ONE-bit and the shorter pulses indicating a ZERO-bit. The delayed pulses at the outputs of the multi-vibrator **134** occur at times $T_{1+\tau}$, $T_{4+\tau}$, $T_{6+\tau}$, and $T_{9+\tau}$, These pulses are shaped to a proper width Δ by being fed through a second one-shot multi-vibrator **138.** The outputs of the multi-vibrator **138** are transmitted along line **139** to the clock, **153** of a shift register **152.** The data input of the register **152** is connected from the output of an inverter amplifier **141** which has its input **142** also connected to line **11.** The register **152** operates to AND, thus, the delayed pulses on line **139** and the signal **106** from the termination unit **10** distinguish between 1 and 0 code. For example, an output signal will only occur from the AND-gate **140** at time $T_{1+\tau}$ and $T_{6+\tau}$. This signal is transmitted to a data input **151** of the four-position shift register **152.** The clock input **153** of the shift register **152** enters from the line **139** so that each of the delayed pulses will clock the shift register **152.** Thus, at time $T_{1+\tau}$ a shift register will be clocked but a zero bit will enter the shift register **152.** Similarly, a one will enter a time $T_{6+\tau}$ and a zero at time $T_{9+\tau}$. Thus, the shift register will attain a final data content of 1-0-1-0. The outputs of the bit positions from the shift register **152** are each communicated to a respective one of a set of four two-input Exclusive-OR gates **161.** The other input of these Exclusive-OR gates is connected to a signal standard source **162.** This source **162** consists of a plug-board **163** which selectably connects the inputs of the respective Exclusive-OR gates **161** to either positive or negative signal sources thus establishing a reference signal. When an exact coincidence exists between the content of the shift register **152** and the reference signal provided by the plugboard **163,** a zero will appear at the output of the Exclusive-OR gates **165** which has its outputs of the Exclusive-OR gates **161.** This condition is tested at the end of the interrogation pulse by a NOR-gate **166** which has one input connected to the output of OR-gate **165** and the other input connected along line **167** to the line **11.** Thus, the output of the OR-gate **165** is interrogated only at time T_z at the end of the interrogation pulse. Only if coincidence does occur will a positive signal appear at the output of the NOR-gate **166** and be transmitted to a reset input **171** of an integrator **172.** The integrator **172** has its output **173** connected to the input of the OR-gate **117** to trigger the alarm generator **120.** The integrator **172** has its input **175** connected to a positive signal source. Thus, the integrator **172** will continue to constantly integrate at a slow rate and, if not reset, eventually provide an alarm signal along line **173** to trigger the alarm generator **120.** A coincidence, therefore, as detected by the NOR-gate **166,** will reset the integrator through input **171** and prevent it from ultimately obtaining an alarm condition. The time constant of the integrator **172** is such that it will take several noncomparison occurrences to allow an alarm to be triggered. This will prevent the indication of an alarm condition due to erroneous information caused by noise on the transmission lines.

The device described above operates very effectively to monitor the security of a line between a central alarm unit and a remote location such as a door to a closure. The termination unit of the system described above does not require a power source but derives all its power from the lines **11** and **12.** The termination unit can be manufactured in an extremely compact form of at most a few cubic inches with conventional solid-state components. The double reset circuitry in the termination unit, particularly the reset circuitry **54** which operates upon completion of the generation of the responding signal and in addition the reset circuitry **52** which insures that the register is reset at the beginning of every pulse serves to effectively synchronize the response to the interrogation pulse with the decoder in the central or panel unit. This effectively provides a means for employing randomly spaced interrogation pulses, thus enhancing the security of the lines in an extremely simple and compact security unit.

What is claimed is:

1. A line security premise unit having a line connectable to a central station, said unit being capable of transmitting on said line, in response to interrogation signals on said line, coded response signals, said premise unit comprising:

a counter;

a transmitter for generating a coded pulse signal on said line in response to the stepping of said counter;

said counter being started in response to the occurrence of each said interrogation signal on said line; and

said counter being reset in response to the termination of each said interrogation signal;

whereby said coded pulse signals are maintained in synchronism with said interrogation signals.

2. The premise unit of claim **1** further comprising:

an oscillator for generating a periodic series of pulses to trigger said counter, said oscillator starting in response to the occurrence of each interrogation signal on said line.

3. The premise unit of claim **1** further comprising:

a plugboard coder connected between the output of said counter and said line for establishing the code of said pulse signals on said line.

4. The premise unit of claim **1** further comprising:

a counter inhibit circuit responsive to a predetermined state of said counter for stopping the generation of coded information.

5. The premise unit of claim **4** further comprising:

an inhibit disabling circuit being set in response to the termination of said interrogation pulse and being reset after the start of said counter but before said counter reaches said predetermined state.

6. The premise unit of claim **1** further comprising:

a power storage element connected to said line;

said counter and transmitter being powered by energy from said storage element;

said storage unit being charged by energy from said central station.

7. A line security premise unit having a line connectable to a central station, said unit being capable of transmitting on said line, in response to and in synchronism with random interrogation signals on said line, coded response signals, said premise unit comprising:

a counter;

a transmitter for generating a coded pulse signal on said line in response to the stepping of said counter;

an oscillator for generating a periodic series of pulses to trigger said counter, said oscillator starting in response to the occurence of each interrogation signal on said line;

a counter inhibit circuit responsive to a predetermined state of said counter for stopping the generation of coded information;

an inhibit disabling circuit being set in response to the termination of said interrogation pulse and being reset after the start of said counter but before said counter reaches said predetermined state; and

a counter reset responsive to the termination of each said interrogation signal on said line.

8. The premise unit of claim **7** further comprising:

means for selectively connecting the outputs of said counter to said transmitter to establish the code of said pulse signals on said line.

9. A synchronized random interrogation line security system comprising:

a central unit;

a premise unit located remote from said central unit;

a line electrically interconnecting said central unit and said premise unit;

said central unit comprising:

a. a signal generator for generating randomly spaced interrogation signals, said generator having an output connected to said line,

b. an alarm signal generator,

c. a receiver having an input connected to said line, said receiver being operative to decode pulse signals on said line;

d. a reference signal source,

e. means timed by said interrogation signal for comparing said decoded signal and said reference signal, and

f. means for actuating said alarm signal generator in accordance with the results of said comparison; and

said premise unit comprising:

a counter;

a transmitter for generating a coded pulse signal on said line in response to the stepping of said counter;

said counter being started in response to the occurrence of each said interrogation signal on said line; and

said counter being reset in response to the termination of each said interrogation signal;

whereby said coded pulse signals are maintained in synchronism with said interrogation signals.

10. The system of claim **9** wherein said premise unit further comprises:

an oscillator for generating a periodic series of pulses to trigger said counter, said oscillator starting in response to the occurrence of each interrogation signal on said line.

11. The system of claim **10** wherein said premise unit further comprises:

a plugboard coder connected between the output of said counter and said line for establishing the code of said pulse signals on said line.

12. The system of claim **9** wherein said premise unit further comprises:

a counter inhibit circuit responsive to a predetermined state of said counter for stopping the generation of coded information.

13. The system of claim **9** wherein said premise unit further comprises:

an inhibit disabling circuit being set in response to the termination of said interrogation pulse and being reset after the start of said counter but before said counter reaches said predetermined state.

14. The system of claim **9** wherein said premise unit further comprises:

a power storage element connected to said line;

said counter and transmitter being powered by energy from said storage element;

said storage unit being charged by energy from said central station.

15. The system of claim **9** wherein said receiver further comprises a register for storing said decoded pulse signal; and

said comparing means are timed by the termination of said interrogation pulse.

16. The system of claim **9** wherein said central unit further comprises:

means responsive to the absence of information on said line for actuating said alarm signal generator.

17. The system of claim **9** wherein said central unit further comprises:

an integrator having a signal input independent of said coded signal and an output connected to said alarm signal generator for actuating said alarm when said integrator output reaches a predetermined value; and

the output of said comparison means being connected to said integrator so as to reset said interrogation upon coincidence of said decoded signal and said reference signal.

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