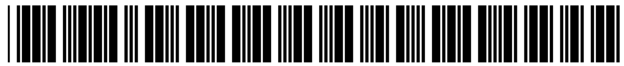

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(12) United States Patent
Marmillion et al.

(10) **Patent No.: US 6,333,546 B1**

(45) **Date of Patent: Dec. 25, 2001**

(54) **MICRO FUSIBLE LINK FOR SEMICONDUCTOR DEVICES AND METHOD OF MANUFACTURE**

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(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/692,539**

(22) Filed: **Oct. 20, 2000**

Related U.S. Application Data

(62) Division of application No. 09/074,353, filed on May 7, 1998.

(51) **Int. Cl.**[7] **H01L 29/00**

(52) **U.S. Cl.** **257/529**; 438/601

(58) **Field of Search** 257/529, 536, 257/537, 665, 910; 438/601

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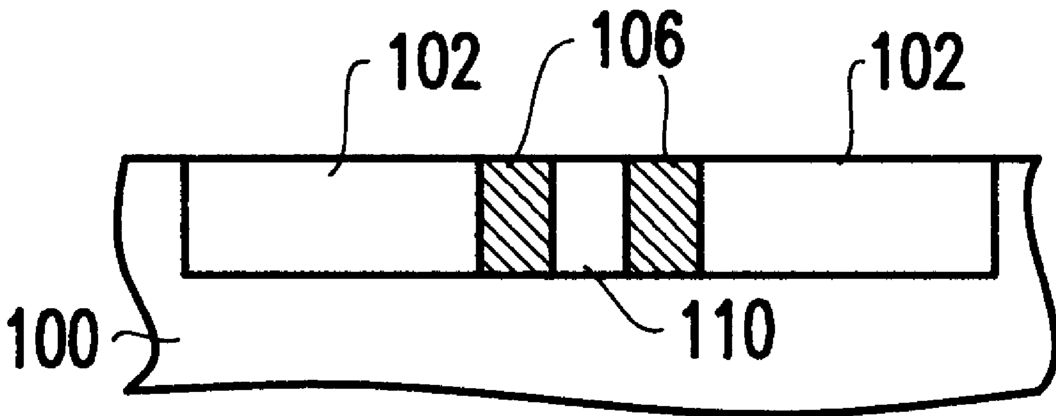
Primary Examiner—David Nelms
Assistant Examiner—Quoc Hoang
(74) *Attorney, Agent, or Firm*—McGuireWoods, LLP; Daryl K. Neff

(57) **ABSTRACT**

An electrically activated fuse with a high melting point heater element in series with a low melting point fusible link. The heater element has a higher resistivity and larger cross-sectional area than the fusible link in order to withstand heat that the heater element generates bringing the fusible link to its melting point. Fuse dimensions (width and length) are each between 0.1 and 2.0 microns, with a thermal mass of the heater element being sufficient to melt the fusible link.

6 Claims, 5 Drawing Sheets



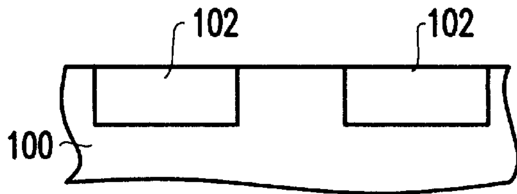


FIG.1A

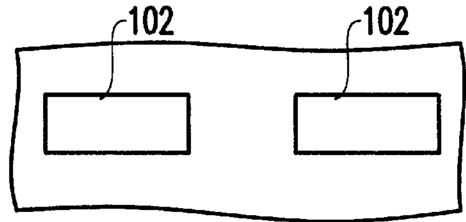


FIG.2A

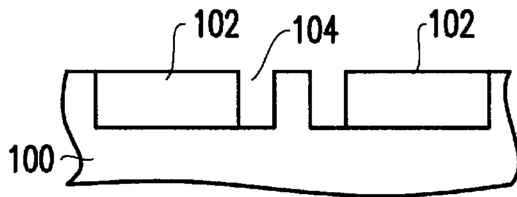


FIG.1B

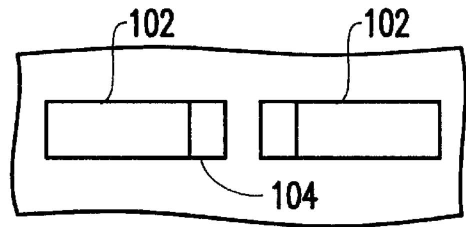


FIG.2B

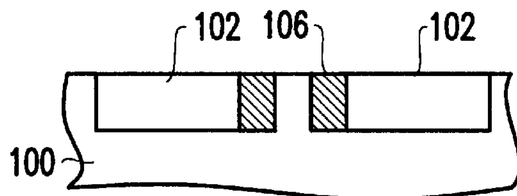


FIG.1C

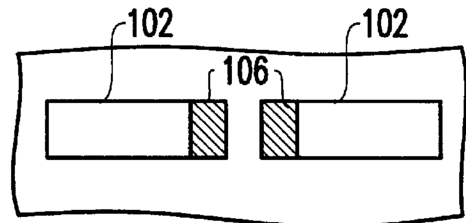


FIG.2C

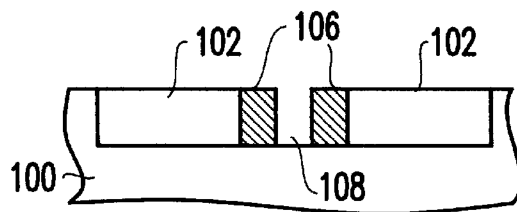


FIG.1D

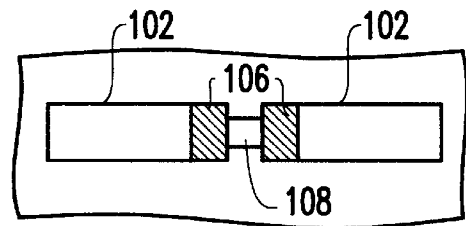


FIG.2D

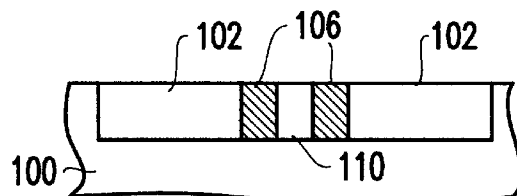


FIG.1E

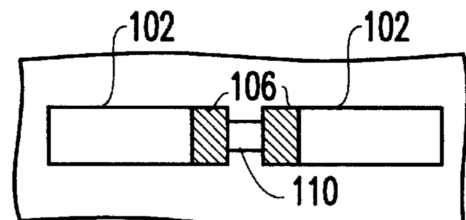


FIG.2E

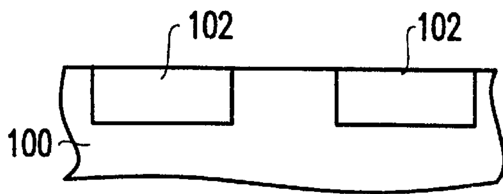
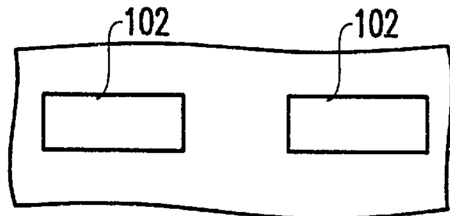


FIG.3A



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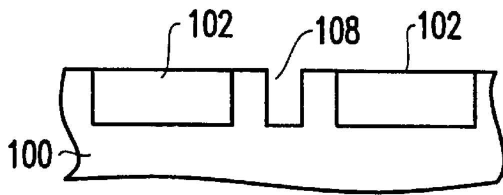


FIG.3B

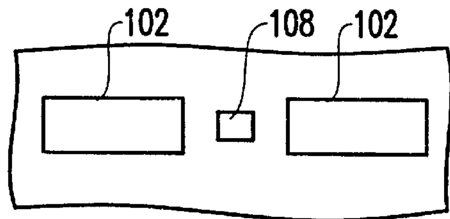
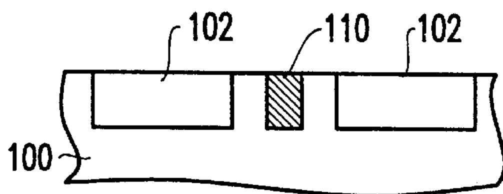


FIG.4B



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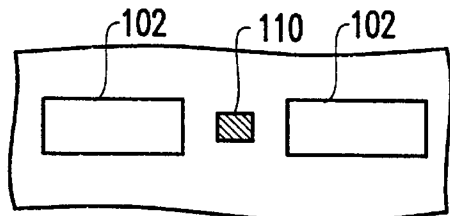

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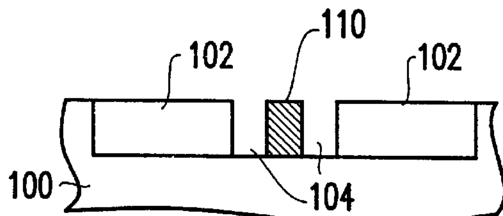

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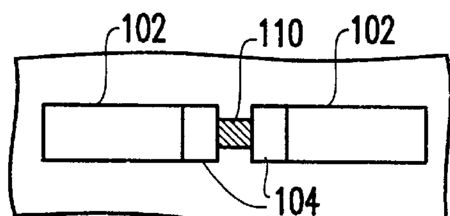

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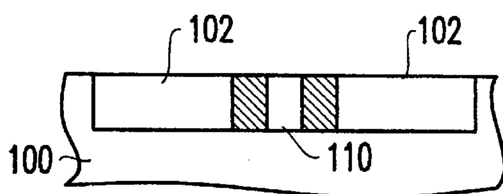
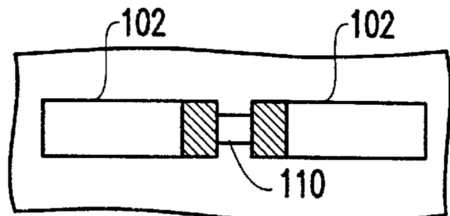


FIG.3E



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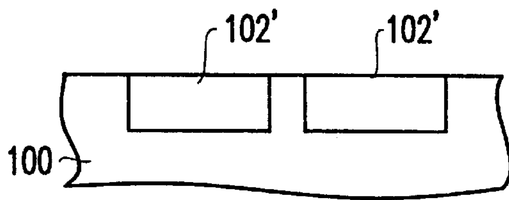

FIG.5A

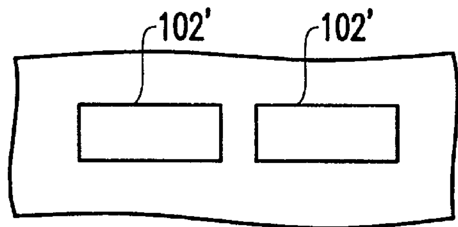

FIG.6A

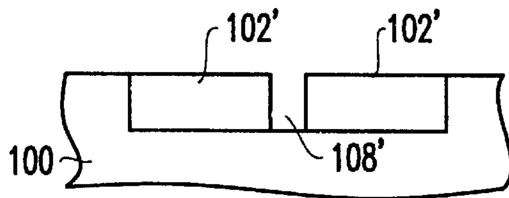

FIG.5B

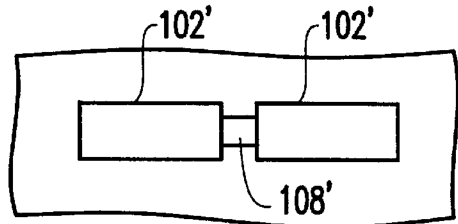

FIG.6B

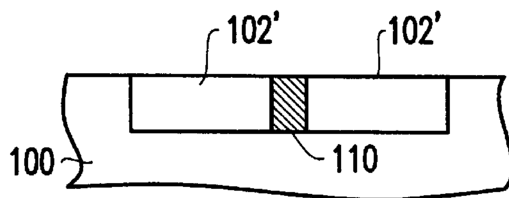

FIG.5C

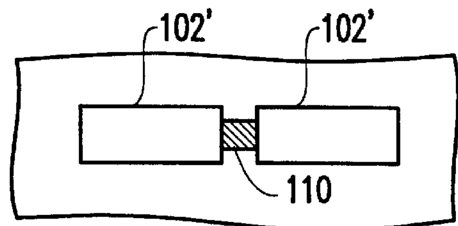

FIG.6C

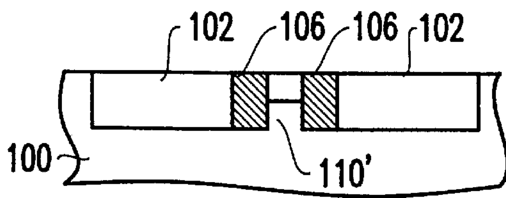

FIG.7A

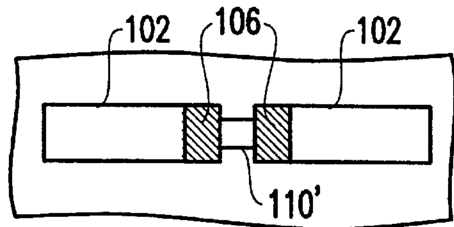

FIG.7B

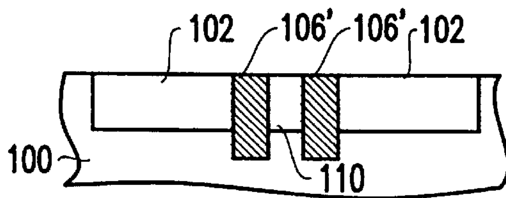

FIG.8A

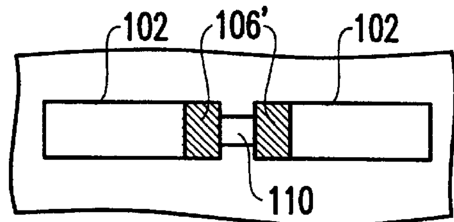

FIG.8B

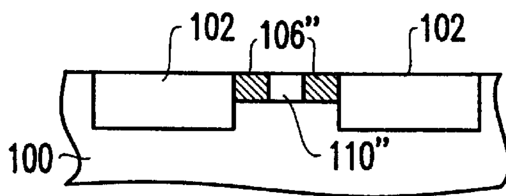

FIG.9A

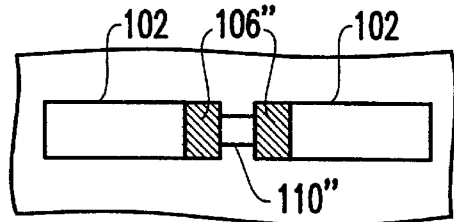

FIG.9B

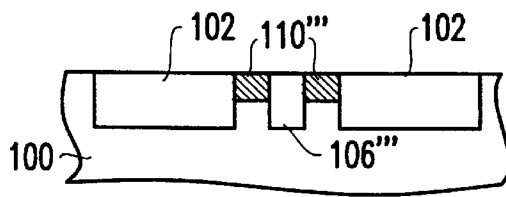

FIG.10A

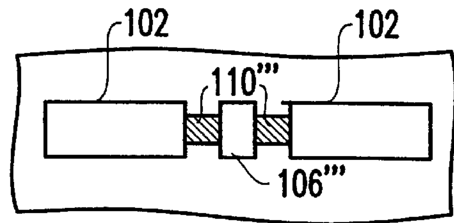

FIG.10B

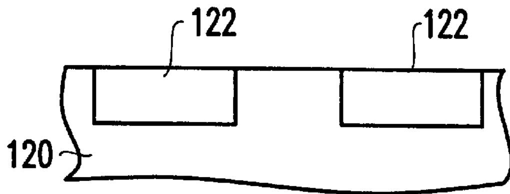

FIG.11A

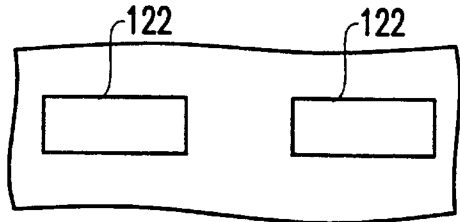

FIG.12A

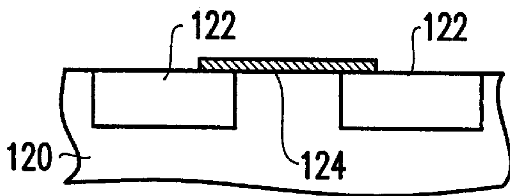

FIG.11B

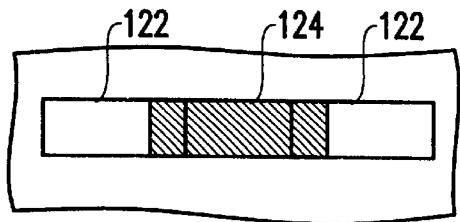

FIG.12B

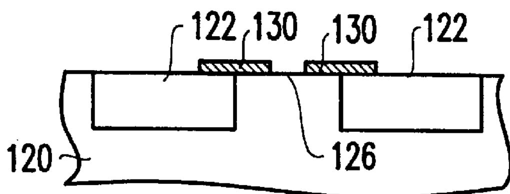

FIG.11C

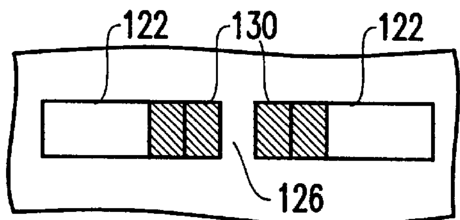

FIG.12C

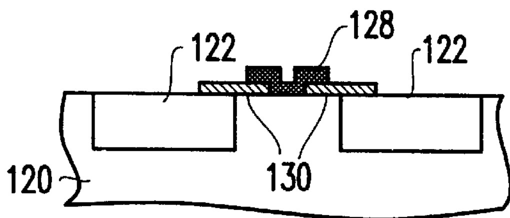

FIG.11D

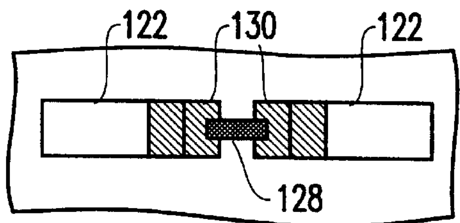

FIG.12D

MICRO FUSIBLE LINK FOR SEMICONDUCTOR DEVICES AND METHOD OF MANUFACTURE

This application is a division of U.S. patent application Ser. No. 09/074,353 filed May 7, 1998.

BACKGROUND OF THE INVENTION

1. Fieid of the Invention

The present invention is related to semiconductor devices with heat-fusible elements and, more particularly, to a method of forming heat-fusible elements on integrated circuit (IC) chips.

2. Background Description

Semiconductor fusible links are used for both activating redundancy in memory chips and for programming functions and codes in logic chips. Typical fusible links may are large structures blown by eternal heat, e.g. from a laser, or from electrical current passed through the fuse.

A typical laser blown fuse is 1 μm wide by 8 μm long. Also, because of the size of the laser spot used to program the fuses, laser blown fuse links must be spaced some distance apart (approximately 10 μm) and, in some instances, guard structures must be placed between fuses to prevent damage to adjacent fuses.

Typically, state of the art electrically blown fusible links, must not melt at normal operating current/voltage chip conditions to avoid inadvertently blown fuses. So, state of the art electrically programmed fuses require relatively large currents to open the fuse link. Therefore, higher current/voltage levels are supplied, typically, by external sources to program electrically blown fuses.

One way of facilitating melting fuse links is to provide a resistive heat source under the fusible link. See, for example, U.S. Pat. No. 4,814,853 entitled "Semiconductor Device With Programmable Fuse" to Uchida. Uchida teaches placing a fusible link on a thin insulator above a resistive wire. The resistive wire heats the fusible link to near its melting point and current passing through the link opens it. Unfortunately, Uchida requires that two sets of wires be provided to each fusible link, one for the fusible link and the other for the heater. Also, some of the heat generated in the resistive wire is partially thermally insulated by the insulating film dissipates into the chip below it.

Consequently, state of the art fusible link structures currently use a significant amount of chip surface area. Space is also required to provide clearance for the physical disruption of the link and its surrounding area that may occur when the fusible link is blown. Thus, the area above and around the fusible link must be kept clear. There is a limit to wiring that can occur under the fusible link as well. As circuit density increases and chip sizes decreases, the area occupied by large fusible links remains a problem.

Thus, there is a need for a very small and compact fusible link that uses less chip surface space.

SUMMARY OF THE INVENTION

It is a purpose of the invention to provide an electrically fusible link that is small in size;

It is another purpose of the present invention to allow more and/or denser arrangements of fusible links;

It is yet another purpose of the present invention to reduce the current/voltage required to fuse fusible links.

The present invention is an electrically programmed fuse and the method of manufacture thereof. The preferred fuse structure includes a high melting point heater element in series with a low melting point fusible link. The heater element has a higher resistivity and larger cross-sectional area than the fusible link in order to withstand heat that the heater element generates to bring the fusible link to its melting point, with a thermal mass of the heater element being sufficient to melt the fusible link. The fuse may be formed on or in the surface of an integrated circuit (IC) chip. Preferred fuse dimensions (width and length) are each between 0.1 and 1 micron.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

FIGS. **1**A–E show the steps of a first preferred embodiment method of forming fuses through a cross-sectional area of a semiconductor chip;

FIGS. **2**A–E show a top view of the steps of the first preferred embodiment method of forming fuses at each of/the steps of FIGS. **1**A–E;

FIGS. **3**A–E show the steps of a second preferred embodiment method of forming fuses through a cross-sectional area of a semiconductor chip;

FIGS. **4**A–E show a top view of the steps of the second preferred embodiment method of forming fuses at each of the steps of FIGS. **3**A–E;

FIGS. **5**A–C show the steps of a third preferred embodiment method of forming fuses through a cross-sectional area of a semiconductor chip;

FIGS. **6**A–C show a top view of the steps of the third preferred embodiment method of forming fuses at each of the steps of FIGS. **5**A–C;

FIGS. **7**A–B show a first variation of the preferred embodiment fuse;

FIGS. **8**A–B show a second variation of the preferred embodiment fuse;

FIGS. **9**A–B show a third variation of the preferred embodiment fuse; FIGS. **10**A–B show a fourth variation of the preferred embodiment fuse;

FIGS. **11**A–D show the steps of an alternate embodiment method of forming fuses through a cross-sectional area o a semiconductor chip; and

FIGS. **12**A–D show a top view of the steps of the alternate embodiment method of forming fuses at each of the steps of FIGS. **11**A–D.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Referring now to the drawings, and more particularly to FIG. **1**A–E which show the steps of a first preferred embodiment method of forming fuses through a cross-sectional area of a semiconductor chip. FIGS. **2**A–E show a top view of the steps of the first preferred embodiment method of forming fuses at each of the steps of FIGS. **1**A–E.

First, in FIGS. **1**A and **2**A an oxide surface layer **100** is recessed and metal contacts **102** are formed in the recessed surface. Preferably, the metal contacts **102** are copper, aluminum, tungsten or, composite films of Ti/AlCu, Ti/TiN/AlCu or any suitably metal or metal alloy. Next, in FIGS. **1**B and **2**B trenches **104** are formed in oxide surface layer **100** between two contacts **102**, spaced apart by 0.1–1.0 μm of

oxide. In,FIGS. **1**C and **2**C, trenches **104** are filled with resistive element **106**, and in FIGS. **1**D and **2**D a second trench **108**, preferably as deep as trenches **104** (0.5–2.0 μm) is formed between the resistive elements **106**. Finally, in FIGS. **1**E and **2**E fuse material **110** is deposited into the second trench **108**.

The volume of the preferred fusible element **110** is minimized, while its contact area with the resistive element is maximized. The preferred width and length of the fusible link in FIG. **2**E is between 0.1–1.0 μm. When passing current through the preferred fusible link, most heat generated in resistive heating elements **106** is thermally insulated from other structures and so, dissipates into the fusible links **110** and the contacts **102**, which have a high thermal mass compared to the fusible links **110**. Consequently, the fusible link's temperature will be higher than the contacts **102** or the resistive heating elements **106**.

Preferably, the resistive element **106** (or heater element) of the fusible link has a high melting point and a high resistivity. The resistive element **106** generates heat easily but does not dissipate heat by changing states, i.e., by melting. Therefore, energy so generated transfers to the fusible element **110** sandwiched between and in contact with heating elements **106**. Thus, the preferred fusible element **110** is selected to have a comparatively low melting point. Also, the preferred fusible element **110** has a comparatively high resistivity, although a low resistivity is acceptable.

Suitable preferred resistive element **106** materials include:

Material	Melting Point	Resistivity Ω-cm
Tantalum	2996° C.	13×10^{-6}
Titanium	1800° C.	
Tungsten	3370° C.	5×10^{-6}
Titanium Nitride	2930° C.	21.7×10^{-6}
Titanium Nitride	3090° C.	135×10^{-6}
Titanium Silicide	1540° C.	123×10^{-6}
Titanium Silicide	2050° C.	33×10^{-6}
Doped Polysilicon	1420° C.	1×10^{4} Intrinsic 1×10^{2} @ 10^{14} atm/cm^3 1 @ 10^{16} atm/cm^3 1×10^{-2} @ 10^{18} atm/cm^3 1×10^{-4} @ 10^{21} atm/cm^3

Suitable preferred fusible link **110** materials include:

Material	Melting Point	Resistivity Ω-cm
Copper	1083° C.	2×10^{-6}
Aluminum	660° C.	2.8×10^{-6}
Bismuth	271° C.	120×10^{-6}
Indium	156° C.	8×10^{-6}
Tin	231° C.	11.5×10^{-6}

Preferably, materials with a melting point that falls between characteristically low melting point (LMP) and high melting point (HMP) materials may be used either for the heater elements **106** or the fusible link **110**, depending upon the material composition of the other element. For example, lightly doped or intrinsic polycrystalline silicon (poly-Si) may be used as the HMP heater element **106** when combined with a fusible link **110** of an LMP metal such as tin. Alternatively, more heavily doped poly-Si can be used as the fusible link **110** in combination with a heater element **106** of tungsten.

FIGS. **3**A–E show the steps of a second preferred embodiment method of forming fuses through a cross-sectional area of a semiconductor chip. FIGS. **4**A–E show the steps of the second preferred embodiment method of forming fuses at each of the steps of FIGS. **3**A–E. The second preferred method is essentially the same as the first except that the fusible element **110** is formed immediately after forming contacts **102**, instead of last. Thus, FIGS. **3**B–C and **4**B–C correspond to FIGS. **1**D–E and **2**D–E, respectively, and FIGS. **3**D–E and **4**D–E correspond to FIGS. **1**B–C and **2**B–C, respectively. The second preferred method provides better dimensional control for the fusible link **110**.

Alternatively, the fusible link of either embodiment may be of the same material as the contact **102**. Thus, for example, both may be copper.

FIGS. **5**A–C show the steps of a third preferred embodiment method of forming fuses through a cross-sectional area of a semiconductor chip. FIGS. **6**A–C show the steps of the second preferred embodiment method of forming fuses at each of the steps of FIGS. **5**A–C. In this embodiment, the contacts **102**' are extended and also act as a resistive element, eliminating the requirement for a separate resistive heating elements **106** of the first two preferred embodiments. For this preferred embodiment, it is critical for the contact/resistive element **102**' to have a melting point much higher than the fusible link **110** material. The preferred fusible link **110** material for this embodiment is bismuth, which has high resistivity and a low melting point compared to other materials.

FIGS. **7**A–B, **8**A–B, **9**A–B and **10**A–B show two variations on fusible links made according to the first two preferred embodiments. In these variations, the size ratio of the resistive elements **106**, **106**', **106**" and **106**"' to the fusible element **110**', **110**, **110**" and **110**"', respectively, is maintained or increased. Thus, in FIGS. **7**A–B, the depth of the fusible link **110**' is reduced and in FIGS. **8**A–B resistive elements **106**' are extended. In FIGS. **9**A–B, the depth of both the resistive elements **106**" and the fusible link **110**" is reduced to reduce the possibility of damage to underlying structures during programming. In FIGS. **10**A–B, the location of heater element **106**"' is swapped with and surrounded by two fusible links **110**"'.

FIGS. **11**A–D show-the steps of an alternate embodiment method of forming fuses through a cross-sectional area of a semiconductor chip. FIGS. **12**A–D show the steps of the alternate embodiment method of forming fuses at each of the steps of FIGS. **11**A–D. In this embodiment, in FIGS. **11**A and **12**A contacts **122** are formed in an oxide layer **120**. In FIGS. **11**B and **12**B, a strip of resistive material **124** is formed on the oxide layer **120** spanning oxide between the metal contacts **122**. In FIGS. **11**C and **12**C a gap **126** is formed in the resistive strip **124**. Finally, in FIGS. **11**D and **12**D, a fusible element **128** is formed over the gap **126** on the oxide layer **120** between resistive element segments **130**. In this embodiment, it is preferable that the fusible element be thin as well as narrow. The preferred fusible link's width and thickness is between 0.1–2.0 μm and most preferably, 0.1–0.5 μm.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

We claim:

1. A fusible link comprising:

a resistive element;

a fusible element contacting said resistive element, whereby a programming current passing through said

resistive element and said fusible element heats said resistive element to a temperature at least at the melting point of said fusible element, heat from said resistive element and said programming current opening said fusible element.

2. The fusible link of claim **1**, wherein said resistive element is a pair of resistive elements on opposite sides of said fusible link.

3. The fusible link of claim **1**, wherein said fusible link is a pair of fusible links on opposite sides of said resistive element.

4. The fusible link of claim **2**, wherein said fusible link has a surface area between 0.01–1 μm^2.

5. The fusible link of claim **2** wherein the resistive element material is selected from the group consisting of tantalum, titanium, tungsten, titanium nitride, titanium silicide and doped polysilicon.

6. The fusible link of claim **2** wherein the fusible link material is selected from the group consisting of copper, aluminum, bismuth, indium and tin.

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