United States Patent

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[54] **LINEAR ERROR COMPENSATOR FOR NUMERICALLY CONTROLLED MACHINE TOOLS**
4 Claims, 11 Drawing Figs.

[52] **U.S. Cl.** **235/151.11,** 318/600, 318/569
[51] **Int. Cl.** **H02p 1/54,** G06f 15/46
[50] **Field of Search** 235/151.1, 151.11; 318/567, 569, 600

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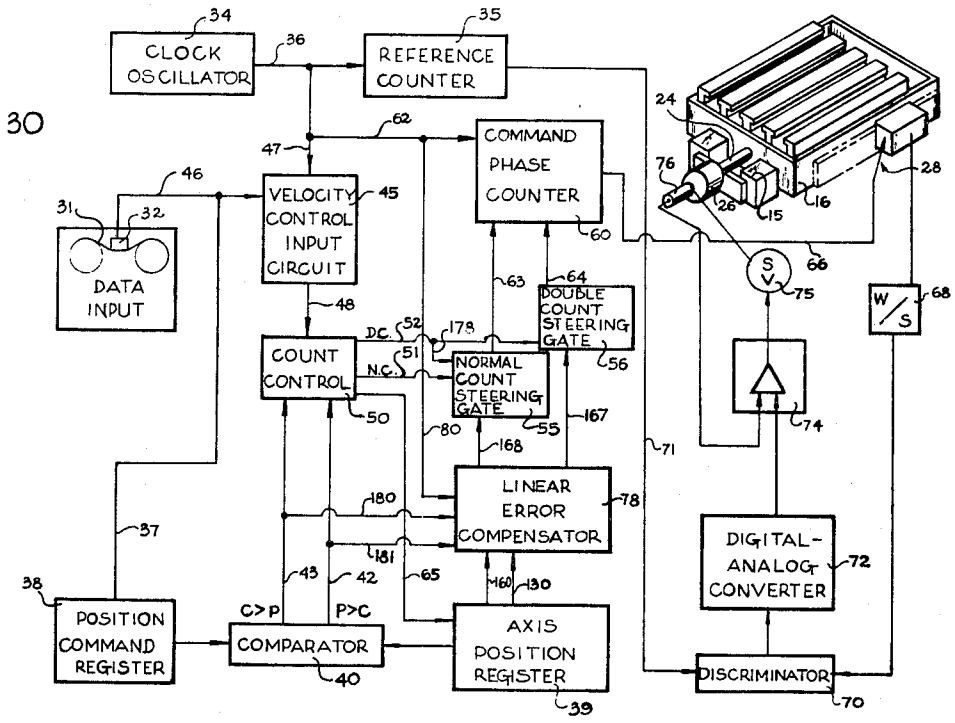
ABSTRACT: Within a pulse-counting numerical control system for a machine tool, a signal modifier is connected to effect the addition or subtraction of a predetermined number of pulses to the control system to compensate for repeatable linear errors that may appear in the machine's slidable members.



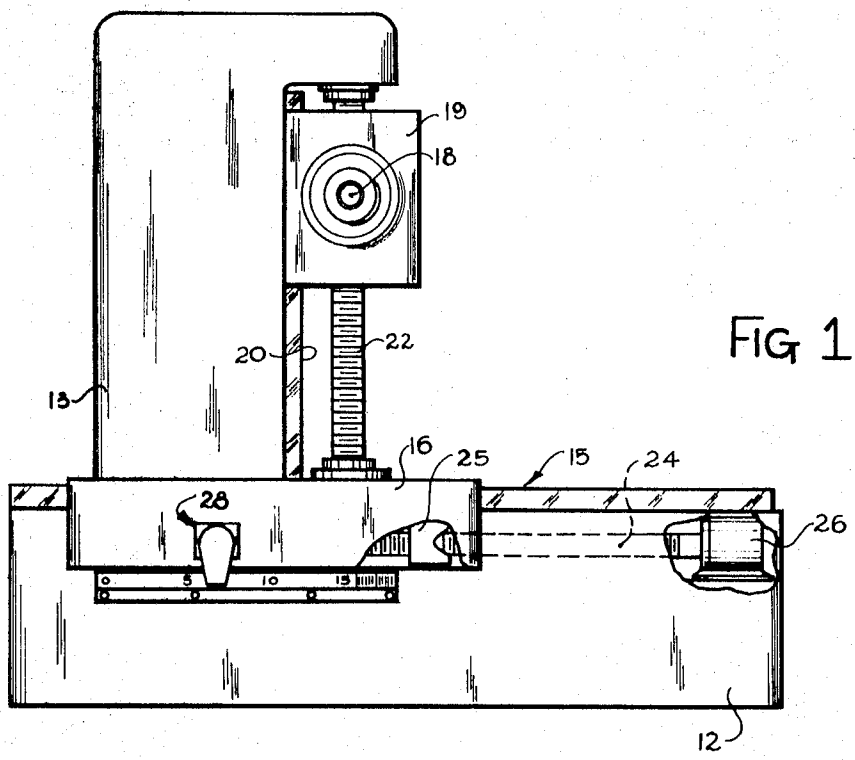


FIG 1

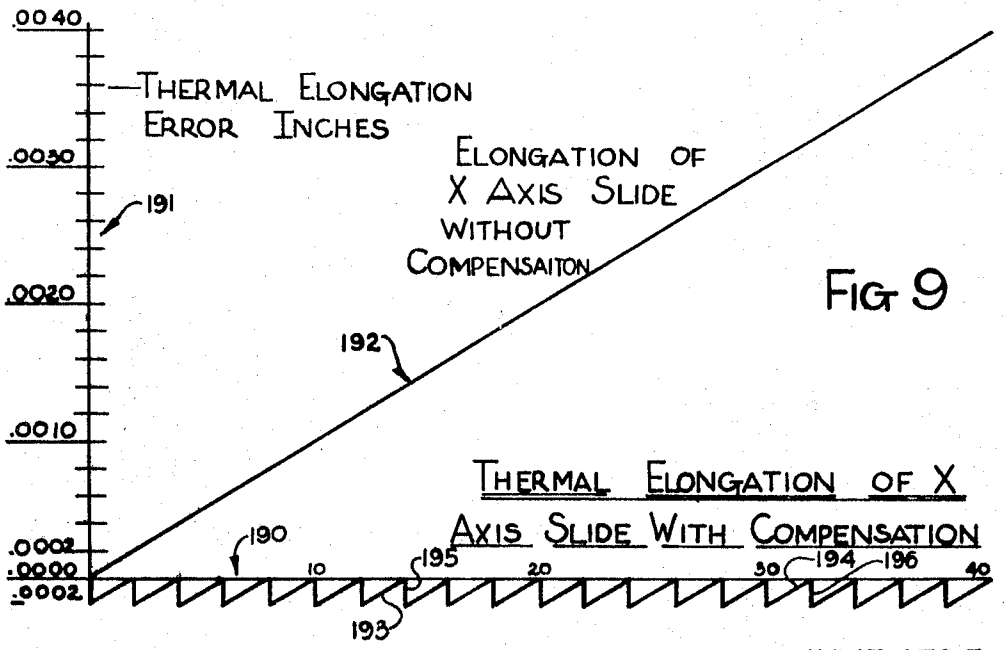


FIG 9

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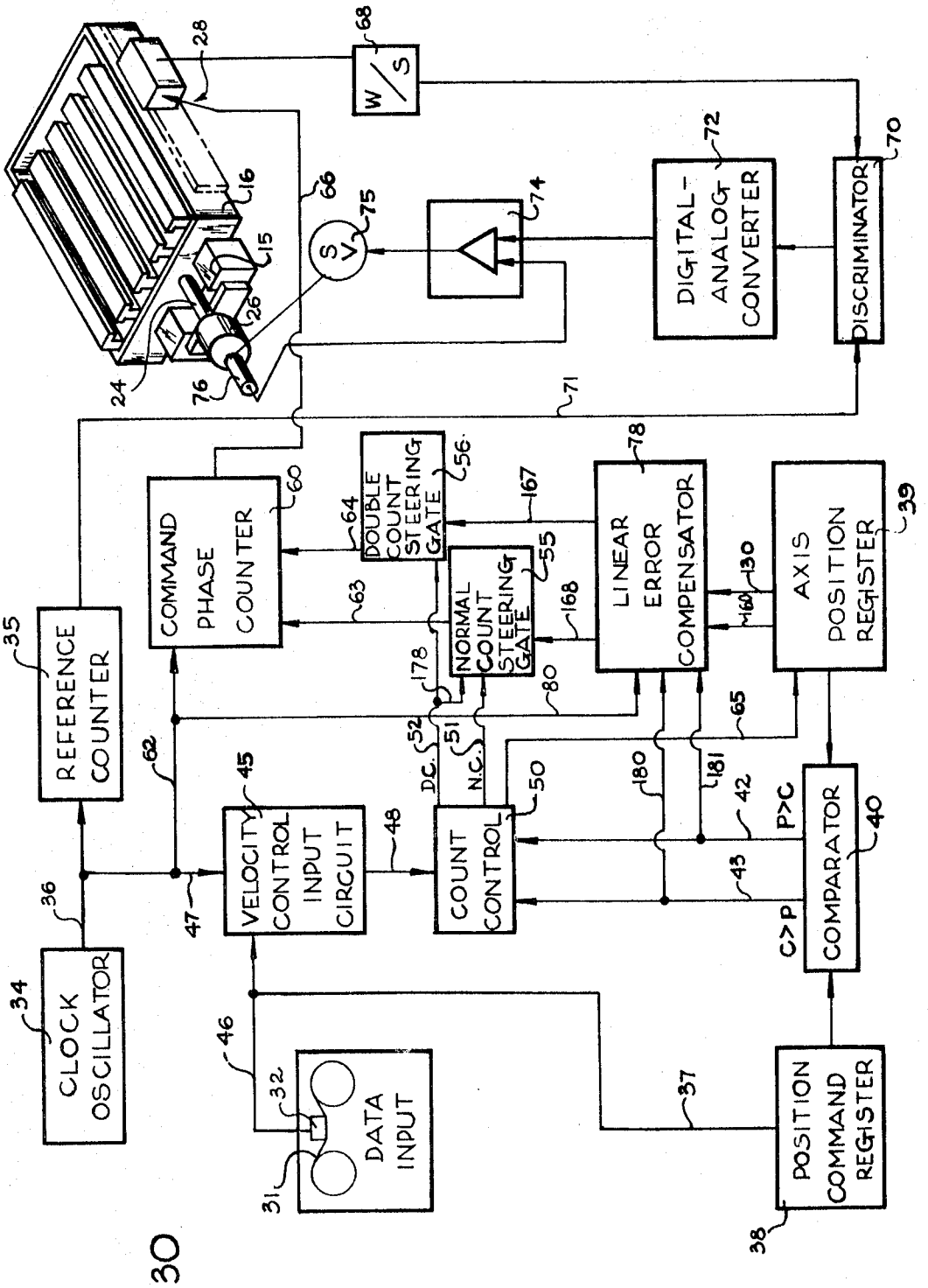

FIG 2

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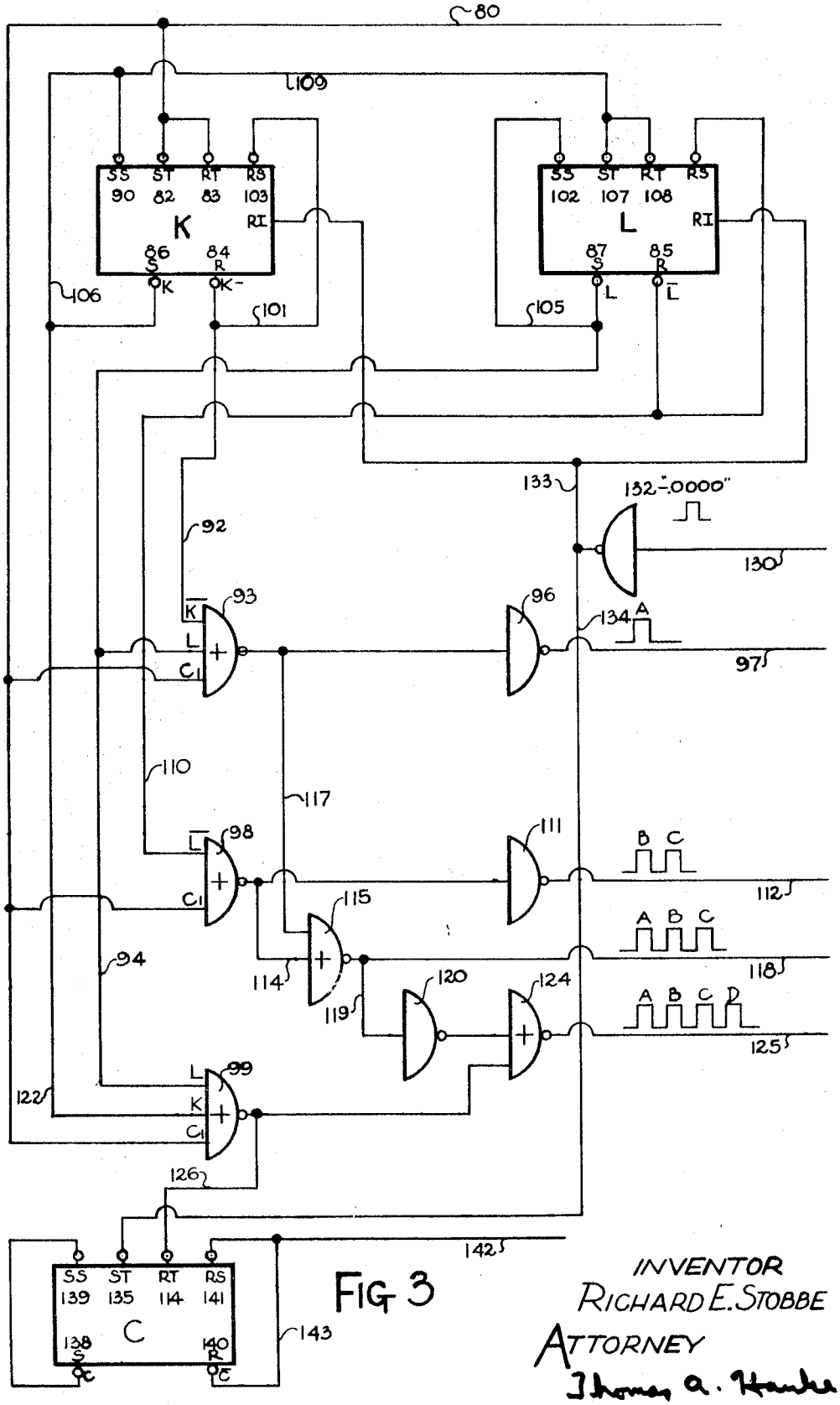

FIG 3

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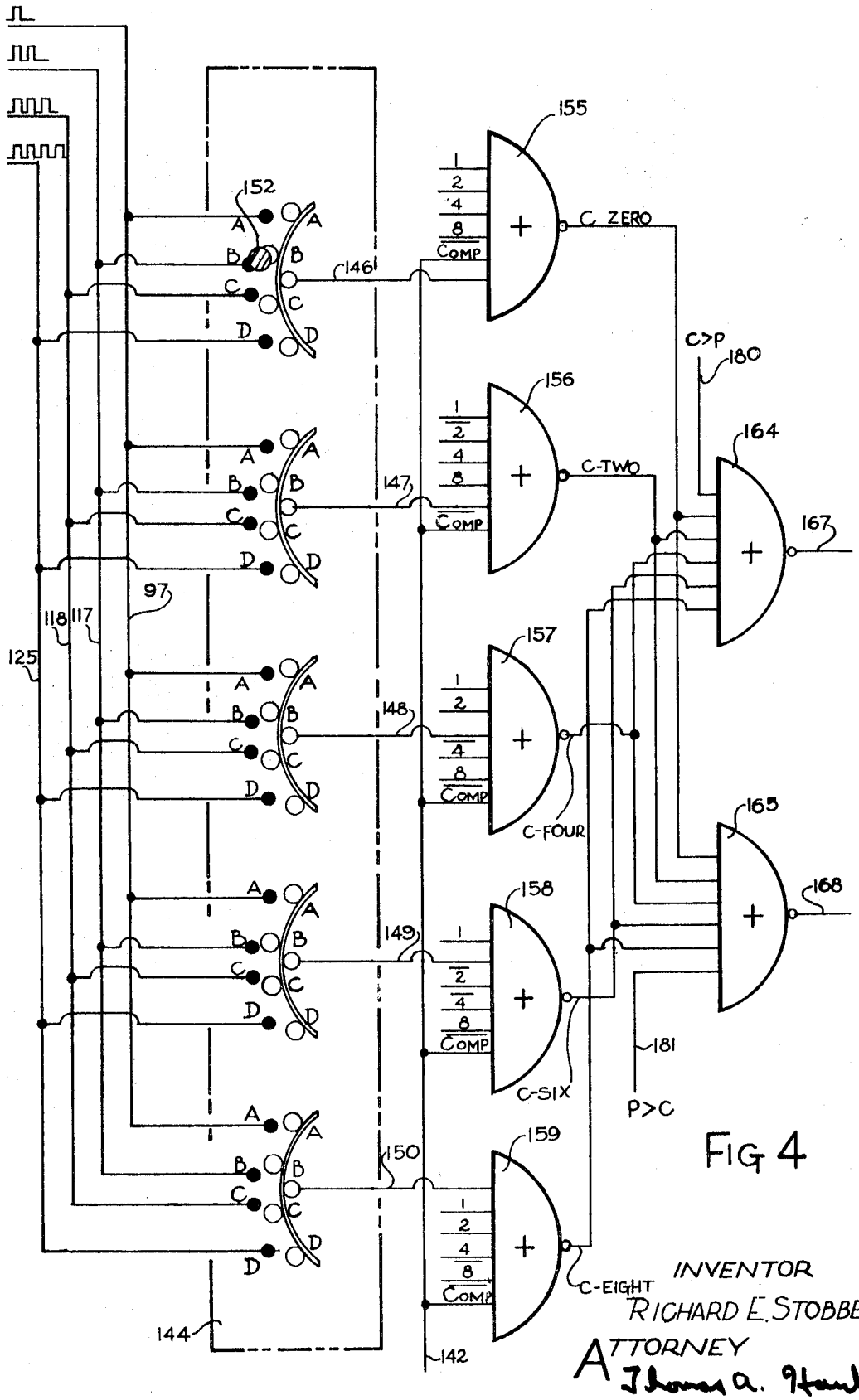

FIG 4

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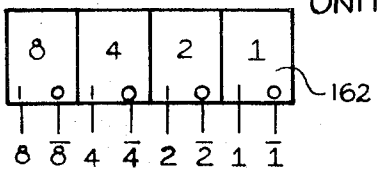

FIG 8A

FIG 8B

INPUT PULSES	FLIP FLOP STATE				REPRESENTS BINARY	REPRESENTS DECIMAL
0	$\bar{8}$	$\bar{4}$	$\bar{2}$	$\bar{1}$	0 0 0 0	0 (ZERO)
1	$\bar{8}$	$\bar{4}$	$\bar{2}$	1	0 0 0 1	1
2	$\bar{8}$	$\bar{4}$	2	$\bar{1}$	0 0 1 0	2
3	$\bar{8}$	$\bar{4}$	2	1	0 0 1 1	3
4	$\bar{8}$	4	$\bar{2}$	$\bar{1}$	0 1 0 0	4
5	$\bar{8}$	4	$\bar{2}$	1	0 1 0 1	5
6	$\bar{8}$	4	2	$\bar{1}$	0 1 1 0	6
7	$\bar{8}$	4	2	1	0 1 1 1	7
8	8	$\bar{4}$	$\bar{2}$	$\bar{1}$	1 0 0 0	8
9	8	$\bar{4}$	$\bar{2}$	1	1 0 0 1	9

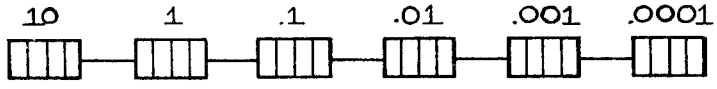

FIG 8

FIG 3	FIG 4

FIG 5

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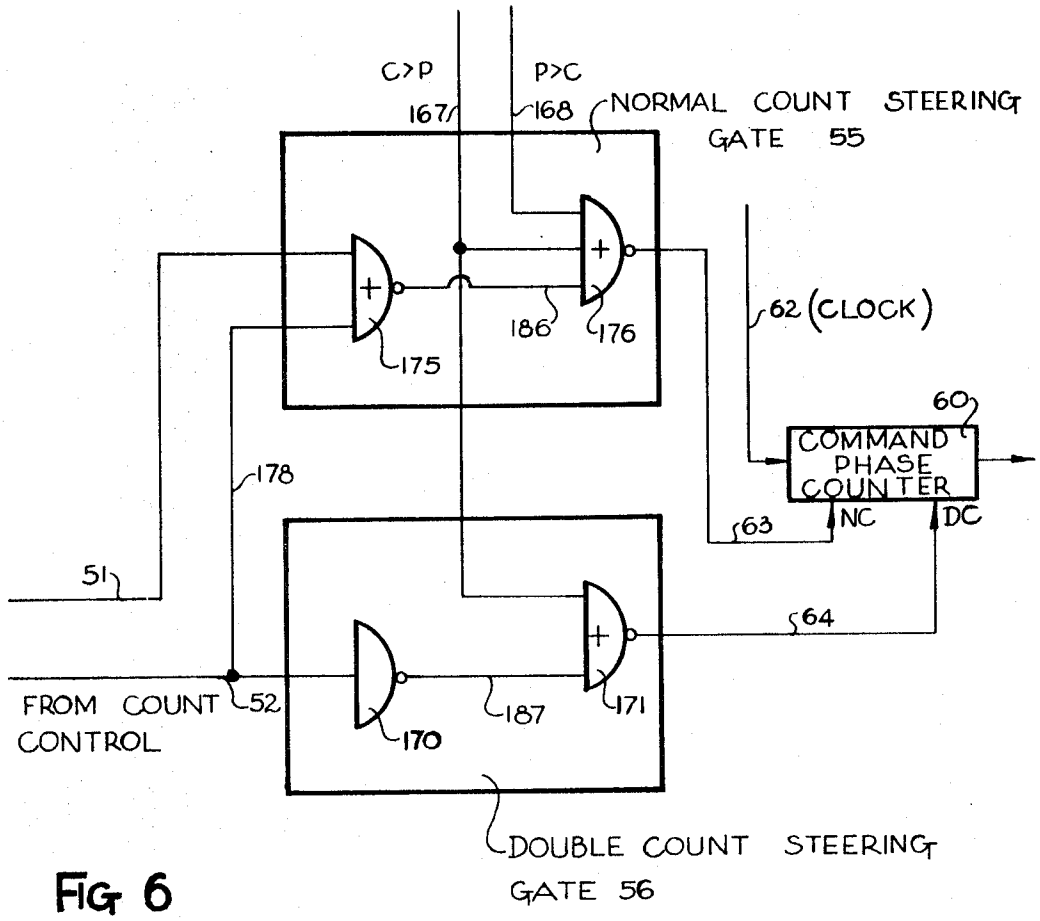

FIG 6

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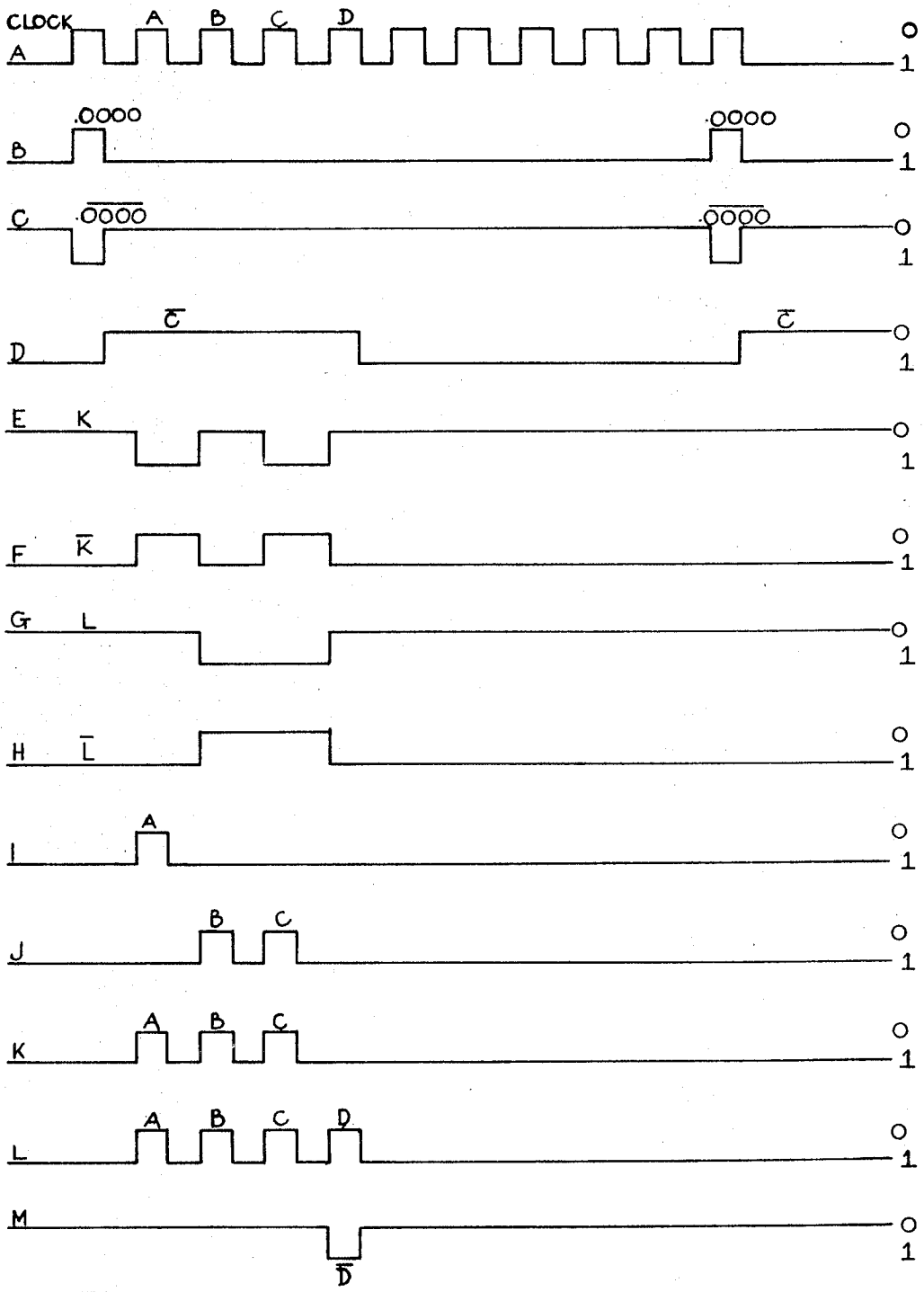

FIG 7

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LINEAR ERROR COMPENSATOR FOR NUMERICALLY CONTROLLED MACHINE TOOLS

BACKGROUND OF THE INVENTION

The present invention relates generally to precision positioning control circuitry for a machine tool and more particularly to an electrical compensating circuit for modifying a positional control signal to effect a correction for repeatable linear errors such as the dimensional changes in the machine structure due to changes induced into the structure by operating temperature changes.

Before this invention, gating circuitry was interconnected with the position register of the numerical control system, to provide a controlling signal to effect actuation of an error compensator. The error compensator then being operative to signal the occurrence of compensating control pulses at certain predetermined increments of machine member movement. Gating circuitry had to be provided for each spaced-apart increment of travel along the total range of member movement at which compensation was desired. As the range of machine member movement is ever increasing in the machine tool industry, the gating circuitry is becoming a more and more costly item to supply. The present invention overcomes the problem of mounting gating circuitry costs by providing a linear error compensator that uses a minimum of gating circuitry components.

SUMMARY OF THE INVENTION

According to this invention, there is provided a machine tool comprising a pair of members carried for relative movement; a servomotor connected to effect relative movement between the said members; a numerical control system operative to provide output command signals connected to actuate the servomotor for effecting predetermined relative movement between the members; and a linear error compensator actuated in response to predetermined incremental relative movement between the members and arranged to vary the output of the command signals from the control system, selectively and predeterminately.

A principal object of this invention is to provide an electrical error compensator for a numerical control system of a machine tool.

Another object of the invention is to provide an auxiliary signal controller operable to compensate for thermal distortion in the cooperatively associated part of a machine tool.

Another object of the invention is to provide a signal modifier predeterminately operative to modify a positional command signal from a numerical control system.

Another object of this invention is to provide a signal modifier that materially reduces the number of components used to correct for linear machine errors thereby effecting a substantial reduction in the manufacturing cost.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a view in front elevation of a machine tool incorporating the invention;

FIG. 2 is a schematic diagram of a numerical control system which incorporates the invention in combination with a movable member;

FIGS. 3 and 4, taken together as shown in FIG. 5, present the detailed logic circuit of the linear error compensator in accordance with the principles of the invention;

FIG. 6 is a schematic representation of the normal and double count steering gates of FIG. 1;

FIG. 7 is a timing diagram of the waveforms useful in explaining the action of the linear error compensator circuit;

FIG. 8 shows the symbolic representation of six decades of the axis position register, with each decade having a distinct decimal weighting;

FIG. 8A shows the symbolic representation of a binary-coded-decimal counter;

FIG. 8B is a table of binary-coded-decimal states of the decade representing the unit decimal digits; and,

FIG. 9 is a graph showing the thermal elongation of the X-axis slide with and without compensation.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, and more specifically to FIG. 1 thereof, illustrating a machine tool incorporating the features of the present invention. As there shown, the machine tool is provided with a horizontally extending bed **12** and a vertical upright or column **13** secured thereto constituting a principal support frame. Horizontal ways **15** presented by the upper portion of the bed **12** slidably support a worktable **16** for selective horizontal movement. The usual gibs (not shown) are arranged in well-known manner to retain the worktable **16** in slidable engagement with the horizontal bed ways **15** for movement along the horizontal X-axis.

A rotatable tool-receiving spindle **18** is journaled to rotate about a horizontal axis in a spindle head **19** mounted for vertical sliding movement along vertical ways **20** presented by the column upright **13**. For effecting selective vertical movement of the spindle head **19**, a rotatable elevating screw **22** journaled at its opposite ends in an overhanging portion of the column **13** and the bed **12** engages a cooperating nut (now shown) carried by the spindle head **19**. The usual power drives (not shown) are respectively connected to rotate the tool spindle **18** at a selected rate, and to rotate the elevating screw **22** for effecting vertical movement of the spindle lead **19**.

Thus, to perform machining operations, the tool spindle **18** is selectively movable along a vertical axis relative to a workpiece (not shown) secured to the worktable **16** which is movable along the horizontal axis. For moving the worktable **16**, an internally threaded nut **25** fixedly secured thereto is threadedly engaged by a cooperating rotatable translating screw **24** journaled to rotate in the bed **12**. A servomotor **26** mounted within the rightward end of the bed **12** is connected to rotate the table screw **24** for moving the worktable **16** at a selected rate and in a selected direction of movement along the X-axis.

A linear position feedback transducer **28** is operatively interconnected between the bed **12** and horizontally movable worktable **16** carried thereby, as shown in FIG. **1**. The position feedback transducer **28** can be of a bridge network type as shown and described in U.S. Pat. No. 3,010,063 issued to J. M. Rhodes on Nov. 21, 1961, or of a Selyn type, both of which are well-known in the art.

The numerical control system **30** schematically illustrated in FIG. **2** is of the well-known pulse-counting type produced commercially by several different manufacturers and incorporating well-known digital techniques. To employ digital control techniques, the numerical control system includes a means to generate the pulse signals. These pulses are cyclical in nature with each complete cycle or pulse of the signal representing an increment of movement of the working tool or the workpiece. For example, each pulse signal when utilized by the control and applied to the machine tool may cause 0.0001 inch of movement of the worktable **16** mounting the workpiece.

The number of pulses so generated may thus be considered a function of the amount of movement of the worktable since each pulse causes a certain incremental movement. Likewise, the rate of frequency at which the pulses are generated is a function of the velocity of the worktable as the pulse rate represents the number of incremental movements per unit of time.

The numerical control system, shown in FIG. **2**, controls the relative position of the worktable **16** by keeping track of the total number of pulses generated, for example, by feeding the counts to counters or registers. Thus, a counter controlling movement along the X-axis will receive 10,000 counts for each inch of travel of worktable **16** along that axis. By the use of preset counters or comparators, which provide an actuating signal after the preset count is attained in the counter, control may direct worktable **16** into a desired location by moving the

worktable until the preset count is recorded on the counter. The actuating signal from the counter is then used to arrest the movement of the worktable.

In a similar manner, control **30** controls the velocity or rate of movement of worktable **16** along the X-axis by means of circuitry responsive to the frequency at which the pulses are generated, or the pulse rate. The responsive circuitry moves worktable **16** through the number of incremental movements per unit of time corresponding to the pulse rate.

A program is encoded or punched on a tape **31** so as to provide data input signals to control **30** by means of a tape reader **32**. In addition to the tape reader **32**, the input circuitry to control **30** includes a clock oscillator **34**. Clock oscillator **34** produced stable high-frequency pulse signals, for example, a pulse train having a frequency of 250 kilohertz. Each pulse of this pulse train when employed by control **30** represent 0.0001 inch of movement of the worktable **16**. The pulse signals from clock oscillator **34** are in the form of symmetrical square waves; that is, the interval of each pulse signal, or the pulse width, is equal to the interval between pulses.

The pulses are formed by periodically changing the output state of clock oscillator **34** from one state to another state. For example, the clock oscillator may initially provide no output signal, then provide an output signal for the interval of a pulse, then revert to a state of providing no output signal for a similar interval, then provide an output signal for the interval of a second pulse, and so on. Only the provision of the output signal is important to digital control, not the magnitude thereof. In digital control terminology, the two states of the output signal of the clock oscillator and other components of control **30** are termed the logic 1 signal state and the logic 0 signal state. It may be noted that, depending on the type of digital control technique utilized the logic signal state may or may not correspond to the electrical signal state. Thus, a logic 1 signal may indicate the presence of an actual electric signal or may indicate the absence of an actual electrical signal.

The output from clock oscillator **34** is supplied to other portions of control **30** and to reference counter **35**, via conductor **36**. Reference counter **35** produces a plurality of lower frequency of pulse signals which are employed by the other components of control **30**.

For reasons of simplicity, FIG. **2** shows the position control circuitry and the velocity control circuitry for only one axis of movement of machine tool. Thus, the position control circuitry and the velocity control circuitry controlling and regulating the position and velocity of worktable **16** along the X-axis of the machine tool are shown in FIG. **2**.

Tape reader **32** provides a position command signal via conductor **37** to position command register **38**. This input signal presets that register or counter in accordance with the desired position of worktable **16** on the X-axis.

The position control circuitry also includes an axis position register **39** which records the actual movement of worktable **16** in terms of the pulse signals representing 0.0001 inch of movement. Since one pulse signal or count from clock oscillator **34** represents 0.0001 inch of movement, to command a movement of worktable **16** one inch along the Y-axis, 10,000 counts must be added to or subtracted from the count on position register **39**. Whether the counts will be added or subtracted depends on the desired direction of movement of worktable **16**. The pulse signals or counts are supplied to axis position register **39** in a manner hereinafter described.

The output signal from position command register **38** and axis position register **39** are supplied to a comparator **40** which determines whether the number of counts in the axis position register **39** is greater or less than the number of counts in the position command register **38**. Comparator **40** provides an output signal to conductor **42** indicating that the position registered in the axis position register **39** is greater than the position registered in the command position register **38**. Comparator **40** provides an output signal to conductor **43** indicating the position registered in the axis position register **39** is less than the position registered in the axis position register **38**. When the position registered in the axis position register **39** equals the position registered in the command position register **38**, indicating that worktable **16** is in the command position, comparator **40** provides a signal in conductors **42** and **43** which operates control **30** to stop the movement of worktable **16**.

As previously noted, control **30** employs the frequency at which the pulses representing 0.0001 inch of movement are generated to control the velocity of worktable **16**. As control **30** moves worktable **16** 0.0001 inches for every such pulse generated, the greater the number of pulses generated per unit of time, the greater the number of incremental movements per unit of time and the greater the velocity of worktable **16**.

To detect the frequency of rate at which pulses are being generated, the velocity control circuitry of control **30** employs a pair of low-frequency pulse trains as carrier signals. The phase of this signal remains constant. The other carrier signal is responsive to the rate of pulse generation and the phase of this other carrier signal may be phase shifted at a rate equal to the rate of pulse generation.

As the rate of change of the phase shift difference between the constant phase reference carrier signal and the phase shifted carrier signal is equal to the rate of pulse generation, this rate of change may be detected and a signal corresponding thereto provided to the hydraulic motor energizing worktable **16** to move worktable **16** through the required number of incremental movements per unit of time. A feedback signal is provided in the velocity control circuitry of control **30** to indicate actual movement of worktable **16**, also in terms of a phase shift of the second carrier signal. In the normal manner of a regulator, the feedback signal operates to shift the phase of the carrier into conformity with the phase of the reference carrier signal, thereby indicating that the worktable **16** is moving at the desired velocity.

The velocity control circuitry of control **30** includes a velocity control input circuit **45** which receives and stores the velocity input command signals from tape reader **32**, via conductor **46**.

The velocity input circuitry **45** also receives the high frequency pulse signals from clock oscillator **34**, via conductor **47**. These high frequency pulse signals are formed by velocity control input circuit **45** into an output pulse train, the frequency, or rate of pulse generation, of which corresponds to the desired speed of worktable **16**. For example, velocity control input circuit **45** may reduce the 250 kilohertz pulse train of clock oscillator **34** to a 10 kilohertz output signal. The 10 kilohertz frequency of this signal represents a desired speed of one inch per second of worktable **16**, since 10,000 pulses are being generated each second, each pulse being equal to 0.0001 inches of movement of worktable **16**.

The pulse train output signal of velocity control input circuit **45** in conductor **48** and the output signals from comparator **40** are supplied to count control circuit **50**. Count control circuit **50** thus receives an input signal relating to the desired rate of movement of worktable **16**, as provided by the 10 kilohertz pulse train from velocity control input circuit **45** and a signal relating to the direction of such movement, as provided by comparator **40**. Circuit **50** provides an output signal in conductors **51** and **52** in response to the input signals thereto which controls the operation of a normal count steering "gates" **55** and a double-count steering "gates" **56**, respectively, which in turn control the operation of command phase counter **60**.

Command phase counter **60** generates the second or phase shifted carrier signal employed by the velocity control circuitry of control **30**. Command phase counter **60** receives the 250 kilohertz pulse train from clock oscillator **34**, via conductor **62** and divides this 250 kilohertz input signal by 1,000 to produce a 250 hertz low-frequency pulse train carrier signal. The input signal from count control circuit **50** operates command phase counter **60** to advance or retard the phase of the 250 hertz carrier signal at a rate equal to the frequency of the pulse train signal from velocity control input circuit **45**. The

direction in which the signal is shifted, that is, whether the signal is advanced or retarded in phase, is determined by a signal from comparator **40** to count control circuit **50** and determines the direction of movement of worktable **16**.

To advance or retard the phase of the 250 hertz carrier signal from command phase counter **60**, the pulse train signal from count control **50** is employed to affect the divide by 1,000 operation of command phase counter **60**, and specifically, the application of the 250 kilohertz pulses from clock oscillator **34** to the counter. If, as in the previously used example, it is desired to move worktable **16** at a velocity of one inch per second, the phase of the 250 hertz carrier signal must be phase shifted by a total of 10,000 pulses over the time period of a second. The 250 hertz carrier signal of command phase counter **60** must be phase shifted one pulse every 100 microseconds in order to provide the required phase shift rate of 10,000 pulses per second. It may be noted that a phase shift of 10,000 pulses represents a phase shift of ten complete cycles of 250 hertz carrier signal.

This phase shift is provided by utilizing the 10,000 hertz pulse train signal from count control **50** to affect the application to command phase counter **60** of one pulse out of every 25 pulses of the 250 kilohertz, or 250,000 hertz, clock oscillator **34** pulse train. If it is desired to retard the phase of the 250 hertz carrier signal of command phase counter **60**, the count control **50** generates the required signal pulses transmitted via a conductor **51** to the normal count steering "gates" **55**. From normal count "gates" **55**, the signal continues via conductor **63** to clock one out of every 25 clock oscillator pulses supplied to command phase counter **60**, thereby retarding the generation and phase of the carrier signal provided by command phase counter **60** by the amount of the one blocked clock oscillator pulse. Over the period of a second, 10,000 clock oscillator pulses supplied to command phase counter **60** will be blocked, thus providing the desired rate of change, or phase shift, to the 250 hertz carrier signal of command phase counter **60**. If it is desired to advance the phase of the 250 hertz carrier signal of command phase counter **60**, the count control **50** generates the required signal pulses transmitted via a conductor **52** to the double-count steering "gates" **56**, the signal continues via conductor **64** to operate command phase counter **60** to add the equivalent of one clock oscillator pulse every 25 clock oscillator pulses supplied to command phase counter **60**, thereby advancing the phase of the carrier signal by the amount of the added clock oscillator pulse.

As each of the 250 kilohertz clock oscillator pulses added or blocked in the advancing or retarding the 250 hertz second carrier signal of command phase counter **60** by count control **50** represents 0.0001 inch of movement of worktable **16**, a signal corresponding to the additional or blocking of these pulses is supplied via conductor **65** to axis position register **39** which records the movement of worktable **16**. The movement of worktable **16** and the addition or removal of pulses to axis position register **39** will be such as to bring the number of pulses recorded in axis position register **39** into conformity with the position recorded in position command register **38**. Thus, if the position registered in position command register **38** commands one inch of movement of worktable **16** along the X-axis, 10,000 pulses will be added to axis position register **39** by the resulting action of count control circuit **50**.

The phase shifted signal from command phase counter **60** in conductor **66** is fed to transducer **28**. Transducer **28** is responsive to the actual movement of worktable **16** along ways **15** and provides a phase shift to the output signal from command phase counter **60** proportional to this movement. This phase shift to the output signal of command phase counter **60** is opposite to the phase shift provided by count control **50** as it indicates actual movement of worktable **16**. This phase shifting of the output signal of transducer **28** is applied to the already phase shifted carrier signal of command phase counter **60** and acts to restore the 250 hertz signal from command phase counter **60** to its original phase.

The output signal from transducer **28** is supplied through a wave shaper **68** to discriminator **70**. Wave shaper **68** restores the signal from transducer **28** to a square wave signal. Discriminator **70** also receives a 250 hertz signal from reference counter **35** in conductor **71**. The 250 hertz signal to discriminator **70** from reference counter **35** forms the reference carrier signal. The phase of the reference carrier signal remains constant. Discriminator **70** acts to determine the phase difference between the constant phase reference carrier signal from reference counter **35** and the phase shifted feedback signal from transducer **28** and to supply a digital difference signal corresponding to analog converter **72**.

Digital to analog converter **72** converts the digital difference signal between the constant phase reference signal and the phase shifted feedback signal into an analog output signal proportional to the digital difference signal and capable of operating servo amplifier **74**. Servo amplifier **74**, in turn, operates servo valve **75** and hydraulic motor **26** connected to lead screw **24**, to move worktable **16** fastened to nut **25** along the screw at a velocity corresponding to the frequency of the pulse train output signal of velocity control input circuit **45**. Tachometer **76** connected to hydraulic motor **26** and servo amplifier **74** assists in the control of the velocity of worktable **16**.

FIGS. **3** and **4**, taken together as shown in FIG. **5**, present the detailed logic circuit of the linear error compensator **78**.

FIG. **3** illustrates the portion of the linear error compensator **78** which provides a plurality of compensating pulse rates which are selectively used to provide the required correction to the numerical control system **30**. The flip-flops K, L and C shown in FIG. **3** are of the standard bistable type well known in the art.

The input and output signals to the flip-flop are divided into two general groups; the "set" input signals controlling the "set" output and the "reset" input signals controlling the "reset" output signal. The set output signal and the reset output signal are mutually exclusive so that if a signal having the logic state of 1 appears at the set output terminal S, a signal having the logic state of 0 must appear at the reset output terminal R, and vice versa. When, for example, the set output signal goes from a logic 1 state to a logic 0 state, the reset output goes from a logic 0 state to a logic 1 state. When the set output goes from a logic 0 state to a logic 1 state, the reset output goes from a logic 1 state to a logic 0 state.

The state and change of the set output signal at the set output terminal S is controlled by three input signals; the set-steering signal applied to terminal SS, the set trigger signal applied to terminal ST, and the reset input signal applied to terminal RI.

The set-steering signal applied at terminal SS is so termed because it controls or steers the operation of the flip-flop. Thus, the steering signal applied to terminal SS of the flip-flop must be a logic 0 signal for the flip-flop to be operated by the set trigger signal applied to terminal ST. If the set-steering signal at terminal SS is a logic 1 signal, the set output signal at terminal S will remain in the previous state, whatever that state may be, regardless of the set trigger signal applied to terminal ST. A set-steering signal of the logic state of 1 is said to block the flip-flop. Further, when the set-steering signal at terminal SS is a logic 0 signal, and the set trigger signal applied to terminal ST is a logic 0 signal or changes from a logic 0 signal state to a logic 1 signal state, the set output signal at terminal S also remains in its previous state.

When, however, the set-steering signal is in the logic 0 signal state and the set trigger signal applied to the flip-flop at terminal ST changes from a logic 1 signal state to a logic 0 signal state, the set output signal at terminal S assumes the logic 1 signal state, if it is not already in that state. As the set output signal at terminal S and the reset signal at terminal R are mutually exclusive, the reset output signal goes to the logic 0 signal state when the set output signal goes to the logic 1 signal state. If the set trigger signal remains at the logic 0 signal state or changes from a logic 0 signal state to a logic 1 signal state, no change in the set output signal at terminal S occurs.

The reset input signal to terminal RI is not controlled or steered by the set-steering signal so that any time the reset input signal to terminal RI assumes the logic 1 signal state, the reset output signal at terminal R becomes a logic 1 signal and the set output signal at terminal S becomes a logic 0 signal.

As shown in FIG. 3, the 250 kilohertz clock signal is applied on conductor **80** to the set trigger terminal **82** and reset trigger terminal **83** of flip-flop K. The clock pulses and the interaction of the K and L flip-flops with their associated gating are used to produce four desired pulse trains. The pulse trains are comprised of one, two, three and four pulses.

Reference should be made to FIG. 7 which includes a timing diagram of the waveforms useful in explaining the operation of the linear error compensator **78**. Assuming now that the K and L flip-flops are in their reset condition with a logic 1 signal at their reset terminals **84** and **85**, respectively, and a logic 0 signal at the set terminals **86** and **87**, respectively. The reset steering signal of flip-flop K is the reset output signal of flip-flop K. Assume now the clock pulse A is supplied through conductor **80** to the set trigger **82** and reset trigger **83** of flip-flop K. Since the signal at the set steering terminal **90** of flip-flop K is at logic 0, as pulse A at the set trigger terminal **82** goes from the logic state of 1 to the logic state of 0 it will act to set flip-flop K. The reset output terminal **84** of flip-flop K is connected, via conductor **92**, to NOR gate **93** along with the set output terminal **87** of flip-flop L, via conductor **94**, and along with the clock pulse train C1. The output of NOR gate **93** is supplied through inverting gate **96** to conductor **97**. The logic 0 signal from the reset output terminal **84** of flip-flop K is to NOR gate **93** along with the clock pulse A which is in a logic 0 state. The signal from the set terminal **87** of flip-flop L which is at a logic 0 state during the duration of pulse A is also supplied to NOR gate **93**. As all three inputs to NOR gate **93** are at the logic 0 state, the state of the output signal of this gate goes to the logic state of 1. At the end of pulse A as pulse A changes from the logic state of 0 to the logic state of 1, the logic state of the output changes from logic 1 to logic 0. This single pulse is inverted by inverter gate **96** and passes along conductor **97**. Pulse A is also applied to NOR gates **98** and **99**. Both of these gates are blocked by logic 1 signals so pulse A is not passed through. NOR gate **98** is blocked by the logic 1 signal coming from the reset output terminal **85** of flip-flop L which is in its reset condition during the duration of pulse A. NOR gate **99** is blocked by the logic 1 signal coming from the set output terminal **86** of flip-flop K which is in its set condition during the duration of pulse A.

Since flip-flop K is presently in the set condition, there is a logic 0 signal at the reset output terminal **84** of flip-flop K which in turn is supplied in conductor **101** to the reset-steering terminal **103** of flip-flop K. Clock pulse B is now supplied to the set trigger **82** and reset trigger **83** of flip-flop K. As pulse B at the reset trigger terminal **83** of flip-flop K goes from the logic state of 1 to the logic state of 0 it resets flip-flop K. The set output signal of flip-flop K is connected by conductor **106** to the set-steering terminal **90** of flip-flop K. The set output signal of flip-flop K then continues via conductor **109** to the set trigger terminal **107** and reset trigger terminal **108** of flip-flop L. As the set output signal of flip-flop K goes from a logic 1 to a logic 0 it will put flip-flop L in its set condition. The reset output terminal **85** of flip-flop L is conducted via conductor **110**, to NOR gate **98** along with the clock pulse train C1. The logic 0 signal from the reset output terminal **85** of flip-flop L is supplied to NOR gate **98** along with the clock pulse B which is in a logic 0 state. As the two inputs to NOR gate **98** are at the logic 0 state, the state of the output signal of this gate goes to the logic state of 1 . At the end of pulse B, when it changes from the logic state of 0 to the logic state of 1 , the logic state of the output of NOR gate **98** changes from logic 1 to logic state 0. This pulse is inverted by inverter gate **111** and passes along conductor **112**. Pulse B is also applied to NOR gates **93** and **99**. NOR gate **93** is blocked by the logic 1 signal coming from the set output terminal **87** of flip-flop L, which is in its set condition during the duration of pulse B, as shown in FIG. 7. NOR gate **99** also is blocked by the logic 1 signal coming from the set output terminal **87** of flip-flop L via conductor **94**.

Clock pulse C is now supplied to the set trigger **82** and reset trigger **83** of flip-flop K. Since flip-flop K is presently in the reset condition there is a logic 0 signal at the set-steering terminal **90** of flip-flop K. As pulse C, at the set trigger terminal **82** of flip-flop K, goes from the logic state of 1 to the logic state of 0 it sets flip-flop K. The set output signal of flip-flop K is connected by conductors **106** and **109** to the set trigger terminal **107** and reset trigger terminal **108** of flip-flop L. As the set output signal of flip-flop K goes from a logic 0 to a logic 1 state, it will have no effect on flip-flop L and flip-flop L will remain in its set condition. The logic 0 signal from the reset output terminal **85** of flip-flop L is supplied to NOR gate **98** via conductor **110** along with the clock pulse C. As the two inputs to NOR gate **98** are at the logic 0 state, the state of the output signal of this gate goes to the logic state of 1 . At the end of pulse C when it changes from the logic state of 0 to the logic state of 1, the logic state of the output of NOR gate **98** changes from logic 1 to logic state 0 . This pulse is inverted by inverter gate **111** and passes along conductor **112**. Pulse C is also applied to NOR gates **93** and **99**. NOR gate **93** is blocked by the logic 1 signal coming from the set output terminal **87** of flip-flop L which is in its set condition during the duration of pulse C. NOR gate **99** is also blocked by the logic 1 signal coming from the set output terminal **87** of flip-flop L.

The output of NOR gate **98** is also supplied via conductor **114** to NOR gate **115**. The output of NOR gate **93** is also supplied via conductor **117** to NOR gate **115**. Pulse A which is passed by NOR gate **93** and pulses B and C which are passed by NOR gate **98** will be passed by NOR gate **115**. The logic state of the output of NOR gate **115** will change from the logic state 1 to the logic state 0 , as the three pulses are inverted by NOR gate **115**, to form a three pulse train on conductor **118**. The output of NOR gate **115** is also supplied, via conductor **119**, to inverter gate **120**.

Clock pulse D is now supplied to the set trigger **82** and reset trigger **83** of flip-flop K. Since flip-flop K is presently in the set condition, there is a logic 0 signal at the reset output terminal **84** of flip-flop K which in turn is supplied in conductor **101** to the reset-steering terminal **103** of flip-flop K. Also, since flip-flop L is in the reset condition, there is a logic 0 signal at the set output terminal **87** of flip-flop L which in turn is supplied in conductor **105** to the set-steering terminal **102** of flip-flop L. As pulse D at the reset trigger terminal **83** of flip-flop K goes from the logic state of 1 to the logic state of 0 it resets flip-flop K. The set output signal of flip-flop K is connected by conductors **106** and **109** to the set trigger terminal **107** and the reset trigger terminal **108** of flip-flop L. As the set output signal of flip-flop K goes from a logic 1 to a logic 0 it will put flip-flop L in its reset condition. The set output terminal of flip-flop L is conducted, via conductor **94**, to NOR gate **99** along with the clock pulse train C1 and the set output signal via conductor **122** of flip-flop K. As the three inputs to NOR gate **99** are at the logic 0 state, the state of the output signal of this gate goes to the logic state of 1 . At the end of pulse D, when it changes from the logic state of 0 to the logic state of 1 , the logic state of the output of NOR gate **99** changes from logic 1 to logic state 0 .

The output of NOR gate **99** along with the output of inverter gate **120** is supplied to NOR gate **124**. Pulse A, B and C, which is passed by inverter gate **120**, and pulse D, which is passed by NOR gate **99**, will now be passed by NOR gate **124** to form a four pulse train on conductor **125**. The output of NOR gate **99** is also supplied via conductor **126** to the reset trigger terminal **114** of a compensation flip-flop C.

The compensation flip-flop C functions to supply a signal from its reset output terminal **140** to a set of matrix output NOR gates, hereinafter to be explained, which enables the matrix output NOR gates to pass a predetermined number of compensating pulses which are supplied from the above described pulse trains.

FIG. 8 shows the decimal weights assigned to the various decades of the axis position register 39. The four least significant decades represent the tenths, hundredths, thousandths and ten thousandths of an inch position of worktable 16. When these last four decades register a zero, a 0.0000 signal pulse will originate from the axis position register 39 and be supplied, via conductor 130, to the linear error compensator 78, as shown in FIG. 2. The 0.0000 signal occurring at the 1.0000 inch, 2.0000 inch, 3.0000 inch, etc. position on the X-axis. The details of the origin of the 0.0000 signal from a position register is well known in the art. Assuming that flip-flop C is in the reset condition, as shown in FIG. 3, the 0.0000 pulse, from the axis position register 39, passes through inverter gate 132 to simultaneously supply a logic 1 signal to the reset input terminals R1 of flip-flop K and L via conductor 133 and also to supply a logic 1 signal to the set trigger terminal 135 of flip-flop C via conductor 134. The logic 1 signal at the reset input terminals of flip-flops K and L will immediately place them in the reset condition. The set output terminal 138 of flip-flop C is connected to the set-steering terminal 139 of flip-flop C. Therefore, with flip-flop C in its reset condition, there will be a logic 0 signal at the set steering terminal 139. As the inverted 0.0000 signal pulse, as shown in FIG. 7 (*c*) and (*d*), goes from its logic 1 state to its logic 0 state, it will put flip-flop C in its set condition. With flip-flop C in its set condition, there will be a logic 0 signal at the reset output terminal 140 of flip-flop C. This logic 0 signal is supplied to the set of matrix output NOR gates via conductor 142. This logic 0 signal is also supplied to the reset-steering terminal 141 via conductor 143. As shown in FIG. 7 (*d*) and (*m*), as inverted clock pulse D, on conductor 126, goes from its logic 1 state to its logic 0 state, it will put flip-flop C back in its reset condition.

As shown in FIGS. 4 and 7 (*i*, *j*, *k* and *l*), the pulse trains on conductors 97, 117, 118 and 125 are supplied to a compensation selection matrix 144 comprising principally the output conductors 146, 147, 148, 149 and 150. Depending upon the particular error curve found in a machine, the output conductors are predeterminately connectable to the pulse train which will supply the desired compensation. For example, the output conductor 146 can be interconnected with the different pulse trains by insertion of a screw connector 152 between the conductor and points A, B, C or D, depending if one, two, three or four pulses of compensation are needed. If no screw connector is used there will of course be no compensating pulses on the output connector.

The output conductors 146, 147, 148, and 150 are connected to the matrix output NOR gates 155, 156, 157, 158 and 159, respectively.

The reset output signal of flip-flop C is supplied to each of the matrix output NOR gates 155, 156, 157, 158 and 159. The rest of the inputs to NOR gates 155, 156, 157, 158 and 159 are connected to various flip-flops of a binary-coded decimal counter located in the axis position register 39. The signals from these various flip-flops are supplied via conductor 160, as shown in FIG. 2, to the linear error compensator 78. A typical binary-coded decimal counter 162 is illustrated in FIG. 8A. The particular decade use in this embodiment of the invention is the unit decade which represents the table position from 0 to 9 inches and multiples of 10 thereof. If the addition of count to the decade causes the total registered in that decade to exceed nine, as the count changes from nine to zero, a carry signal will be propagated to the next most significant decade, increasing its registration by one.

As shown by the chart in FIG. 8B, the output of the four flip-flops of binary counter 162 will be in their reset state when the counter represents the decimal position of 0 . This will occur when the table 16 is at the 0, 10, 20, 30, 40, etc. inch position along the horizontal ways 15. Therefore, there will be a logic 0 signal on the set outputs of flip-flops 1, 2, 4 and 8. All the inputs to NOR gate 155, as shown in FIG. 4, will be at logic 0 when there is a 0 registered in the unit decade counter 162. At this time, either one, two, three or four compensating pulses, depending upon the placement of the screw connector 152, will be transmitted via conductor 146 through NOR gate 155. The output of NOR gate 155 will swing from logic 0 to its logic 1 state as the compensating pulses are passed by NOR gate 155.

Similarly, the outputs of the 8, 4 and 1 flip-flops will be in the reset condition and the 2 flip-flop will be in the set condition when the counter represents the decimal position of 2 . This will occur when the table 16 is at the 2, 12, 22, 32, etc. inch position along the horizontal ways 15. Therefore, there will be a logic 0 signal on the set outputs of flip-flops 1, 4 and 8 and a logic 0 signal on the reset output of flip-flop 2. All the inputs to NOR gate 156 will be at logic 0 when there is a 2 registered in the unit decade counter 162. At this time either one, two, three or four compensating pulses, depending upon the placement of screw connector 152 will be transmitted via conductor 147 through NOR gate 156. The output of NOR gate 156 will swing from logic 0 to logic 1 as the compensating pulses are passed by NOR gate 156.

Similarly, NOR gate 157 will pass compensating pulses only when the decade counter registers a 4, 14, 24, 34 inch, etc. table position.

Similarly, NOR gate 158 will pass compensating pulses only when the decade counter registers 6, 16, 26, 36 inch, etc. table position.

Similarly NOR gate 159 will pass compensating pulses only when the decade counter registers 8, 18, 28, 38 inch, etc. table position.

The output conductors of NOR gate 155, 156, 157, 158 and 159 are respectively connected to each of the compensator output NOR gates 164 and 165.

NOR gates 164 and 165 function to pass the compensation pulses from the various matrix output gates to the desired steering gates. As shown in FIGS. 4 and 6, the output conductor 167 of NOR gate 164 is connected to the double-count steering "gates" 56 and the output conductor 168 of NOR gate 165 is connected to the normal count steering gates 55. Double count steering gates is comprised of an inverter gate 170 and a NOR gate 171. Normal count steering gates is comprised of two NOR gates 175 and 176.

Compensator output NOR gate 164 will only pass compensation pulses when the commanded table position as registered on the position command register 38 is greater than the actual table position as registered on the axis position register 39. When this condition exists, the comparator 40 provides a signal along conductor 43 and 180 to provide a logic zero signal to NOR gate 164.

NOR gate 165 will only pass compensation pulses when the commanded table position as registered on the position command register 38 is less than the actual table position as registered on the axis position register 39. When this condition exists, the comparator 40 provides a signal along conductor 42 and 181 to provide a logic zero signal to NOR gate 165.

If no screw connectors 152 are inserted in the compensation selection matrix 144, there will be no compensating pulses going out on output conductors 167 and 168 and these conductors will continue to carry a logic zero signal to NOR gates 176 and 171. The normal and double count steering gates will then be controlled by the logic state of the output signals on conductors 51 and 52 coming from the count control circuit 50.

To advance or retard the phase of the 250 hertz carrier signal from command phase counter 60, the pulse train signal from count control 50 is employed to affect the divide by 1,000 operation of command phase counter 60, and specifically, the application of the 250 kilohertz pulses from clock oscillator 34 to the counter. If, as in the previously used example, it is desired to move worktable 16 at a velocity of one inch per second, the phase of the 250 hertz carrier signal must be phase shifted by a total of 10,000 pulses over the time period of a second. The 250 hertz carrier signal of command phase counter 60 must be phase shifted one pulse every 100 microseconds in order to provide the required phase shift rate of 10,000 pulses per second. It may be noted that a phase shift

of 10,000 pulses represents a phase shift of 10 complete cycles of the 250 hertz carrier signal.

The phase shift is provided by utilizing the 10,000 hertz pulse train signal from count control **50** to affect the application to command phase counter **60** of one pulse out of every 25 pulses of the 250 kilohertz, or 250,000 cycle per second, clock oscillator **34** pulse train. If it is desired to retard the phase of the 250 hertz carrier signal of command phase counter **60**, the count control **50** generates the required signal pulses transmitted via a conductor **51** to the NOR gate **175** of the normal count steering gates **55**. There will be a logic zero signal standing on conductors **52** and consequently **178** as long as the actual position of table **16** is greater than the commanded position as indicated by the axis position register **39** and the position command register **38**, respectively. The signal pulses on conductor **51** will be passed and inverted by NOR gate **175**. The output of NOR gate **175** is supplied via conductor **186** to NOR gate **176**. Since there is a logic 0 signal standing on conductor **168**, NOR gate **176** will invert the pulses passed by NOR gate **175**.

From normal count gates **55**, the signal continues via conductor **63** to block one out of every 25 clock oscillator pulses supplied to command phase counter **60**, thereby retarding the generation and phase of the carrier signal provided by command phase counter **60** by the amount of the one blocked clock oscillator pulse. Over the period of a second, 10,000 clock oscillator pulses supplied to command phase counter **60** will be blocked, thus providing the desired rate of change, or phase shift, to the 250 hertz carrier signal of command phase counter **60**. If it is desired to advance the phase of the 250 hertz carrier signal of command phase counter **60**, the count control **50** generates the required signal pulses transmitted via a conductor **52** to the inverter gate **170** of the double-count steering gates **56**. The required signal pulses are also transmitted via conductors **52** and **178** to NOR gate **175** of the normal count steering gate **55**. The required signal pulses on conductor **52** will be inverted by inverter gate **170** and pass via conductor **187** to NOR gate **171**. Since there is a logic 0 signal standing on conductor **167**, NOR gate **171** will invert the pulses passed by inverter gate **170**.

The signal pulses continue via conductor **64** to operate command phase counter **60** to add the equivalent of one clock oscillator pulse every 25 clock oscillator pulses supplied to command phase counter **60**, thereby advancing the phase of the carrier signal by the amount of the added clock oscillator pulse. Though a pulse on conductor **64** acts to effect the addition of two pulses to the command phase counter **60**, we see we also pass a signal pulse along conductors **52** and **178** to the normal count steering gates **53**. These pulses are passed along to the NC terminal of the command phase counter **60** to effect the blocking out of one of the clock pulses for every two that are added by the pulse along conductor **64**. So, in effect, we add the equivalent of one clock oscillator pulse to every 25 clock oscillator pulses supplied to command phase counter **60**. The details of command phase counter **60** are not illustrated since they form no part of the invention and are old and well known in the art. For example, reference may be had to U.S. Pat. No. 3,173,001, issued Mar. 9, 1965 to J. T. Evans.

When a machine tool is operated, its temperature may rise substantially as a result of the heat that is generated by the friction that develops in the various mechanical components of the machine tool slides, such as the bearing, gears and the motor. Such temperature variation results in the expansion and contraction in the length of the slide structure by reason of its coefficient of expansion. This expansion and contraction operates to displace the tool carrying end of the spindle from the established reference position on the machine tool slide. In machine tools in which relative positioning between the tool-carrying slide is effected automatically, the positioning movement is made with respect to an established reference plane on the machine tool slide. Thus, a precise relationship may be established between the workpiece and the tool-carrying spindle. However, if the machine slide is displaced from an established position by reason of its expansion or contraction, an error is introduced which is detrimental in automatic high precision types of work operations.

To facilitate describing the invention, a rate of longitudinal expansion of 0.0001 of an inch per lineal inch has been arbitrarily selected as schematically indicated in FIG. **9**. As there shown, the 40 inch range of movement indicated by the horizontal line **190** is shown in relation to the cumulative elongation as indicated by the vertical line **191**. Obviously, under some conditions of operation, the rate of expansion or elongation of the machine slide structure in response to heat may be considerably less than 0.0001 of an inch, and in other cases considerably greater than this amount. Further, for illustrative purposes, position compensating command signals of 0.0002 of an inch are provided incrementally for every 2 lineal inches of travel to compensate for the predetermined described rate of expansion.

In FIG. **9**, a continuous angular line **192** graphically indicates the cumulative error for the 0.0001 per inch expansion in the absence of corrective command signals. The short, symmetrically repetitive, angularly inclined, individual lines, such as **193** and **194**, illustrate the abortive effect produced by applying corrective compensating signals every two lineal inches of travel. Thus, as indicated by the repetitive short vertical lines, such as **195** and **196**, corrective command signals of 0.0002 of an inch compensate for a like expansion or elongation of the X-axis structure during predetermined increments of movement, in this case for each successive two inches of travel along the X-axis.

To compensate for the 0.0001 of an inch per lineal inch thermal expansion of the X-axis slide structure, compensating signals of 2 pulses, for each successive 2 inches of travel along the X-axis, was selected. These two pulses represent 0.0002 of an inch of compensation. To accomplish this amount of correction, the individual screw connectors **152** of the compensation selection matrix **144** are placed between the five leads **117B** coming from conductor **117** and points **146B**, **147B**, **148B**, **149B** and **150B**. This will effect the connection of the two pulse, pulse train to the matrix output conductors **146**, **147**, **148**, **149** and **150**.

As the feed rate pulses to the count control **50** effect the movement of table **16** along the X-axis, the unit decade counter **162** will by its changing flip-flop states allow matrix output NOR gates **155**, **156**, **157**, **158** and **159** to pass the two compensating pulses that are being carried by the various matrix output conductors. It was described earlier that the compensating flip-flop C is put into its set condition at the end of every 0.0000 signal pulse, coming from the four least significant decades of the axis position register **39**, and, subsequently, put back into its reset condition at the end of the fourth subsequent clock pulse. Therefore, the compensating pulses are always added between the 0.0000 signal pulses, which occur at each inch movement of table **16** travel, when the compensating flip-flop C is in its set condition and there is a logic 0 signal being applied from the reset output terminal **140** via conductor **142** to the various matrix output NOR gates **164** and **165**. If the commanded table position as registered on the position command register is greater than the actual table position as registered on the axis position register **39**, then NOR gate **164** will pass the compensation pulses via conductor **167** to NOR gates **176** and **171**, as shown in FIG. **6**. Under the above conditions, there being a logic 0 signal standing on conductor **168**, **186** and **187**, the compensation pulses will be passed by NOR gates **171** and **176** to effect the adding of the equivalent of one clock oscillator pulse supplied to command phase counter **60**, thereby advancing the phase of the carrier signal by the amount of the added clock pulse.

If the commanded position as registered on the position command register **38** is less than the actual table position as registered on the axis position register **39**, then NOR gate **165** will pass the compensation pulses via conductor **168** to NOR gate **176**. Under the above conditions there being a logic 0 signal standing on conductor **167** and **186**, the compensation

pulses will be passed by NOR gate **176** to block out one of the clock oscillator pulses supplied to command phase counter **60**, thereby retarding the generation and phase of the carrier signal provided by command phase counter **60** by the amount of the one blocked clock oscillator pulse.

In the above example, the linear error compensator **78** is used to correct a positive linear elongation error caused by the thermal expansion of the X-axis slide structure. Compensator **78** could also be used to correct a negative linear error by switching conductor **168** from NOR gate **165** to **164** and, in turn, switching conductor **167** from NOR gate **164** to NOR gate **165**.

Although the illustrative embodiment of the invention has been described in considerable detail for the purpose of disclosing a practical operative structure whereby the invention may be practiced advantageously, it is to be understood that the particular apparatus described is intended to be illustrative only and that the novel characteristics of the invention may be incorporated in other structural forms without departing from the spirit and scope of the invention as defined in the subjoined claims.

The principles of this invention having now been fully explained in connection with the foregoing description, I hereby claim as my invention:

1. In a machine tool having a movable member;

drive means connected to effect relative positioning movement of said member;

a positioning control system including a source of control pulses individually representative of uniform increments of movement and being operable to regulate the operation of said drive means to effect accurate positioning of said member;

an error compensator control operable to transmit a compensating signal to said numerical control system for modifying the number of said control pulses to compensate for positioning errors due to inaccuracies in the machine structure;

first means in said error compensation control for producing a plurality of pulse trains with each train providing a different number of compensating pulses; and

second means in said error compensation control to select one of said pulse trains for insertion into said control system at a predetermined position of said movable member to compensate for a predetermined inaccuracy of the machine at that position.

2. A machine tool according to claim **1**,

wherein said second means provides for the selection of any one of said pulse trains for insertion into said control system at different positions of said movable member to effect the compensation through the entire range of movement of said movable member at predetermined intervals of movement.

3. A machine tool according to claim **1**,

wherein said compensating pulses serve to add or subtract pulses in said control system depending upon the type of correction required to improve the accuracy of the machine.

4. A machine tool according to claim **1**,

wherein said second means comprises a compensation selector matrix settable to select the desired pulse train for introduction into said control system upon completion of each predetermined increments of movement of said movable member.

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,612,840 Dated October 12, 1971

Inventor(s) Richard E. Stobbe

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 2, line 23, "now" should read -- not --. Column 3, line 14, "produced" should read -- produces --; line 35, "electric" should read -- electrical --; line 45, insert -- for -- after "circuitry"; line 73, "axis" should read -- command --. Column 4, line 14, "of" should read -- or --; line 16, "One of the carrier signals is utilized as a phase reference signal.", should read -- One of the carrier signals is utilized as a reference signal. --. Column 6, line 12, after "corresponding to" should read -- the difference berween the phase of the two signals to digital to --; line 69, after "reset" should read -- output --. Column 7, line 29, after "is" should read -- supplied --.

Signed and sealed this 24th day of October 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

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