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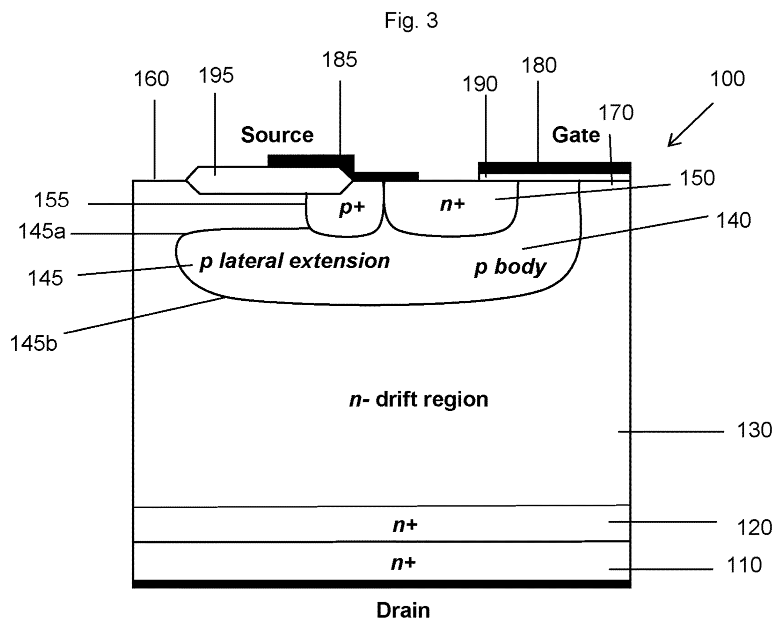
(54) Title of the Invention: **High voltage semiconductor devices**
Abstract Title: **High voltage device with lateral extending body region**

(57) We disclose a wide band-gap power transistor including a semiconductor substrate (110); a semiconductor drift region (130) of a second conductivity type disposed on the semiconductor substrate (110); a body region (140) of a first conductivity type, opposite the second conductivity type, located within the semiconductor drift region (130); In one embodiment a source region (150) of the second conductivity type is located within the body region (140) and a gate (180) placed above the source region (150), the gate to control charge in a channel region between the semiconductor drift region and the source region and to thereby control flow of charge within the semiconductor drift region. In other embodiments a Schottky metal contact could be formed on the drift region. The body region (140) includes a lateral extension (145) of the first conductivity type extending laterally into the drift region, the lateral extension being spaced from the surface (160) of the transistor. The device may be a vertical MOSFET or a insulated gate bipolar transistor IGBT, and could be used in high voltage applications.

Fig. 3



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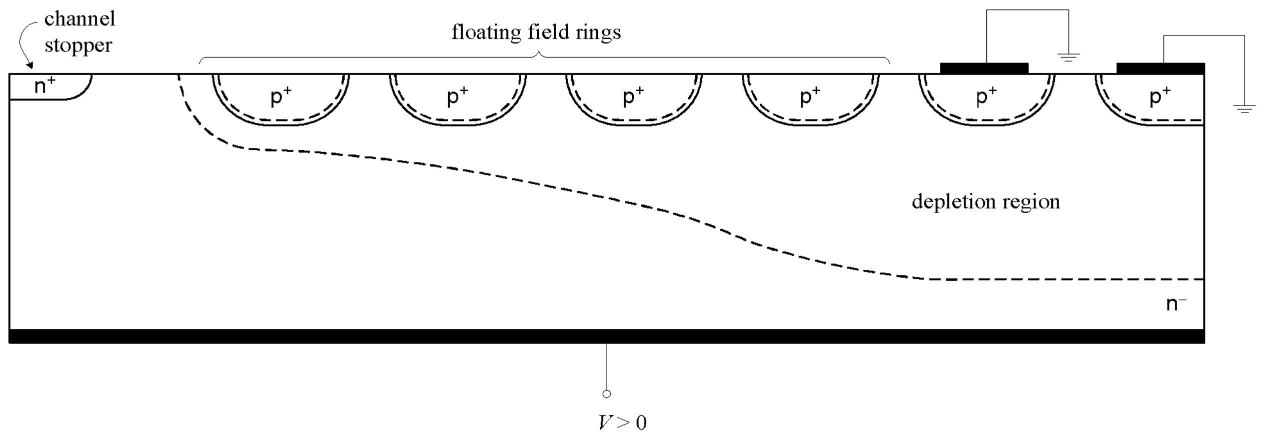

Fig. 1

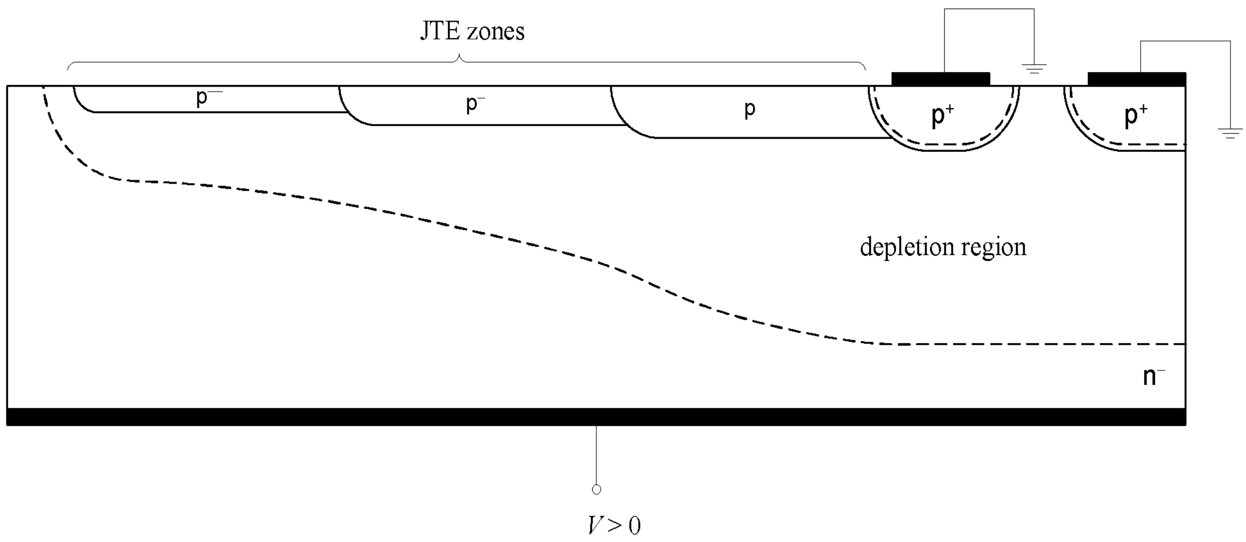

Fig. 2

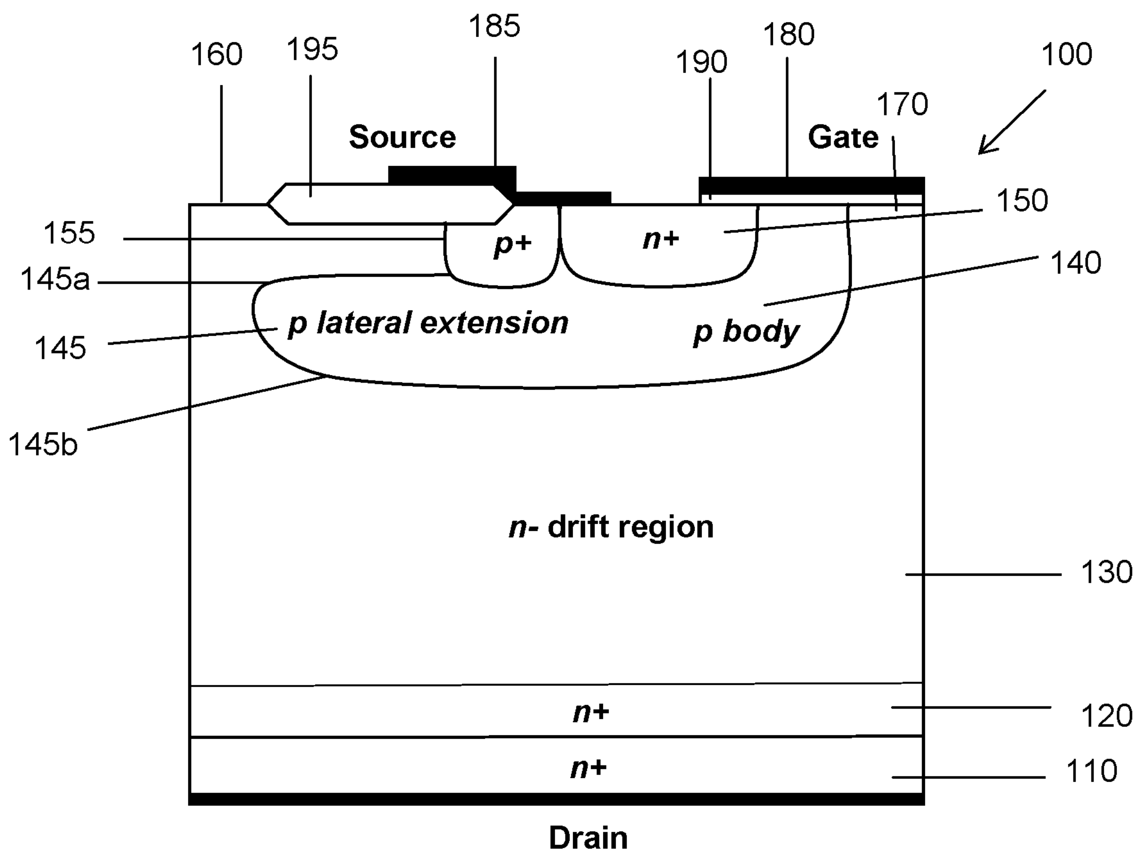

Fig. 3

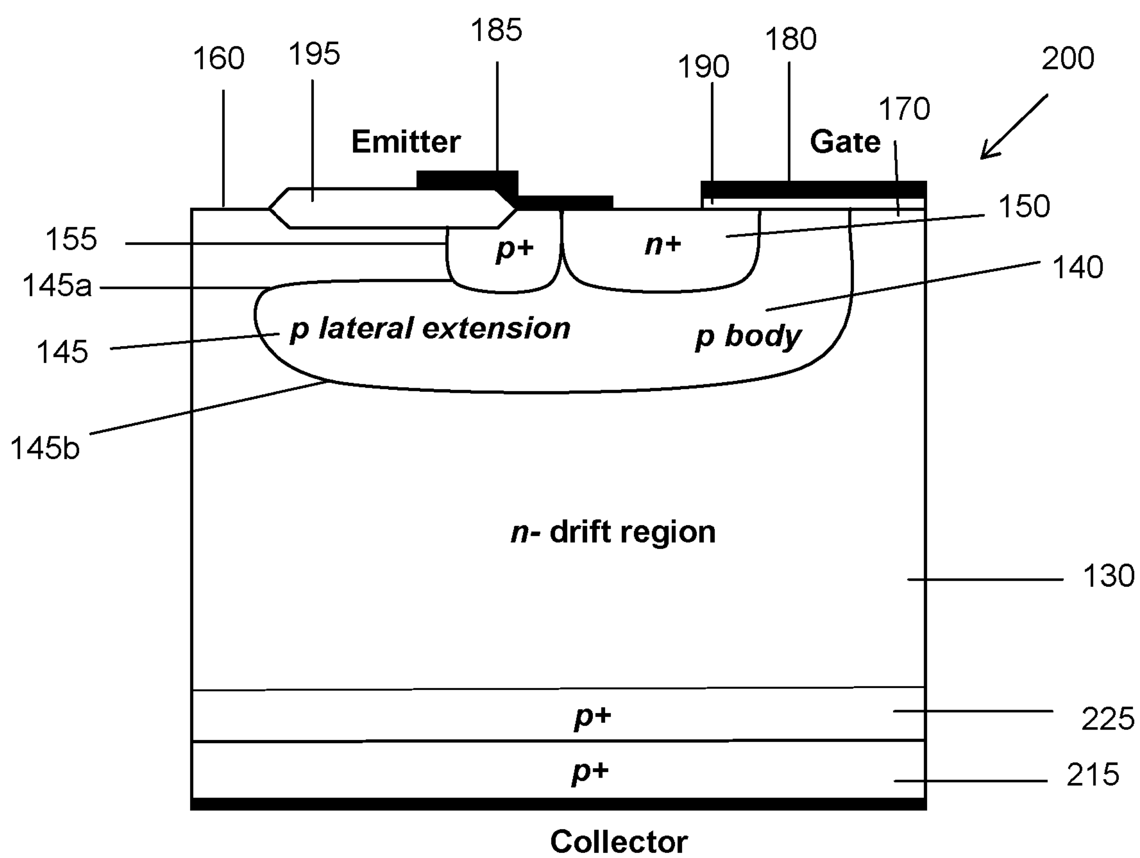

Fig. 4

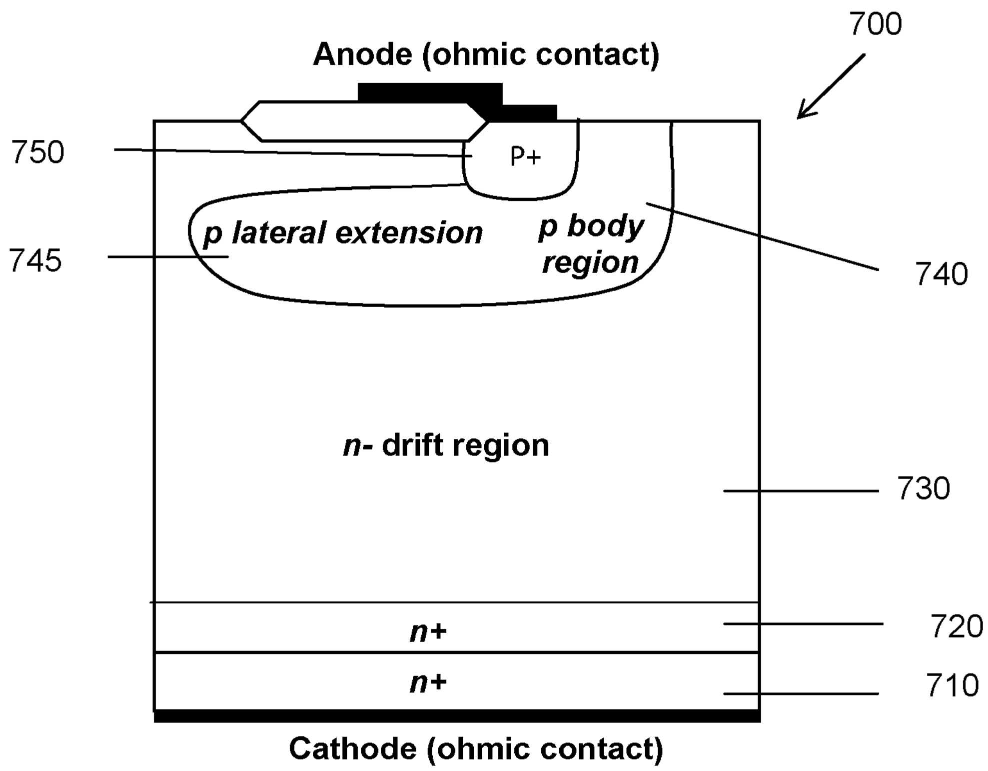

Fig. 5

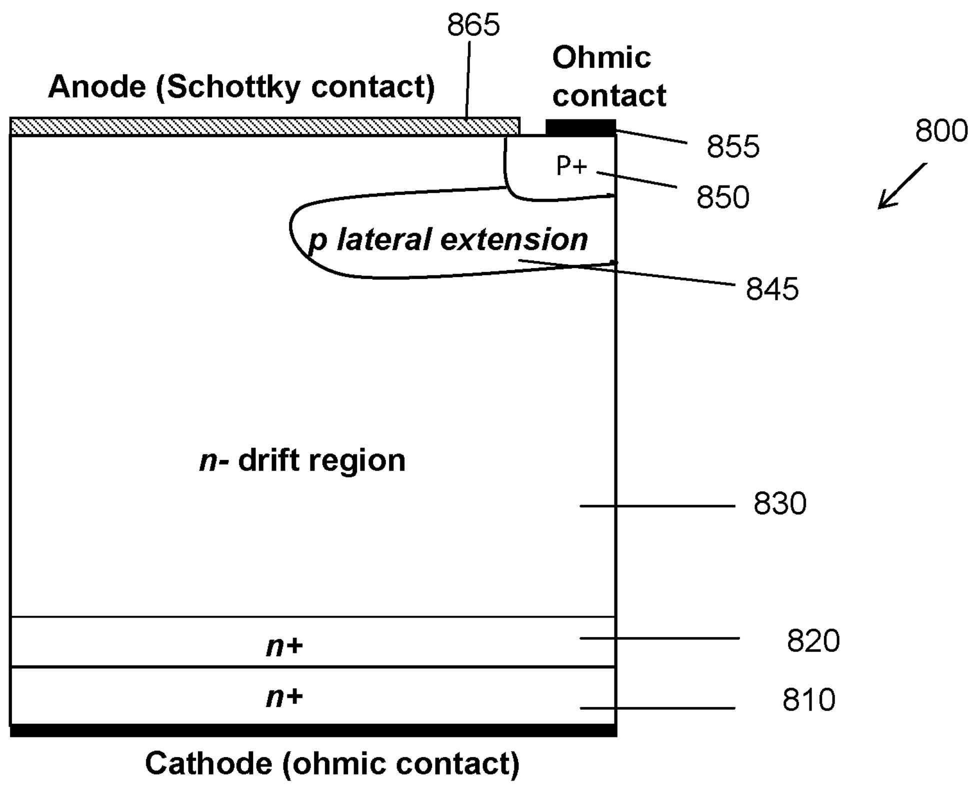

Fig. 6

High Voltage Semiconductor Devices

FIELD OF THE INVENTION

This invention relates to a power semiconductor device, particularly but not exclusively, to a wide band-gap material based power semiconductor device.

BACKGROUND TO THE INVENTION

The wide band-gap of SiC (irrespective of polytype) results in a very high critical electrical field before avalanche breakdown. This critical field is roughly ten times that of Si and as a consequence one tenth of the thickness of material is needed to sustain a given voltage in the off state, which in turn leads to a much lower resistance in the on-state. This lower resistance reduces the power dissipation in the device resulting in overall system energy savings.

However, care must be taken when calculating the actual breakdown voltage of a real device since the theoretical critical electric fields assume an infinite planar junction. However, in the real case field intensification occurs around the edges of a diffused region and the breakdown voltage is reduced as a strong function of the radius of curvature of the structure. (see for example: J Baliga, Fundamentals of Power Semiconductor Devices, page 108).

This problem is well understood in the context of Si devices and solutions are found by adding further field relief structures around the edges of active junction (J Baliga, Fundamentals of Power Semiconductor Devices, page 130). Such a field relief structure is shown in Figure 1. The field relief structures can gradually release the depletion region at the edge of the device. The voltage is supported between each pair of p+ rings, thus reducing the crowding of the electric field at the surface. The spacing and depth of the rings are designed such that the electric field peaks at the surface between each pair of rings are almost equal and the breakdown voltage of the final structure is significantly increased.

Junction Termination Extension (JTE) structures have also been proposed in Si based devices. Such a JTE structure is shown in Figure 2. This structure uses multiple zones

with the doping level decreasing from the active area towards the end of the termination. The effect is similar to that achieved by the field rings – that is the gradual release of the depletion region at the edge of the device. The voltage is ideally supported uniformly along the JTE zones.

5

However, SiC presents new challenges in this area, most importantly as mentioned above, the electric fields in SiC are very high and so this field intensification problem is much more severe. Consequently to extrapolate the Si solution above to SiC would result in very complex structures with much smaller dimensions to the extent of not
10 being practical using normal production equipment.

Furthermore, the material itself presents problems; since dopant diffusion is negligible in SiC the deep, slowly curving diffused structures used in Si cannot be reproduced, and the alternative dopant introduction method of ion implantation by its very nature
15 cannot give the same structure. In fact the only practical method of introducing localised doping in SiC is ion implantation, but again keeping implantation energies within the scope of production equipment results is rather shallow junctions of the order of 0.5 microns deep which exacerbates the whole problem.

20 It is an object of the present invention to address the problems above.

SUMMARY

According to one aspect of the present invention, there is provided a wide band-gap
25 high voltage semiconductor device comprising:

a semiconductor substrate;

a semiconductor drift region of a second conductivity type disposed on the semiconductor substrate;

a body region of a first conductivity type, opposite to the second conductivity
30 type, located within the semiconductor drift region;

a source region of the second conductivity type located within the body region;

a gate placed above and in contact to the source region, the gate to control charge in a channel region between the semiconductor drift region and the source region and to thereby control flow of charge within the semiconductor drift region;

wherein the body region comprises a lateral extension of the first conductivity type extending laterally into the drift region, the lateral extension being spaced from the surface of the transistor.

5 The surface of the transistor may be parallel to the channel region. The surface of the device may be defined by a plane on which the source contact and the gate of the transistor are formed.

The lateral extension may be vertically spaced from the surface of the transistor. The 10 term “vertical” is related to a transverse distance from the gate.

The entire lateral extension may be vertically spaced from the surface of the transistor.

The body region may comprise a first portion adjacent (or immediately below) the gate 15 and a second portion located deeper than the first portion, the doping concentration of the first portion may be higher than the doping concentration of the second portion. The body region may also include a p+ region in contact with the n+ source region. The p+ and n+ regions are shorted with a source contact or electrode. When shorted, the p+ region may also form part of the source region. It will be appreciated that the source 20 region is the same as the collector of an insulated gate bipolar transistor (IGBT), and therefore the source region also covers the collector operation when the IGBT structure is considered.

The lateral extension may extend laterally only from the second deeper portion of the 25 body region. The term “lateral” is related to extending in a direction parallel to the gate or other contacts of the device.

The doping concentration of the lateral extension may be substantially the same as the doping concentration of the second deeper portion of the body region. The term 30 “substantially” relates to almost the same. It will be appreciated that the doping concentration or dose of the lateral extension can be optimised during the manufacturing process so that an improved (desired) breakdown voltage can be achieved.

The lateral extension may extend from the body region in a lateral direction which is opposite to a direction to which the gate extends from the source to the drift region. The transistor may include a field oxide or insulator adjacent or in contact with the source terminal/electrode. The source electrode may extend over the field oxide to form a field plate. The lateral extension may laterally extend further into the drift region compared to the field plate extension over the field oxide. The thickness of the field plate may be optimised and combined with the field plate extension and the dose optimisation of the lateral extension to achieve an improved breakdown voltage. The length of the lateral extension may be varied to achieve an improved breakdown voltage. It will be appreciated that the term “length” refers to the distance between the edge of the p+ region and the outer edge of the lateral extension.

The lateral extension may operate as a termination structure in the transistor. The lateral extension may be used in transistor structures located on the periphery of a device where a termination structure (or a guard ring) is generally desirable.

The transistor may be configured such that the electric field formed at the vertical junctions between the lateral extension and the drift region reduces the electric field formed between the body region and drift region at the surface of the transistor. It will be appreciated that the vertical junction is a p-n junction in which the p region and the n region are located vertically to one another. The electric field created by the vertical junctions between the lateral extension and the drift region are particularly advantageous. The p-n junction created at the surface by the body region and drift region is a lateral junction as the p region (body region) and the n region (drift region) are formed laterally to one another. Therefore the lateral extension is configured to reduce peak electric field in both the active and termination areas of the device.

The drift region may be configured to be depleted of mobile carriers at breakdown voltage during an off-state blocking mode of the transistor and able to conduct charge during an on-state conducting mode of the transistor.

The semiconductor substrate may comprise monocrystalline silicon material.

The semiconductor drift region, the body region and the source region may each comprise a material comprising 3-step cubic silicon carbide (3C-SiC).

The semiconductor substrate, the semiconductor drift region, the body region and the source region may each comprise a material comprising 4-step hexagonal silicon Carbide (4H-SiC.

5

The semiconductor substrate, the semiconductor drift region, the body region, the lateral extension and the source region may each comprise a material comprising gallium nitride (GaN).

10 The semiconductor substrate may comprise monocrystalline silicon material, and the semiconductor drift region, the body region, the lateral extension and the source region may each comprise a material comprising GaN. Alternatively the semiconductor substrate may comprise SiC material, and the semiconductor drift region, the body region, the lateral extension and the source region may each comprise a material
15 comprising GaN.

The transistor may further comprise a first semiconductor region disposed between the semiconductor substrate and the drift region, the first semiconductor region comprising a material comprising 3C-SiC, 4H-SiC or GaN. It will be appreciated that the transistor
20 structure can be made of other wide band-gap materials such as 6H-SiC and diamond. It will be also appreciated that the lateral extension as described above can be used in a lateral high-electron-mobility transistor (HEMT) using GaN material. The skilled person would understand that the HEMT is generally a lateral semiconductor device in which the lateral extension can be used as a termination structure.

25

The first semiconductor region may be of a second conductivity type and the semiconductor substrate may be of a second conductivity type. The transistor may be a vertical power metal-oxide-semiconductor field effect transistor (MOSFET).

30 The first semiconductor region may be of a first conductivity type and the semiconductor substrate is of a first conductivity type. The transistor may be a vertical power insulated gate bipolar transistor (IGBT).

According to a further aspect of the invention, there is provided a wide band-gap high
35 voltage semiconductor device comprising:

a semiconductor substrate of a second conductivity type;

a first semiconductor region of the second conductivity type disposed on the semiconductor substrate;

a semiconductor drift region of the second conductivity type disposed on the
5 first semiconductor region, the first semiconductor region having higher doping concentration than the drift region;

a body region of the first conductivity type, opposite the second conductivity type, located within the semiconductor drift region;

wherein the body region comprises a lateral extension of the first conductivity
10 type extending laterally into the drift region, the lateral extension being spaced from the surface of the device.

The lateral extension may be vertically spaced from the surface of the device. The entire lateral extension may be vertically spaced from the surface of the device. The
15 device may be a vertical PIN diode.

The semiconductor substrate may comprise monocrystalline silicon material. The first semiconductor region, the semiconductor drift region, the lateral extension and the body region may each comprise a material comprising 3-step cubic silicon carbide (3C-
20 SiC).

The semiconductor substrate, the first semiconductor region, the semiconductor drift region, the lateral extension and the body region may each comprise a material comprising 4H-SiC.

25

The semiconductor substrate, the first semiconductor region, the semiconductor drift region, the lateral extension and the body region may each comprise a material comprising GaN.

30 The semiconductor substrate may comprise monocrystalline silicon material, and the first semiconductor region, the semiconductor drift region, the lateral extension and the body region may each comprise a material comprising GaN.

The semiconductor substrate may comprise SiC material, and the first semiconductor region, the semiconductor drift region, the lateral extension and the body region may each comprise a material comprising GaN.

According to a further aspect of the present invention, there is provided a high voltage semiconductor device comprising:

a semiconductor substrate of a second conductivity type;

a first semiconductor region of the second conductivity type disposed on the semiconductor substrate;

a semiconductor drift region of the second conductivity type disposed on the first semiconductor region, the first semiconductor region having higher doping concentration than the drift region;

a Schottky metal contact formed directly on the semiconductor drift region on a surface of the device;

a second semiconductor region of a first conductivity type, opposite to the second conductivity type, formed on the surface of the device and within the semiconductor drift region, the second semiconductor region having higher doping concentration than the drift region; and

a lateral extension of the first conductivity type extending laterally from the second semiconductor region into the drift region, the lateral extension being spaced from the surface of the device.

The lateral extension may be vertically spaced from the surface of the device. The entire lateral extension may be vertically spaced from the surface of the device.

The lateral extension may extend laterally only from a deeper portion of the second semiconductor region. The doping concentration of the lateral extension may be lower than the second semiconductor region. The lateral extension may extend laterally towards the Schottky metal contact. The length of the lateral extension may be adjusted to achieve the optimum result in the Schottky diode. Here the term “length” refers to the distance from the edge of the second semiconductor region to the edge of the lateral extension under the Schottky contact. The lateral extension under the edges of the Schottky region may act as a shield in a reverse bias operation.

The device may further comprise a first ohmic contact operatively connected to the first semiconductor region and a second ohmic contact formed on the second semiconductor region.

5 The semiconductor substrate, the first semiconductor region, the drift region, the second semiconductor region and the lateral extension may each comprise monocrystalline silicon material.

The semiconductor substrate, the first semiconductor region, the drift region, the
10 second semiconductor region and the lateral extension may each comprise 4H-SiC.

The semiconductor substrate may comprise monocrystalline silicon material, and the first semiconductor region, the drift region, the second semiconductor region and the lateral extension may each comprise 3C-SiC.

15

The semiconductor substrate, the first semiconductor region, the drift region, the second semiconductor region and the lateral extension may each comprise GaN.

The semiconductor substrate may comprise monocrystalline silicon material, and the
20 first semiconductor region, the drift region, the second semiconductor region and the lateral extension may each comprise GaN.

The semiconductor substrate may comprise SiC material, and the first semiconductor region, the drift region, the second semiconductor region and the lateral extension may
25 each comprise GaN.

According to a further aspect of the present invention, there is provided a method for manufacturing a wide band-gap high voltage semiconductor transistor, the method comprising:

30 forming a semiconductor substrate;

forming a semiconductor drift region of a second conductivity type on the semiconductor substrate;

forming a body region of a first conductivity type, opposite the second conductivity type, located within the semiconductor drift region;

forming a lateral extension of the first conductivity type extending laterally from the body region into the drift region, the lateral extension being spaced from the surface of the transistor;

forming a source region of the second conductivity type located within the body region;

forming a gate placed above and in contact to the source region, the gate to control charge in a channel region between the semiconductor drift region and the source region and to thereby control flow of charge within the semiconductor drift region.

The forming of the lateral extension may comprise applying a two stage photo-masking to implant the lateral extension. The lateral extension may be ion-implanted using Aluminium or Boron material. It will be appreciated that using Boron can be advantageous because Boron has a lighter atom and therefore it is generally easier to form a deeper implant using this material.

The method may further comprise vertically spacing the lateral extension from the surface of the transistor.

The method may further comprise forming a first semiconductor region between the semiconductor substrate and the drift region.

The method may further comprise forming the semiconductor substrate using a material comprising monocrystalline silicon, and forming each of the semiconductor drift region, the first semiconductor region, the body region, the lateral extension and the source region using a material comprising 3-step cubic silicon carbide (3C-SiC).

The method may further comprise forming each of the semiconductor substrate, the first semiconductor region, the semiconductor drift region, the body region, the lateral extension and the source region using a material comprising 4H-SiC.

The method may further comprise forming each of the semiconductor substrate, the semiconductor drift region, the body region, the lateral extension and the source region using a material comprising GaN.

The method may further comprise forming the semiconductor substrate using monocrystalline silicon material, and forming each of the semiconductor drift region, the body region, the lateral extension and the source region using a material comprising GaN.

The method may further comprise forming the semiconductor substrate using SiC material, and forming each of the semiconductor drift region, the body region and the source region using a material comprising GaN.

According to a further aspect of the present invention there is provided a method of manufacturing a high voltage semiconductor device, the method comprising:

forming a semiconductor substrate of a second conductivity type;

forming a first semiconductor region of the second conductivity type disposed on the semiconductor substrate;

forming a semiconductor drift region of the second conductivity type disposed on the first semiconductor region, the first semiconductor region having higher doping concentration than the drift region;

forming a Schottky metal contact formed directly on the semiconductor drift region on a surface of the device;

forming a second semiconductor region of a first conductivity type, opposite to the second conductivity type, formed on the surface of the device and within the semiconductor drift region, the second semiconductor region having higher doping concentration than the drift region; and

forming a lateral extension of the first conductivity type extending laterally from the second semiconductor region into the drift region, the lateral extension being spaced from the surface of the device.

The step of forming the lateral extension may comprise applying a two stage photo-masking to implant the lateral extension. The lateral extension may be ion-implanted using Aluminium or Boron material.

The method may further comprise vertically spacing the lateral extension from the surface of the device.

The method may further comprise forming an ohmic contact on the second semiconductor material, the ohmic contact comprising titanium disilicide material.

The method may further comprise forming the Schottky contact using a relatively low
5 temperature compared to that used for forming the ohmic contact, the Schottky contact comprising nickel material.

BRIEF DESCRIPTION OF THE DRAWINGS

10 The present disclosure will be understood more fully from the detailed description that follows and from the accompanying drawings, which however, should not be taken to limit the invention to the specific embodiments shown, but are for explanation and understanding only.

15 Figure 1 illustrates a prior art Si based device in which floating field rings are formed to reduce curvature effect;
Figure 2 illustrates a prior art Si based device in which junction termination structures are formed to reduce curvature effect;
Figure 3 illustrates a schematic cross section of a vertical MOSFET;
20 Figure 4 illustrates a schematic cross section of a vertical IGBT;
Figure 5 illustrates a schematic cross section of a vertical PIN diode, and
Figure 6 illustrates a schematic cross section of a vertical Schottky diode.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

25

Referring to Figure 3, an example of a SiC based vertical power semiconductor transistor 100 in the form of a metal-oxide-semiconductor field effect transistor (MOSFET) is shown. A highly doped n-type drain layer (or the first semiconductor region) 120 is formed on an n-type substrate 110. A drift region 130 is formed on the
30 drain layer 120. A p-type well 140 is formed within the drift region 130. An n-type highly doped source region 150 is formed within the p-type well region 140. A p-type highly doped region is formed within the p-type well 140. The highly doped p and n type regions 150, 155 are shorted using a source contact or electrode 185. A field oxide or insulator 195 is also formed adjacent the highly doped p-type region 155 and the
35 source contact extends over the field oxide 195. The extended source contact is

generally termed as a field plate. The P-type well 140 at the surface 160 of the epitaxial layer or the drift region 130 provides a body region. The N-type well 150 within the p-type wells 140 provides a contact region and provides a source. A channel 170 is formed beneath a gate 180 which is separated using a gate dielectric layer 190.

The MOSFET 100 also includes a lateral extension region 145 extending from the body region 140. The lateral extension 145 extends laterally from the lower part of the body region 140 into the drift region 130. The lateral extension 145 is formed using ion implantation together with two stage photomasking to extend the lower part of the junction laterally. This lower implant is optimised in terms of dose and dimensions and is combined with an optimised field oxide 195 thickness and metal field plate 185. The lateral extension 145 extends towards the direction to which the field plate 185 extends over the field oxide 195 adjacent the source region. Generally the lateral extension 145 extends further/more than the field plate 195 extension. The lateral extension 145 allows higher breakdown voltage (Vbr) to be achieved than theoretical limits predict for the given doping level. Due to the presence of the lateral extension 145, a vertical p-n junction is formed between the upper surface 145a of the lateral extension and the drift region 130 which reduces peak electric field (EF). This structure is different from existing solutions which use lateral p-n junctions to achieve a similar result. A further vertical p-n junction is formed by the lower surface 145b of the lateral extension 145 and the drift region 130. This p-n junction can also contribute to achieve higher breakdown voltage.

The p-type body region 140 can have two portions. The first portion is the top portion in which the channel region 170 is formed. The highly doped p region 155 is also formed in the top portion of the body region 140. The top portion includes relatively higher doping concentration. The second portion is below the top portion and therefore is deeper than the top portion. The deeper portion includes relatively less doping concentration than the top portion. The lateral extension 145 is extended from the deeper portion of the body region 145. The doping concentration of the lateral extension is generally substantially the same as the doping concentration of the deeper portion of the body region 145. The doping concentration of the lateral extension is generally about 10^{16} cm^{-3} to 10^{18} cm^{-3}, preferably less than about 10^{17} cm^{-3}. The lateral extension 145 is formed in such a way that there is a vertical space between the lateral extension 145 and the surface 160 of the device. In one example, the vertical space

between the lateral extension 145 and the surface 160 of the device is about 0.05 μm to 0.6 μm, preferably about 0.1 μm.

The proposed lateral extension 145 (deep p-implant) can also help to reduce the peak electric field in the active area (e.g. in the drift region 130), at the top portion of the body region 140 and drift region junction (p+/n-epi junction) at the surface 160 of the device. Generally, in a conventional device, high drift region (n-epi) doping and p+ body region (in the top portion of the body region) curvature can lead to a higher electric field (EF) at the edge of the p+ body compared to the electric field (EF) at the vertical p+ body/n-epi junction in the active area of the device (when there is no lateral extension present in the structure). Lowering the drift region (n-epi) doping is not always possible and without it, the maximum achievable breakdown voltage (Vbr) will be limited by the curvature of the p+/n-epi junction. Using this lowly doped deep p-implant 145, or the lateral extension 145, as an extension of the body region 140 in the active area too, the peak electric field (EF) can be reduced leading to an increased breakdown voltage of the device (providing that the breakdown voltage in the termination is always higher than in the active region). The lateral extension 145 is formed by ion implantation of the aluminum material which is fully compatible in wide band-gap material (e.g. SiC) based fabrication techniques.

It will be appreciated that the p-type lateral extension 145 is used as a termination structure in a high voltage device. The lateral extension 145 is only implanted in devices which are located near the perimeter, outside or outer devices of an array of devices, where a typical termination structure otherwise is generally employed. The devices located in the central portion of the array may not have such lateral extension 145 structures. The lateral extension structure 145 generally extends laterally into the drift region in a direction which is opposite to the direction to which the gate extends from source to the drift region. In other words, the lateral extension 145 is generally not below the channel region 170 in the device.

The transistor of Fig.3 can be manufactured using a wide band-gap semiconductor material, for example, SiC, GaN and/or diamond. In one embodiment, the substrate 110, the drain contact layer 120, the drift region 130, the body region 140, the lateral extension 145, the source region 150 each include 4H-SiC material. Alternatively, the substrate 110 can include silicon material and the remaining regions can have 3C-SiC

material. In this particular example, the MOSFET shown in Figure 3 is able to support much greater breakdown voltages due to the use of 3C-SiC in the epitaxial drift region 130. At the same time the on-resistance of the 3C-SiC MOSFET can be significantly lower than the 4H-SiC MOSFET. This is because a better channel mobility is observed
5 in 3C-SiC (compared to 4H-SiC) and therefore the on-resistance of the channel region formed between the drift region 130 and the source region 150 can be significantly reduced. It will be appreciated that, in an alternative embodiment, the substrate 110 can include GaN and the remaining regions can have GaN as well. It is also possible that the substrate includes silicon material and the remaining regions each include
10 GaN. In one embodiment, the substrate 110 can include SiC and the remaining regions each include GaN.

Referring to Figure 4, an example of a vertical power semiconductor transistor 200 in the form of an insulated gate bipolar transistor (IGBT) is shown. Many features of the
15 IGBT in Figure 4 are the same as the MOSFET of Figure 3 and therefore carry the same reference numerals, except the IGBT 200 includes a p+ type substrate 215 and a p+ type collector layer or the first semiconductor region 225. The first semiconductor region 225 forms a carrier injector region in the IGBT. It will be appreciated that the off-state operation of the IGBT 200 is substantially similar to that of the MOSFET 100 of
20 Figure 3. In the off-state, the vertical junctions 145a, 145b between the lateral extension and drift region 130 help to reduce the peak electric field at the surface 160 of the device. Therefore the p-lateral extension 145 in the IGBT can act as a termination structure in the device. The doping concentration of the lateral extension 145 is substantially the same as that described for the MOSFET structure 100 in Figure
25 1. The vertical distance between the p-lateral extension 145 and the surface 160 of the device is also substantially the same as the MOSFET 100 of Figure 3.

In one embodiment, all the layers of the IGBT can have 4H-SiC. Alternatively, the p+ substrate can be made of silicon and the remaining layers can include 3C-SiC. It will be
30 appreciated that a heterostructure is formed between the p+ silicon substrate 215 and p+ 3C-SiC layer 225. The 3C-SiC material in the first semiconductor (epitaxial) region 225 (~2 microns) just above the SiC/Si interface is very heavily defective because of the lattice miss-match between the two materials and heavily doped with Al as-grown, consequently this defective region is very conductive. In this way the heterojunction
35 structure and consequent potential barriers can be overcome by becoming a

quasi-metallic interface due to the presence of the dislocations, Al doping during epitaxial growth and Boron up-diffusion from the Si substrate. It will be appreciated that, in an alternative embodiment, the substrate 215 can include GaN and the remaining regions can have GaN as well. It is also possible that the substrate 215 includes silicon material and the remaining regions each may include GaN. In one embodiment, the substrate 215 can include SiC and the remaining regions each may include GaN.

Referring to Figure 5, an example of a vertical PIN diode 700 is shown. The PIN diode 700 includes a substrate 710 on which an n-type epitaxial layer (or the first semiconductor region) 720 is formed to provide a cathode contact. An n-type lowly doped drift region 730 is formed on the n-type epitaxial layer 720. A p-type body region 740 is formed within the drift region 730 and highly doped p+ type region 750 is formed within the body region 740. The p+ doped region 750 forms an anode contact region. A lateral extension 745 is formed from the deeper part of the body region 740 extending laterally into the drift region 730. In the off-state, the lateral extension 745 operates in the same way as described above in respect of the MOSFETs and IGBTs above. The vertical junctions between the lateral extension 745 and the drift region 730 helps to reduce the peak electric field at the surface of the device which is otherwise created due to the curvature of the body region 740 at the surface of the device. Similar to the embodiments described above, the substrate 710 can include silicon material and the remaining layers can include 3C-SiC. Alternatively, all the layers of the PIN diode 700 can be made of 4H-SiC. Yet alternatively, the substrate 215 can include GaN and the remaining regions can have GaN as well. It is also possible that the substrate 215 includes silicon material and the remaining regions each include GaN. In one embodiment, the substrate 215 can include SiC and the remaining regions each may include GaN.

Referring to Figure 6, an example of a vertical Schottky diode 800 is shown. The Schottky diode 800 includes a substrate 810 on which an n-type epitaxial layer (or the first semiconductor region) 820 is formed to provide a cathode contact. Both the substrate 810 and the n-type epitaxial layer 820 are highly doped and thus the cathode contact is an ohmic contact. An n-type lowly doped drift region 830 is formed on the n-type epitaxial layer 820. A highly doped p+ doped region 850 (or the second semiconductor region) is formed within the drift region 830. A local ohmic metal contact

855 over the p+ doped region 850 is firstly formed using a high temperature. After this, a Schottky metal contact 865 is formed directly on the drift region 830. The Schottky contact 865 is formed using a relatively lower temperature compared to the temperature used for forming the ohmic contact on the p+ doped region 850. The
5 Schottky contact 865 and ohmic contact 855 may be made of Nickel and the ohmic contact 855 may be made of titanium disilicide (TiSi2), although other suitable materials may be used. It will be appreciated that TiSi2 may be used when the Schottky diode uses 3C-SiC material. Furthermore, an Aluminium contact (not shown) is formed on the Schottky contact 865 and the ohmic contact 855 to short these
10 together and to form a high conductivity connection layer.

In Figure 6, a lateral extension 845 is formed from the deeper part of the p+ doped region 850 extending laterally into the drift region 830. The p+ doped region 850 is used to connect to a guard ring structure. At high voltage/current the p+ doped region
15 850 forward biases and conductivity modulates the drift region 830, reducing its resistance and moderating the power dissipated. This is advantageous for a robust power component. The lateral extension 845 extends under the edges of the Schottky contact 865 to act as a shield in a reverse bias operation. The length of the Schottky contact 865 is about 8 μm. The length of the lateral extension towards the Schottky
20 contact 865 can be about 2 μm.

In the structure of Figure 6, all the layers can include silicon material. Alternatively, it is possible that the substrate 810 has silicon material and the remaining layers have 3C-SiC material. It may be also possible that all the regions of the diode 800 have 4H-SiC
25 material. Other wide band-gap semiconductor materials such as GaN or diamond are possible to use. For example, all the regions of the diode may have GaN material. Alternatively, the substrate may have SiC material and the remaining layers may have GaN. Yet alternatively, the substrate may have silicon material and the remaining layers may have GaN.

30

Although the aforementioned description states the use of mainly SiC and GaN, it would be apparent to the skilled person that other polytypes of wide band-gap semiconductor materials can be equally used in the devices described above.

Although the aforementioned description illustrates mainly vertical semiconductor device, it would be appreciated that the lateral extensions can be used in lateral power devices as well, such as lateral MOSFETs, IGBTs and diodes. In lateral devices, the lateral extensions would be used as interconnects and/or insulating means from the surrounding low voltage devices. It will be also appreciated that the lateral extension disclosed above can also be used in a lateral-high-electron-mobility-transistor (HEMT) using GaN material.

It will be appreciated that the lateral extension from the deeper part of the body region can be introduced in a wide band-gap semiconductor based thyristor, a gate turn-off (GTO) thyristor, a gate-commutated thyristor (GCT), and/or a bipolar junction transistor (BJT). It will be appreciated that the layout of the lateral extension extending from the deeper part of the body region is not limited to what has been presented as hereinbefore as long as the concept is the same.

It will also be appreciated that terms such as "top" and "bottom", "above" and "below", "lateral" and "vertical", and “under” and “over”, “front” and “behind”, “underlying”, etc. may be used in this specification by convention and that no particular physical orientation of the device as a whole is implied.

It will be appreciated that the doping concentrations of various layers of the transistors discussed with reference to Figures 3 to 6 are those used in the corresponding state of the art transistors.

It will be noted that the term “first conductivity type” can refer to a p-type doping polarity and the term “second conductivity” can refer to a n-type doping polarity. However, these terms are not restrictive. It will be appreciated that all doping polarities mentioned above could be reversed, the resulting devices still being in accordance with the present invention. It will be appreciated that the emitter, collector and gate could be arranged to be out-of-plane or to be differently aligned so that the direction of the carriers is not exactly as described above, the resulting devices still being in accordance with the present invention.

Although the invention has been described in terms of preferred embodiments as set forth above, it should be understood that these embodiments are illustrative only and that the claims are not limited to those embodiments. Those skilled in the art will be able to make modifications and alternatives in view of the disclosure which are
5 contemplated as falling within the scope of the appended claims. Each feature disclosed or illustrated in the present specification may be incorporated in the invention, whether alone or in any appropriate combination with any other feature disclosed or illustrated herein.

10

CLAIMS:

1. A wide band-gap high voltage semiconductor transistor comprising:

a semiconductor substrate;

5 a semiconductor drift region of a second conductivity type disposed on the semiconductor substrate;

a body region of a first conductivity type, opposite the second conductivity type, located within the semiconductor drift region;

a source region of the second conductivity type located within the body region;

10 a gate placed above and in contact to the source region, the gate to control charge in a channel region between the semiconductor drift region and the source region and to thereby control flow of charge within the semiconductor drift region;

wherein the body region comprises a lateral extension of the first conductivity type extending laterally into the drift region, the lateral extension being spaced from the 15 surface of the transistor.

2. A transistor according to claim 1, wherein the surface of the transistor is parallel to the channel region.

20 3. A transistor according to claim 1 or 2, wherein the lateral extension is vertically spaced from the surface of the transistor.

4. A transistor according to any preceding claim, wherein the body region comprises a first portion adjacent the gate and a second portion located deeper than 25 the first portion, the doping concentration of the first portion being higher than the doping concentration of the second portion.

5. A transistor according to claim 4, wherein the lateral extension extends laterally only from the second deeper portion of the body region.

30

6. A transistor according to claim 4 or 5, wherein the doping concentration of the lateral extension is substantially the same as the doping concentration of the second deeper portion of the body region.

7. A transistor according to any preceding claim, wherein the lateral extension extends from the body region in a lateral direction which is opposite to a direction to which the gate extends from the source to the drift region.

5 8. A transistor according to any preceding claim, wherein the lateral extension forms a termination structure in the transistor.

9. A transistor according to any preceding claim, further comprising a field insulator adjacent the source region and a source electrode extending over the field
10 insulator, wherein the lateral extension extends further into the drift region compared to the field plate extending over the field insulator.

10. A transistor according to claim 9, wherein the thickness of the field insulator, the doping concentration of the lateral extension and the field plate extension over the field
15 insulator are adjusted together so that an improved breakdown voltage is achieved.

11. A transistor according to any preceding claim, wherein the transistor is configured such that the electric field formed at vertical junctions between the lateral extension and the drift region reduces an electric field formed between the body region
20 and drift region at the surface of the transistor.

12. A transistor according to any preceding claim, wherein the semiconductor substrate comprises monocrystalline silicon material.

25 13. A transistor according to claim 12, wherein the semiconductor drift region, the body region, the lateral extension and the source region each comprise a material comprising 3-step cubic silicon carbide (3C-SiC).

14. A transistor according to any one of claims 1 to 11, wherein the semiconductor
30 substrate, the semiconductor drift region, the body region, the lateral extension and the source region each comprise a material comprising 4H-SiC.

15. A transistor according to any one of claims 1 to 11, wherein the semiconductor substrate, the semiconductor drift region, the body region, the lateral extension and the
35 source region each comprise a material comprising GaN.

16. A transistor according to any one of claims 1 to 11, wherein the semiconductor substrate comprises monocrystalline silicon material, and the semiconductor drift region, the body region, the lateral extension and the source region each comprise a material comprising GaN.

5

17. A transistor according to any one of claims 1 to 11, wherein the semiconductor substrate comprises SiC material, and the semiconductor drift region, the body region, the lateral extension and the source region each comprise a material comprising GaN.

10 18. A transistor according to any preceding claim, further comprising a first semiconductor region disposed between the semiconductor substrate and the drift region, the first semiconductor region comprising a material comprising 3C-SiC, 4H-SiC or GaN.

15 19. A transistor according to claim 18, wherein the first semiconductor region is of the second conductivity type and the semiconductor substrate is of the second conductivity type.

20. A transistor according to claim 19, wherein the transistor is a vertical power
20 metal-oxide-semiconductor field effect transistor (MOSFET).

21. A transistor according to claim 18, wherein the first semiconductor region is of the first conductivity type and the semiconductor substrate is of the first conductivity type.

25

22. A transistor according to claim 21, wherein the transistor is a vertical power insulated gate bipolar transistor (IGBT).

23. A wide band-gap high voltage semiconductor device comprising:
30 a semiconductor substrate of a second conductivity type;
a first semiconductor region of the second conductivity type disposed on the semiconductor substrate;
a semiconductor drift region of the second conductivity type disposed on the first semiconductor region, the first semiconductor region having higher doping
35 concentration than the drift region;

a body region of the first conductivity type, opposite the second conductivity type, located within the semiconductor drift region;

wherein the body region comprises a lateral extension of the first conductivity type extending laterally into the drift region, the lateral extension being spaced from the surface of the device.

24. A device according to claim 23, wherein the lateral extension is vertically spaced from the surface of the device.

25. A device according to claim 23 or 24, wherein the entire lateral extension is vertically spaced from the surface of the device.

26. A device according to any one of claims 23 to 25, wherein the device is a vertical PIN diode.

27. A device according to any of claims 23 to 26, wherein the semiconductor substrate comprises monocrystalline silicon material.

28. A device according to claim 27, wherein the first semiconductor region, the semiconductor drift region, the lateral extension and the body region each comprise a material comprising 3-step cubic silicon carbide (3C-SiC).

29. A device according to any of claims 23 to 26, wherein the semiconductor substrate, the first semiconductor region, the semiconductor drift region, the lateral extension and the body region each comprise a material comprising 4H-SiC.

30. A device according to any one of claims 23 to 26, wherein the semiconductor substrate, the first semiconductor region, the semiconductor drift region, the lateral extension and the body region each comprise a material comprising GaN.

31. A device according to any one of claims 23 to 26, wherein the semiconductor substrate comprises monocrystalline silicon material, and the first semiconductor region, the semiconductor drift region, the lateral extension and the body region each comprise a material comprising GaN.

32. A device according to any one of claims 23 to 26, wherein the semiconductor substrate comprises SiC material, and the first semiconductor region, the semiconductor drift region, the lateral extension and the body region each comprise a material comprising GaN.

5

33. A high voltage semiconductor device comprising:

a semiconductor substrate of a second conductivity type;

a first semiconductor region of the second conductivity type disposed on the semiconductor substrate;

10 a semiconductor drift region of the second conductivity type disposed on the first semiconductor region, the first semiconductor region having higher doping concentration than the drift region;

a Schottky metal contact formed directly on the semiconductor drift region on a surface of the device;

15 a second semiconductor region of a first conductivity type, opposite to the second conductivity type, formed on the surface of the device and within the semiconductor drift region, the second semiconductor region having higher doping concentration than the drift region; and

a lateral extension of the first conductivity type extending laterally from the 20 second semiconductor region into the drift region, the lateral extension being spaced from the surface of the device.

34. A device according to claim 33, wherein the lateral extension is vertically spaced from the surface of the device.

25

35. A device according to claim 33 or 34, wherein the entire lateral extension is vertically spaced from the surface of the device.

36. A device according to claim 33, 34 or 35, wherein the lateral extension extends 30 laterally only from a deeper portion of the second semiconductor region.

37. A device according to any of claims 33 to 36, wherein the doping concentration of the lateral extension is lower than the second semiconductor region.

38. A device according to any of claims 33 to 37, wherein the lateral extension extends laterally towards the Schottky metal contact.

39. A device according to any of claims 33 to 38, further comprising a first ohmic
5 contact operatively connected to the first semiconductor region and a second ohmic contact formed on the second semiconductor region.

40. A device according to any of claims 33 to 39, wherein the semiconductor substrate, the first semiconductor region, the drift region, the second semiconductor
10 region and the lateral extension each comprise monocrystalline silicon material.

41. A device according to any of claims 33 to 39, wherein the semiconductor substrate, the first semiconductor region, the drift region, the second semiconductor region and the lateral extension each comprise 4H-SiC.
15

42. A device according to any of claims 33 to 39, wherein the semiconductor substrate comprises monocrystalline silicon material, and the first semiconductor region, the drift region, the second semiconductor region and the lateral extension each comprise 3C-SiC.
20

43. A device according to any of claims 33 to 39, wherein the semiconductor substrate, the first semiconductor region, the drift region, the second semiconductor region and the lateral extension each comprise GaN.

25 44. A device according to any of claims 33 to 39, wherein the semiconductor substrate comprises moncrystalline silicon material, and the first semiconductor region, the drift region, the second semiconductor region and the lateral extension each comprise GaN.

30 45. A device according to any of claims 33 to 39, wherein the semiconductor substrate comprises SiC material, and the first semiconductor region, the drift region, the second semiconductor region and the lateral extension each comprise GaN.

46. A method for manufacturing a wide band-gap high voltage semiconductor transistor, the method comprising:

forming a semiconductor substrate;

forming a semiconductor drift region of a second conductivity type on the semiconductor substrate;

forming a body region of a first conductivity type, opposite the second conductivity type, located within the semiconductor drift region;

forming a lateral extension of the first conductivity type extending laterally from the body region into the drift region, the lateral extension being spaced from the surface of the transistor;

forming a source region of the second conductivity type located within the body region;

forming a gate placed above and in contact to the source region, the gate to control charge in a channel region between the semiconductor drift region and the source region and to thereby control flow of charge within the semiconductor drift region.

47. A method according to claim 46, wherein forming the lateral extension comprises applying a two stage photo-masking to implant the lateral extension.

48. A method according to claim 46 or 47, wherein the lateral extension is ion-implanted using Aluminium or Boron material.

49. A method according to claim 46, 47, or 48, further comprising vertically spacing the lateral extension from the surface of the transistor.

50. A method according any of claims 46 to 49, further comprising forming a first semiconductor region between the semiconductor substrate and the drift region.

51. A method according to claim 50, further comprising forming the semiconductor substrate using a material comprising monocrystalline silicon, and forming each of the semiconductor drift region, the first semiconductor region, the body region, the lateral extension and the source region using a material comprising 3-step cubic silicon carbide (3C-SiC).

52. A method according to claim 50, further comprising forming each of the semiconductor substrate, the first semiconductor region, the semiconductor drift region, the body region, the lateral extension and the source region using a material comprising 4H-SiC.

5

53. A method according to claim 50, further comprising forming each of the semiconductor substrate, the semiconductor drift region, the body region, the lateral extension and the source region using a material comprising GaN.

10 54. A method according to claim 50, further comprising forming the semiconductor substrate using monocrystalline silicon material, and forming each of the semiconductor drift region, the body region, the lateral extension and the source region using a material comprising GaN.

15 55. A method according to claim 50, further comprising forming the semiconductor substrate using SiC material, and forming each of the semiconductor drift region, the body region and the source region using a material comprising GaN.

56. A method of manufacturing a high voltage semiconductor device, the method
20 comprising:

forming a semiconductor substrate of a second conductivity type;

forming a first semiconductor region of the second conductivity type disposed on the semiconductor substrate;

forming a semiconductor drift region of the second conductivity type disposed
25 on the first semiconductor region, the first semiconductor region having higher doping concentration than the drift region;

forming a Schottky metal contact formed directly on the semiconductor drift region on a surface of the device;

forming a second semiconductor region of a first conductivity type, opposite to
30 the second conductivity type, formed on the surface of the device and within the semiconductor drift region, the second semiconductor region having higher doping concentration than the drift region; and

forming a lateral extension of the first conductivity type extending laterally from the second semiconductor region into the drift region, the lateral extension being
35 spaced from the surface of the device.

57. A method according to claim 56, wherein forming the lateral extension comprises applying a two stage photo-masking to implant the lateral extension.

5 58. A method according to claim 56 or 57, wherein the lateral extension is ion-implanted using Aluminium or Boron material.

59. A method according to claim 56, 57, or 58, further comprising vertically spacing the lateral extension from the surface of the device.

10

60. A method according to any of claims 56 to 59, further comprising forming an ohmic contact on the second semiconductor material, the ohmic contact comprising titanium disilicide material.

15 61. A method according to claim 60, further comprising forming the Schottky contact using a relatively low temperature compared to that used for forming the ohmic contact, the Schottky contact comprising nickel material.

62. A semiconductor device, and a method for manufacturing the semiconductor
20 device, substantially as hereinbefore described with reference to and as illustrated, in the accompanying drawings.

Intellectual Property Office

Application No:	GB1416403.2	**Examiner:**	Mr Huw Thomas
Claims searched:	1-22, 46-55	**Date of search:**	10 March 2015

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1-3, 11-14, 22, 46-52	EP0869558 A2 (MOTOROLA INC) - See figure 3 and abstract at least.
X	1-3, 11-12, 46-50	US2003/218188 A1 (JEON) - See figure 4 at least.
X	1-3, 11-12, 46-50	US2009/294849 A1 (MIN) - See figure 1 at least.
A	--	EP0822600 A1 (MOTOROLA INC) - See figure 10.
A	--	US2011/241114 A1 (SU) - See figure 2.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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Field of Search:

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H01L

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EPODOC, WPI.

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International Classification:

Subclass	Subgroup	Valid From
H01L	0029/10	01/01/2006
H01L	0029/66	01/01/2006

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Application No:	GB1416403.2	**Examiner:**	Mr Huw Thomas
Claims searched:	33-45, 56-61	**Date of search:**	29 June 2015

Patents Act 1977
Further Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	--	WO02/084745 A2 (SILICON WIRELESS CORP) - See figure 1 and abstract.
A	--	US2004/232450 A1 (YILMAZ) - See figures

Categories:

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Application No:	GB1416403.2	**Examiner:**	Mr Huw Thomas
Claims searched:	23-32	**Date of search:**	29 June 2015

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Further Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
Y	23-32	US5780878 A (BHATNAGAR) - See figure 1
Y	23-32	US4837606 A (GOODMAN) - See figure 2
A	--	US2009/114969 A1 (SUZUKI) - See claims at least.
A	--	CN201725794 U (WEI) - See "Embodiment 1"

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&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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H01L	0029/66	01/01/2006