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(54) **Improvements relating to data transmission systems**

(57) A data transmission system in which a train of rectangular data pulses of logic 0 and/or logic 1 significance is produced in synchronism with a train of rectangular timing signals and in which the baud rate of the timing signals is measured by timing signal sampling means and the degree of steepness of the leading and trailing edges of the data pulses is automatically adjusted in dependence upon the measured baud rate.

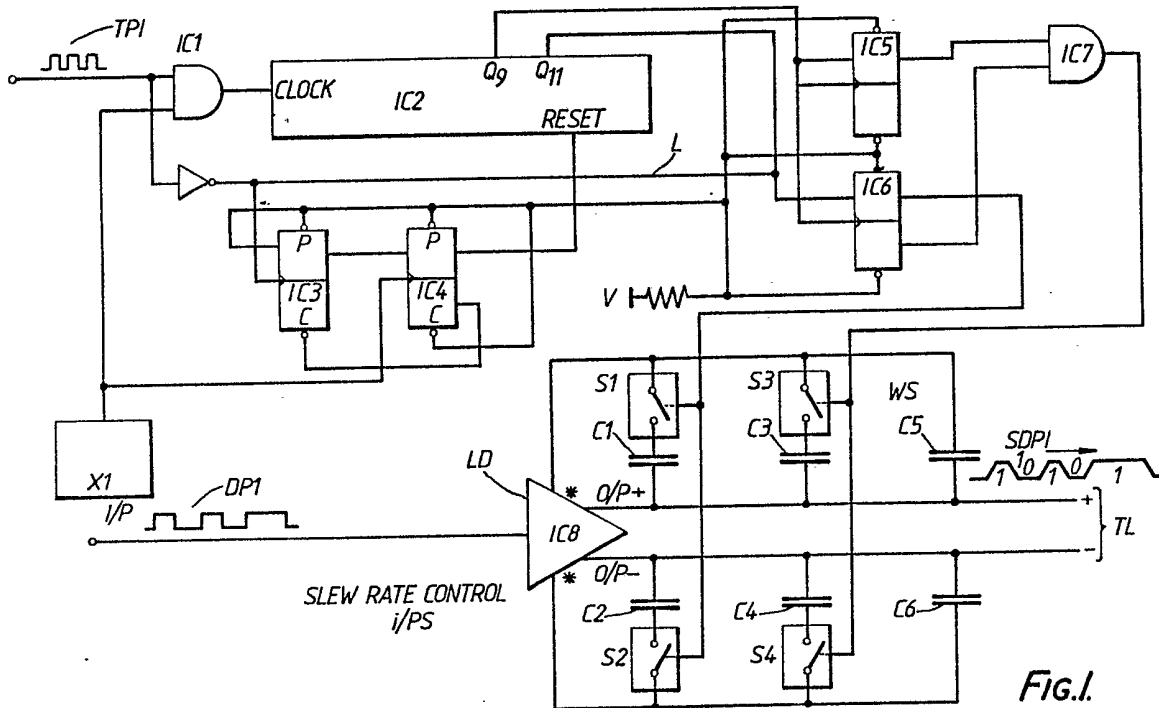


Fig.1.

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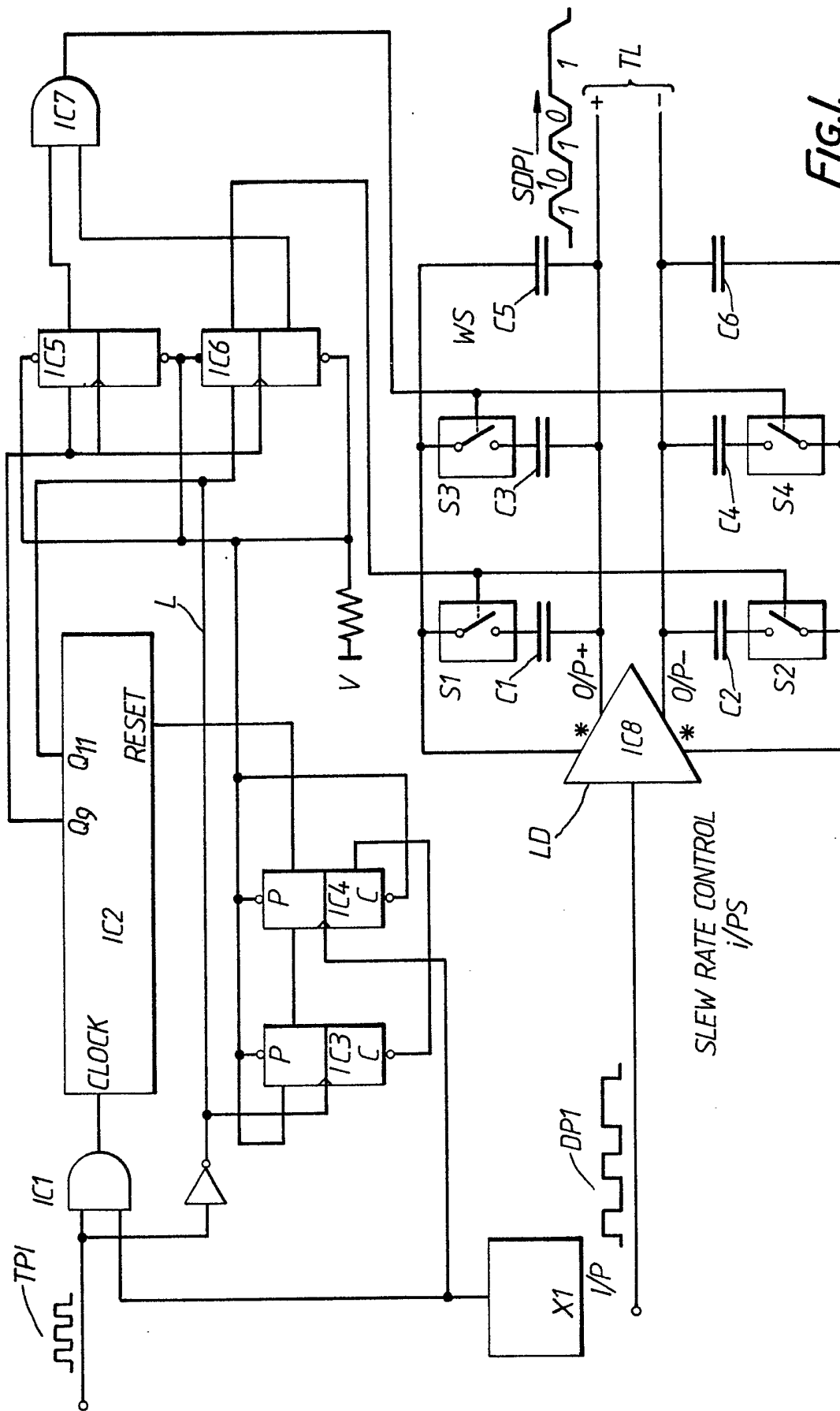
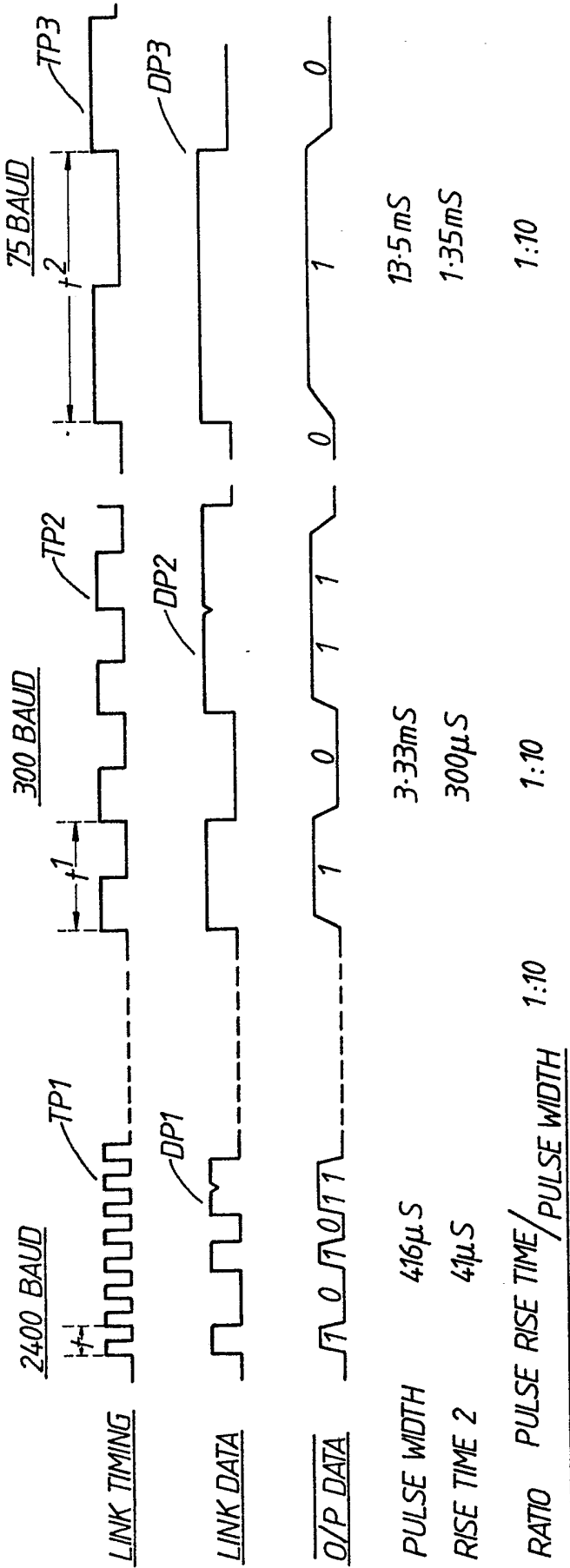
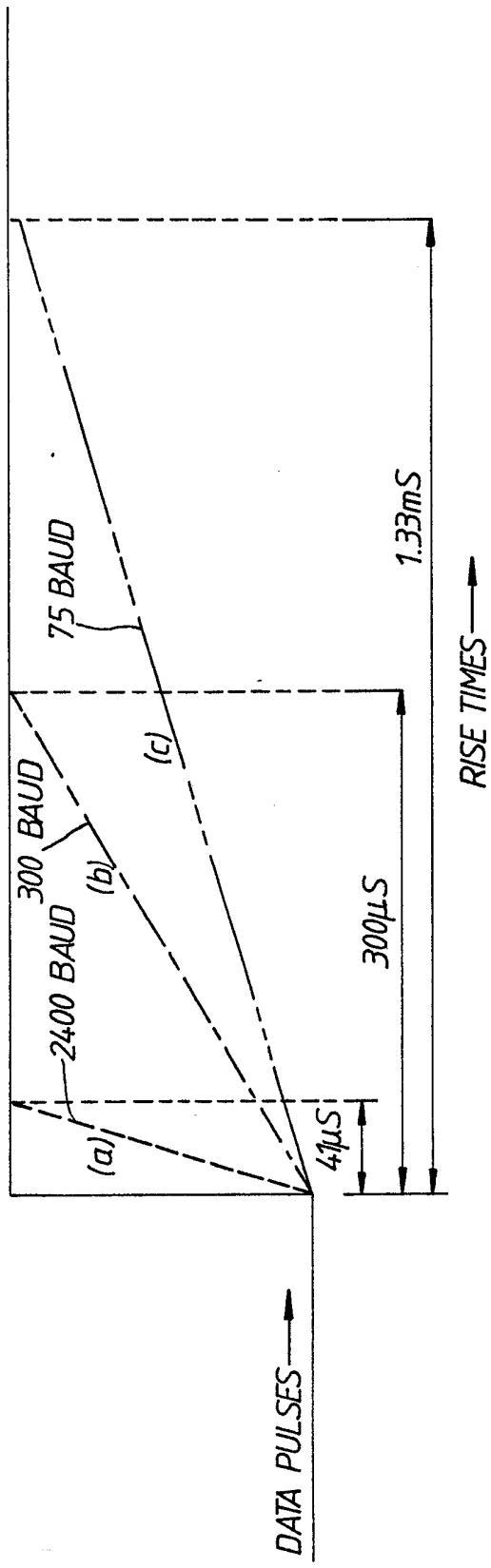


FIG.1.



BAUD RATE	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q1
2400	10	10	10	10	10	10	10	10	10	10	1	---
300	10	10	10	10	10	1	10	1	1	1	1	---
75	10	10	10	1	10	1	1	1	1	1	1	---

FIG.2.



BAUD RATE	SWITCHES OPEN	SWITCHES CLOSED
2400	S1, S2, S3, S4	—
300	S1, S2	S3, S4
75	S3, S4	S1, S2

FIG.3.

## SPECIFICATION

**Improvements relating to data transmission systems**

5 This invention relates to data transmission systems in which trains of data pulses of logic 0 and/or logic 1 significance are transmitted over serial data links.

10 In data transmission systems handling secure data, serial data links may constitute a potential source of inadvertent data leakage due to information radiation resulting from square-wave characteristics of the transmitted data pulses. For the avoidance of such data leakage, it is necessary for  
15 the steepness of the leading and trailing edges of the data pulses to be reduced in dependence upon the baud rate of the data to be transmitted over the serial link.

20 According to the present invention there is provided a data transmission system in which a train of rectangular data pulses of logic 0 and/or logic 1 significance is produced in synchronism with a train of rectangular timing signals and in which the baud rate of the timing signals is measured by timing  
25 signal sampling means and the degree of steepness of the leading and trailing edges of the data pulses is automatically adjusted in dependence upon the measured baud rate.

30 In carrying out the present invention the timing signal sampling means may comprise a binary counter which may be stepped during the positive excursion of each timing signal by clock pulses having a relatively high repetition frequency compared to the frequency of the timing signals. An output from the  
35 binary counter at the end of the positive excursion of a timing signal may be arranged to produce the selective operation of switching means for the adjustment of the capacitance of a wave-shaping circuit in order to shape, as required, the data pulses to be  
40 transmitted over a data transmission serial link or channel. The switching means may be operated by the outputs from flip-flop means connected to respective output terminals of the binary counter and these flip-flop means may be arranged to be latched  
45 by the trailing or negative-going edge of each timing signal as sampling takes place, thereby allowing the binary counter to be re-set in readiness for sampling the next timing signal.

50 By way of example the present invention will now be described with reference to the accompanying drawings in which:

55 *Figure 1* shows part of a data transmission system including a wave-shaping circuit capable of being automatically adjusted in accordance with the baud rate of data pulses to be transmitted over a serial link or channel;

*Figure 2* shows the wave-shaping of data pulses having different baud rates, as well as a count table for the binary counter of the system of *Figure 1*; and,

60 *Figure 3* shows specific detail relating to the wave-shaping of the data pulses, as well as a table indicating the switch operation that takes place in the wave-shaping circuit of *Figure 1*.

65 In operation of the data transmission system shown in part in the drawings, a train of rectangular

timing signals TP1, TP2 or TP3 are produced having a baud rate of 2,400, 300 or 75 (see *Figure 2*) which may be preselected by computer software means (not shown) in accordance with the character of the transmission line or channel TL to be used for data transmission purposes. The timing signals, such as the signals TP1, are applied to a gate IC1 which is opened by the positive-going edge of a timing signal to allow a binary counter IC2 to be stepped by clocking pulses  
70 derived from an oscillator X1 having a high frequency (e.g. 230KHz) compared to the frequency or baud rate of the timing signals TP1, TP2 or TP3.

75 At the end of the positive excursion of a timing signal, the binary counter will be providing specific logic 1 and/or logic 0 outputs at the counter output terminals Q9 and Q11 (See table in *Figure 2*) and these outputs are stored in bistable devices IC5 and IC6, respectively, as they become latched by the trailing or negative-going edge of the positive excursion  
80 of a timing signal received over line L. This trailing edge also causes monostable switching-means comprising devices IC3 and IC4 to be triggered for providing outputs for resetting the binary counter IC2 in readiness for commencement of the next counting operation at the beginning of the positive half-cycle of the next timing signal. The bistable device IC5 produces a logic 1 or logic 0 output corresponding to that of output terminal Q9 of the binary counter whilst the bistable device IC6 produces complementary logic outputs the upper of which, as  
85 viewed in *Figure 1*, corresponds to that of the output terminal Q11 of the binary counter. Exemplary logic outputs from the binary counter, including the outputs from terminals Q9 and Q11 for different baud rates of timing signals are shown in the count table embodied in *Figure 2* of the drawings.

90 The logic output from the bistable device IC5 and the complementary count logic output from the bistable device IC6 are applied to an AND gate IC7. The output from this AND gate and the logic count output from the bistable IC6 are applied to analogue switching means S1 to S4 of a wave-shaping circuit WS including capacitors C1 to C6 of which the capacitors C1 to C4 are arranged to be selectively connected, or  
95 disconnected, by the analogue switching means S1 to S4 into or out of circuit with a line driver LD for shaping data pulses DP1 which are synchronised with the timing signals TP1 having a period "t" and which are applied to the input of the line driver LD.  
100 After shaping, the data pulses SDP1 are transmitted over the transmission channel TL.

105 As will be appreciated, the device IC6 and the AND gate IC7 produce mutually exclusive outputs. Consequently, when the switches S1 and S2 are closed the switches S3 and S4 are open and vice versa. In the absence of a logic 1 output from the gate IC7 or the device IC6 all switches S1 to S4 are open and the baud rate of 2400 is selected. It will also be appreciated that to prevent spurious outputs from low order counter outputs the lowest baud rate (i.e. highest count) outputs inhibit other high baud rate outputs by means of the gate IC7.

110 The selective operation of the analogue switching means S1 to S4 for producing the requisite shaping of the data pulses of the respective baud rates of  
125  
130

2,400, 300 and 75 is shown in the table of Figure 3. By referring to the binary counter output table in Figure 2 it will readily be seen that the logic 0 and/or 1 outputs at terminals Q9 and Q11 for the respective baud rates will produce the switch operations shown in Figure 3.

The pulse widths and rise times for the shaped data pulses at the three baud rates concerned are shown in Figures 2 and 3.

As will be appreciated from the foregoing, during transmission of data pulses the incoming timing signals will be continuously sampled by the clock binary counter IC2 and a change in baud rate of these timing signals will produce a different binary count output at terminals Q9 and Q11 at the end of a positive excursion of timing signal which in turn will produce modification of the capacitive wave-shaping circuit to vary, as appropriate, the shaping of the data pulses for transmission over the data transmission line or channel TL.

It will of course be appreciated that the circuit arrangement described may readily be modified to provide for an extended range of baud rates (e.g. 75, 150, 300, 600, 1,200 and 2,400, 4,800 or 9,600 or subsets thereof).

#### CLAIMS

1. A data transmission system in which a train of rectangular data pulses of logic 0 and/or logic 1 significance is produced in synchronism with a train of rectangular timing signals and in which the baud rate of the timing signals is measured by timing signal sampling means and the degree of steepness of the leading and trailing edges of the data pulses is automatically adjusted in dependence upon the measured baud rate.

2. A data transmission system as claimed in claim 1, in which the timing signal sampling means comprises a binary counter which is stepped by clock pulses having a relatively high repetition frequency compared to the frequency of the timing signals.

3. A data transmission system as claimed in claim 2, in which the binary counter is stepped by the clock pulses during the positive excursion of each timing signal.

4. A data transmission system as claimed in claim 3, in which an output from the binary counter at the end of the positive excursion of a timing signal produces selective operation of switching means for the adjustment of the effective capacitance of a wave-shaping circuit in order to shape the data pulses to be transmitted over the serial link transmission path.

5. A data transmission system as claimed in claim 4, in which the switching means is operated by outputs from flip-flop means connected to respective output terminals of the binary counter.

6. A data transmission system as claimed in claim 5, in which the flip-flop means are arranged to be latched by the trailing edge of each timing signal during sampling, thereby allowing the binary counter to be re-set in readiness for sampling the next timing signal.

7. A data transmission system substantially as hereinbefore described with reference to the accompanying drawings.

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