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(71)(72) Applicant and Inventor: SCHULTZ, Richard, M. [US/US]; 3370 Executive Drive, Marengo, IL 60152 (US).

(72) Inventors: RETYCH, James ; P.O. Box 851, Crystal Lake, IL 60014 (US). LAFRENZ, Joseph ; 710 Shaw Court, Schaumburg, IL 60194 (US). DOLEJS, Raymond ; 303 S. Prindle Avenue, Arlington Heights, IL 60004 (US).

(74) Agent: SHAPE, Steven, M.; 181 West Madison, Suite 4600, Chicago, IL 60602 (US).

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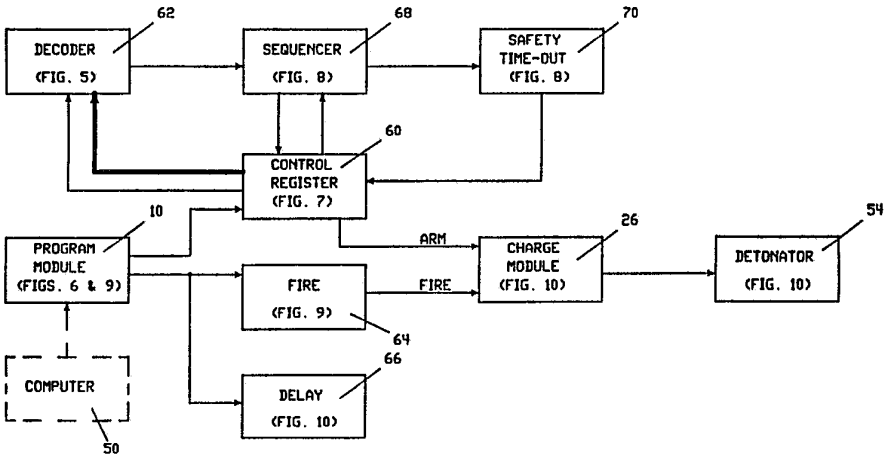

(57) Abstract

A control system for detonating a plurality of blast explosives is programmable to receive and store an arming sequence and firing sequence which is compared with an operator entered command. The system generates both an ARM signal and a FIRE signal, wherein the ARM signal initiates a charge circuit (26) to charge up a detonation circuit (54) and the FIRE command releases the charge to fire the circuit. The firing sequence contains a programmable delay (66) making sequential blasting possible. The system is designed to fail safely in the event both the ARM signal and the FIRE signal do not appear within a predetermined time frame.

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+ DESIGNATIONS OF "SU"

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ELECTRONIC CONTROL SYSTEM FOR EXPLOSIVES

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates generally to electronic detonator units and control systems for blasting operations, and particularly to secure programmable digital electronic sequential detonator systems.

Description of the Prior Art

Electronic detonators for discharging and igniting pyrotechnic devices in blasting operations have been available for at least 25 years. African Explosives and Chemical Industries, Ltd., now AECI, Ltd., pioneered some of the early developments in this field and a number of designs offered by AECI illustrate the advancement of the technology.

In the mid-60s, AECI developed a method for sequential activation of explosive detonators by electrical means, utilizing a pulse generator connected to a plurality of detonators. The pulse generator passed an electrical current through the first detonator in sequence, the current having a magnitude sufficient to energize and discharge the first detonator, the second detonator being initially charged upon discharge of the first, in sequential fashion. The energization of each detonator in the series was dependent upon the discharge of the detonator just ahead of it in the series. In electrical systems such as these, the current in the detonator charging circuit was sufficient to activate and fire the detonator, that is, the signaling circuit and the charging circuit were one and the same.

The next significant advance in the art, also by AECI, was the development of low energy signaling circuits to be used in conjunction with high power detonation circuits. In one such device, a network of propagating units was coupled to a like network of full strength detonators. As each propagator unit was energized in sequence by the low power signal, it would close a power circuit to the detonator and energize it for discharge. This system was advantageous over earlier systems in that it permitted use of a more accurate low power control signal to control the sequencing and triggering of the high

power detonator, relying on full power for energization while not using full power for control.

More recently, solid-state circuitry has been incorporated in sequential detonator systems, wherein the triggering circuitry is made up of low-level digital electronic components for triggering each high power detonator in the series via a relay and switching control system. These devices were more accurate and reliable than either analog or hard wired devices.

While the more recent advances in the art have provided more reliable low powered detonator systems, there remain many disadvantages in the detonator systems of the prior art. For example, safe, methodical shutdown in the event of signal error has been largely ignored. Programming has been complex and time consuming, and re-arming after shutdown or misfire has typically required a complicated rewiring procedure. Further, neither redundant comparison and confirmation of proper signals during operation, nor unauthorized operation lockout has been previously successful in a cost-efficient manner.

SUMMARY OF THE INVENTION

The detonator control circuit of the subject invention seeks to overcome the disadvantages of the prior art by providing an intelligent, secure detonator unit which is inexpensive to manufacture, easy to use, and provides substantially improved fail safe, security and shutdown features.

The detonator unit comprises a solid-state electronic programmer module for receiving programmed sequencing and firing data, and generating ARM and FIRE signals in accordance with the program data in response to a command sent from the programming or master computer. The programmer module is computer compatible so that all programmed input may be controlled by a host computer.

The detonator unit includes a low energy, fail safe dropout feature preventing units from detonating after a predetermined period of time in the event an accurate firing signal has not been generated. The unit permits a predetermined number of ref ire attempts in the event of dropout, prior to shutdown.

It is, therefore, an object and feature of the invention

to provide a programmable, secure detonator unit using low energy control signals to charge and fire a high energy detonator.

It is another object and feature of the invention to provide a detonator unit with secure, redundant, fail safe firing and, if necessary, shutdown procedures.

A further object and feature of the invention is to provide a cost-efficient detonator unit which can be easily programmed and reprogrammed for secure, fail safe use.

Other objects and features of the invention will be readily apparent from the drawings and description which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a hand-held computer compatible programmer for the detonator unit of the subject invention.

Fig. 2 is a diagrammatic side view of the interior of the detonator unit.

Fig. 3 is an overall system block diagram for the detonator unit.

Fig. 4 is a functional block diagram of the sequencing, arming and firing circuitry of a detonator unit made in accordance with the subject invention.

Fig. 5 is a detailed schematic diagram of the decoder unit illustrated in Fig. 4.

Fig. 6 is a detailed schematic diagram of the program module and delay circuitry shown in Fig. 4.

Fig. 7 is a detailed schematic of the control registers of the detonator unit shown in Fig. 4.

Fig. 8 is a detailed schematic of the sequencer circuit and safety time-out circuit of the detonator unit shown in Fig. 4.

Fig. 9 is a detailed schematic of the fire circuit of the detonator unit shown in Fig. 4.

Fig. 10 is a detailed schematic of the charge module and detonator circuitry of the detonator unit shown in Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in Fig. 1, the detonator control unit of the

present invention is adapted to include the hand-held programming module or programmer 10, having a computer compatible programming feature and adapted for connecting the module to a host computer at interface connector 12. The module includes a keypad 14 for entering firing codes to discharge the detonators. The control and FIRE signals may be hard wired to the detonators through cable 16 or may be transmitted by a wire less radio transmitter and receiver, as shown here (Figs. 2 and 3). The programmer 10 includes a display panel 18 which provides the operator with a readout of the firing command entered and a status of the program after programming has commenced at address line 20. Information as to the status of the charge on the charging module or battery is displayed at line 22, and the program delay cycle is displayed at line 24.

As shown in Fig. 2, the control module is hermetically sealed and is impervious to temperature and humidity. The control module 32 and charging circuit 26 are designed to fit in a control module 10 of approximately 20 millimeters x 125 millimeters x 70 millimeters, and can be easily hand held. An aperture 36 is provided in one end of the control module 10 or passing the fuse leads 40 and the transmitter antenna 42. A hermetic sealant 43 seals the hole against moisture and other contaminants. The fuse leads are connected directly to the detonator firing circuit and the control signals are transmitted via radio waves to a receiver associated with the detonator at the blast site. Alternatively, the programming function and energy control function may be carried out by separate hand-held units based on the desired application of the detonator unit.

The system block diagram of Fig. 3 illustrates how the program and detonator module fit within an operating system. The master computer 50 is hard wired to the programmer 10 through the computer interface connector 12. The control module transmits firing energy directly to the receiver detonator 54 by the fuse leads 40. The programmer 10 and computer 50 are linked to the radio transmitter 41 for sending control and fire commands to each of the detonator circuits 54, each of which include a receiving antenna 52. As shown, the

detonator unit can control up to 256 separate receiver detonators.

Typically, the master computer 50 is used to provide control and sequencing data to the programmer 10. A series of receiver/detonators 54 and associated blast charges including blasting caps are strategically placed at the blast site. The blasting caps are typically hard wired through fuse leads 40 to the detonator module 10. When the program data is properly entered, the operator enters a unique, secure firing code on the keypad of the programmer 10. If this matches the security code entered through the computer, the control and signal data are transmitted to the detonator 54 by the transmitter 41, antenna 42 and antenna 52, and the detonator module 10 simultaneously initiates the charge cycle for charging the charge module 26 (Fig. 4). At the programmed time, the charge is discharged via fuse leads 40 and energizes the detonator 54 for triggering the blast, as controlled by the control and FIRE signals received from the transmitter 41.

A functional circuit diagram is shown in Fig. 4. It will be understood that the modules and circuits there shown are for functional clarity only and are not intended to represent any physical configuration or any relationship relative to the modules described in Figs. 1-3. The functional diagram is supported by the detailed schematics of Figs. 5-10, and the appropriate figure (Fig.) number identified in each block of the diagram of Fig. 4 contains a substantially complete schematic for the module or circuit identified.

The detonator unit includes low-cost electronic control circuitry for energy storage and secure communications as shown in control module 10. The unit is designed to respond to a coded, secure, precisely timed transmission by delaying a programmable time interval and delivering a high energy, short duration electrical pulse to activate a detonator and blast explosive. The system can be programmed with a distinct code from 1 to 256, thereby allowing up to 256 detonations in a single program cycle. Discrete time delays for each detonator can be programmed, allowing sequencing of explosive charges to occur. A fail safe, low energy, dropout feature prevents the

detonators from detonating after a fixed period of time. The programmer module 10 is controlled by a host computer and is designed to include fail safe operation for the trigger command, including improper code lockout. The detonator control circuit of the invention also includes features to prevent random generation of the firing code. A remote transmitter assembly may be utilized to minimize RF radiation and pickup. As illustrated in Figs. 4-10, the device is structured to be integrated into one or two custom CMOS LSI circuits. Basically, the circuit design includes nine separate modules. As illustrated, the circuitry uses conventional SSI and MSI devices. Standard engineering nomenclature is used.

Referring specifically to Figs. 3 and 4, the specific sequencing and firing commands are entered into the program module 10 via the computer 50. At this time, unique firing codes are also entered. This program data is stored by the control register circuit 60 and is loaded into the comparator/decoder circuit 62 once the firing sequence is initiated. An operator enters a firing code into the program module 10 and this is compared by the decoder circuit 62 with the programmed firing code previously entered via the computer. If the codes match, the firing sequence is initiated.

Assuming a firing sequence is properly initiated, the control register circuit 60 outputs an ARM signal to the charge module 26, initiating an electrical energy charge sufficient to energize the detonator 54. The control register circuit 60 also sends a signal to the fire circuit 64 to accept the FIRE command entered at programmer 10. At this time, a predetermined programmed delay is initiated by the delay circuit 66, for delaying the generation of a FIRE signal by the fire circuit 64. The sequencer 68 determines the proper timing cycle of the unit and assures that the ARM signal is sent to the proper detonator 54 via the charge module 26. When the delay is complete, a FIRE signal is generated by the fire circuit 64 and the charge module releases a triggering pulse to the selected detonator 54. The circuit is designed so that both an ARM and a FIRE signal must be present at charge module 26 before a trigger pulse can be released. If either signal is

absent for any reason, the system is rendered inoperative.

The safety time out circuit 70 confirms that once the ARM signal has been generated within a specified period of time, the signal generated by the delay circuit 66 is also present. In the event the delay timer does not produce an output within a predetermined period of time, the safety time out circuit generates a signal to reset the control registers, rendering the circuit temporarily inoperative. After reset, the system repeats all sequences in a "retry" mode. If after the programmed number of retries the ARM and FIRE signals are not present within the specified period of time, the safety time out circuit 70 generates a "dump" signal to remove or dump all information in the control register circuit 60 and the decoder circuit 62, and to discharge the charge module 26, rendering the system inert until it is reprogrammed.

It should be appreciated by those skilled in the art that only one embodiment of the invention is illustrated by the specific electronic schematic diagrams of Figs. 5-10. It should also be appreciated that all modifications to these specific schematic diagrams (Figs. 5-10) and other configurations of electronic circuitry are contemplated by the present invention and fall within the scope of the claims herein. In the schematic diagrams of Figs. 5-10, standard design electrical/electronic nomenclature is utilized. Where required, the circuit components are identified by the standard component part number adapted by integrated circuit component manufacturers. Furthermore, the various signal lines continuing from one figure of the drawings to another are identified by matching reference numerals in all figures. For example, line 6A in Fig. 5 is continued as line 6A in Fig. 7.

Turning now to Fig. 5, a combination of the logic elements used in the decoder circuit 62 for bit timing, counting and decoding is shown in schematic form. The incoming serial data stream is controlled through a modulation scheme. Preferably, a modified "return to 0" modulation scheme having a six millisecond bit time is utilized. Each bit preferably has a rising edge at its beginning. In the illustrated embodiment, a logic 0 is represented by a 1 millisecond/5 millisecond

on/off ratio while a logic 1 is represented by a 5 millisecond/1 millisecond on/off ratio. The rising edge of each bit serves to resynchronize the bit timer consisting of the HC390 circuit U14 and the HC4017 circuit U15. The HC74 flip-flops U1A and U1B form the demodulator for the incoming data stream and are preferably "D" type or "Data" flip-flips. The HC4024 binary counter U2 is used to direct the signals to the various parts of the circuitry based upon total bits detected. The circuit concept is based upon the utilization of an ARM command and a FIRE command. These signals are independently generated and sent, and are separated in time by a time interval, preferably a minimum of 1 second. The ARM command consists of a 32 bit sequence and the FIRE command consists of an 8 bit sequence. The HC74 flip-flop U3A is set after the receipt of the 32nd bit and generates a greater than 32 bit signal. The HC74 flip-flop U3B is set after the receipt of the 40th bit and is used to start the timer if both FIRE and ARM codes have matched by generating a greater than 40 bit signal. Timing is initiated only after a proper match of all 40 bits has been detected.

As shown in Fig. 6 and Fig. 9, the programmer module 10 includes a series of 8 bit HC595 registers U34-U41. These registers contain the data bit patterns for the ARM code, FIRE code, delay time and detonator identification. These registers are programmed initially through the programmer 10 and are entered into the program at the "data-in" signal point 72 (Fig. 6). These registers define the primary data registers for the unit. All data received by the serial registers is compared to these bit patterns. The first 16 bits in the HC595 shift registers U35 and U34 (see Fig. 9) contain the detonator identification information and are not used internally within the device. The HC595 shift register U41 (also Fig. 9) contains the 8 bit delay time representation. In Fig. 6, shift registers U36, U37, U38 and U39 contain the ARM code. Shift register U40 contains the FIRE code. A state machine sequencer (Fig. 8), described herein, is used to perform the comparisons between the data pattern in these registers and the data registers.

The schematic for the control register module 60 of Fig. 4 is shown in Fig. 7. The control register module consists of five sequential 8 bit HC595 shift registers U25, U26, U27, U28 and U29. These devices make up the data registers within the detonator control system. The data which is detected by the RF receiver is sequentially shifted into this register chain. Upon the receipt of the 32nd bit of input data, steering logic in the decode circuit 62 redirects the data to the shift register U29, i.e. , the next 8 bits are directed into the FIRE code register U29. After receipt of the 32nd bit, the state machine in the sequencer network 68 begins operation.

The sequencer circuit 68 is illustrated in Fig. 8. Basically, the sequencing circuit comprises a sequential state machine. Its purpose is to do a byte-by-byte comparison between the program data registers U36, U37, U38, U39 and U40 and the control register mode namely data registers U25, U26, U27, and U28. The sequencer comprises the HC4017 module designated U18. After the receipt of the 32nd bit, the sequencer starts its cycle. The 4 bytes in data registers U25-U28 are sequentially compared with the 4 bytes in the programmed ARM code register. The comparisons are done byte-by-byte by comparator U31 (Fig. 7). Match or mismatched data is stored in the four independent KC74 flip-flop circuits U32A, U32B, U42A and U42B. Flip-flop circuits U32A, U32B, U42A and U42B are preferably "D" or "Data" type flip-flops. If a match has occurred on all 4 pairs of registers, then an ARM signal is generated at the HC11 gate U33 on pin 6. After the 32nd bit has been received, the steering circuitry in the decoder 62 redirects the input data to the FIRE code register U29. When 8 bits have been shifted into FIRE code register U29, the greater than 40 bit signal is generated. This signal is delayed and used to sample the register comparator for FIRE code match. If a match is then detected between the FIRE code control register and the programmed FIRE code register, a FIRE signal is generated. This FIRE signal is conditioned with the ARM signal and then serves to enable the delay timer 66 of Fig. 4.

The delay timer consists of a precision timer accurate to

1 millisecond. Preferably, the timer is programmable in increments from 1 millisecond to 25 milliseconds, but this range could be varied as necessary based on the particular application desired. The illustrated embodiment herein includes an 8 bit counter and an 8 bit comparator. The timer enable signal ("TIMEREN") releases the divider chain formed by the counters of the HC390 modules 48A and 48B (Fig. 9). The output of these two centers is a 1 millisecond clock. The reset state of the delay timer is 0. To ensure the safe and proper operation of the detonator unit, the reset state of the delay timer has been decoded and is not used as a delay time. A minimum delay of 1 millisecond from the receipt of the 40th bit will be used, however, various delay times are attainable by this invention. The comparator output generates both a FIRE and NOT FIRE signal. These inverse signals are precautionary in nature and are used to ensure safe operation of the detonator unit and preclude single gate failures from causing an early trigger.

The fire module 64 is illustrated in Figs. 6 and 9. This module consists of a time base generator and includes the latch delay circuit 66, also illustrated in Fig. 6. The timer comprises a 4060 oscillator (U45), a 4024 binary counter (U46), an HC74 "D" or "Data" type flip-flop (U47). Time base generation is preferably performed by the 4060 RC CMOS oscillator (U45). A 4024 counter (U46) follows the oscillator and generates various clocks for use within the device. The latch delay generator is used in conjunction with the 4024 counter (U46) and the HC74 flip-flop (U47). The counter is reset with the shift clock signal from the programmer 10 (line 7B). When the programmer is connected and data is being shifted into the 8 shift registers (U25-U28 and U36-U39 of Fig. 6) the counter is held at reset. When the programmer is disconnected, the counter is allowed to count up and after approximately 1/2 second, accomplishes transfer of the data from the shift registers to the output latches (D6-D7 of shift registers U25-U28 and U36-U39). This will preclude a shifting data pattern from causing output transients within the detonator unit.

The charge module 26 and detonator circuit 54 are illustrated in Fig. 10. The circuit consists primarily of a regulator and charge pump. A low power ICL7663CPA regulator U56 is used to supply all of the logic on the system. There are a series of N-channel MOSFETS used to hold the charge on the energy storage devices to 0 except when the device is armed. When an ARM command has been received, and a match detected, the MOSFETS Q2 and Q3 present power to the charge pumps U57 and U58, comprising ICL7662CPA modules. With a proper ARM command, the FETs Q6, Q5, Q8, and Q7 are all effectively removed from the circuit. The P-channel MOSFET Q2 allows current stored in the external capacitor C13 to be introduced into the first charge pump U56. The voltage level on the capacitor C13 is then doubled and presented to the charge pump U58. A second doubling occurs, pumping current into the capacitor C55. As charges are transferred from the external storage capacitor C13 to the fire storage capacitor C55, the voltage on capacitor C13 is reduced. This aspect of operation of the illustrated circuit provides the charge module 22 with the proper input to effectively increase the energy available at fire storage capacitor 55 and is necessary for proper operation of the charge module. The N-channel FET Q4 is provided to dump the charge from the external storage capacitor C13. A charge dump is initiated by the safety time out circuit 70 of Fig. 8 and will render the system inoperative and unable to perform detonation.

The firing circuitry for detonator 54 is also shown in Fig. 10. Two series P-channel FETs Q9 and Q11 are used. Energy stored on the fire charge storage capacitor C55 is presented to the detonator 54 when both MOSFETS Q10 and Q12 are properly biased. A separate gating function is provided to combine the FIRE, ARM, and NOT FIRE signals. It should be recognized that the voltage level on the external storage capacitor C13 is not high enough to in itself trigger the detonator. It is only after the operation of charge module 22, described above, that the energy is stored at a level sufficient to trigger detonator 54.

As shown in Fig. 8, the safety time out module 70 includes

two distinct safety time out systems. After receipt of an ARM code, a 62 second timer, comprising the 4024 binary counter (U21) and the HC74 "D" or "Data" type flip-flops U22, U22A and U22B, is started. If after 62 seconds the unit has not been fired, a reset command is issued to the ARM and FIRE code register. This reset command also resets the bit counter comprising the circuits of U2, U3A and U3B in the decoder (Fig. 5). This allows recovery from a faulty transmitted sequence, noise, or other interference with the proper triggering of the system. As here shown, the disarm timer has been provided with a four try capability. If after the fourth attempted arming sequence, a match has not occurred, then the system will be rendered inoperative by causing the dump signal to be asserted at the output of the gate U20. The number of tries is programmable and arbitrary. An additional time out is provided at approximately 62 minutes. At this time it is assumed that a fault in the triggering sequence has occurred. The system is again rendered inoperative by assertion of the dump signal and discharging the external storage capacitor C13.

While certain features and embodiments of the invention have been described in detail herein, it will be understood that the invention encompasses all modifications and alternatives within the scope and spirit of the following claims.

CLAIMS

What is claimed is:

1. A control system for sequential detonation of blast explosives comprising:

a. means for receiving and storing a programmed signal representing the timing sequence and firing sequence of the detonation of each explosive;

b. means for receiving and storing a fire command to initiate the timing sequence and the firing sequence; and

c. control means for comparing the fire command with the programmed signal, and responsive to a predetermined correspondence thereof for initiating the timing sequence and the firing sequence.

2. The control system of Claim 1, the control means

further comprising means for generating a FIRE signal and an ARM signal in response to the predetermined correspondence of the fire command and the programmed signal, wherein the initiation of the firing sequence is responsive only to the presence of both the FIRE and ARM signals.

3. The control system of Claim 2, further comprising:

a. a detonator firing circuit;

b. means for generating a firing charge sufficient to detonate a blast explosive and for releasing said charge to the detonator firing circuit; and

c. means for delaying the generation of the FIRE signal for a predetermined time after the generation of the ARM signal, said charge generating means responsive to the ARM signal for generating said firing charge and responsive to the FIRE signal for releasing said firing charge to the detonator firing circuit.

4. The control system of Claim 3, further comprising means for disabling the charge generating means when said FIRE signal is not generated within a predetermined time of said ARM signal.

5. The control system of Claim 1, wherein the programmed signal and the fire command each comprise a sequential series of binary bit signals, said control means including comparing means for making a bit-by-bit comparison thereof.

6. The control system of Claim 3, the firing charge generating means comprising a plurality of charge means for generating at least a portion of said firing charge connected in sequential relationship with one another, each succeeding charge means in sequence for generating a multiple of the charge generated by the charge means immediately in advance thereof.

7. The control system of Claim 6, wherein said charge means includes electrical charge pump circuitry.

8. The control system of Claim 4, further comprising means for deleting the fire command from the storing means when said FIRE signal is not generated within a predetermined period of time after the ARM signal.

9. The control system of Claim 8, further comprising means

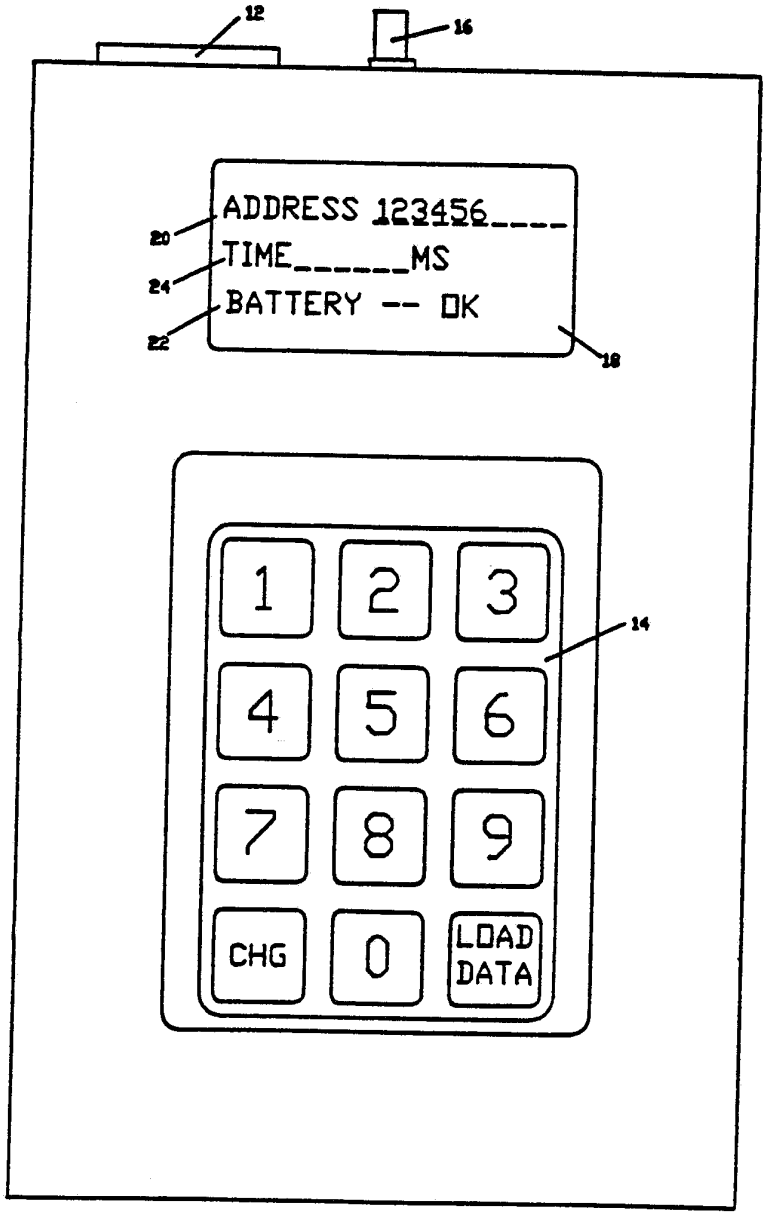
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FIG. 1

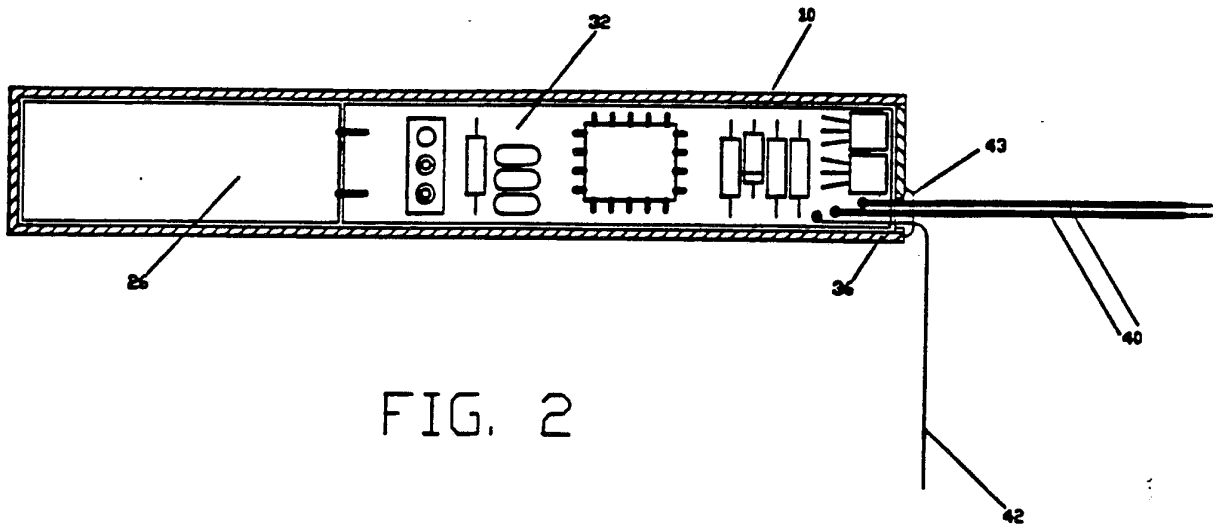


FIG. 2

SYSTEM BLOCK DIAGRAM

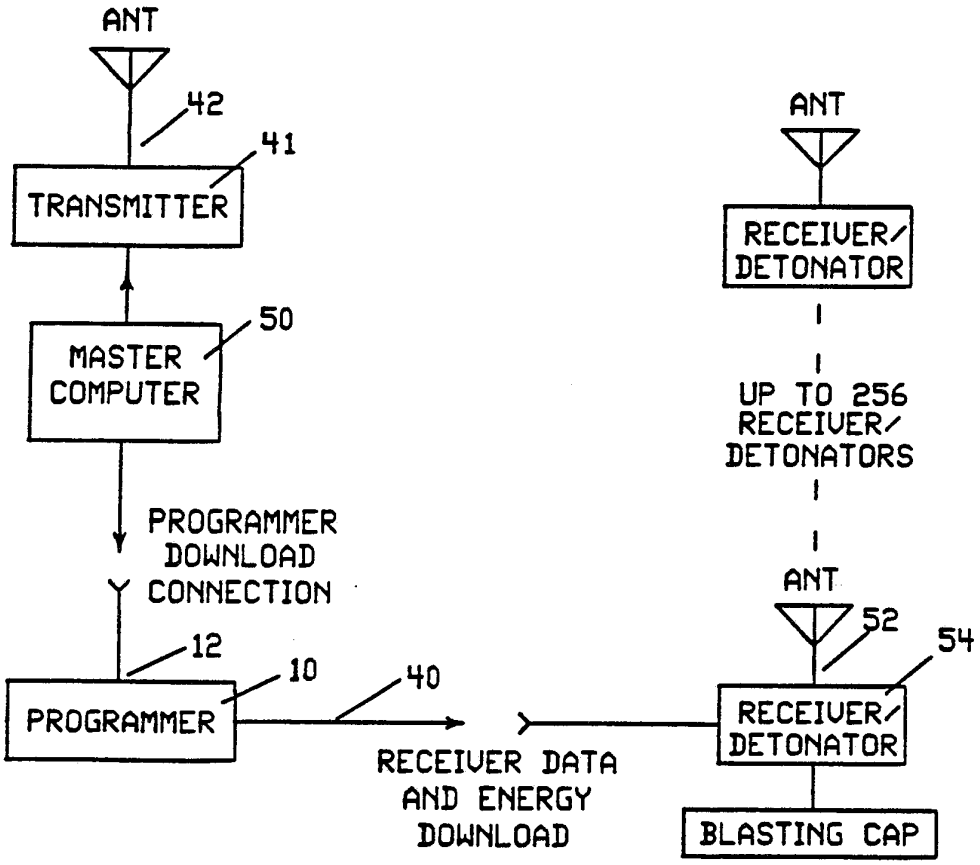


FIG. 3

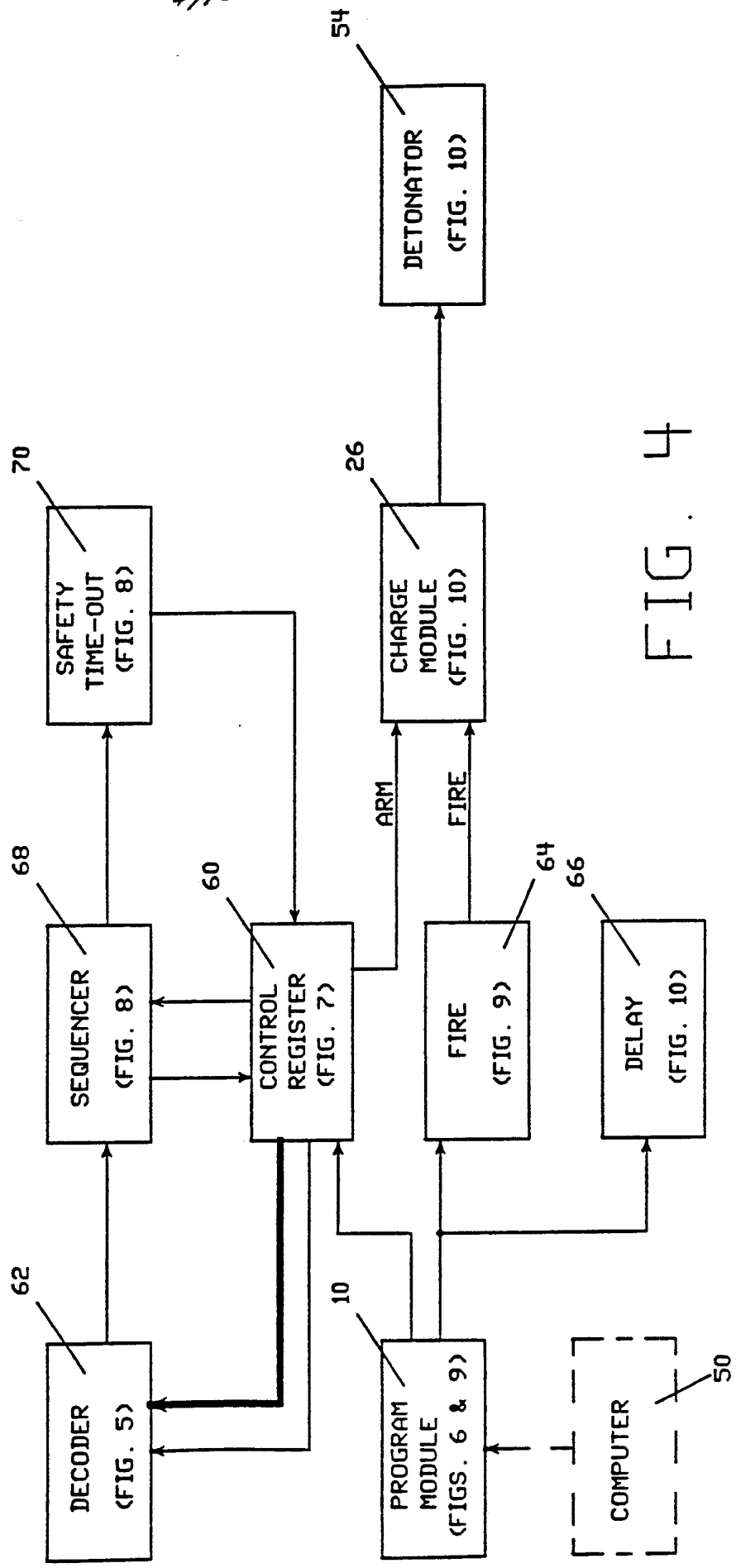
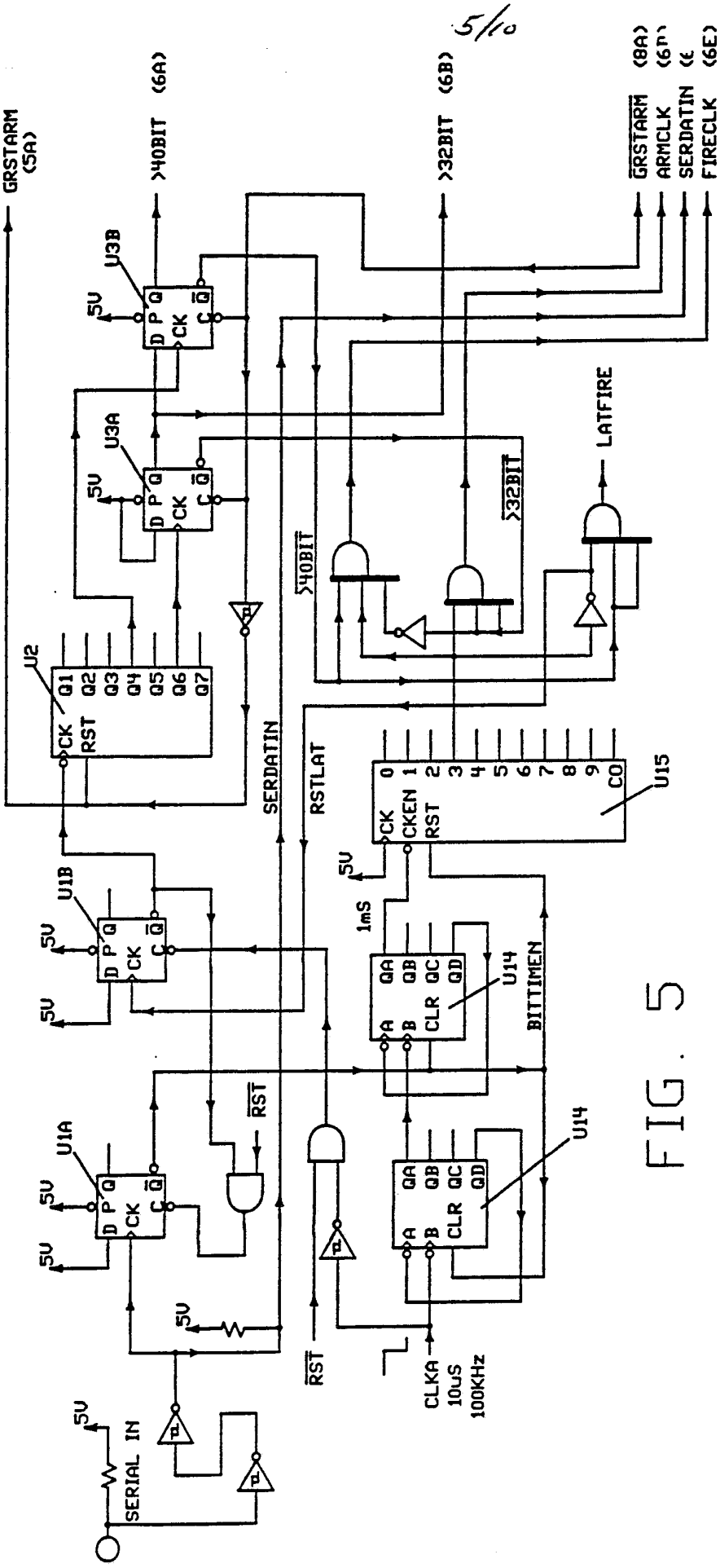

54
DETONATOR (FIG. 10)
70
SAFETY TIME-OUT (FIG. 8)
26
CHARGE MODULE (FIG. 10)
68
SEQUENCER (FIG. 8)
60
CONTROL REGISTER (FIG. 7)
ARM
FIRE
64
FIRE (FIG. 9)
66
DELAY (FIG. 10)
62
DECODER (FIG. 5)
10
PROGRAM MODULE (FIGS. 6 & 9)
COMPUTER
50

FIG. 4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SERIAL IN
5V

FIG. 5

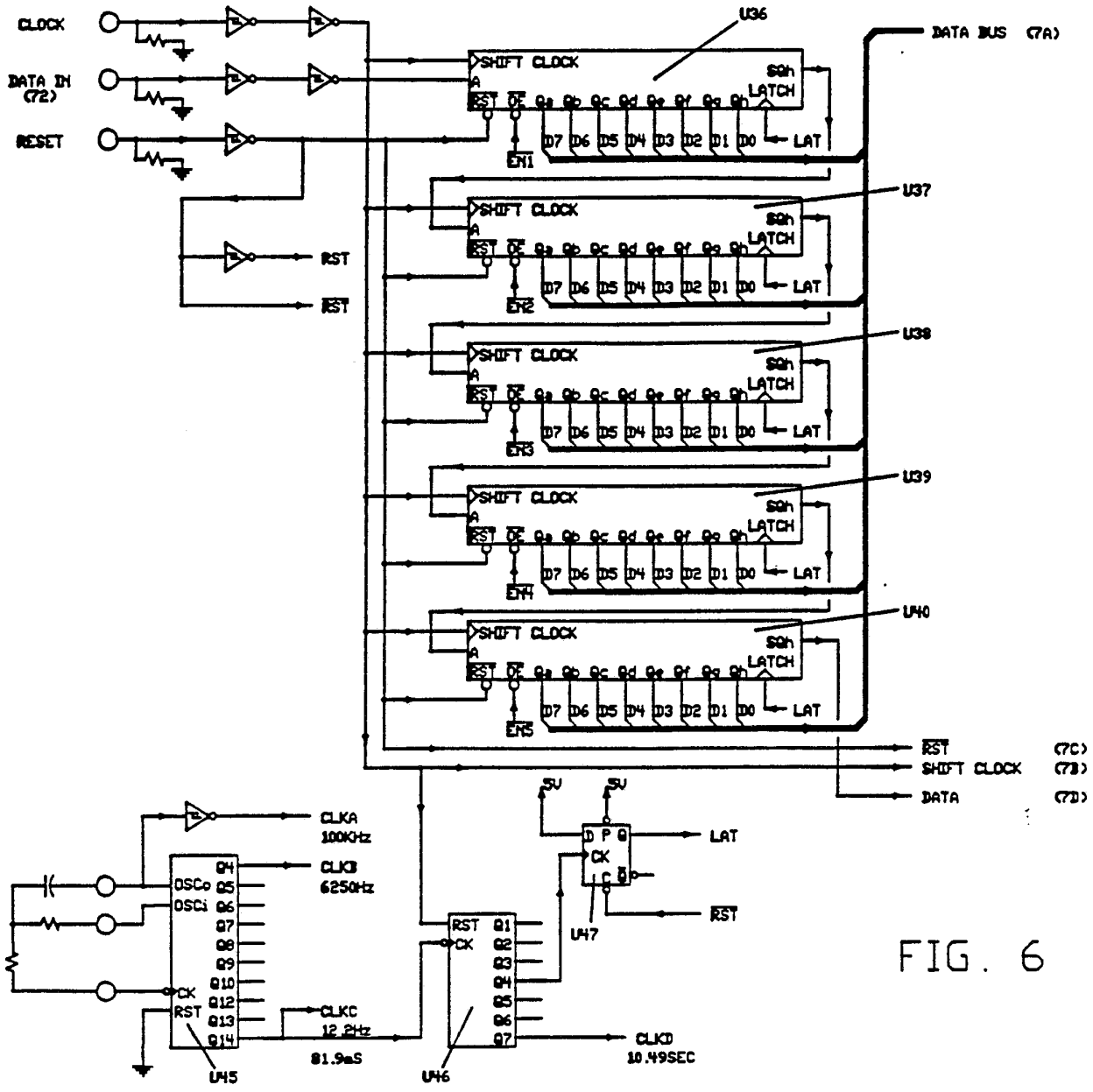
CLOCK
DATA IN (72)
RESET
RST
RST
U36
U37
U38
U39
U40
SHIFT CLOCK
LATCH
LAT
DATA BUS (7A)
RST (7C)
SHIFT CLOCK (7B)
DATA (7D)
5V
CLKA 100KHz
CLKB 6250Hz
CLKC 12.2Hz 81.9mS
CLKD 10.49SEC
OSCo
OSCi
U45
U46
U47

FIG. 6

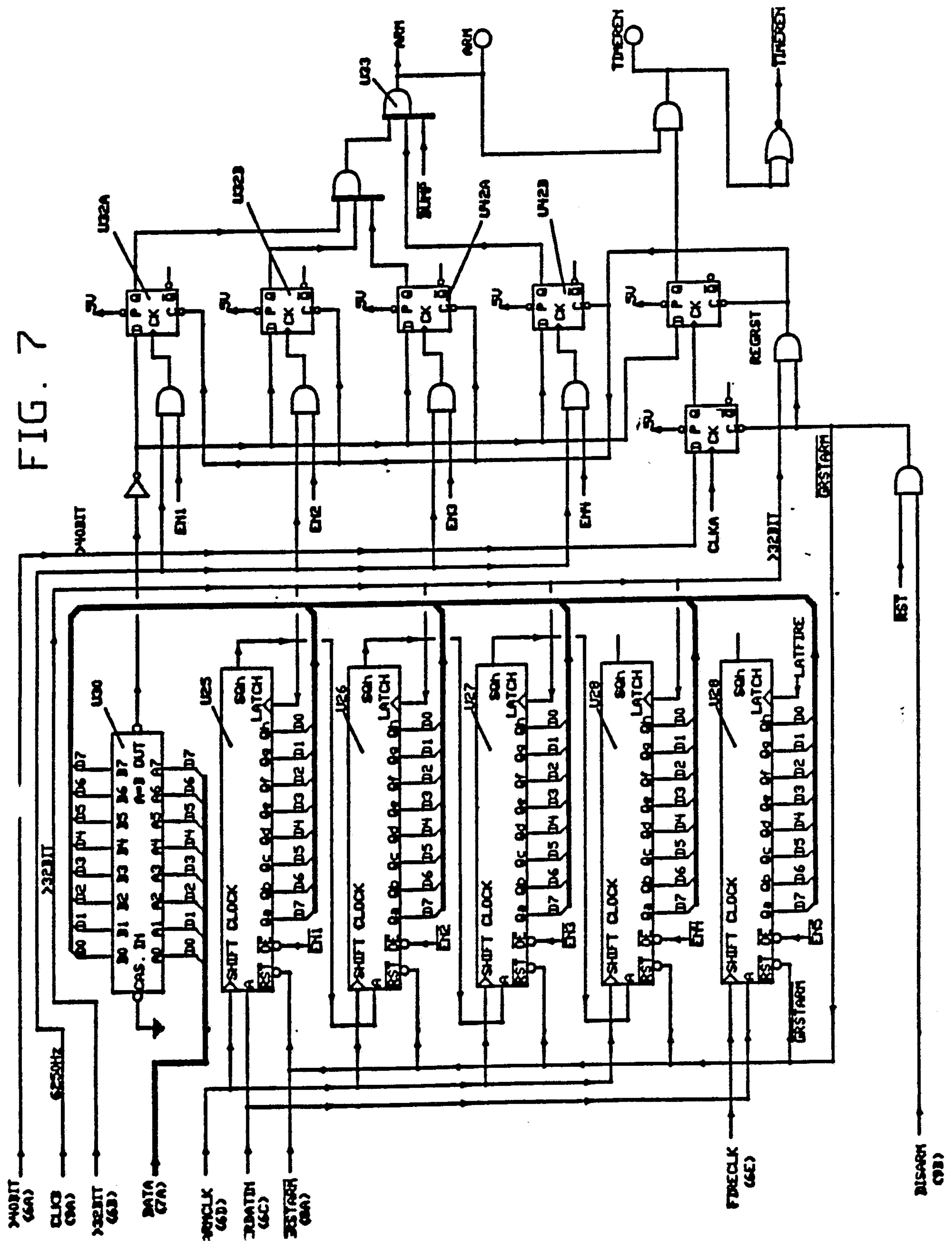
U23
U32A
U32B
U42A
U42B
U30
U25
U26
U27
U28
ARM
TIMEREN
EN1
EN2
EN3
EN4
EN5
CLKA
REGRST
>40BIT
>32BIT
625kHz
DATA (7A)
FIRECLK (6E)
DISARM (9B)
RST
SHIFT CLOCK
LATCH
LATFIRE
CAS. IN
A=B OUT

FIG. 7

8/10

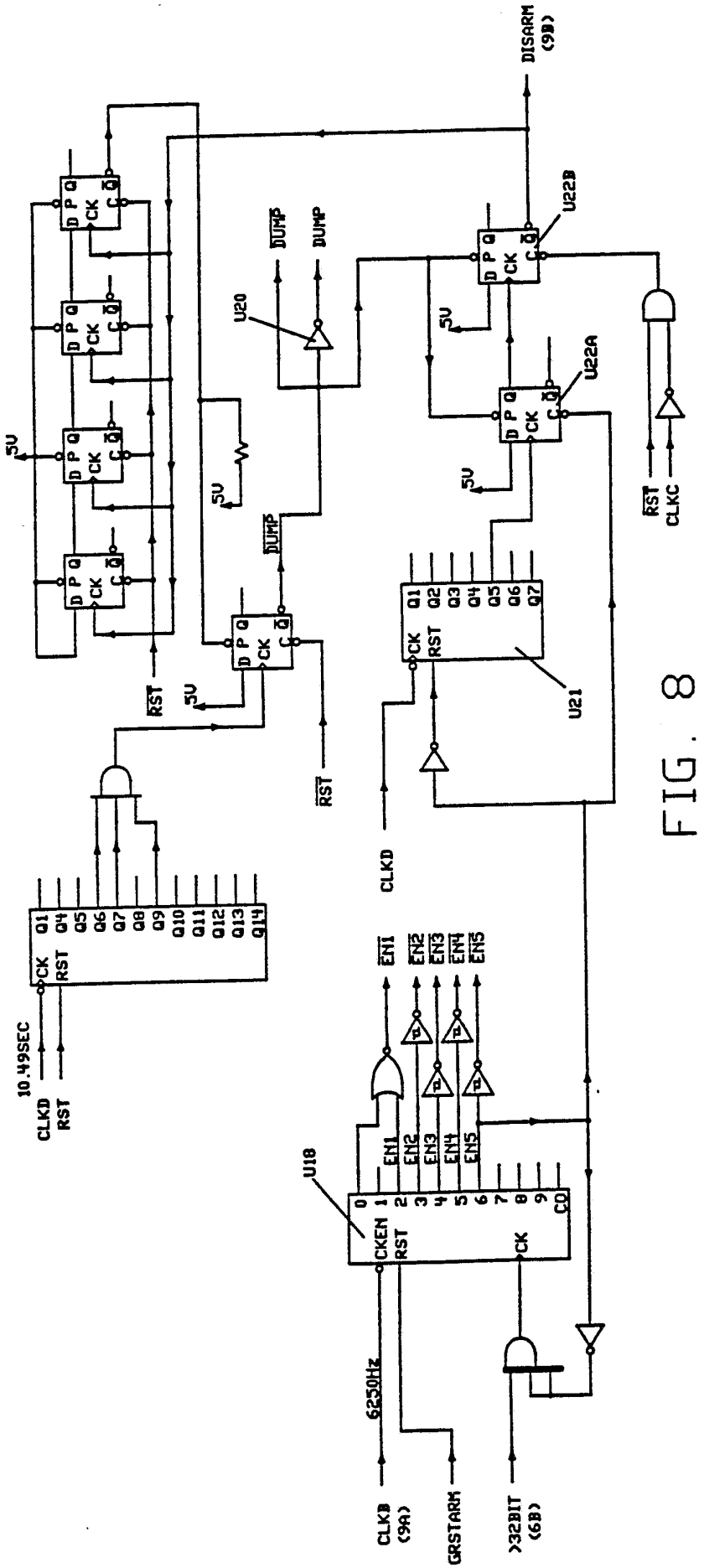
DISARM (9B)
U22B
U22A
U20
U21
U18
DUMP
DUMP
DUMP
5V
RST
RST
RST
CLKC
CLKD
CLKD
10.49SEC
RST
EN1
EN2
EN3
EN4
EN5
6250Hz
CLKB (9A)
GRSTARM
>32BIT (6B)

FIG. 8

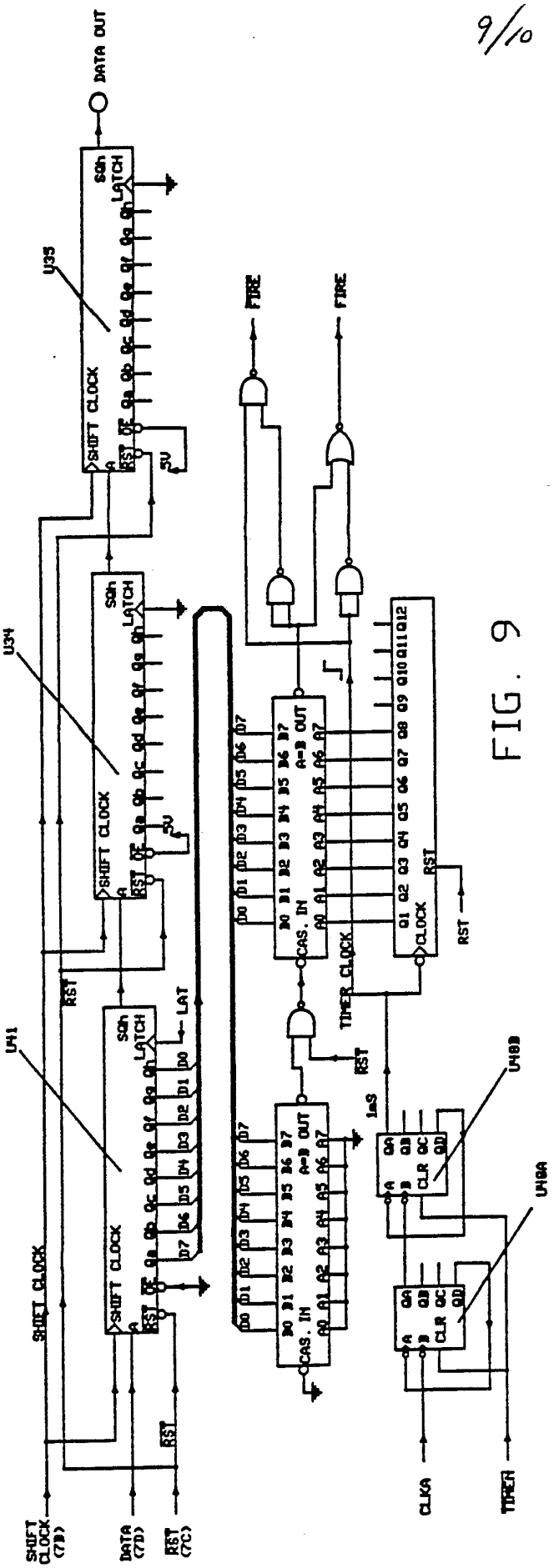
DATA OUT
U35
U34
U41
SHIFT CLOCK
LATCH
FIRE
FIRE
RST
LAT
TIMER CLOCK
CLOCK
CAS. IN
A=B OUT
U10B
U10A
CLR
1mS
CLKA
TIMER
SHIFT CLOCK (7B)
DATA (7D)
RST (7C)

FIG. 9

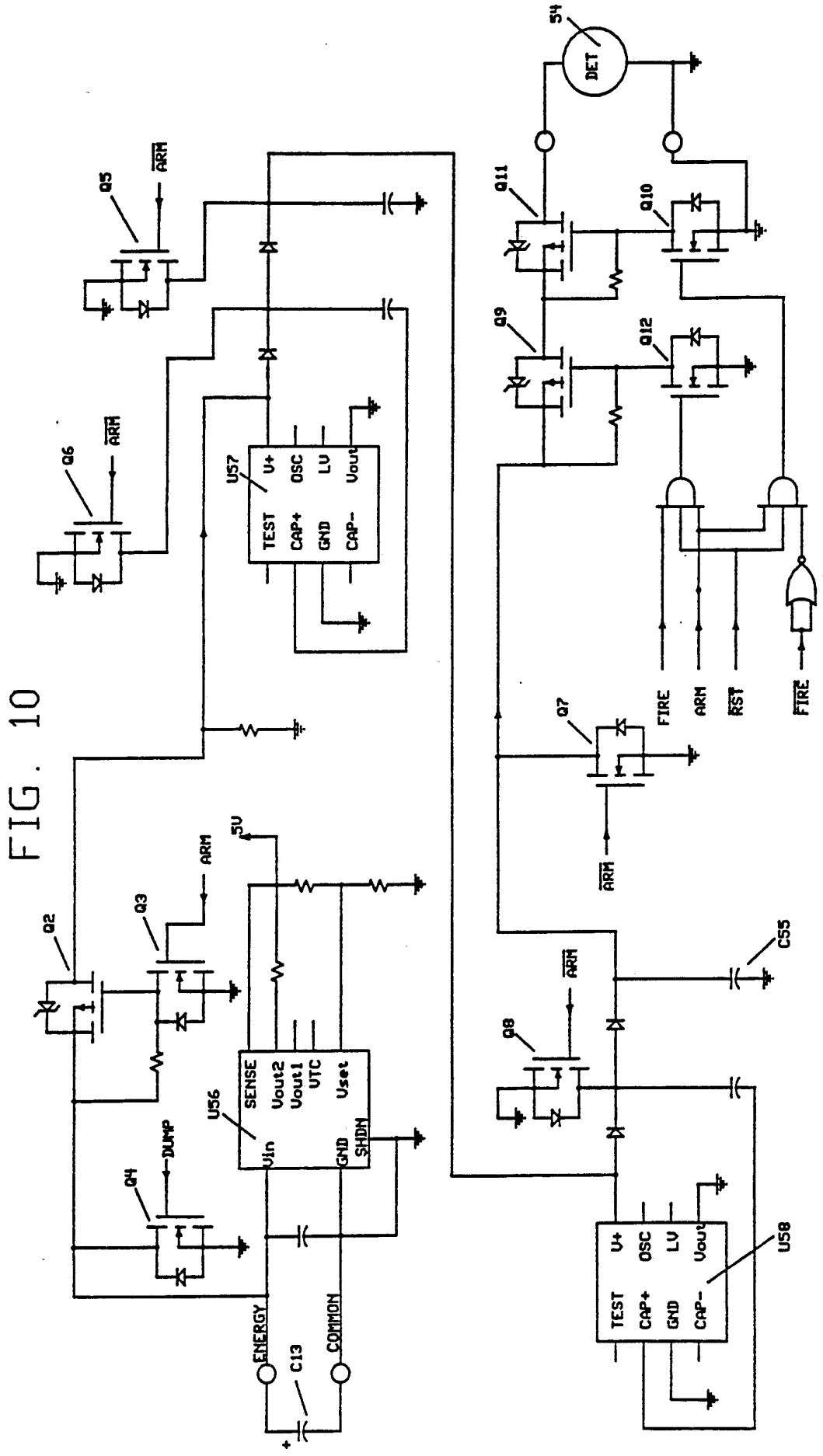
S4
DET
Q11
Q10
Q9
Q12
FIRE
ARM
RST
FIRE
Q7
ARM
C55
Q8
ARM
U58
TEST
CAP+
GND
CAP-
V+
OSC
LV
Vout
Q5
ARM
Q6
ARM
U57
TEST
CAP+
GND
CAP-
V+
OSC
LV
Vout
5V
Q2
Q3
ARM
U56
SENSE
Vout2
Vout1
UTC
Vset
Vin
GND
SHDN
Q4
DUMP
ENERGY
C13
COMMON

FIG. 10

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/08337

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): F23Q 21/00

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.Cl.	102/217,215

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	US, A, 4,934,269 (POWELL) 19 June 1990 See col. 3, lines 1-26 and 35-43.	1, 10
X	US, A, 3,979,580 (CRILLY ET AL.) 07 September 1976 See col. 2, lines 30-59.	1, 5, 10
X	US, A, 4,527,636 (BORDON) 09 July 1985 See abstract; col. 8, lines 40-42; col. 9, lines 22-61; col. 10, lines 55-59; col. 11, lines 8-12 and 34-37; and col. 14, lines 21-24 and 45-69.	1-2, 5, 10
X	US, A, 4,674,047 (TYLER ET AL.) 16 June 1987 See col. 7, lines 19-34; col. 9, lines 15-28; col. 10, lines 8-9, 43-46, and 55-57; col. 11, lines 32-46; col. 12, lines 10-13 and 53-58; col. 13, lines 6-12; and col. 16, lines 42-65.	1-3, 5, 10-11

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
31 January 1992	23 MAR 1992
International Searching Authority	**Signature of Authorized Officer**
ISA/US	Stephen M. Johnson