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**None**

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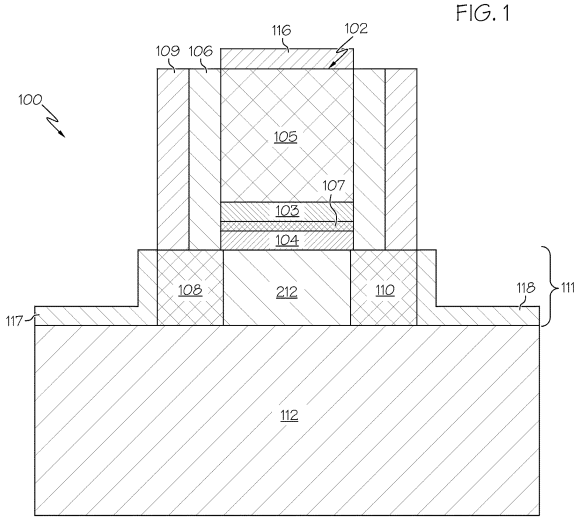
(54) Title of the Invention: **Finfet with merged fins and vertical silicide**
Abstract Title: **Finfet with merged fins and vertical silicide**

(57) A method is provided for fabricating a finFET device. Fin structures are formed over a BOX layer. The fin structures include a semiconductor layer and extend in a first direction. A gate stack is formed on the BOX layer over the fin structures and extending in a second direction. The gate stack includes a high-K dielectric layer and a metal gate. Gate spacers are formed on sidewalls of the gate stack, and an epi layer is deposited to merge the fin structures. Ions are implanted to form source and drain regions, and dummy spacers are formed on sidewalls of the gate spacers. The dummy spacers are used as a mask to recess or completely remove an exposed portion of the epi layer. Silicidation forms silicide regions that abut the source and drain regions and each include a vertical portion located on the vertical sidewall of the source or drain region.

FIG. 1




GB 2511445 A