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(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Blvd., M.S RNB-4-150, Santa Clara, California 95054 (US).

(72) Inventors; and
(71) Applicants: LIN, Kevin [US/US]; 19953 SW Mohican St, Beaverton, Oregon 97006 (US). JUN, Kimin [KR/US]; 2501 NW 229th Ave., RA3-252, Hillsboro, Oregon 97124 (US). MOHAMMED, Edris [ET/US]; 16800 NW Paddington Drive, Beaverton, Oregon 97006 (US).

(74) Agent: BRASK, Justin, K. et al.; Schwabe, Williamson & Wyatt, 1211 SW 5th Ave., Suite 1900, Portland, OR 97204 (US).

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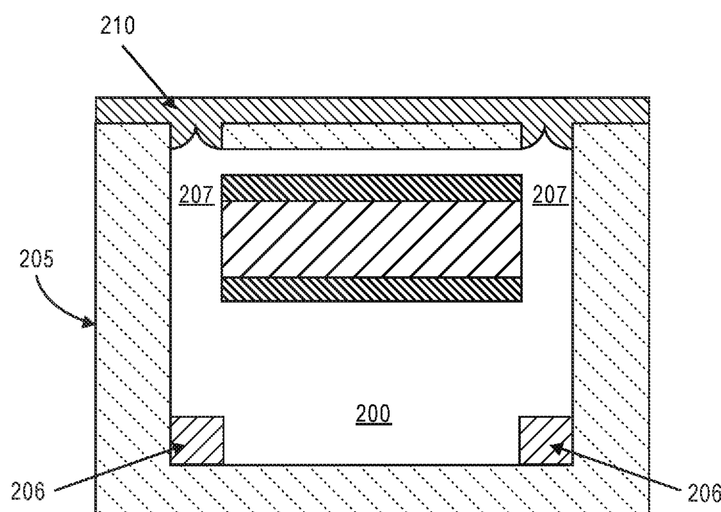

FIG. 2

(57) Abstract: The RF filters used in conventional mobile devices often include resonator structures, which often require free-standing air-gap structure to prevent mechanical vibrations of the resonator from being damped by a bulk material. A method for fabricating a resonator structure comprises depositing a non-conformal thin-film to the resonator structure to seal air gap cavities in the resonator structure.

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RESONATOR STRUCTURE ENCAPSULATION

FIELD

The present disclosure generally relates to a resonator structure.

5 BACKGROUND

The development of mobile telecommunications continues towards ever smaller and increasingly complicated handheld units. The development leads to increasing requirements on the miniaturization of the components and structures used in the mobile communication means. This development effects radio frequency (RF) filter structures as 10 well, which despite the increasing miniaturization should be able to withstand considerable power levels, have very steep passband edges, and low losses.

The RF filters used in conventional mobile devices often include resonator structures, which often require free-standing air-gap structures to prevent mechanical vibrations of the resonator from being damped by a bulk material. However, air gap 15 structures are difficult to integrate on silicon integrated circuits (ICs) because of increased silicon processing complexity. Further, the air gap must be hermetically sealed to minimize device performance changes during the operational lifetime of the material.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates one embodiment of a resonator structure.

20 **Figure 2** illustrates a resonator structure according to one embodiment.

Figure 3 is a flow diagram illustrating one embodiment of a process for fabricating a resonator structure.

Figures 4A – 4F illustrate embodiments of a resonator structure during fabrication.

Figure 5 illustrates a system in which a resonator structure may be implemented.

25 DETAILED DESCRIPTION

In the following description, numerous specific details are set forth in order to provide a thorough understanding of various embodiments. However, various embodiments of the invention may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been 30 described in detail so as not to obscure the particular embodiments of the invention.

Figure 1 illustrates one embodiment of a resonator structure 200. As shown in **Figure 1**, resonator structure 200 includes sidewalls 205, deposition layers 206 and air cavities 207 that are implemented to prevent mechanical vibrations of the resonator structure from being damped by a bulk material. As discussed above, air gap structures are 35 difficult to integrate because of increased processing complexity. According to one

embodiment, a fabrication process is disclosed that implements a non-conformal thin-film deposition to hermetically seal the air gap cavities of resonator structure 200.

Figure 2 illustrates an embodiment of a resonator structure 200 having a deposition layer 210 covering air gaps 207. In one embodiment, deposition layer 210 is a non-conformal deposition applied via a Chemical Vapor Deposition (CVD) or Physical Vapor Deposition (PVD) type deposition. In such an embodiment, the deposition rate of layer 210 on top of structure 200 is faster than the deposition rate of side-wall 205, resulting in pinching off and sealing of air gap 207 cavities once enough material has been deposited.

Figure 3 is a flow diagram illustrating one embodiment of a process for fabricating a resonator structure, such as resonator structure 200. At processing block 310, a sacrificial material is patterned and polished. In one embodiment, the sacrificial material may be comprised of silicon. However in other embodiments the sacrificial material may be comprised of silicon dioxide or titanium nitride (TiN). **Figure 4A** illustrates one embodiment of the resonator structure after the sacrificial material is patterned.

At processing block 320, the resonator structure is patterned. In one embodiment, resonator structure patterning includes patterning a bottom electrode on the sacrificial material (processing block 322), depositing and patterning a piezoelectric material on the bottom electrode (processing block 324), patterning a top electrode on the piezoelectric material (processing block 326) and patterning the top sacrificial material (processing block 328). **Figure 4B** illustrates one embodiment of the resonator structure after patterning. As shown in **Figure 4B**, the resonator structure includes bottom electrode 410 and top electrode 420. According to one embodiment, the bottom and top electrodes may be comprised one of tantalum (Ta) copper (Cu), molybdenum (Mo), ruthenium (Ru), tungsten (W), titanium (Ti), titanium-nitride (TiN) aluminum (Al) and nickel (Ni).

At processing block 330, spacer deposition and patterning of a sidewall sacrificial material is performed. **Figure 4C** illustrates one embodiment of the resonator structure after spacer 430 deposition and patterning of a sidewall sacrificial material. At processing block 340, interlayer deposition (ILD) and polishing is performed for planarization. **Figure 4D** illustrates one embodiment of the structure after ILD and polishing.

At processing block 350, release holes are patterned through the ILD material. **Figure 4E** illustrates one embodiment of the structure after the release holes have been cut. At processing block 360, the sacrificial material is removed. In one embodiment, the sacrificial material is removed via an isotropic (dry or wet) etch. For example, silicon can be removed by xenon di-fluoride selective to other materials; silicon dioxide can be removed using hydrogen fluoride (HF) liquid or vapor selective to other materials; and TiN

may be removed using peroxide chemistries selective to other materials. **Figure 4F** illustrates one embodiment of the structure after the sacrificial material has been removed.

At processing block 370, a plug material is deposited to seal the release holes (or openings in the air gaps). As discussed above, the deposition is a non-conformal
5 deposition applied via a CVD or PVD type deposition. For instance, the deposition may be a plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide, silicon nitride, or silicon carbide deposition; or a PVD silicon or TiN deposition. The resulting structure is resonator structure 200 disclosed in **Figure 2**.

The above described process results in a hermetically sealed resonator structure with
10 reliable performance over lifetime. Further, the sealing of the resonator structure enables down-stream processing and fabrication compatibility. Although discussed with reference to a resonator structure, other embodiments may be implemented from microelectromechanical systems (MEMS) materials that require a mechanical isolation via air gap cavity and a necessity to seal such a device.

15 **Figure 5** illustrates one embodiment of a computer system 600 in which a resonator structure may be implemented. The computer system 600 (also referred to as the electronic system 600) as depicted can embody a semiconductor die packaged with one or more ACIs having metal-density layer units of fractal geometry according to any of the several disclosed embodiments and their equivalents as set forth in this disclosure. The computer
20 system 600 may be a mobile device such as a netbook computer. The computer system 600 may be a mobile device such as a wireless smart phone. The computer system 600 may be a desktop computer. The computer system 600 may be a hand-held reader. The computer system 600 may be a server system. The computer system 600 may be a supercomputer or high-performance computing system.

25 In an embodiment, the electronic system 600 is a computer system that includes a system bus 620 to electrically couple the various components of the electronic system 600. The system bus 620 is a single bus or any combination of busses according to various embodiments. The electronic system 600 includes a voltage source 630 that provides power to the integrated circuit 610. In some embodiments, the voltage source 630 supplies
30 current to the integrated circuit 610 through the system bus 620.

The integrated circuit 610 is electrically coupled to the system bus 620 and includes any circuit, or combination of circuits according to an embodiment. In an embodiment, the integrated circuit 610 includes a processor 612 that can be of any type. As used herein, the processor 612 may mean any type of circuit such as, but not limited to, a microprocessor, a
35 microcontroller, a graphics processor, a digital signal processor, or another processor. In

an embodiment, the processor 612 includes a semiconductor die packaged with one or more ACIs having metal-density layer units of fractal geometry, as disclosed herein. In an embodiment, SRAM embodiments are found in memory caches of the processor. Other types of circuits that can be included in the integrated circuit 610 are a custom circuit or an
5 application-specific integrated circuit (ASIC), such as a communications circuit 614 for use in wireless devices such as cellular telephones, smart phones, pagers, portable computers, two-way radios, and similar electronic systems, or a communications circuit for servers. In an embodiment, the integrated circuit 610 includes on-die memory 616 such as static random-access memory (SRAM). In an embodiment, the integrated circuit 610 includes
10 embedded on-die memory 616 such as embedded dynamic random-access memory (eDRAM).

In an embodiment, the integrated circuit 610 is complemented with a subsequent integrated circuit 611. Useful embodiments include a dual processor 613 and a dual communications circuit 615 and dual on-die memory 617 such as SRAM. In an
15 embodiment, the dual integrated circuit 610 includes embedded on-die memory 617 such as eDRAM.

In an embodiment, the electronic system 600 also includes an external memory 640 that in turn may include one or more memory elements suitable to the particular application, such as a main memory 642 in the form of RAM, one or more hard drives 644,
20 and/or one or more drives that handle removable media 646, such as diskettes, compact disks (CDs), digital variable disks (DVDs), flash memory drives, and other removable media known in the art. The external memory 640 may also be embedded memory 648 such as the first die in an embedded TSV die stack, according to an embodiment.

In an embodiment, the electronic system 600 also includes a display device 650, an
25 audio output 660. In an embodiment, the electronic system 600 includes an input device such as a controller 670 that may be a keyboard, mouse, trackball, game controller, microphone, voice-recognition device, or any other input device that inputs information into the electronic system 600. In an embodiment, an input device 670 is a camera. In an embodiment, an input device 670 is a digital sound recorder. In an embodiment, an input
30 device 670 is a camera and a digital sound recorder.

As shown herein, the integrated circuit 610 can be implemented in a number of different embodiments, including a semiconductor die packaged with one or more ACIs having metal-density layer units of fractal geometry according to any of the several disclosed embodiments and their equivalents, an electronic system, a computer system, one
35 or more methods of fabricating an integrated circuit, and one or more methods of

fabricating an electronic assembly that includes a semiconductor die packaged with one or more ACIs having metal-density layer units of fractal geometry according to any of the several disclosed embodiments as set forth herein in the various embodiments and their art-recognized equivalents. The elements, materials, geometries, dimensions, and sequence of
5 operations can all be varied to suit particular I/O coupling requirements including array contact count, array contact configuration for a microelectronic die embedded in a processor mounting substrate according to any of the several disclosed semiconductor die packaged with one or more ACIs having metal-density layer units of fractal geometry embodiments and their equivalents. A foundation substrate may be included, as
10 represented by the dashed line of **Figure 5**. Passive devices may also be included, as is also depicted in **Figure 5**.

References to "one embodiment", "an embodiment", "example embodiment", "various embodiments", etc., indicate that the embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily
15 includes the particular features, structures, or characteristics. Further, some embodiments may have some, all, or none of the features described for other embodiments.

In the following description and claims, the term "coupled" along with its derivatives, may be used. "Coupled" is used to indicate that two or more elements co-operate or interact with each other, but they may or may not have intervening physical or electrical components between
20 them.

As used in the claims, unless otherwise specified the use of the ordinal adjectives "first", "second", "third", etc., to describe a common element, merely indicate that different instances of like elements are being referred to, and are not intended to imply that the elements so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.
25 The following clauses and/or examples pertain to further embodiments or examples. Specifics in the examples may be used anywhere in one or more embodiments. The various features of the different embodiments or examples may be variously combined with some features included and others excluded to suit a variety of different applications. Examples may include subject matter such as a method, means for performing acts of the method, at least one
30 machine-readable medium including instructions that, when performed by a machine cause the machine to performs acts of the method, or of an apparatus or system for facilitating hybrid communication according to embodiments and examples described herein.

Some embodiments pertain to Example 1 that includes a method comprising fabricating a resonator structure including depositing a non-conformal thin-film to the resonator structure to
35 seal air gap cavities in the resonator structure.

Example 2 includes the subject matter of Example 1, wherein fabricating the resonator structure further comprises patterning a sacrificial material and patterning the resonator structure.

Example 3 includes the subject matter of Examples 1 and 2, wherein patterning the resonator structure comprises patterning a bottom electrode on the sacrificial material, depositing 5 a piezoelectric material on the bottom electrode, patterning a top electrode on the piezoelectric material and patterning a top sacrificial material.

Example 4 includes the subject matter of Examples 1-3, wherein fabricating the resonator structure further comprises depositing a spacer and patterning a sidewall sacrificial material.

Example 5 includes the subject matter of Examples 1-4, wherein fabricating the resonator 10 structure further comprises depositing an interlayer dialectic layer (ILD) and polishing the ILD.

Example 6 includes the subject matter of Examples 1-5, wherein fabricating the resonator structure further comprises patterning release holes through the ILD to form the air gaps.

Example 7 includes the subject matter of Examples 1-6, wherein fabricating the resonator structure further comprises removing the sacrificial material and depositing the non-conformal 15 thin-film.

Example 8 includes the subject matter of Examples 1-7, wherein depositing the non-conformal thin-film comprises depositing a plug material to fill openings in the air gaps.

Example 9 includes the subject matter of Examples 1-8, wherein the depositing of the non-conformal thin-film is applied via Chemical Vapor Deposition (CVD).

20 Example 10 includes the subject matter of Examples 1-9, wherein the depositing of the non-conformal thin-film is applied via Physical Vapor Deposition (PVD).

Some embodiments pertain to Example 11 that includes an integrated circuit (IC) comprising a resonator structure, including a resonator and a non-conformal thin-film deposited over the resonator to seal the air gap cavities in the resonator structure.

25 Example 12 includes the subject matter of Example 11, wherein the resonator comprises a bottom electrode patterned over sacrificial material, a piezoelectric material deposited on the bottom electrode and a top electrode patterned on the piezoelectric material.

Example 13 includes the subject matter of Examples 11 and 12, wherein the resonator structure further comprises a bulk material, a sacrificial material deposited over the bulk material 30 and the resonator patterned over the sacrificial material.

Example 14 includes the subject matter of Examples 11-13, wherein the resonator structure further comprises an interlayer dielectric layer (ILD) patterned over the resonator, release holes patterned through the ILD to form air gaps and a non-conformal thin-film deposited over the ILD to seal the air gap cavities in the resonator structure.

Example 15 includes the subject matter of Examples 11-14, wherein the non-conformal thin-film is applied via Chemical Vapor Deposition (CVD).

Example 16 includes the subject matter of Examples 11-15, wherein the non-conformal thin-film is applied via Physical Vapor Deposition (PVD).

5 Some embodiments pertain to Example 17 that includes a resonator structure, comprising a resonator and a non-conformal thin-film deposited over the resonator to seal the air gap cavities in the resonator structure.

Example 18 includes the subject matter of Example 17, further comprising a bottom electrode patterned over sacrificial material, a piezoelectric material deposited on the bottom 10 electrode and a top electrode patterned on the piezoelectric material.

Example 19 includes the subject matter of Examples 17 and 18, further comprising a bulk material, a sacrificial material deposited over the bulk material and the resonator patterned over the sacrificial material.

Example 20 includes the subject matter of Examples 17-19, further comprising an 15 interlayer dielectric layer (ILD) patterned over the resonator, release holes patterned through the ILD to form air gaps and a non-conformal thin-film deposited over the ILD to seal the air gap cavities in the resonator structure.

Although embodiments of the invention have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter 20 may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

CLAIMS

What is claimed is:

1. A method comprising, fabricating a resonator structure including depositing a non-conformal thin-film to the resonator structure to seal air gap cavities in the resonator structure.

5 2. The method of claim 1, wherein fabricating the resonator structure further comprises:

patterning a sacrificial material; and

patterning the resonator structure.

3. The method of claim 1, wherein patterning the resonator structure comprises:

patterning a bottom electrode on the sacrificial material;

10 depositing a piezoelectric material on the bottom electrode;

patterning a top electrode on the piezoelectric material; and

patterning a top sacrificial material.

4. The method of claim 2, wherein fabricating the resonator structure further comprises:

depositing a spacer; and

15 patterning a sidewall sacrificial material.

5. The method of claim 4, wherein fabricating the resonator structure further comprises:

depositing an interlayer dialectic layer (ILD); and

polishing the ILD.

6. The method of claim 5, wherein fabricating the resonator structure further comprises

20 patterning release holes through the ILD to form the air gaps.

7. The method of claim 6, wherein fabricating the resonator structure further comprises:

removing the sacrificial material; and

depositing the non-conformal thin-film.

8. The method of claim 7, wherein depositing the non-conformal thin-film comprises depositing a plug material to fill openings in the air gaps.

9. The method of claim 8, wherein the depositing of the non-conformal thin-film is applied via Chemical Vapor Deposition (CVD).

5 10. The method of claim 8, wherein the depositing of the non-conformal thin-film is applied via Physical Vapor Deposition (PVD).

11. An integrated circuit (IC) comprising a resonator structure, including:

a resonator; and

10 a non-conformal thin-film deposited over the resonator to seal the air gap cavities in the resonator structure.

12. The IC of claim 11, wherein the resonator comprises:

a bottom electrode patterned over sacrificial material;

a piezoelectric material deposited on the bottom electrode; and

15 a top electrode patterned on the piezoelectric material.

13. The IC of claim 12, wherein the resonator structure further comprises:

a bulk material;

a sacrificial material deposited over the bulk material; and

the resonator patterned over the sacrificial material.

20 14. The IC of claim 13, wherein the resonator structure further comprises:

an interlayer dielectric layer (ILD) patterned over the resonator;

release holes patterned through the ILD to form air gaps; and

a non-conformal thin-film deposited over the ILD to seal the air gap cavities in the resonator structure.

15. The IC of claim 14, wherein the non-conformal thin-film is applied via Chemical Vapor Deposition (CVD).

16. The IC of claim 14, wherein the non-conformal thin-film is applied via Physical Vapor Deposition (PVD).

5 17. A resonator structure, comprising:

a resonator; and

a non-conformal thin-film deposited over the resonator to seal the air gap cavities in the resonator structure.

18. The resonator structure of claim 17, wherein the resonator comprises:

10 a bottom electrode;

a piezoelectric material deposited on the bottom electrode; and

a top electrode patterned on the piezoelectric material.

19. The resonator structure of claim 18, further comprising:

a bulk material;

15 a sacrificial material deposited over the bulk material; and

the resonator patterned over the sacrificial material.

20. The resonator structure of claim 19, further comprising:

an interlayer dialectic layer (ILD) patterned over the resonator;

release holes patterned through the ILD to form air gaps; and

20 a non-conformal thin-film deposited over the ILD to seal the air gap cavities in the resonator structure.

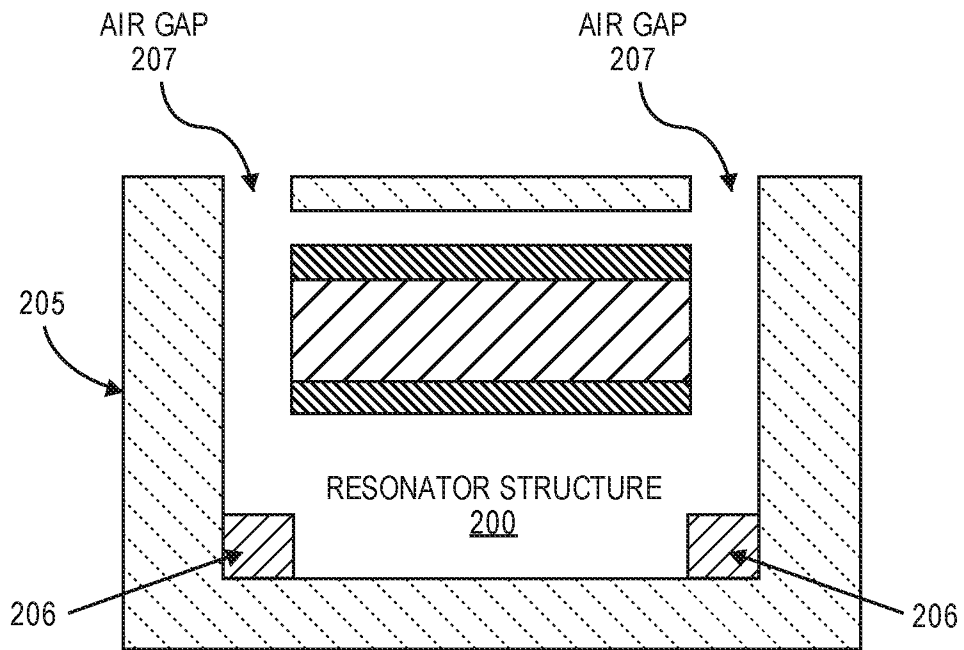

FIG. 1

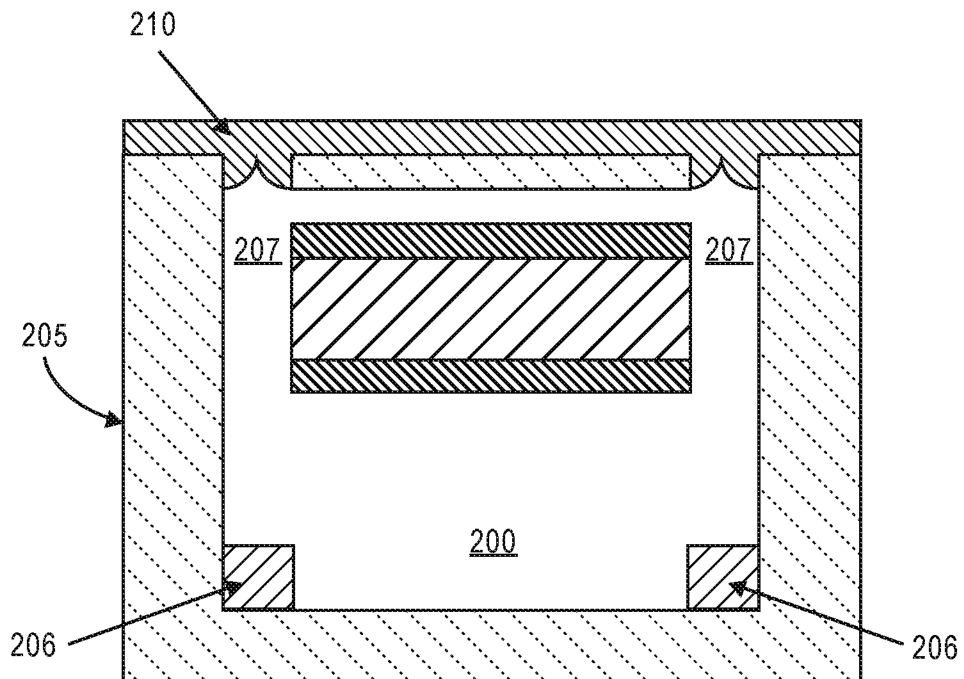

FIG. 2

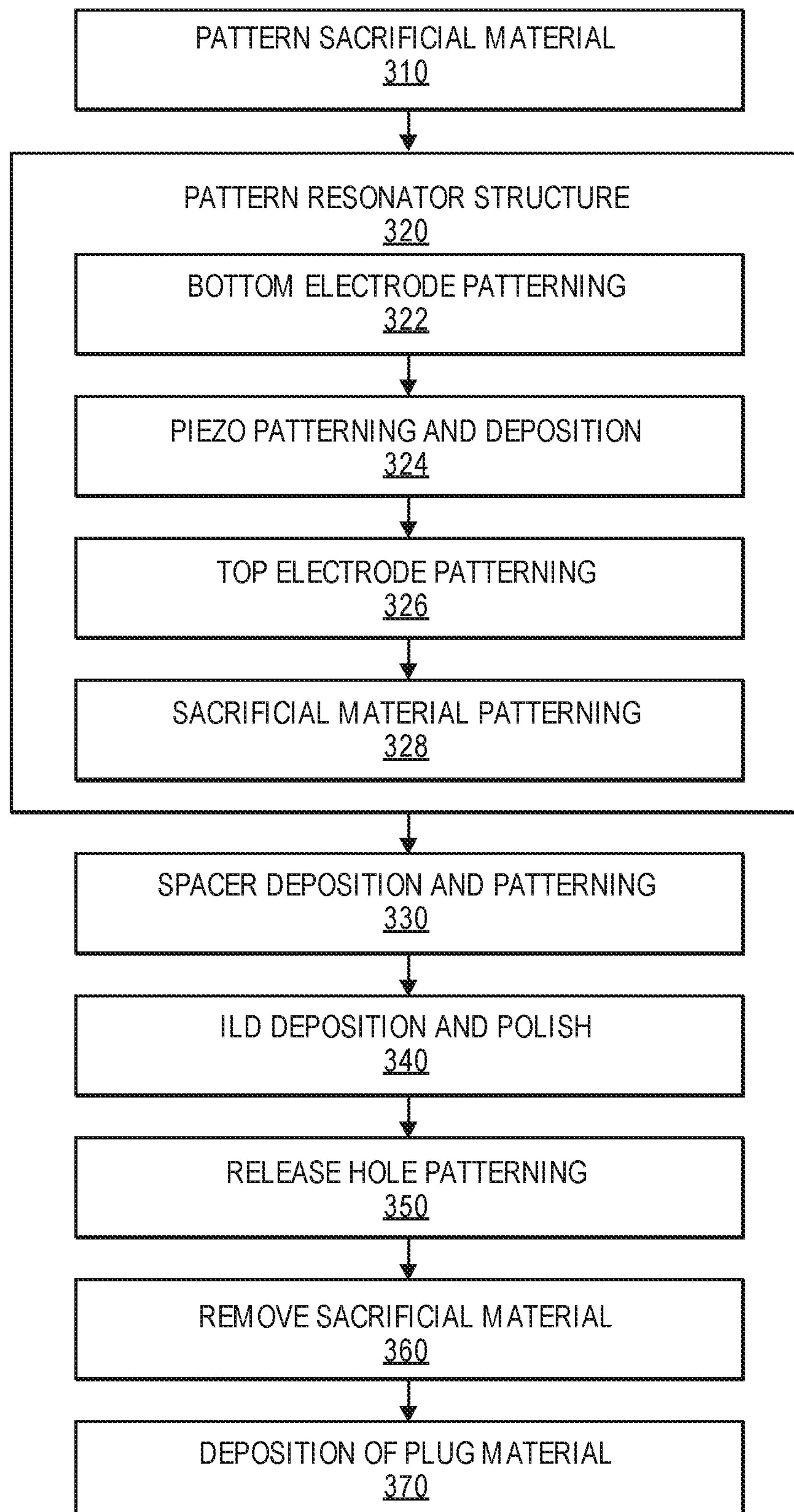

FIG. 3

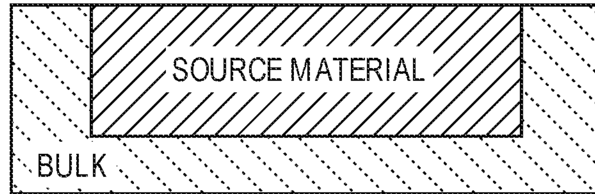

FIG. 4A

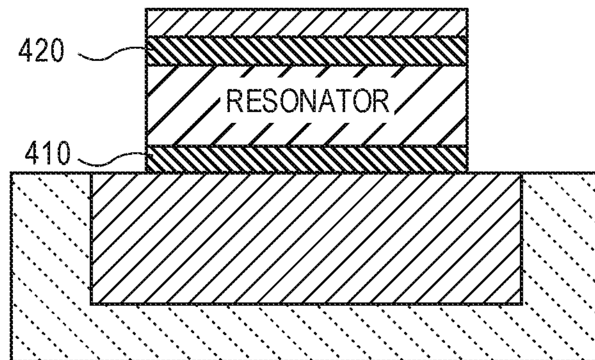

FIG. 4B

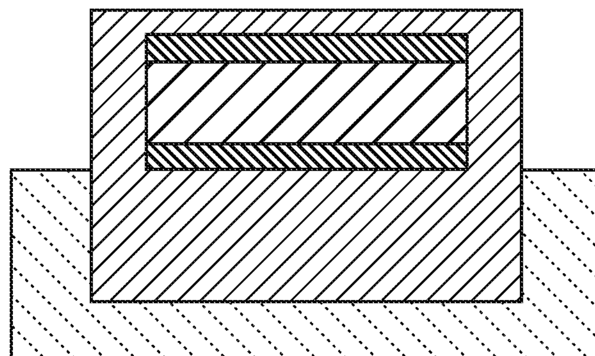

FIG. 4C

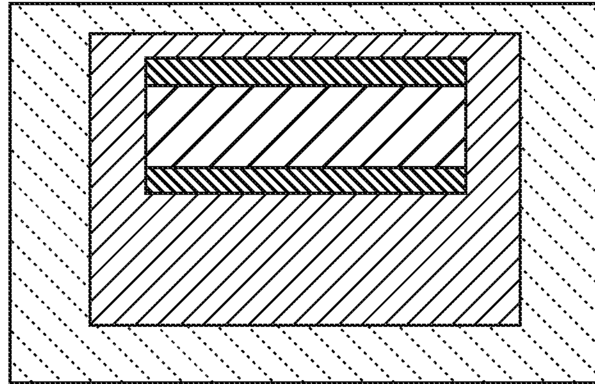

FIG. 4D

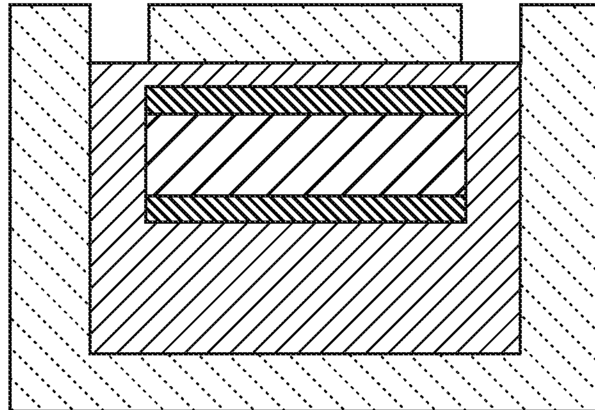

FIG. 4E

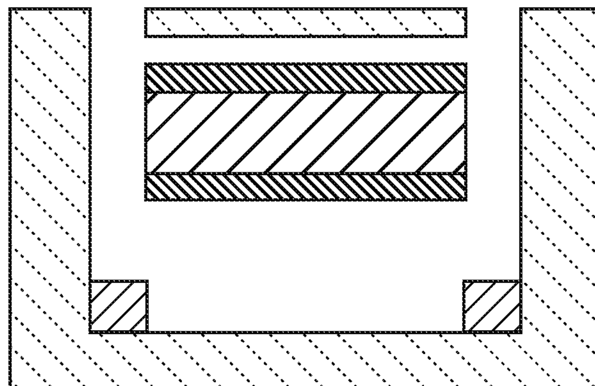

FIG. 4F

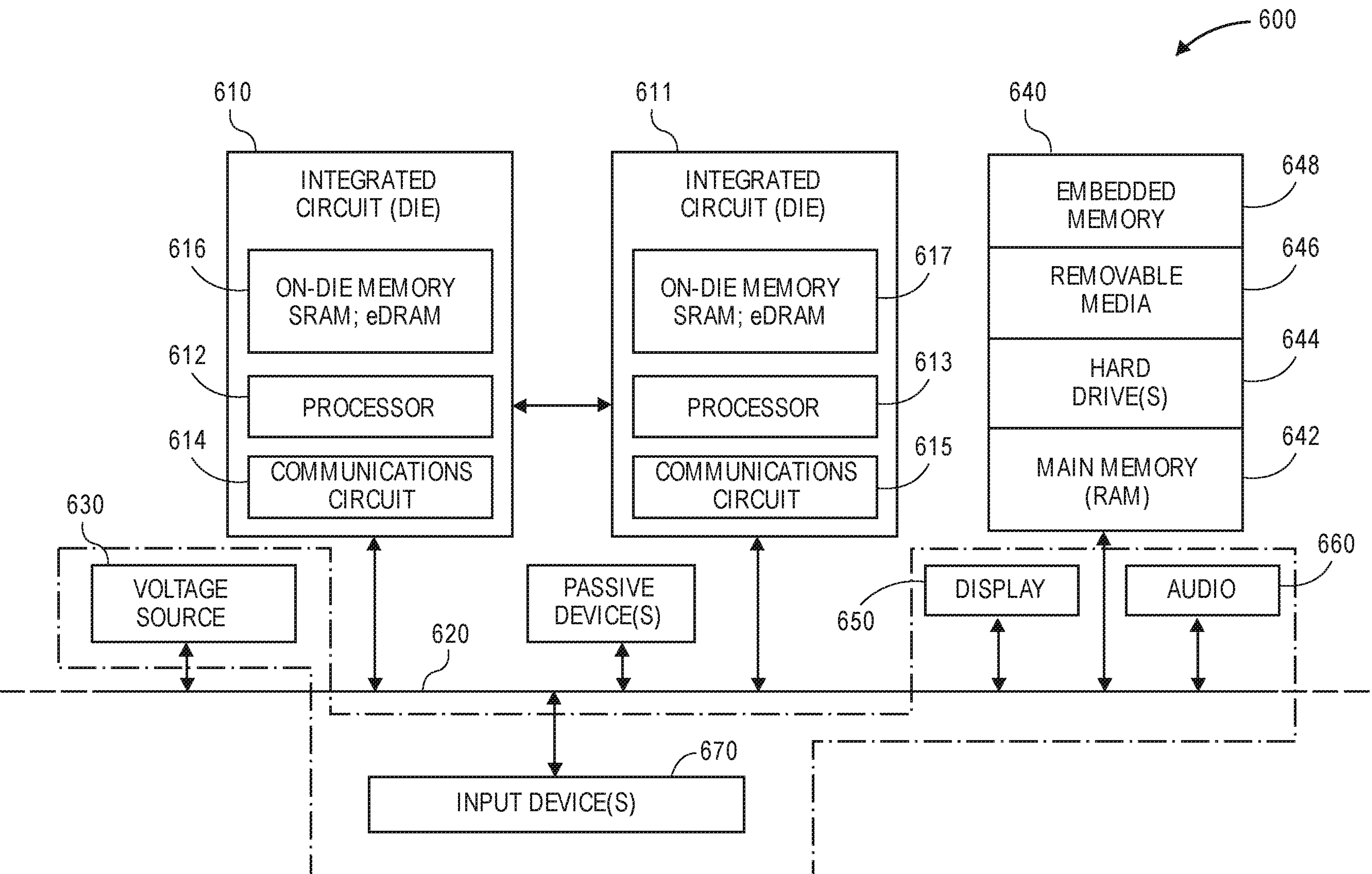

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/069315

A. CLASSIFICATION OF SUBJECT MATTER

H03H 9/25(2006.01)i, H03H 9/145(2006.01)i, H03H 9/205(2006.01)i, H03H 3/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H 9/25; H01L 21/311; H01L 27/02; H01L 29/84; H01L 21/00; H03H 9/145; H03H 9/205; H03H 3/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: FBAR, resonator, non, conformal, cavity

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2006-0258039 A1 (MARKUS LUTZ et al.) 16 November 2006 See paragraphs [0002], [0012], [0038]-[0052]; claim 1; and figures 4C-4F.	1,2,11,17 3-10,12-16,18-20
Y	US 2013-0126989 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 23 May 2013 See paragraphs [0004], [0018]-[0027]; claims 1, 3; and figure 2.	3-10,12-16,18-20
Y	US 2012-0190204 A1 (TROY L. GRAVES-ABE et al.) 26 July 2012 See paragraph [0027]; claims 1, 3; and figure 2.	10,16
A	US 2008-0160679 A1 (EVAN G. COLGAN et al.) 03 July 2008 See paragraphs [0026]-[0033]; claims 1-13; and figures 1B, 2B.	1-20
A	US 2009-0261453 A1 (PHILLIP D. MATZ et al.) 22 October 2009 See paragraph [0026]; claims 1-5; and figure 2G.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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Date of the actual completion of the international search
22 September 2017 (22.09.2017)

Date of mailing of the international search report
25 September 2017 (25.09.2017)

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
AHN, Jeong Hwan
Telephone No. +82-42-481-8633

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/069315

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