PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 3 :		(11) International Publication Number: WO 83/ 03029
H01L 21/225	A1	(43) International Publication Date: 1 September 1983 (01.09.83)

(21) International Application Number: PCT/US83/00169

(22) International Filing Date: 9 February 1983 (09.02.83)

(31) Priority Application Number: 352,519

(32) Priority Date: 26 February 1982 (26.02.82)

(33) Priority Country: US

(71) Applicant: WESTERN ELECTRIC COMPANY, INC. [US/US]; 222 Broadway, New York, NY 10038 (US).

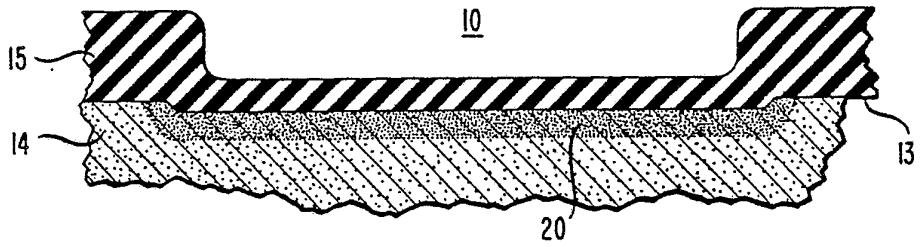
(72) Inventor: KINSBRON, Eliezer ; 233 South Fourth Avenue, Highland Park, NJ 08904 (US).

(74) Agents: HIRSCH, A., E., Jr. et al.; Post Office Box 901, Princeton, NJ 08540 (US).

(81) Designated States: DE (European patent), FR (European patent), JP, NL (European patent).

Published
With international search report.
With amended claims.

(54) Title: DIFFUSION OF SHALLOW REGIONS



(57) Abstract

A method for forming a shallow and highly concentrated arsenic doped surface layer (20) in a silicon bulk region includes the steps of forming an arsenic doped polysilicon layer (11) in contact with a preselected area of a bulk region (14) surface in which the surface layer is to be formed and completely oxidizing the polysilicon layer at a rate exceeding the rate at which arsenic diffuses in the bulk region. Since arsenic has a relatively high silicon/silicon dioxide segregation coefficient and the oxidation rate exceeds the arsenic diffusion rate, arsenic accumulates at the silicon dioxide/silicon interface during oxidation, and nearly all of the arsenic in the region of the polysilicon layer above the preselected area is driven into the bulk region surface by the oxidation to form an impurity layer having a very high surface concentration of arsenic.

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DIFUSSION OF SHALLOW REGIONS

This invention relates to a method for fabricating a semiconductor device comprising a shallow impurity layer in a semiconductor.

In the fabrication of semiconductor devices, such as integrated circuits, it is generally required that significant dopant impurities be introduced into a surface of a semiconductive region in order to form a surface impurity layer having electrical characteristics which are different from those of the rest of the region. By using appropriate impurities in appropriate amounts there may be formed a surface layer of the opposite conductivity type to that of the rest of the region, a surface layer of the same conductivity type as the rest of the region but having a lower resistivity or a surface layer of the same conductivity type as the rest of the region but having a higher resistivity. This invention provides a novel and advantageous method for forming such a surface impurity layer.

For example, in the fabrication of integrated circuits, it is generally desirable to reduce the lateral dimensions of circuit features to achieve a higher packing density, improved performance and a lower power dissipation. Recently, the development of improved lithographic and etching techniques have made it possible to form circuit features having lateral dimensions of less than 1 μm. However, in order to fabricate integrated circuits having such submicron features, it is necessary and/or desirable to provide relatively shallow surface impurity layers having relatively low sheet resistances.

In the case of metal-oxide-semiconductor (MOS) circuits, a reduction in the channel length of a MOS transistor necessitates a corresponding reduction in the depths of the source/drain regions of the transistor in

order to avoid unwanted short channel effects and excessive parasitic capacitances. For example, in an N-channel MOS transistor having an effective channel length of 0.5 μm, a gate oxide thickness of 250 Angstroms and a channel doping concentration of 4×10^{16} cm^{-3}, short channel effects are substantially avoided if the depths of the source/drain regions are less than 1000 Angstroms below the surface of the channel. In addition, it is also desirable for the source/drain regions to have a relatively low sheet resistance (e.g., less than 70 ohms per square) to permit rapid operation of the transistor.

In the case of bipolar circuits, a reduction in the lateral spacings between the various regions of a bipolar transistor necessitates a corresponding reduction in the respective depths of those regions. For example, in a vertical bipolar transistor structure having a minimum feature size of 1 μm, it is desirable that the emitter region be less than 2000 Angstroms in order to insure control over the base width and the total base charge. Moreover, it is also desirable for the emitter region to have a relatively low sheet resistance in order to provide a high minority carrier injection efficiency and to minimize the emitter crowding effect.

In the prior art surface impurity layers are most frequently formed by either conventional diffusion or ion implantation. In a conventional diffusion process impurities are first introduced into a semiconductor surface by diffusion from an appropriate predeposition source, such as a heavily doped semiconductor oxide layer or polycrystalline semiconductor layer in contact with the surface. The impurities are then thermally driven to a desired depth in a separate drive-in step. Although surface impurity layers as shallow as 500 Angstroms may be formed by conventional diffusion by using relatively low temperatures and short diffusion times, such layers tend to have relatively low impurity concentrations and therefore relatively high sheet resistances. Since the rate of

transport of impurities into a semiconductor by conventional diffusion is generally limited by the solid solubility of the impurities in the semiconductor at the diffusion temperature, conventional diffusion has the disadvantage of ordinarily not being able to provide a shallow layer with a sufficiently high impurity concentration to result in a relatively low sheet resistance.

In the case of ion implantation, impurities are introduced into a semiconductor surface by bombarding the surface with a beam of ionized impurities whose kinetic energy is in the range of one to several hundred kilovolts. Since the rate of implantation is largely independent of solid solubility of the impurities in the semiconductor and the depth of implantation can be precisely controlled, ion implantation can provide relatively shallow impurity layers having much higher impurity concentrations than those obtainable by conventional diffusion. However, ion implantation generally causes lattice damage which significantly lowers the carrier mobility in an implanted region. Consequently, ion implantation has a disadvantage in that even a highly concentrated impurity layer formed thereby generally has a relatively high sheet resistance unless the lattice damage caused by ion implanation is substantially repaired by an appropriate post-implantation annealing treatment. Since such an annealing treatment normally requires heating of the implanted layer for a relatively long time or at a relatively high temperature, the implanted layer will diffuse to a relatively large depth during the annealing treatment. For that reason it is difficult to form by ion implantation a surface impurity layer which is relatively shallow (e.g., less than 2000 Angstroms) and which has a relatively low sheet resistance (e.g., less than 70 ohms per square).

Therefore, a need clearly exists for a method for forming a surface impurity layer which has a lower sheet resistance than a layer of comparable depth formed by

conventional diffusion and which has a shallower depth than a layer of comparable sheet resistance formed by ion implantation.

The foregoing problem is solved according to the invention in a method for forming a shallow impurity layer characterized by the steps of forming a source layer in contact with at least a preselected area of a surface of the semiconductor, the source layer being doped with the impurity; and heating the source layer at an appropriate temperature to cause the impurity to diffuse into the semiconductor, the layer being heated in the presence of an appropriate reactant to cause a reaction which consumes the source layer at a rate exceeding the rate at which the impurity diffuses into the semiconductor.

In the drawing:

FIGS. 1 through 3 show cross-sectional views of a portion of a partially completed semiconductor device illustrating a method for forming a surface impurity layer during fabrication of the semiconductor device according to the preferred embodiment of the present invention.

FIG. 4 shows a graph comparing the arsenic profiles of arsenic doped surface layers formed by prior art methods with those formed by methods in accordance with the present invention.

Referring now to FIGS. 1 through 4, there are shown cross-sectional views of a portion of a partially completed semiconductor device 10 illustrating a method for forming a surface impurity layer in a semiconductive bulk region according to the preferred embodiment of the present invention. The same reference numerals are used throughout FIGS. 1 to 4 to denote like parts or regions of the device. In FIG. 1 a 500 Angstrom layer 11 of polysilicon is formed by conventional low pressure chemical vapor deposition (LPCVD) to be in contact with a preselected area 12 of a surface 13 of a single crystal silicon bulk region 14. The preselected area is defined by an aperture in a SiO_2 layer 15 approximately 3500 Angstroms thick covering the

surface of the bulk region. The SiO_2 layer serves as a diffusion mask and delimits the portion of the surface in which an impurity layer is to be formed. The bulk region may, for example, be a portion of a substrate wafer, an epitaxial layer formed on an appropriate substrate or a relatively thick polysilicon region. The material of the bulk region may be N-type, P-type or undoped. The polysilicon source layer is doped with arsenic to a concentration of 3×10^{20} cm^{-3}. The layer is doped by a conventional method, either in situ during deposition or by ion implantation or conventional diffusion after deposition. If ion implantation is used, the energy of the implant must be such that the ions do not penetrate through the polysilicon layer into bulk region. An energy of 30 KeV was found to be satisfactory for implanting a 500 Angstrom thick polysilicon layer. No annealing of the layer is necessary after the implant.

In FIG. 2, the device is heated at a temperature of approximately 950 degrees C in the presence of steam (H_2O) to effect oxidation of the polysilicon layer. The polysilicon layer is permitted to be entirely consumed by oxidation in approximately 20 minutes. During that time the arsenic in the polysilicon layer can diffuse into the silicon bulk region to form a surface impurity layer 20 extending approximately 500 Angstroms below the surface of the bulk region.

When arsenic doped silicon is oxidized, the SiO_2 yielded by such oxidation has a tendency to reject the arsenic, which is then preferentially segregated in the unoxidized silicon. The ratio of the equilibrium concentration of an impurity in the silicon to that in the silicon dioxide is denoted by the term silicon/SiO_2 segregation coefficient and is defined as

$$m = \frac{\text{Equilibirum Concentration of Impurity in Silicon}}{\text{Equilibrium Concentration of impurity in } SiO_2}$$

Since arsenic has a silicon/SiO_2 segregation coefficient of

approximately 800, nearly all of the arsenic in the polysilicon source layer is segregated in the unoxidized portion of the layer during oxidation. Upon completion of the oxidation, nearly all of the arsenic in the region of the polysilicon layer above the preselected area of the surface will be driven into the bulk region below.

Because the oxidation rate of the polysilicon layer at 950 degrees C in steam is greater than the rate at which arsenic diffuses in the polysilicon layer and the bulk region at that temperature, there is an accumulation of arsenic at the SiO_2/silicon interface which increases with oxidation time. To a lesser extent, there is also an accumulation of arsenic at the polysilicon/single crystal silicon interface due to grain boundary diffusion and segregation of the arsenic. After the polysilicon layer is completely oxidized, the arsenic concentration at the SiO_2 silicon interface in the bulk region is approximately 5×10^{20} cm^{-3}, which is nearly twice the solid solubility of arsenic in silicon at 950 degrees C. Therefore, the oxidation of the arsenic doped polysilicon layer provides a surface impurity layer 20 having a considerably higher surface concentration of arsenic than that which can be provided by conventional diffusion. Steam oxidation of the polysilicon source layer may also be performed at other temperatures, advantageously in the range of 800 to 950 degrees C.

It should be noted that the polysilicon layer 11 does not oxidize uniformly. Owing to the negligibly small diffusivity of arsenic in SiO_2 as compared with that in single crystal silicon, the accumulation of arsenic at the SiO_2/silicon interface is greater in the region of the polysilicon layer above the SiO_2 layer 15 than in the region above the silicon bulk region. Since the oxidation rate of silicon decreases as the arsenic concentration therein increases, it is necessary to "over-oxidize" the region of the polysilicon layer above the bulk region and consume approximately 200 Angstroms of the bulk region in

order to obtain complete oxidation of the polysilicon layer above the SiO_2 layer. Over-oxidation may be avoided by forming the source layer to cover only the preselected area of the bulk region surface or by doping only the region of the source layer above the preselected area.

After complete oxidation of the polysilicon layer, the surface impurity layer 20 has a relatively high sheet resistance of approximately 140 ohms per square, owing to a significant portion of the arsenic impurities in the layer not occupying proper substitutional lattice sites. However, the oxidation of the polysilicon layer causes relatively little lattice damage in the bulk region. Therefore, only a relatively short annealing treatment of approximately 30 minutes at approximately 950 degrees C in nitrogen is required to activate substantially all the arsenic impurities therein. As shown in FIG. 3, the annealing causes the surface impurity layer to diffuse further into the bulk region to a depth of approximately 1000 Angstroms below the surface of the bulk region, and the sheet resistance of the layer goes to a relatively low value of approximately 67 ohms per square. The annealing, which is required only when the surface concentration of the impurity layer exceeds the solid solubility, may be performed at other temperatures, advantageously in the range of 850 to 1000 degrees C, and for other durations, advantageously in the range of 10 minutes to 4 hours.

Referring now to FIG. 4 there is shown a graph comparing the arsenic concentration profiles of arsenic doped surface impurity layers formed by various methods. Curve I represents the impurity profile(arsenic concentration versus depth below the silicon surface) of an arsenic doped layer in silicon formed by conventional diffusion at a temperature of approximately 950 degrees C for approximately 20 minutes. The diffused layer has a depth of approximately 500 Angstroms, a sheet resistance of approximately 176 ohms per square, and a surface concentration of approximately 2.2×10^{20} cm^{-3}, which is

about the solid solubility of arsenic in silicon at 950 degrees C. Curve II represents the impurity profile of the layer represented by curve I after a drive-in at approximately 950 degrees C for approximately 30 minutes. After annealing the diffused layer has a depth of approximately 900 Angstroms and a sheet resistance of approximately 140 ohms per square.

Curve III represents the impurity profile of an arsenic doped layer in silicon formed by ion implantation at a dose of approximately 3×10^{15} cm^{-2} and an implant energy of approximately 30 KeV. After implantation the sample was annealed at 900 degrees C in dry oxygen for 30 minutes and at 950 degrees C in nitrogen for 30 minutes. This relatively long annealing treatment is conventionally used to repair the lattice damage caused by the ion implantation. After the annealing, the implanted layer has a depth of approximately 2000 Angstroms and a sheet resistance of approximately 44 ohms per square.

Curve IV represents the impurity profile of an arsenic doped layer in silicon formed according to the present invention by oxidation of a polysilicon layer approximately 500 Angstroms thick and uniformly doped with arsenic at a concentration of approximately 3×10^{20} cm^{-3}. The polysilicon layer was completely oxidized at approximately 950 degrees C in steam in approximately 20 minutes. After oxidation the arsenic doped layer is approximately 450 Angstroms in depth and has a sheet resistance of approximately 140 ohms per square. Comparing curves I and IV, it will be noted that the impurity layer formed by oxidation has a steeper impurity concentration profile and a higher surface impurity concentration than those of the impurity layer formed by conventional diffusion. Curve V represents the impurity profile of the arsenic doped layer represented by curve IV after annealing at approximately 950 degrees C for approximately 30 minutes to activate the arsenic impurities. The annealing treatment is relatively short since the oxidation method

for forming an impurity layer causes relatively little lattice damage. After the annealing the arsenic doped layer has a depth of approximately 1000 Angstroms and a sheet resistance of approximately 67 ohms per square. From a comparison of curves I-V, it is apparent that the present invention provides a surface impurity layer which has a lower sheet resistance than a layer of comparable depth formed by conventional diffusion and which has a shallower depth than a layer of comparable sheet resistance formed by ion implantation.

Although the preferred embodiment of the present invention uses arsenic for forming a surface impurity layer in silicon by oxidation of an arsenic doped polysilicon source layer, it is contemplated that other suitable species of impurities as well as other source-layer materials may be substituted. For example, other donor impurities for silicon, such as phosphorus and antimony, have silicon/SiO_2 segregation coefficients which are significantly greater than unity and may therefore be substituted for arsenic for forming N-type impurity layers in silicon. However, arsenic has the advantages of a relatively high silicon/SiO_2 segregation coefficient and a relatively low diffusivity which increases with arsenic concentration. For the formation of a shallow impurity layer having a high surface concentration, it is advantageous to select an impurity which has the highest segregation coefficient and the lowest diffusivity.

Given a particular species of impurities and a particular source-layer material, the depth and surface concentration of an impurity layer formed by oxidation of the source layer is a function of the thickness and impurity concentration of the source layer and the rate of oxidation. The conditions of the oxidation, i.e., temperature and ambient, should be selected to provide an oxidation rate which exceeds the rate at which the impurities diffuse in the bulk region at the oxidation temperature and which provides for complete oxidation of

the source layer in a time not longer than that required for the impurities in the source layer to diffuse into the bulk region to form an impurity layer of a desired depth. If annealing of the impurity layer is needed after oxidation, the extent of further diffusion of the impurity layer during annealing should be taken into account. Steam is advantageously used over other oxidizing ambients for silicon, since a steam ambient provides a relatively faster oxidation rate at a given temperature.

Although the present invention provides particular advantages for the formation of relatively shallow impurity layers, it is equally applicable to the formation of relatively thick impurity layers by making appropriate changes in the thickness of the source layer and the conditions of oxidation.

If ion implantation is used to dope the source layer, it may be advantageous, from the standpoint of obtaining shallower impurity layers, to implant only a portion of the source layer adjacent to the target surface. During oxidation of such a nonuniformly implanted source layer, the implanted impurities must first diffuse through the unimplanted portion of the source layer before entering the bulk region. Therefore, for a given oxidation rate the use of such a nonuniformly implanted source layer would provide a shallower impurity layer than the use of a uniformly doped source layer.

Although in the preferred embodiment of the present invention, the sample is heated in an oxidizing ambient to cause oxidation of the source layer, it is also contemplated that another appropriate reactant may be substituted to cause another reaction that would consume the source layer at a rate exceeding the rate at which the impurities diffuse in the bulk region and that would provide a reaction product in which the source-layer-material/reaction-product segregation coefficient is significantly greater than unity. For example, a polysilicon source layer doped with boron may be heated at

an appropriate temperature in the presence of platinum to cause a reaction which consumes the source layer at a rate exceeding the rate at which boron diffuses in silicon. The reaction would replace the polysilicon layer with a layer of PtSi, and boron has a PtSi/silicon segregation coefficient which is significantly greater than unity. The platinum is deposited in a layer over the polysilicon layer, or is deposited simultaneously with the deposition of the polysilicon layer.

It will be understood by those skilled in the art that the foregoing and other modifications and substitutions may be made to the described embodiment without departing from the spirit and scope of the present invention. For example, the source layer may be of a single crystal material such as an epitaxially grown material instead of a polycrystalline material, and the source layer and the bulk region may be of different materials.

Claims

1. A method for fabricating a semiconductor device comprising a shallow impurity layer (20) in a semiconductor (14)

CHARACTERIZED BY the steps of:

forming a source layer (11) in contact with at least a preselected area of a surface of the semiconductor, the source layer being doped with the impurity;

and heating the source layer at an appropriate temperature to cause the impurity to diffuse into the semiconductor, the layer being heated in the presence of an appropriate reactant to cause a reaction which consumes the source layer at a rate exceeding the rate at which the impurity diffuses into the semiconductor.

2. The method of claim 1

FURTHER CHARACTERIZED IN THAT

the reaction yields a reaction product, and the impurity has a source-layer-material/reaction-product segregation coefficient which is significantly greater than one.

3. A method as recited in claim 2

FURTHER CHARACTERIZED IN THAT

the reactant is an appropriate oxidizing ambient, the reaction is oxidation, and the reaction product is an oxide of the source layer material.

4. A method as recited in claim 3

FURTHER CHARACTERIZED IN THAT

the thickness of the source layer, the impurities in the source layer, the concentration thereof and the temperature and ambient of the oxidation are selected to provide an impurity layer of a desired depth and surface concentration.

5. A method as recited in claim 4

FURTHER CHARACTERIZED IN THAT

the bulk region is single crystal silicon, the source layer is polycrystalline silicon, and the source-layer-material oxide is silicon dioxide.

6. A method as recited in claim 5 FURTHER CHARACTERIZED IN THAT the polycrystalline silicon source layer is formed by chemical vapor phase deposition and doped in situ.

7. A method as recited in claim 5 FURTHER CHARACTERIZED IN THAT the polycrystalline silicon source layer is formed by chemical vapor phase deposition and is doped by ion implantation after deposition.

8. A method as recited in claim 7 FURTHER CHARACTERIZED IN THAT only a portion of the source layer is doped by ion implantation.

9. A method as recited in claims 6 or 7, 8 FURTHER CHARACTERIZED IN THAT the source layer is doped with arsenic, the source layer is heated in a steam ambient at a temperature in the range of 800 degrees C to 950 degrees C to cause complete oxidation thereof, and after oxidation of the source layer the bulk region is annealed at a temperature in the range of 850 to 1000 degrees C for a time in the range of 10 minutes to 4 hours.

AMENDED CLAIMS

[received by the International Bureau on 05 May 1983 (05.05.83); original claims 1 to 9 have been replaced by the amended claims 1 to 8]

1. (Amended) A method for fabricating a semiconductor device comprising a shallow impurity layer (20) in a semiconductor (14)

CHARACTERIZED BY the steps of:

forming a source layer (11) in contact with at least a preselected area of a surface of the semiconductor, the source layer being doped with the impurity;

and heating the source layer at an appropriate temperature in the presence of an appropriate reactant to cause a reaction which consumes the source layer at a rate exceeding the rate at which the impurity diffuses in the bulk of the semiconductor, the reaction yielding a reaction product, and the impurity having a source-layer-material/reaction-product segregation coefficient which is significantly greater than one.

2. (Previous claim 3) A method as recited in claim 1

FURTHER CHARACTERIZED IN THAT

the reactant is an appropriate oxidizing ambient, the reaction is oxidation, and the reaction product is an oxide of the source layer material.

3. (Previous claim 4) A method as recited in claim 2

FURTHER CHARACTERIZED IN THAT

the thickness of the source layer, the impurities in the source layer, the concentration thereof and the temperature and ambient of the oxidation are selected to provide an impurity layer of a desired depth and surface concentration.

4. (Previous claim 5) A method as recited in claim 3

FURTHER CHARACTERIZED IN THAT

the bulk region is single crystal silicon, the source layer is polycrystalline silicon, and the source-layer-material oxide is silicon dioxide.

5. (Previous claim 6) A method as recited in claim 4

FURTHER CHARACTERIZED IN THAT

the polycrystalline silicon source layer is formed by chemical vapor phase deposition and doped in situ.

6. (Previous claim 7) A method as recited in claim 4

FURTHER CHARACTERIZED IN THAT

the polycrystalline silicon source layer is formed by chemical vapor phase deposition and is doped by ion implantation after deposition.

7. (Previous claim 8) A method as recited in claim 6

FURTHER CHARACTERIZED IN THAT

only a portion of the source layer is doped by ion implantation.

8. (Previous claim 9) A method as recited in claims 5, 6 or 7

FURTHER CHARACTERIZED IN THAT

the source layer is doped with arsenic, the source layer is heated in a steam ambient at a temperature in the range of 800 degrees C to 950 degrees C to cause complete oxidation thereof, and after oxidation of the source layer the bulk region is annealed at a temperature in the range of 850 to 1000 degrees C for a time in the range of 10 minutes to 4 hours.

FIG. 1

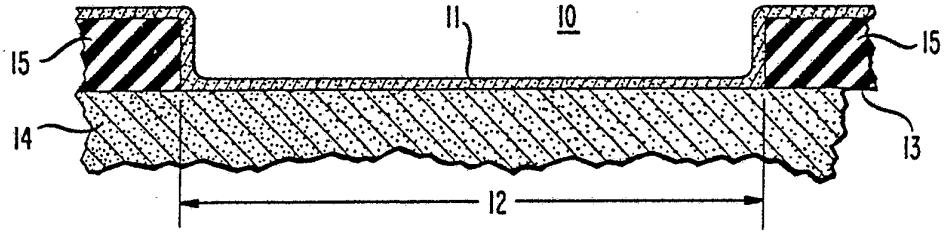


FIG. 2

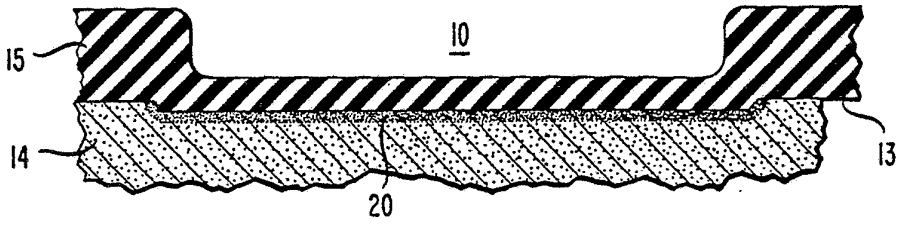


FIG. 3

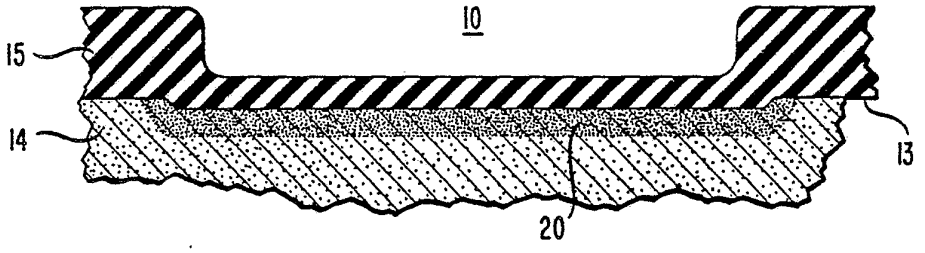
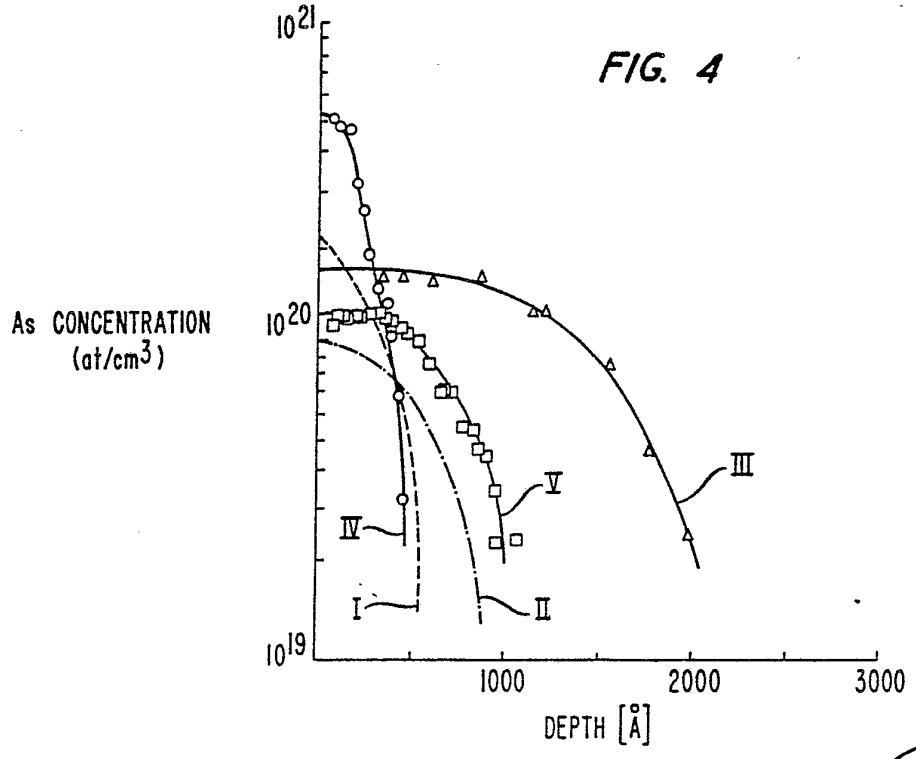


FIG. 4



INTERNATIONAL SEARCH REPORT

International Application No PCT/US83/00169

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL[3] H01L 21/225
U.S. CL 148/188

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	29/591; 148/186,187,188

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X,Y	US, A, 4,274,892, (TEMPLIN), 23 June 1981	1-9
X,Y	US, A, 3,928,095, (HARIGAYA et al.) 23 December 1975	1-9
Y	US, A, 2,802,760, (DERICK et al.), 13 August 1957	9
Y	US, A, 4,063,967, (GRAUL et al.), 20 December 1977	7,8
Y	US, A, 4,136,434, (THIBAULT), 30 January 1979	9
A	US, A, 3,502,517, (SUSSMANN), 24 March 1970	9
A	US, A, 2,953,486, (ATALLA), 20 September 1960	1
A	US, A, 3,418,180, (KU), 24 December 1968	1
A	US, A, 3,664,896, (DUNCAN), 23 May 1972	7
A	US, A, 3,808,060, (HAYS et al), 30 April 1974	9

* Special categories of cited documents: [15]

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"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
29 March 1983	07 APR 1983
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	George T. Ozaki George T. Ozaki