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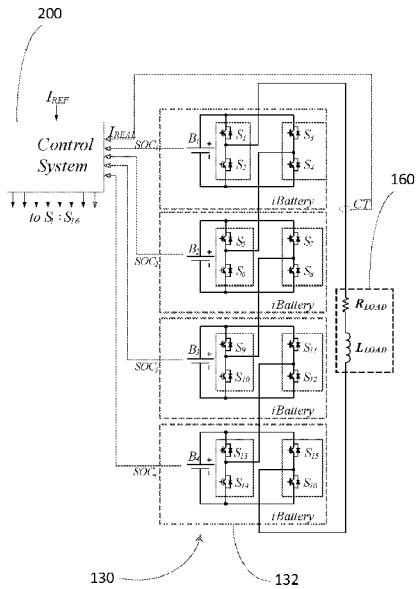

FIGURE 21

(57) Abstract: Systems and methods directed to improved battery management, motor control, energy storage and battery charging. The systems and methods enable vehicle electrification and provides a paradigm changing platform that enables integration of battery management, charging and motor controls with means to manage regenerative braking, traction and handling. In embodiments, systems and methods are directed to a unified modular battery pack system having a cascaded architecture comprising an integrated combination of a networked low voltage converter/controller with peer-to-peer communication capability, embedded ultra-capacitor or other secondary energy storage element, battery management system and serially connected set of individual cells as the fundamental building block.

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SYSTEMS AND METHODS FOR POWER MANAGEMENT AND CONTROL

FIELD

[0001] The present disclosure relates to electric power management and control of battery systems, and more particularly to systems and methods that facilitate improved battery management, motor control, energy storage, and battery charging for electric vehicles and other stationary applications.

BACKGROUND

[0002] Today's automobile technology, as evolved over the past century, is characterized, amongst many things, by an interplay of motors, mechanical elements, and electronics. These are the key components that impact vehicle performance and driver experience. Motors are of the combustion or electric type and one usually finds one motor per car, exceptions being cars with hybrid drivetrains, featuring a combination of a combustion engine with one or two electric motors, or performance oriented electric vehicles that are outfitted with two motors. In almost all cases the rotational energy from the motor(s) is delivered via a set of highly sophisticated mechanical elements, such as clutches, transmissions, differentials, drive shafts, torque tubes, couplers, etc. These parts control to a large degree torque conversion and power distribution to the wheels and are key elements to define the performance of the car. They also impact road handling. Over the years individual car manufacturers have highly optimized these mechanical parts to provide better performance, higher fuel efficiency and ultimately differentiation in the market place. On the control side, apart from driver comforts such as entertainment, navigation and human machine interface elements, there are typically only a few clusters of specialty electronics hardware and embedded software that control/optimize motors, clutch/transmission operation and road holding/handling.

[0003] Today's electric automobiles or vehicles (EVs) have largely adopted most of the hundred-year old design paradigm of a combustion vehicle, with the obvious substitutions of batteries, charging systems and electric motors for the usual gas tank, fuel pumps/injectors and combustion engine. While the control electronics are adapted to the difference in components, it is important to realize that most of the mechanical drivetrain parts described above are still there (see, e.g., Figures 1A and 1B). This is to say that the overall design philosophy of current EVs has moved little beyond the conventional paradigm. As such, the true potential of electrification is not being realized.

[0004] An EV comprises various electrical systems that are related to the drivetrain including, among others, the battery, the charger and motor control. A short inventory of the current capabilities and shortcomings of these electrical systems include:

Conventional Battery Design

[0005] At the moment, high voltage battery packs are typically organized in a serial chain of lower voltage battery modules. Each such module is further comprised of a serially connected set of individual cells and a simple embedded battery management system to regulate basic cell related characteristics, such as state of charge and voltage. Electronics with more sophisticated capabilities or some form of smart interconnectedness is absent. As a consequence, any monitoring or control function is handled by a separate system, which, if at all present elsewhere in the car, lacks the ability to monitor individual cell health, state of charge, temperature and other performance impacting metrics. There is also no ability to adjust power draw per individual cell in any form. Some of the major consequences are: (1) the weakest cell constrains the overall performance of the entire battery pack, (2) failure of any cell or module leads to a need for replacement of the entire pack, (3) battery reliability and safety are considerably reduced, (4) battery life is limited, (5) thermal management is difficult, (6) battery packs always operate below maximum capabilities, (7) sudden inrush into the battery packs of regenerative breaking derived electric power cannot be readily stored in the batteries and will require dissipation via a dump resistor.

Current Charger Design

[0006] Charging circuits are typically realized in separate on-board systems. They stage power coming from outside the EV in the form of an AC signal or a DC signal, convert it to DC and feed it to the battery pack(s). Charging systems monitor voltage and current and typically supply a steady constant feed. Given the design of the battery packs and typical charging circuits, there is little ability to tailor charging flows to individual battery modules based on cell health, performance characteristics, temperature, etc. Charging cycles are also typically long as the charging systems and battery packs lack the circuitry to allow for pulsed charging or other techniques that would optimize the charge transfer or total charge achievable.

Current Motor Control Design

[0007] Conventional controls contain DC to DC conversion stages to adjust battery pack voltage levels to the bus voltage of the EV's electrical system. Motors, in turn, are then driven by simple two-level multiphase converters that provide the required AC signal(s) to the electric motor.

Each motor is traditionally controlled by a separate controller, which drives the motor in a 3-phase design. Dual motor EVs would require two controllers, while EVs using four in-wheel motors would require 4 individual controllers. The conventional controller design also lacks the ability to drive next generation motors, such as switch reluctance motors (SRM), characterized by higher number of pole pieces. Adaptation would require higher phase designs, making the systems more complex and ultimately fail to address electric noise and driving performance, such as high torque ripple and acoustical noise.

[0008] In view of the foregoing limitations, systems and methods that facilitate improved battery management, motor control, power storage, and battery charging are desirable to address the above noted shortcomings and provide a paradigm changing platform.

SUMMARY

[0009] The embodiments of the present disclosure are directed to systems and methods that facilitate improved battery management, motor control, energy storage and battery charging. As such, the systems and methods provided herein enable realization of the true potential of vehicle electrification and provide a paradigm changing platform that intelligently integrates battery management, charging and motor controls with means to manage regenerative braking, traction and handling.

[0010] Exemplary embodiments of the present disclosure are preferably directed to a unified modular battery pack system having a cascaded architecture comprising an integrated combination of a networked low voltage converter/controller with peer-to-peer communication capability, embedded ultra-capacitor or other secondary energy storage element, battery management system and serially connected set of individual cells as the fundamental building block. An interconnected assembly of such intelligent battery modules becomes effectively a smart electrical "neural network" and the replacement for: (1) a charging system, (2) battery management modules, (3) DC to DC converter, and (4) motor controller(s).

[0011] This modular smart battery pack system is not only combinable with conventional EV motors and drive trains, it is combinable with new in-wheel EV motors being developed for use in future EVs.

[0012] In exemplary embodiments provided herein, the electronics of each modular smart battery pack are based on a multilevel controller, which in certain exemplary embodiments is preferably a bi-directional multilevel hysteresis controller, combined with temperature sensors and networking interface logic. This design provides a long list of advantages: (1) Improved battery utilization through individual switching of modules based on their age, thermal condition and

performance characteristics; (2) reduced thermal losses in cells through careful power consumption or power generation balancing; (3) slowed cell aging through better individual thermal management and filtering of high-order current harmonics; (4) capability of granular monitoring of battery health and early warning of servicing need; (5) fail-save and redundant design capable of maintaining drivability, even under individual module failure; (6) higher efficiency and better economics through utilization of new semiconductor technologies operating at lower component voltages to reduce power losses and cost; (7) software based optimization of topologies and control methods to adapt to different vehicle characteristics; (8) close to full recuperation of energy from regenerative breaking and fast response on acceleration by virtue of embedded ultra-capacitors; (9) integrated on-board optimized charging due to individual cell load balancing and monitoring, including ultra-fast pulsed charging driven by intelligent controller circuitry; (10) reduced electromagnet interference and sensitivity of the circuit topology; (11) adaptive neural-net based coordination between modules to enhance overall system performance, response time, thermal management and collective system efficiency; (12) elimination of mechanical drivetrain components and associated losses when combined with in-wheel motors; (13) reduction of overall drivetrain magnetic and electric losses; (14) increased power density when used with in-wheel motors; (15) reduction of torque ripple and increased passenger comfort due to reduced electrical and mechanical noise from refined motor control and electrical filtering; (16) ability to adapt to and be optimized for all current and next generation motor designs; (17) reduction in space providing more room for passengers/cargo/additional batteries (more range); (18) reduction in weight providing for better performance, higher vehicle efficiency, farther driving range; (19) superior handling and better traction when combined with in-wheel motors; (20) universal building block, adaptable for use from small passenger cars to large buses and commercial trucks; (21) software based differentiation of vehicle characteristic instead of via traditional mechanical component designs.

[0013] Other systems, methods, features and advantages of the example embodiments will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The details of the example embodiments, including structure and operation, may be gleaned in part by study of the accompanying figures, in which like reference numerals refer to like parts. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the disclosure. Moreover, all illustrations are intended to convey concepts, where relative sizes, shapes and other detailed attributes may be illustrated schematically rather than literally or precisely.

[0015] Figure 1 illustrates a simplified schematic of the power electronic circuit and electric motor of a conventional battery electric vehicle

[0016] Figure 2 illustrates a schematic of a power electronic circuit and electric motor for a battery electric vehicle according to embodiments of the present disclosure having a unified modular system with cascaded architecture including an intelligent modular AC battery pack comprising a series connection of intelligent low voltage battery modules.

[0017] Figures 3A through 3I illustrate schematics showing the power electronic circuit according to embodiments of the present disclosure as an intelligent, modular representation of the conventional high voltage power electronic circuit for a battery electric vehicle shown in Figure 1; Figure 3A shows the high voltage battery pack comprising a serial chain of low voltage battery modules; Figure 3B shows each battery module comprising a series connection of lower voltage battery cells and an integrated battery management or control system; Figure 3C shows the high voltage DC/AC converter split into multiple low voltage DC/AC converters in series; Figure 3D shows an individual low voltage DC/AC converter integrated within an individual battery module; Figure 3E shows an ultra- or super- capacitor integrated within an individual battery module to intermittently store in-rush of breaking power; Figure 3F shows an high voltage intelligent modular AC battery pack comprising a series connection of lower voltage intelligent battery modules integrated with battery management or control systems, low voltage converters and ultra-capacitors; Figures 3G and 3H shows the DC/DC converter removed from the power electronic circuit; Figure 3I shows the AC/DC converter/charger removed from the power electronic circuit.

[0018] Figure 4 illustrates a perspective view conceptual representation of an intelligent battery module comprising a battery integrated with a battery management and control system, a low voltage converter and an ultra-capacitor according to embodiments of the present disclosure.

[0019] Figure 5 illustrates a schematic diagram of an intelligent battery module according to embodiments of the present disclosure coupled to a battery module control system (or local electronic control unit (ECU)) and a master control system (or master ECU).

[0020] Figure 6 illustrates a schematic diagram of multiple intelligent modular AC battery packs according to embodiments of the present disclosure coupled to a three phase motor and a charging coupling for coupling to a single or three phase grid or power source.

[0021] Figures 7A and 7B illustrate graphs of typical waveforms of output voltages for one (1) intelligent battery module (Figure 7A) and one (1) phase of the intelligent modular AC battery pack with six (6) intelligent battery modules connected in series in each phase (Figure 7B).

[0022] Figures 8A, 8B, 8C and 8D illustrate graphs showing the principle of phase shifted carrier technique.

[0023] Figure 9 illustrates a schematic of a functional diagram of voltage level selector of a nine-level four-quadrant hysteresis controller.

[0024] Figures 10A, 10 B and 10C illustrates graphs showing the operation of a nine-level four-quadrant hysteresis controller; Figure 10A illustrates the current control error I_{ERROR}, as a difference between I_{REAL} and I_{REF}; Figure 10 B illustrates the reference current I_{REF} and real current I_{REAL} in motor phase; Figure 10C illustrates the converter output voltage V_{OUT}.

[0025] Figure 11 illustrates a functional diagram of a 9-level, 4-quadrant hysteresis current controller with state of charge (SOC) balancing and zero state rotation.

[0026] Figure 12 illustrates a functional diagram of an intelligent battery module rotation controller.

[0027] Figure 13 illustrates a functional diagram of a *di/dt* Estimator.

[0028] Figures 14A and 14B illustrate functional diagrams of *–0VDC Rotation* (Figure 14A) and *+0VDC Rotation* (Figure 14B) blocks.

[0029] Figures 15A and 15B illustrate functional diagrams of *+1VDC Rotation* (Figure 15A) and *–1VDC Rotation* (Figure 15B) blocks.

[0030] Figures 16A, 16B, 16C and 16D illustrate functional diagrams of *0VDC Rotation Generator* (Figure 16A), *1VDC Rotation Generator* (Figure 16B), *2VDC Rotation Generator* (Figure 16C) and *3VDC Rotation Generator* (Figure 16D).

[0031] Figure 17 illustrates a schematic diagram of a centralized connection of all intelligent modules to a master ECU for state of charge (SOC) balancing.

[0032] Figure 18 illustrates a flow diagram of structure power flow management in the intelligent battery module.

[0033] Figure 19 illustrates a circuit diagram showing the topology of the intelligent battery module and currents in node 1.

[0034] Figure 20 illustrates graphs of currents in the intelligent battery module, when the supercapacitor module operates as an active filter.

[0035] Figure 21 illustrates a single-phase intelligent battery pack connected to a single-phase load.

[0036] Figure 22 illustrates a three-phase intelligent battery pack connected to Switched Reluctance Motor.

[0037] It should be noted that elements of similar structures or functions are generally represented by like reference numerals for illustrative purpose throughout the figures. It should also be noted that the figures are only intended to facilitate the description of the preferred embodiments.

DETAILED DESCRIPTION

[0038] The following embodiments are described in detail to enable those skilled in the art to make and use various embodiments of the present disclosure. It is understood that other embodiments would be evident based on the present disclosure, and that system, process, or changes may be made without departing from the scope of the present embodiments.

[0039] The embodiments of the present disclosure are directed to systems and methods that facilitate improved battery management, motor control, energy storage and battery charging. As such, the systems and methods provided herein enable realization of the true potential of vehicle electrification and provide a paradigm changing platform that intelligently integrates battery management, charging and motor controls with means to manage regenerative braking, traction and handling.

[0040] Exemplary embodiments of the present disclosure are preferably directed to a unified modular battery pack system having a cascaded architecture comprising an integrated combination of a networked low voltage converter/controller with peer-to-peer communication capability, embedded ultra-capacitor, battery management system and serially connected set of individual cells as the fundamental building block. An interconnected assembly of such intelligent battery modules becomes effectively a smart electrical "neural network" and the replacement for: (1) a charging system, (2) battery management modules, (3) DC to DC converter, and (4) motor controller(s).

[0041] This modular smart battery pack system is not only combinable with conventional EV motors and drive trains, it is combinable with new in-wheel EV motors being developed for use in future EVs.

[0042] In exemplary embodiments provided herein, the electronics are based on a bi-directional multilevel controller, combined with temperature sensors and networking interface logic. In certain exemplary embodiments the bi-directional controller is a bi-directional multilevel hysteresis controller.

[0043] Turning in detail to the figures, a simplified schematic of a conventional power electronic circuit 10 and electric motor 70 is shown in Figure 1. As shown in Figure 1, the power electronic circuit 10 typically includes a charger 20 comprising an AC-DC converter, a high voltage battery pack 30 electrically coupled to the charger 20, a DC-DC converter 40 electrically coupled to the high voltage battery pack 30, an DC-AC converter 50 electrically coupled to the DC-DC converter 40, and an electric motor 60 electrically coupled to the DC-AC converter 50.

[0044] Conventional high voltage battery packs 30 are typically organized in a serial chain of low voltage battery modules 32 (see, e.g., Figures 3A and 3B). Each such module 32 is further comprised of a serially connected set of individual lower voltage cells 34 and a simple embedded battery management system 36 to regulate basic cell related characteristics, such as state of charge and voltage (see, e.g., Figure 3B). Electronics with more sophisticated capabilities or some form of smart interconnectedness is absent. As a consequence, there is also no ability to adjust power draw per individual cell 34 in any form. Some of the major consequences are: (1) the weakest cell constrains the overall performance of the entire battery pack, (2) failure of any cell/module leads to a need for replacement of the entire pack, (3) battery reliability and safety are considerably reduced, (4) battery life is limited, (5) thermal management is difficult, (6) packs always operate below maximum capabilities, (7) sudden inrush of regenerative breaking derived electric power cannot be readily stored in the batteries..

[0045] Conventional charging circuits or systems, such as those represented by the charger 20, are usually realized in separate on-board systems. Such charging systems stage power (AC or DC signal) coming from outside the EV and convert it to DC and feed it to the battery pack(s) 30. The charging systems monitor voltage and current and typically supply a steady constant feed. Given the design of the batteries and typical charging circuits, there is little ability to tailor charging flows to individual battery modules 32 of the battery pack 30 based on cell health, performance characteristics, temperature, etc. Charging cycles are also typically long as the charging systems and battery packs 30 and individual modules 32 lack the circuitry to allow for pulsed charging or other techniques that would optimize the charge transfer or total charge achievable.

[0046] Conventional controls contain DC to DC conversion stages (see, e.g., DC-DC converter 40) to adjust the voltage levels of the battery pack 30 to the bus voltage of the electrical system of the EV. Motors, such as motor 60, in turn, are then driven by simple two-level multiphase converters (see, e.g., DC-AC converter 50) that provide the required AC signal(s) to the electric motor 60. Each motor is traditionally controlled by a separate controller, which drives the motor in a 3-phase design. Dual motor EVs would require two controllers, while EVs using four in-

wheel motors would require 4 individual controllers. The conventional controller design also lacks the ability to drive next generation motors, such as, e.g., switch reluctance motors (SRM), which are characterized by a higher number of pole pieces. Adaptation would require higher phase designs, making the systems more complex and ultimately fail to address electric noise and driving performance, such as high torque ripple and acoustical noise.

[0047] In contrast to the complex power electronic circuit 10 of conventional EVs, exemplary embodiments provided herein as illustrated in Figure 2, replace the charging system 20, battery management modules, DC to DC converter 40, and motor controller(s) 50 with an intelligent or smart modular AC battery pack 130 comprising an interconnected assembly of intelligent or smart battery modules 132 effectively providing a smart electrical "neural network".

[0048] Turning to Figures 3A through 3I, a series of schematics illustrating simplification of the complex high voltage power electronic circuit 10 for conventional EVs shown in Figure 1 to an intelligent or smart battery pack 130, as shown in Figure 2, comprising an interconnected assembly of intelligent battery modules 132 according to exemplary embodiments of the present disclosure. As shown in Figure 3A, the high voltage battery pack 30 comprising a serial chain of lower voltage battery modules 32, each of which comprises a series connection of lower voltage battery cells 34 and an integrated battery management and control system 36 as shown in Figure 3B. The high voltage DC/AC converter 50 can be split into multiple low voltage DC/AC converters 52 connected in series as shown in Figure 3C. Each of the individual low voltage DC/AC converters 52 can be integrated within an individual battery module to form a smart or intelligent battery module 132 as shown in Figure 3D. To intermittently store an in-rush of breaking power, Figure 3E shows an ultra-capacitor 38 integrated within an individual intelligent battery module 132 (see also, e.g., Figure 4). As depicted in Figure 3F, a high voltage intelligent battery pack 130 comprises an interconnected assembly of intelligent battery modules 132. As shown in Figures 3G and 3H, the high voltage intelligent battery pack 130 effectively eliminates the need for the DC/DC converter 40. As shown in Figures 3H and 3I, the high voltage intelligent battery pack 130, which is effectively an intelligent modular AC battery pack 130, effectively eliminates the need for the AC/DC converter/charger 20.

Intelligent Battery Module Architecture

[0049] Figures 4 and 5 show a perspective view and a diagram, respectively, of intelligent a battery module 132 with the regenerative breaking/acceleration capability using supercapacitors (or ultracaps). It has three main components: the battery 32 with a BMS 36, the supercapacitor module 38 with bidirectional DC-DC converter based on MOSFET Transistors (MOSFETs) S1

and S2 with supercapacitor bank CSC and coupling inductor LC, and the output converter 52 based on four-quadrant H-bridge topology with four MOSFETs S3 – S6. As shown in Figure 5, the intelligent battery module 132 is coupled to a battery module control system 200 (or local electronic control unit (ECU)) and a master control system 210 (or master ECU)

ACi Battery Pack Principle of Operation

[0050] Figure 6 depicts a topology of 3-phase ACi battery pack (130A, 130B, 130C) connected to the motor 60 and comprising N intelligent battery modules connected in series in each phase. Each intelligent battery module in Figures 5 and 6 can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC-voltage (of battery) VDC to the AC output by different combinations of the four switches, S_3, S_4, S_5, and S_6. To obtain $+V_{dc}$, switches S_3 and S_6 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_4 and S_5. By turning on S_3 and S_5 or S_4 and S_6, the output voltage is 0. The AC outputs of each of the different output converter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in ACi battery pack is defined by $m = 2s+1$, where s is the number of intelligent battery modules. An example phase voltage waveform for pulse wave modulation (PWM) modulated 13-level ACi battery pack with six intelligent battery modules connected in series in each phase is presented in Figure 7B and an output voltage of one of the intelligent battery modules 132 is shown in Figure 7A.

[0051] The ACi battery pack can also serve as a rectifier/charger for the batteries of the intelligent battery modules 132 while the vehicle is connected to an AC supply as shown in Figure 6.

[0052] The switching signals $S_3 \div S_6$ (See Figures 5 and 6) for the switches $S_3 \div S_6$ of the output converter 152 in each intelligent battery module 132 may be generated in different ways depending on the flexibility and requirements of the adopted control hardware. One approach is to use space vector modulation or sine PWM to generate the reference voltage for each phase of the intelligent battery module 132. The switching signals for each intelligent battery module's output converter may then be generated using phase shifted carrier technique. This technique ensures that the cells are continuously rotated, and the power is almost equally distributed among them.

Modulation of Output Voltage in ACi Battery Pack— Multi-level PWM Modulation

[0053] The principle of the phase shifted technique is to generate the multilevel output PWM waveform using incrementally shifted two-level waveforms. Therefore, an N-level PWM

waveform is created by the summation of N-1 two-level PWM waveforms. These two-level waveforms are generated by comparing the reference waveform to triangular carriers that are incrementally shifted by 360°/(N-1). A 9-level example is shown in Figure 8A. The carriers are incrementally shifted by 360°/(9-1) = 45° and compared to the reference waveform. The resulted two-level PWM waveforms are shown in Figure 8C. These two-level waveforms may be used as the gate signals for the output converter (H-Bridge) MOSFETs in each intelligent battery module. For our 9-level example, which comprises four H-bridges, the 0° signal is used for S_3 and 180° signal for S_6 of the first module, the 45° signal is used for S_3 and 225° signal for S_6 of the second module, and so on. Note that in all H-bridges, the signal for S_4 is complementary to S_3 and the signal for S_5 is complementary to S_6 along with certain dead-time to avoid shoot through of each leg.

[0054] Depending on the resources and limitations of the hardware that is used to implement the modulation, an alternative is to generate the negative reference signal along with the first (N-1)/2 carriers. The 9-level example is shown in Figure 8B. In this case, the 0° to 135° PWM signals are generated by comparing V_{ref} to the corresponding carriers and the 180° to 315° PWM signals are generated by comparing $-V_{ref}$ to carriers of 0° to 135°. However, the logic of the comparison in the latter case must be reversed.

[0055] Other techniques such as a state machine decoder may also be used to generate the gate signals for the H-bridges.

Modulation of Output Voltage in ACi Battery Pack—Multi-level Hysteresis Control

[0056] Another approach to creating the switching signals $S_3 \div S_6$ (See Figures 5 and 6) for the output converter's switches in each intelligent battery module is a multi-level hysteresis control technique. This control method can be used with any type of motor and is very efficient especially for switched reluctance motor (SRM) drives.

[0057] The multi-level hysteresis control is described here for only one of three phases of the three phase ACi battery pack. In case of PMSM motor, three controllers have to be used together with additional circulation current reduction block (not described here). For a SRM motor a number of controllers can be more than three and there is no need in a circulation current reduction block.

[0058] For 9-level ACi battery pack (see Figure 6) comprising four intelligent battery modules 132 connected in series in each phase, all possible switching states for output converter's switches with corresponding output voltage levels are presented in Table 1. Only switching states for odd switching elements (MOSFETs S_3^N and S_5^N, where N=1, 2, 3, 4 is a number of intelligent

battery module) are presented in this table. In fact, to avoid a short circuit of the filtering capacitor C_F^N only one switch in a half-bridge of output H-bridge converter can be ON (in conducting mode) at any moment of time. Thus, the control signals for even switching elements (MOSFETs S_4^N and S_6^N, where N=1, 2, 3, 4 is a number of intelligent battery module) can be easily obtained by reversing the states of odd switching elements of the same half-bridge. For example, if $S_3^N=1$ and $S_5^N=0$, then $S_4^N=0$ and $S_6^N=1$.

Output Voltage	**Switching States**							
	S_3^1	S_5^1	S_3^2	S_5^2	S_3^3	S_5^3	S_3^4	S_5^4
-4VDC	0	1	0	1	0	1	0	1
-3VDC								
-3VDC1	1	1	0	1	0	1	0	1
	0	0	0	1	0	1	0	1
-3VDC2	0	1	1	1	0	1	0	1
	0	1	0	0	0	1	0	1
-3VDC3	0	1	0	1	1	1	0	1
	0	1	0	1	0	0	0	1
-3VDC4	0	1	0	1	0	1	1	1
	0	1	0	1	0	1	0	0
-2VDC								
-2VDC12	1	1	1	1	0	1	0	1
	0	0	0	0	0	1	0	1
-2VDC13	1	1	0	1	1	1	0	1
	0	0	0	1	0	0	0	1
-2VDC14	1	1	0	1	0	1	1	1
	0	0	0	1	0	1	0	0
-2VDC23	0	1	1	1	1	1	0	1
	0	1	0	0	0	0	0	1
-2VDC24	0	1	1	1	0	1	1	1
	0	1	0	0	0	1	0	0
-1VDC								
-1VDC1	0	1	1	1	1	1	1	1
	0	1	0	0	0	0	0	0
-1VDC2	1	1	0	1	1	1	1	1
	0	0	0	1	0	0	0	0
-1VDC3	1	1	1	1	0	1	1	1
	0	0	0	0	0	1	0	0
-1VDC4	1	1	1	1	1	1	0	1
	0	0	0	0	0	0	0	1
0	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0

+1VDC								
+1VDC1	1	0	1	1	1	1	1	1
	1	0	0	0	0	0	0	0
+1VDC2	1	1	1	0	1	1	1	1
	0	0	1	0	0	0	0	0
+1VDC3	1	1	1	1	1	0	1	1
	0	0	0	0	1	0	0	0
+1VDC4	1	1	1	1	1	1	1	0
	0	0	0	0	0	0	1	0
+2VDC								
+2VDC12	1	1	1	1	1	0	1	0
	0	0	0	0	1	0	1	0
+2VDC13	1	1	1	0	1	1	1	0
	0	0	1	0	0	0	1	0
+2VDC14	1	1	1	0	1	0	1	1
	0	0	1	0	1	0	0	0
+2VDC23	1	0	1	1	1	1	1	0
	1	0	0	0	0	0	1	0
+2VDC24	1	0	1	1	1	0	1	1
	1	0	0	0	1	0	0	0
+3VDC								
+3VDC1	1	1	1	0	1	0	1	0
	0	0	1	0	1	0	1	0
+3VDC2	1	0	1	1	1	0	1	0
	1	0	0	0	1	0	1	0
+3VDC3	1	0	1	0	1	1	1	0
	1	0	1	0	0	0	1	0
+3VDC4	1	0	1	0	1	0	1	1
	1	0	1	0	1	0	0	0
+4VDC	1	0	1	0	1	0	1	0

Table 1: Switching States of 9-level 4-quadrant Multilevel Cascaded Converter

[0059] Zero output voltage 0VDC can be ensured if all cells operate at zero state at the same time. This can be obtained bypassing the battery by switching ON either both upper switches or both lower switches. For instance, for intelligent battery module 1: $S_3^1 = 1$, $S_5^1 = 1$, $S_4^1 = 0$, $S_6^1 = 0$ or $S_3^1 = 0$, $S_5^1 = 0$, $S_4^1 = 1$, $S_6^1 = 1$.

[0060] Both voltage levels -3VDC and +3VDC can be obtained using four various combinations ±3VDC1, ±3VDC2, ±3VDC3, ±3VDC4, where the last index corresponds to a number of intelligent battery module operating at zero state, providing output zero voltage. In turn, each zero state can be coded using two mentioned above combinations of switching. Thus, there are eight possible combinations of setting ±3VDC output voltage level.

[0061] Similarly, both voltage levels -2VDC and +2VDC can be set by five different combinations ±2VDC12, ±2VDC13, ±2VDC14, ±2VDC23, ±2VDC24 depending on which two intelligent battery modules operate at zero state voltage. Taking into account a dual possibility of providing a zero state, a total number of possible combinations for ±2VDC is equal to ten.

[0062] Both voltage levels -1VDC and +1VDC can be obtained using four various combinations ±1VDC1, ±1VDC2, ±1VDC3, ±1VDC4. The last index corresponds to a number of intelligent battery modules operating at ±1VDC level. Again, each zero state is obtained dually. Thus, like for ±3VDC level, there are eight possible combinations of providing ±1VDC output voltage level.

[0063] Finally, the maximum voltage levels -4VDC and +4VDC can be provided at the output of converter's phase, when all intelligent battery module in phase are operating at the same time. Thus, there is only one available combination of switching state for each these cases.

Selection of Voltage Levels In Hysteresis Control

[0064] Previously it was explained how every voltage level of nine-level ACi battery pack can be obtained by different switching combinations of output converters of four intelligent battery modules 142. But the most significant task for a multi-level hysteresis controller is the identification of an appropriate output voltage level at any moment of converter operation based on a current feedback (motor phase) signal I_{REAL}.

[0065] A block diagram of voltage level selector 300 is presented in Figure 9. The voltage level selector comprises two sum blocks Sum1 301 and Sum2 307, five hysteresis blocks 302, 303, 304, 305 and 306, and one lookup table for voltage level determination. The real feedback current signal I_{REAL} is subtracted from the reference current I_{REF} and the current error signal I_{ERROR} as their difference comes to the input of all five hysteresis blocks. Each of these blocks has different settings of high (HB) and low (LB) boundary thresholds as presented in Table 2, where ΔI is preset value of maximum permitted current error. When I_{ERROR} reaches the corresponding high boundary (HB) of the hysteresis block, its output value is set to "1" and remains at this level until I_{ERROR} crosses its low boundary (LB). This will set "0" at the output of hysteresis block and the output is maintained at this level until I_{ERROR} reaches HB again. Thus, if low and high boundaries of five Hysteresis Blocks are distributed within a range between $-\Delta I$ and $+\Delta I$ (as shown in Table 2), then the output of Sum2 will be varying from 1 to 6, depending on I_{ERROR} value. A look-up table 308 presented in Figure 9 is used for determination of the required output voltage level based on the total state value (output of Sum2) of the hysteresis blocks and taking into account a sign of the real (or reference) current derivative *di/dt*. As discussed below, a sign of di/dt can be

determined as positive at the moment of time, when Sum2 reaches a value of 6, and will be changed to a negative one, when Sum2 becomes equal to 1.

Hysteresis Boundary	Current threshold
HB1	ΔI/5
LB1	-ΔI/5
HB2	2ΔI/5
LB2	-2ΔI/5
HB3	3ΔI/5
LB3	-3ΔI/5
HB4	4ΔI/5
LB4	-4ΔI/5
HB5	ΔI
LB5	-ΔI

Table 2: Current Threshold Levels for Hysteresis Blocks

Switching Between Voltage Levels in Nine-Level Four-Quadrant Hysteresis Control

[0066] A detailed description of the main principle of switching between voltage levels in a nine-level four-quadrant hysteresis control technique for one phase of nine-level ACi battery Pack operation is presented below.

[0067] In Figure 10B the reference current I_{REF} (red trace) and real current I_{REAL} (blue trace) in motor phase are presented together with five positive (HB1 ÷ HB5) and five negative (LB1 ÷ LB5) hysteresis boundaries (see Table 2 and Figure 10A also), equally distributed between I_{REF}-ΔI and I_{REF}+ΔI and separated by $\Delta I/5$ from each other (green traces). The current control error I_{ERROR}, as a difference between I_{REAL} and I_{REF}, and the converter output voltage V_{OUT} are presented in Figures 10(a) and 10(c), respectively.

[0068] The initial status of V_{OUT} in the considered time window (from 23.06ms) was set previously by the control system at +4VDC (where VDC=80V). At this voltage level the current I_{REAL} is rising up, and when I_{ERROR} hits the first hysteresis boundary LB1 at point A (level -ΔI/5 in Figure 10(a)), the output states of first hysteresis block is changed from "1" to "0", hence a sum at the output of Sum2 block is reduced by one from "6" to "5" (Figure 9). And according to the table in Figure 9 for $di/dt>0$, the voltage V_{OUT} becomes +3VDC.

[0069] From the beginning of considered time window and up to time *t1* (Figure 10C), the current I_{REF} has a positive *di/dt* value and hysteresis controller shall operate with voltage levels presented in the second column of look-up table in Figure 10C (*di/dt>0*). Starting from *t1* the *di/dt* sign of current I_{REF} is negative, but hysteresis controller remains operating as for positive *di/dt* until time *t2*, when I_{ERROR} hits a fifth hysteresis boundary LB5 and Sum2=1. This event will switch an operation of hysteresis controller to the first column of the table for *di/dt<0*. In other words, a sign of *di/dt* can be determined as negative at the moment (*t2*), when Sum2 reaches a value of "1" (and will be changed to a positive, when Sum2 becomes equal to "6"). This logic is implemented in *di/dt estimator* block, which will be presented as described in the next sections of this document.

[0070] While V_{OUT} is at its maximum negative level -4VDC, the current I_{REAL} is falling down (Figure 10(b)) and when it hits point F, which corresponds to the first hysteresis boundary HB1 in Figure 10(a), the output states of first hysteresis block is changed from "0" to "1", hence a sum at the output of Sum2 is increased by one from "1" to "2" (Figure 9). And according to look-up table in Figure9 for *di/dt<0*, the voltage V_{OUT} becomes -3VDC. At point G, when I_{REAL} and I_{ERROR} reach HB2, Sum2 is incremented again and V_{OUT} becomes -2VDC.

[0071] In the hysteresis control method provided herein, the maximum current error ΔI takes place only at the points where *di/dt* value of the reference current I_{REF} changes a sign. Beyond these critical points, the method works in such a way to minimize the current error I_{ERROR} at $\Delta I/5$ as fast as possible at given parameters of the load.

Overall method description

[0072] The generalized functional diagram of a 9-level 4-quadrant hysteresis current controller 500 with state of charge balancing and zero state rotation is presented in Figure 11. It includes the *switch stage selector* 300, which functions as described earlier. The output signal of Sum2 in Figure 9 is named as "Level" in Figure 11. This signal represents a numerical value for a general level (from 1 to 6) of a nine-level hysteresis controller, which is used further in the method to select an appropriate output voltage level of intelligent battery module's output converter.

[0073] According to the look-up table in Figure 9, knowledge of the *di/dt* sign is required to choose an appropriate output voltage level. As it was mentioned earlier, a sign of *di/dt* can be determined as negative at the moment, when "Level" reaches a value of "1", and will be changed to a positive, when "Level" becomes equal to "6". This logic is implemented in *di/dt estimator* block, shown in Figure 13. The *estimator* block comprises two digital comparators (Comp 1 and Comp 2) and RS flip-flop element. Both comparators provide transition pulses from "false" to

"true" at the moments, when "Level" signal is equal to "6" (Comp 1) and "1" (Comp 2). These rising edges are detected by RS flip-flop, which changes its output state accordingly, providing a "true" signal at its non-inverting output Q when $di/dt > 0$, and "false" signal when $di/dt < 0$.

[0074] As it was mentioned earlier and presented in Table 1, there are many switching states available for each voltage level of nine-level ACi battery pack, except of ±4VDC, when all intelligent battery modules are involved in providing a maximum positive or negative output voltage. Thus, there are following major tasks, which have to be resolved controlling the current of the motor, taking into account that hysteresis "Level" and a sign of di/dt are already known parameters:

1) Based on the *state of charge (SOC)* of each intelligent battery module, an identification of the intelligent battery module which has to be switched repetitively for some period of time to provide the required output voltage level and regulation of output current. This identification methodology has to ensure a balancing of the state of charges during an operation of the ACi battery pack. When this is provided, the energy, stored in batteries, or transferred from or to the motor, is equally distributed among all intelligent battery modules. This is a necessary condition of correct operation of ACi battery pack, where each cell has to be designed for a specific temperature profile of semiconductor switches based on their operational regimes. This task is performed by *SOC balancing* block (see Figure 11) in the method provided herein, and the functional diagram of *intelligent battery module rotation controller* 600 as this block's main component is presented in Figure 12.

2) For the intelligent battery module, identified by *SOC balancing block*, a rotation of zero switching state. This rotation provides a distribution of energy among the switches within a specific module in operation. There are two possible combinations of switching to provide a zero voltage at the output of intelligent battery module, as shown in Table 1. The rotation methodology alternates the switches used to provide a zero voltage with every second positive or negative operational level of the cell. In fact, as it will be shown in next section of this document, this rotation reduces twice the switching frequency of the switches in comparison with output voltage frequency of the intelligent battery module and the entire ACi battery pack. There are four *rotation generator* blocks 1001, 1002, 1003, and 1004 in the method provided herein for different levels of output voltage from 0VDC to 3VDC, which are presented in Figures 16A, 16B, 16C and 16D.

[0075] Each of four *rotation generators* in Figures 16A, 16B, 16C and 16D comprises: four digital comparators, one inverting element, four logic elements AND, two SR flip-flops Latch 1

and Latch 2 and two frequency dividers by 2. The structure and operational principle of all *rotation generator* blocks are the same; a difference is in the preset values of digital comparators only. In a *0VDC rotation generator, w*hen "*di/dt*" signal from *di/dt estimator* output is "true", the comparator Comp1 will set SR flip-flop Latch 1 output at 'true" when the "Level" signal is equal to "3", which corresponds to +1VDC of output voltage level. Another comparator Comp2, at positive *di/dt* will reset Latch 2, when the "Level" signal is equal to "2", which corresponds to +OVDC of output voltage level. In other words, a high level of pulse train at the output of Latch 1 will correspond to +1VDC voltage at the output of the nine-level converter, while its zero level will indicate +OVDC voltage level (+0 indicates that 0VDC level is following after and/or before +VDC level). Finally, the circuit included the frequency divider block and logic element AND is intended to set the output signal Rot+ OVDC at "true" with a high level of Latch 1 output, which happens at +1VDC output voltage level, and maintains this "true" signal until a second transition from +OVDC to +1VDC occurs. Such the output signal Rot+ OVDC is used to alternate two possible zero state switching combinations for the intelligent battery module in operation of providing +1VDC voltage level. The same operational logic is behind the Rot -0VDC signal, which is generated by the same *0VDC rotation generator* to alternate two zero state switching combinations for the intelligent battery module in operation of providing -1VDC voltage level.

[0076] The *intelligent battery module rotation controller* 600 and *SOC balancing block* provided herein for a multi-level hysteresis controller are explained further. The detailed functional diagram of *intelligent battery module rotation controller* is presented in Figure 12. The inputs of this block are the measured state of charges SOC1, SOC2, SOC3, and SOC4 from battery management systems (BMS) of all four intelligent battery modules in one phase. The output signals are the numbers of intelligent battery modules (from 1 to 4) with a maximum state of charge SOCmax, minimum state of charge SOCmin, and then SOCrot3 and SOCrot4, distributed as follows: SOCmin<SOCrot4<SOCrot3<SOCmax. In the beginning, SOC1 and SOC2 are compared with each other and if their difference ΔSOC_{12} is higher or lower than positive or negative threshold of hysteresis block Hyst 1, then the output of this block is set to "1" or "0" respectively, otherwise it maintains its previously set value at the output. This threshold helps ignore a noise of certain level in the feedback signal and regulates how often a rotation of intelligent battery modules should occur. Based on Hyst 1 output signal, Switch 1 choses a number of intelligent battery module (1 or 2) with a higher SOC and Switch 5 passes its corresponding SOC value to Sum 3, which compares it with a lowest state of charge of SOC3 and SOC4, which go through the same comparison technique. Thus, at the output of the *intelligent battery module rotation controller* the intelligent battery modules numbers are distributed in

accordance to their SOCs as SOCmin<SOCrot4<SOCrot3<SOCmax. Before going to rotation blocks signals SOCmax and SOCmin are reassigned to SOCrot1 and SOCrot2 in *SOC Balancing* block (see Figure 11) taking into account a sign of reference current I_{REF}. If the current I_{REF} is positive, that corresponds to an energy transferring from intelligent battery modules to the motor, then the intelligent battery module with a maximum SOC participates in a rotation of all positive output voltage levels (but not at the same time). This will cause a faster discharge of this intelligent battery module with a maximum SOC, because at positive output voltage and positive load current there is only one way for energy to be transferred: from the intelligent battery module to the motor. At the same time, at positive output current (or I_{REF}) the intelligent battery module with a minimum SOC has to participate in providing the negative output voltage levels only, to charge up its battery's voltage as soon as possible. That is because at positive load current but negative output voltage of the output converter there is only one direction for energy transfer: from the motor to batteries.

[0077] The *0VDC rotation* and *1VDC rotation* blocks are presented in Figures 14A, 14B, 15A and 15B respectively. Let's describe *+0VDC rotation* first. This block receives one control signal from *intelligent battery module Balancing* block SOCrot1, as well as one signal Rot +0VDC from *OVDC rotation generator,* and provides the control signals for switching elements of nine-level ACi battery pack for +OVDC output voltage, where +0 means that 0VDC level is following after and/or before +VDC level. The multiplexer Switch 1 chooses one of four different combinations of switching signals, based on input signal SOCrot1, indicating which intelligent battery module is operating at the same time in providing +VDC output level. This means that a rotation of zero switching state has to be performed for this specific intelligent battery module (with SOCrot1 number). The input signal Rot +0VDC controls a sequence of switching between two possible zero states [1 1] and [0 0] for the same intelligent battery module.

[0078] Block *+1VDC rotation* has more complicated structure. Besides the control signal Rot +1VDC coming from *1VDC rotation generator* block, It receives two control signals SOCrot1 and SOCrot3 from *SOC balancing block.* The first signal, SOC1rot, is used by multiplexer Switch 1 to set up a positive voltage at the output of intelligent battery module, which number is specified by this signal. This can be done by providing the switching combination [1 0] for that intelligent battery module. All other three intelligent battery modules have to provide a zero switching state. If at the output of converter, the voltage is changing between +0VDC and +1VDC, then the signal Rot+1VDC is always "true" and there is no rotation of zero switching state for other three cells. If the output voltage is varying between +1VDC and +2VDC, then a rotation of zero state has to be performed for only one specific intelligent battery module which is

involved in producing of +2VDC level. The input signal Rot +1VDC controls a sequence of switching between two possible zero states [1 1] and [0 0] for that intelligent battery module.

[0079] The same principle of operation is valid for *-0VDC rotation* and *-1VDC rotation*, with only a difference in input signals SOCrot2, instead of SOCrot1 and Rot-1VDC, instead of Rot+1VDC. The SOCrot3 signal, which indicates a number of cell operating at both +2DC and -2VDC levels, remains the same as for positive *rotation* blocks.

[0080] Blocks *+2VDC rotation* and *+3VDC rotation* have a complex structure with four input signals, where three of them SOCrot1, SOCrot2 and SOCrot3 are coming from SOC balancing block and one signal is either from 2VDC rotation generator or 3VDC rotation generator is intended to control a sequence of changing between zero switching states for the specific intelligent battery module.

[0081] A detailed discussion regarding multi-level hysteresis control is provided in U.S. Provisional Application No. 62/518331, filed June 12, 2017, and U.S. Provisional Application No. 62/521227, filed June 16, 2017, which applications are incorporated by reference as if set forth in full.

Local and Master ECUs Functions

[0082] The power electronics converters and local ECU 200, which manages the intelligent battery module operation 132 (see Figure 5), works through utilizing a state of charge (SOC) estimator to measure the initial SOC of the battery. A master control system (ECU) 210 receives this initial SOC data of all intelligent battery modules, as depicted in Figure 17 (see also Figure 5), and classifies them.

[0083] A SOC balancing technique for multi-level hysteresis controller was described above. For multi-level PWM, this balancing methodology is as follows: assuming all batteries are balanced before discharge, the strongest battery is the one with the highest initial SOC and the weakest battery is the one with the lowest initial SOC when the ACi battery pack is fully charged.

[0084] Depending on this data, the master ECU 210 computes the corresponding switching signals array that is necessary for proper operation of each individual intelligent battery module based on its battery capacity. In other words, in order to balance the state of charge of the modules, the SOC of each module should be compared to the total SOC, which can be calculated as:

$$SOC_{tot} = \frac{\sum_{i=1}^{n} SOC_i Q_i}{\sum_{i=1}^{n} Q_i}$$

Where SOC_i and Q_i – individual SOC and capacity of i-th intelligent battery module's battery and the difference along with a PI controller may be used to control the modulation index (M) of each module. Note that when the modules are charging the direction of the effect of SOC difference must be reversed since in this case the module with higher SOC is expected to receive less energy compared to the other modules.

[0085] The local control system of the intelligent battery module 132 gets this information and thus, there exists different switching signals arrays $S_{1...N}$ for each intelligent battery module which determines the individual DC currents (I_{DC1}, I_{DC2} ... I_{DCN}) and DC-bus voltages (battery voltages V_{B1}, V_{B2}...V_{BN}) of the system. In this way, the power management operates, and built-in power electronics unit manages the output power of each intelligent battery module autonomously. The strongest battery carries the highest current and the weakest battery carries the least current so that the SOC of all the batteries converge at a particular time.

Supercapacitor Module

[0086] The supercapacitor module 38 of intelligent battery module 132 (Figure 5) is connected in parallel to the main battery 32 and to the output converter 52. During acceleration, the capacitor voltage is allowed to discharge from full charge (50Vdc) to approximately one-third of its nominal voltage (17Vdc), allowing it to deliver 11kW of useful energy. This amount of energy allows taking 2.2kW of power during 5 seconds form one intelligent battery module and 66kW in total if 30 intelligent battery modules are placed in an ACi battery pack, which is enough power and time for a good acceleration without detriment to the battery life. During deceleration (regenerative braking), energy is recovered in a similar way, charging back the supercapacitors.

[0087] When the vehicle accelerates, the battery delivers the amount of current the motor needs. If this current exceeds a current limit for the battery, then the supercapacitor provides the difference. The regenerative braking operation is similar. In this case, the motor works as a generator delivering the recovered energy into the battery, but if the current injected exceeds the limit, then the DC-DC converter injects the excess into the supercapacitor.

[0088] The DC-DC converter works in two ways: Boost operation, used for acceleration which discharges the supercapacitor; and Buck operation used for deceleration (regenerative braking), which charges the supercapacitor. During Boost operation (acceleration), the MOSFET S_2 is switched on and off at a controlled duty cycle D, to transfer the required amount of energy from the capacitor to the battery pack. When S_2 is ON, energy is taken from the supercapacitor and stored in the inductor L_C. When S_2 is switched OFF, the energy stored in L_C is transferred into C_F, through S_1, and then into the motor and/or battery. During Buck operation, the converter

introduces energy from the battery to the supercapacitor. That operation is accomplished with a controlled operation on S_1. When S_1 is switched ON, the energy goes from the battery to the supercapacitor, and L_C stores part of this energy. When S_1 is switched OFF, the remaining energy stored in L_C is transferred inside the supercapacitor through diode of S_2.

[0089] The battery as a primary energy source is the one with the highest energy content and should therefore supply the average power needed by the motor. The supercapacitor is a secondary energy source and assists the battery by providing/absorbing the momentary load power peaks.

[0090] The redundant structure of power flow management between two sources and motor is presented in Figure 18. It has the advantage among other power control methods since allows a complete decoupling between the electrical characteristics (terminal voltage and current) of each source and those of the load. The power flow controller 1 receives a signal of reference battery power flow $P_{BATT,REF}$ from local ECU of intelligent battery module. This signal is determined by main power management controller located in a master ECU based on motor power $P_{iBATTERY}$ requirements and SOC of individual intelligent battery module's battery. The power flow controller 1 estimates a maximum allowable battery charge/discharge current and calculate a real permissible battery power flow P_{BATT}. This signal is compared with $P_{iBATTERY}$ and their difference is applied to the power flow controller 2 as a signal $P_{SC,REF}$. This controller calculates I_{SCM} current based on supercapacitor voltage V_{SC} and determines the switching signals S_1 and S_2 for buck/boost converter of Supercapacitor Module, which basic principles of operation are described above. Thus, $P_{iBATTERY}$ flow is provided by the output converter, P_{BATT} is estimated based on a maximum battery current and actual SOC and is ensured as a difference between $P_{iBATTERY}$ and P_{SC}, where the last one is managed by supercapacitor module's converter.

[0091] Another important function performed by supercapacitor module is an active filtering of the second-order current harmonic that appears in the output converter's DC-current I_{DC} as result of the intrinsic pulsating power nature of a single-phase system. Considering $V(t)_{OUT}$ and $I(t)_{OUT}$ as the output voltage and current of intelligent battery module:

$$V(t)_{OUT} = Vm_{OUT}\cos(\omega t)$$
$$I(t)_{OUT} = Im_{OUT}\cos(\omega t + \varphi);$$

The instantaneous input-output power balance of the intelligent battery module gives:

$$P(t)_{OUT} = V(t)_{OUT}I(t)_{OUT} = \frac{1}{2}Vm_{OUT}Im_{OUT}\cos(\varphi) + \frac{1}{2}Vm_{OUT}Im_{OUT}\cos(2\omega t + \varphi)$$

[0092] The first constant term refers to the average power that is used to charge/discharge the battery. The second oscillating term, however, does not contribute to the average battery SOC. This component has a considerable peak-to-peak value, which can reach up to two times the grid current amplitude at a modulation index of unity. The second-order current component exhibits some disadvantages, e.g., increase of the inner battery resistive losses related to the resulting current RMS value as well as periodic change of the battery behavior.

[0093] The main waveforms for the active filtering case are shown in Figures 20A and 20B. The supercapacitor acts as an active filter aiming at the elimination of the second-order harmonic in battery current I_B. Before the compensations starts (before time moment t1), the current of Battery I_B includes DC-component (I_B=130A) and second order component with an amplitude I_{2AC} = 60A. Starting from the time moment t1, the supercapacitor module starts generating supercapacitor current I_{SC}, redirecting the second order harmonic of current I_B to the supercapacitor (see Figure 20B). This current I_{SC} has amplitude of main harmonic equal to that of second order harmonic of I_{DC} current (see Figure 19), but with nearly opposite phase angle, in such a way that the resulting current in battery I_B includes either DC-component only or mostly DC-component with some significantly reduced AC-ripples, as shown in Figure 20A.

[0094] At high RPMs a second-order current harmonic is suppressed significantly by filtering capacitor C_F and operation of supercapacitor module is not required.

[0095] Figure 21 shows the single-phase nine-level four-quadrant intelligent battery pack connected to a single-phase load, which is presented as RL-load. This system can be used for residential or commercial buildings energy storage and interruptible power supply systems.

[0096] Figure 22 shows the three-phase intelligent battery pack comprising three nine-level two quadrant single-phase intellectual battery packs connected to three-phase Switched-Reluctance Motor (SRM). A usage of multi-level hysteresis current controller and intelligent battery pack allows improving efficiency and overall performance of SRM, as well as significant reduction of torque ripples and acoustic noise.

[0097] In the foregoing description, numerous specific details are given to provide a thorough understanding of the present embodiments. However, it will be apparent that the present embodiments may be practiced without these specific details. In order to increase clarity, some well-known circuits, system configurations, and process steps may not be described in detail. In other instances, structures and devices are shown in a block diagram form in order to avoid obscuring the invention.

[0098] The drawings showing embodiments of the present disclosure are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown exaggerated in the drawing Figures.

[0099] Reference in the foregoing description to "one embodiment" or "an embodiment" or "certain embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[00100] Some portions of the detailed description are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the methods used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. An algorithm is here, and generally, conceived to be a self- consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared or otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers or the like.

[00101] It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following disclosure, it is appreciated that throughout the disclosure terms such as "processing," "computing," "calculating," "determining," "displaying" or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system's memories or registers or other such information storage, transmission or display devices.

[00102] The present embodiments also relate to an apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, or it may be a general-purpose computer selectively activated or reconfigured by a computer program stored in the computer. The present embodiments may take the form of an entirely hardware embodiment, an entirely software embodiment or an embodiment including both hardware and software elements. In one embodiment, the present embodiments are implemented in software comprising

instructions or data stored on a computer-readable storage medium, which includes but is not limited to firmware, resident software, microcode or another method for storing instructions for execution by a processor.

[00103] Furthermore, the present embodiments may take the form of a computer program product accessible from a computer-usable or computer-readable storage medium providing program code for use by, or in connection with, a computer or any instruction execution system. For the purposes of this description, a computer-usable or computer readable storage medium is any apparatus that can contain, store or transport the program for use by or in connection with the instruction execution system, apparatus or device. The computer-readable storage medium can be an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system (or apparatus or device) or a propagation medium. Examples of a tangible computer-readable storage medium include, but are not limited to, a semiconductor or solid state memory, magnetic tape, a removable computer diskette, a random access memory (RAM), a read-only memory (ROM), a rigid magnetic disk, an optical disk, an EPROM, an EEPROM, a magnetic card or an optical card, or any type of computer-readable storage medium suitable for storing electronic instructions, and each coupled to a computer system bus. Examples of optical disks include compact disk – read only memory (CD-ROM), compact disk – read/write (CD-R/W) and digital video disc (DVD).

[00104] To the extent the embodiments disclosed herein include or operate in association with memory, storage, and/or computer readable media, then that memory, storage, and/or computer readable media are non-transitory. Accordingly, to the extent that memory, storage, and/or computer readable media are covered by one or more claims, then that memory, storage, and/or computer readable media is only non-transitory. The terms "non-transitory" and "tangible" as used herein, are intended to describe memory, storage, and/or computer readable media excluding propagating electromagnetic signals, but are not intended to limit the type of memory, storage, and/or computer readable media in terms of the persistency of storage or otherwise. For example, "non-transitory" and/or "tangible" memory, storage, and/or computer readable media encompasses volatile and non-volatile media such as random access media (e.g., RAM, SRAM, DRAM, FRAM, etc.), read-only media (e.g., ROM, PROM, EPROM, EEPROM, flash, etc.) and combinations thereof (e.g., hybrid RAM and ROM, NVRAM, etc.) and later-developed variants thereof.

[00105] A data processing system suitable for storing and/or executing program code includes at least one processor coupled directly or indirectly to memory elements through a system bus. The memory elements may include local memory employed during actual execution of the program code, bulk storage and cache memories providing temporary storage of at least some program

code in order to reduce the number of times code must be retrieved from bulk storage during execution. In some embodiments, input/output (I/O) devices (such as keyboards, displays, pointing devices or other devices configured to receive data or to present data) are coupled to the system either directly or through intervening I/O controllers.

[00106] Network adapters may also be coupled to the data processing system to allow coupling to other data processing systems or remote printers or storage devices through intervening private or public networks. Modems, cable modem and Ethernet cards are just examples of the currently available types of network adapters.

[00107] Finally, the methods and displays presented herein are not inherently related to any particular computer or other apparatus. Various general-purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these systems will appear from the description below. It will be appreciated that a variety of programming languages may be used to implement the teachings of the invention as described herein.

[00108] The figures and the detailed description describe certain embodiments by way of illustration only. One skilled in the art will readily recognize from the foregoing description that alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles described herein. Reference will now be made in detail to several embodiments, examples of which are illustrated in the accompanying figures. It is noted that wherever practicable similar or like reference numbers may be used in the figures to indicate similar or like functionality.

[00109] Embodiments of the present disclosure are directed to a converter-battery module architecture for an intelligent battery (iBattery) module used as a building unit of an intelligent battery pack or system of intelligent battery packs. In embodiments, the iBattery module comprises a battery unit, a supercapacitor or ultra-capacitor module unit and an output converter unit. In embodiments, a local control unit of the iBattery module is configured to accept, process, and transmit signals, including, but not limited to, from temperature, voltage and current sensors, and the like, of the iBattery module; triggering and faults signals to and from semiconductor switches; voltages of elementary cells of the battery units and the supercapacitor modules. In embodiments, the local control system performs a communication with and transmission of corresponding control signals to and from a master control unit of an intelligent alternating-current battery pack (ACi-Battery Pack) comprising a plurality of iBattery modules.

[00110] Embodiments of the present disclosure are directed to an intelligent alternating-current battery pack (ACi-Battery Pack) comprising two or more iBattery modules interconnected together in each phase. In embodiments, the output voltage of any shape and frequency can be generated at the outputs of ACi-Battery Pack as a superposition of output voltages of individual iBattery modules.

[00111] Embodiments of the present disclosure are directed to a method of multi-level current hysteresis control to control the ACi-Battery Pack to provide SOC and balancing between iBatteries in ACi-Battery Pack. In embodiments, the method enables power sharing among all iBattery modules in ACi-Battery Pack. In embodiments, the power sharing among all iBattery modules can be used to keep the SOCs of the battery modules of iBatteries balanced at all times during operation, which ensures that the full capacity of each module is utilized regardless of possible differences in the capacities.

[00112] Embodiments of the present disclosure are directed to processes, methodologies and systems described herein relate to a motor vehicle and a stationary energy storage system.

[00113] Embodiments of the present disclosure are directed to an electric vehicle having a chassis, three or more wheels operably coupled to the chassis, one or more electric motors operably coupled to the three or more wheels, one or more intelligent modular battery packs operably coupled to the one or more motors, and a control system operably coupled to the one or more battery packs and the one or more motors.

[00114] In embodiments, the chassis is drivetrain-less. In embodiments, the one or more motors are in-wheel motors.

[00115] In embodiments, the one or more intelligent modular battery packs having a cascaded interconnected architecture.

[00116] In embodiments, the battery packs comprise a plurality of interconnected intelligent battery modules.

[00117] In embodiments, the battery modules comprise an integrated combination of a networked low voltage converter/controller with peer-to-peer communication capability, embedded ultra-capacitor or super-capacitor, a battery management system, and serially connected set of individual cells.

[00118] In embodiments, the battery packs comprise a neural network comprising a plurality of interconnected intelligent battery modules.

[00119] In embodiments, the battery modules comprise an integrated combination of a battery with a BMS, a supercapacitor module, and an output converter.

[00120] In embodiments, the supercapacitor module includes a bidirectional DC-DC converter and a supercapacitor bank.

[00121] In embodiments, the output converter comprises a four-quadrant H-bridge.

[00122] In embodiments, the control system comprises a bi-directional multilevel controller.

[00123] In embodiments, the bi-directional multilevel controller is a bi-directional multilevel hysteresis controller.

[00124] In embodiments, the bi-directional multilevel controller is combined with temperature sensors and networking interface logic.

[00125] In embodiments, the control system is configured to balance battery utilization through individual switching of modules based on module age, thermal condition and performance characteristics.

[00126] In embodiments, the battery packs are switchable to a rectifier/charger operation.

[00127] Embodiments of the present disclosure are directed to an intelligent modular battery pack comprising a cascaded architecture comprising a plurality of inter-connected intelligent battery modules.

[00128] In embodiments, the battery modules comprise an integrated combination of a networked low voltage converter/controller with peer-to-peer communication capability, embedded ultra-capacitor, battery management system and serially connected set of individual cells.

[00129] In embodiments, the inter-connected intelligent battery modules comprise a neural network.

[00130] In embodiments, the battery modules comprise an integrated combination of a battery with a BMS, a supercapacitor module, and an output converter.

[00131] In embodiments, the supercapacitor module includes a bidirectional DC-DC converter and a supercapacitor bank.

[00132] In embodiments, the output converter comprises a four-quadrant H-bridge.

[00133] Embodiments of the present disclosure are directed to an intelligent battery module comprising an integrated low voltage converter/controller with peer-to-peer communication capability, an embedded ultra-capacitor, a battery management system, and a plurality of serially connected set of individual cells.

[00134] Embodiments of the present disclosure are directed to an intelligent battery module comprising a battery with an integrated BMS, a supercapacitor module operably coupled to the battery, and an output converter operably coupled to the battery and the supercapacitor module.

[00135] In embodiments, the supercapacitor module includes a bidirectional DC-DC converter and a supercapacitor bank.

[00136] In embodiments, the output converter comprises a four-quadrant H-bridge.

[00137] All features, elements, components, functions, and steps described with respect to any embodiment provided herein are intended to be freely combinable and substitutable with those from any other embodiment. If a certain feature, element, component, function, or step is described with respect to only one embodiment, then it should be understood that that feature, element, component, function, or step can be used with every other embodiment described herein unless explicitly stated otherwise. This paragraph therefore serves as antecedent basis and written support for the introduction of claims, at any time, that combine features, elements, components, functions, and steps from different embodiments, or that substitute features, elements, components, functions, and steps from one embodiment with those of another, even if the following description does not explicitly state, in a particular instance, that such combinations or substitutions are possible. Express recitation of every possible combination and substitution is overly burdensome, especially given that the permissibility of each and every such combination and substitution will be readily recognized by those of ordinary skill in the art upon reading this description.

[00138] In many instances, entities are described herein as being coupled to other entities. It should be understood that the terms "coupled" and "connected" or any of their forms are used interchangeably herein and, in both cases, are generic to the direct coupling of two entities without any non-negligible e.g., parasitic intervening entities and the indirect coupling of two entities with one or more non-negligible intervening entities. Where entities are shown as being directly coupled together, or described as coupled together without description of any intervening entity, it should be understood that those entities can be indirectly coupled together as well unless the context clearly dictates otherwise.

[00139] While the embodiments are susceptible to various modifications and alternative forms, specific examples thereof have been shown in the drawings and are herein described in detail. It should be understood, however, that these embodiments are not to be limited to the particular form disclosed, but to the contrary, these embodiments are to cover all modifications, equivalents, and alternatives falling within the spirit of the disclosure. Furthermore, any features, functions, steps, or elements of the embodiments may be recited in or added to the claims, as well as negative limitations that define the inventive scope of the claims by features, functions, steps, or elements that are not within that scope.

What is claimed is:

1. An electric vehicle comprising:

a chassis,

three or more wheels operably coupled to the chassis,

one or more electric motors operably coupled to the three or more wheels,

one or more intelligent modular battery packs operably coupled to the one or more motors, and

a control system operably coupled to the one or more battery packs and the one or more motors.

2. The electric vehicle of claim 1 wherein the chassis is drivetrain-less.

3. The electric vehicle of claim 1 wherein the one or more motors are in-wheel motors.

4. The electric vehicle of claim 1 wherein the one or more intelligent modular battery packs having a cascaded architecture.

5. The electric vehicle of claim 4 wherein the battery packs comprise a plurality of interconnected intelligent battery modules.

6. The electric vehicle of claim 5 wherein the battery modules comprise an integrated combination of a networked low voltage converter/controller with peer-to-peer communication capability, embedded ultra-capacitor, battery management system and serially connected set of individual cells.

7. The electric vehicle of claim 1 wherein the battery packs comprise a neural network comprising a plurality of inter-connected intelligent battery modules.

8. The electric vehicle of claim 5 wherein the battery modules comprise an integrated combination of a battery with a BMS, a supercapacitor module, and an output converter.

9. The electric vehicle of claim 8 wherein the supercapacitor module includes a bidirectional DC-DC converter and a supercapacitor bank.

10. The electric vehicle of claim 8 wherein the output converter comprises a four-quadrant H-bridge.

11. The electric vehicle of claim 1 wherein the control system comprises a bi-directional multilevel controller.

12. The electric vehicle of claim 11, wherein the bi-directional multilevel controller is a bi-directional multilevel hysteresis controller.

13. The electric vehicle of claim 11, wherein the bi-directional multilevel controller is combined with temperature sensors and networking interface logic.

14. The electric vehicle of claims 11-13, wherein the control system is configured to balance battery utilization through individual switching of modules based on module age, thermal condition and performance characteristics.

15. The electric vehicle of claims 1-14, wherein the battery packs are switchable to a rectifier/charger operation.

16. An intelligent modular battery pack comprising a cascaded architecture comprising a plurality of inter-connected intelligent battery modules.

17. The intelligent modular battery pack of claim 16 wherein the battery modules comprise an integrated combination of a networked low voltage converter/controller with peer-to-peer communication capability, embedded ultra-capacitor, battery management system and serially connected set of individual cells.

18. The intelligent modular battery pack of claim 16 wherein the inter-connected intelligent battery modules comprise a neural network.

19. The intelligent modular battery pack of claim 16 wherein the battery modules comprise an integrated combination of a battery with a BMS, a supercapacitor module, and an output converter.

20. The intelligent modular battery pack of claim 19 wherein the supercapacitor module includes a bidirectional DC-DC converter and a supercapacitor bank.

21. The intelligent modular battery pack of claim 19 wherein the output converter comprises a four-quadrant H-bridge.

22. An intelligent battery module comprising an integrated low voltage converter/controller with peer-to-peer communication capability, an embedded ultra-capacitor, a battery management system, and a plurality of serially connected set of individual cells.

23. The intelligent battery module of claim 22, wherein the converter/controller comprises a four-quadrant H-bridge.

24. An intelligent battery module comprising
a battery with an integrated BMS,
a supercapacitor module operably coupled to the battery, and
an output converter operably coupled to the battery and the supercapacitor module.

25. The intelligent battery module of claim 24 wherein the supercapacitor module includes a bidirectional DC-DC converter and a supercapacitor bank.

26. The intelligent battery module of claim 24 wherein the output converter comprises a four-quadrant H-bridge.

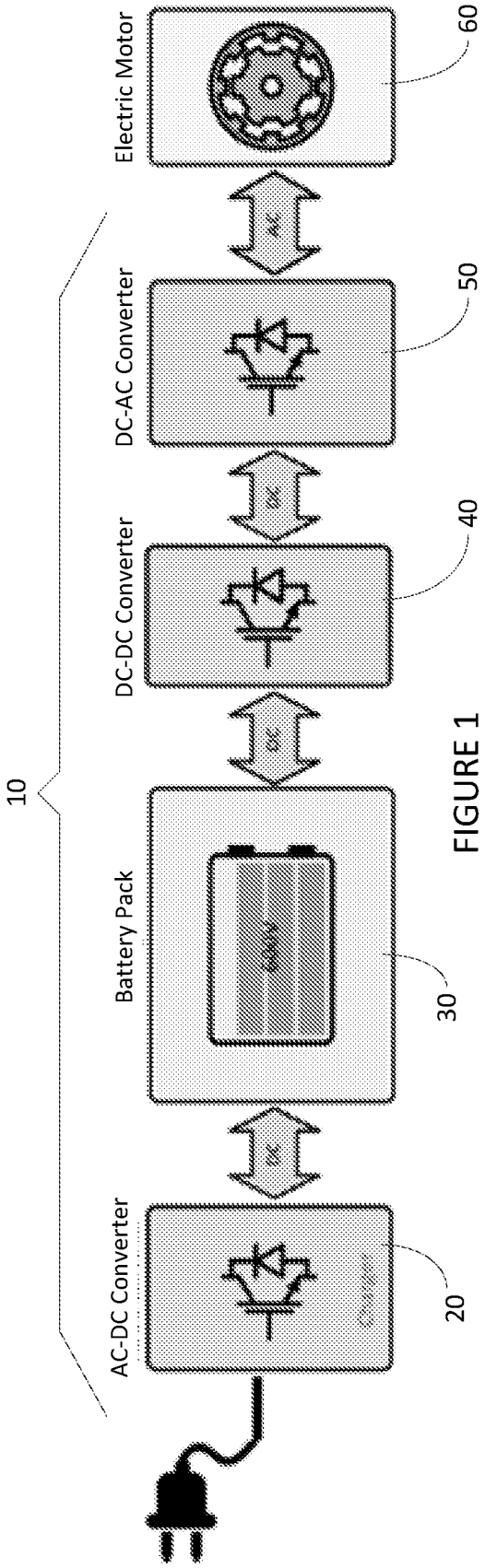


FIGURE 1

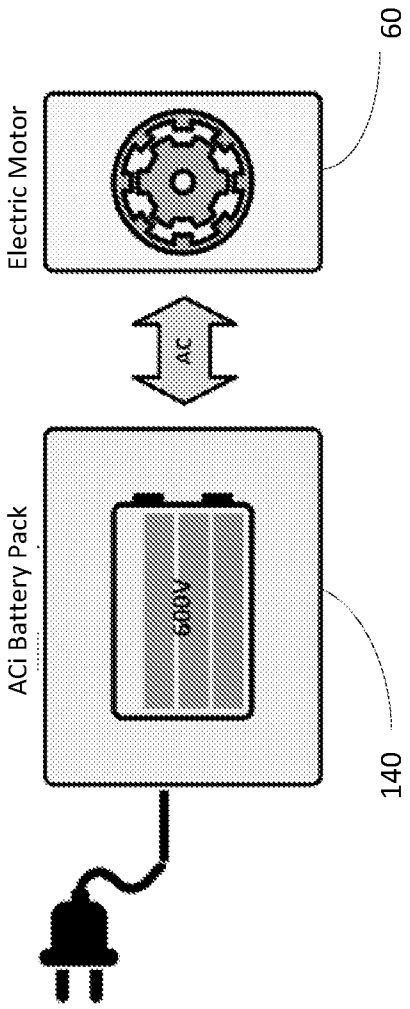


FIGURE 2

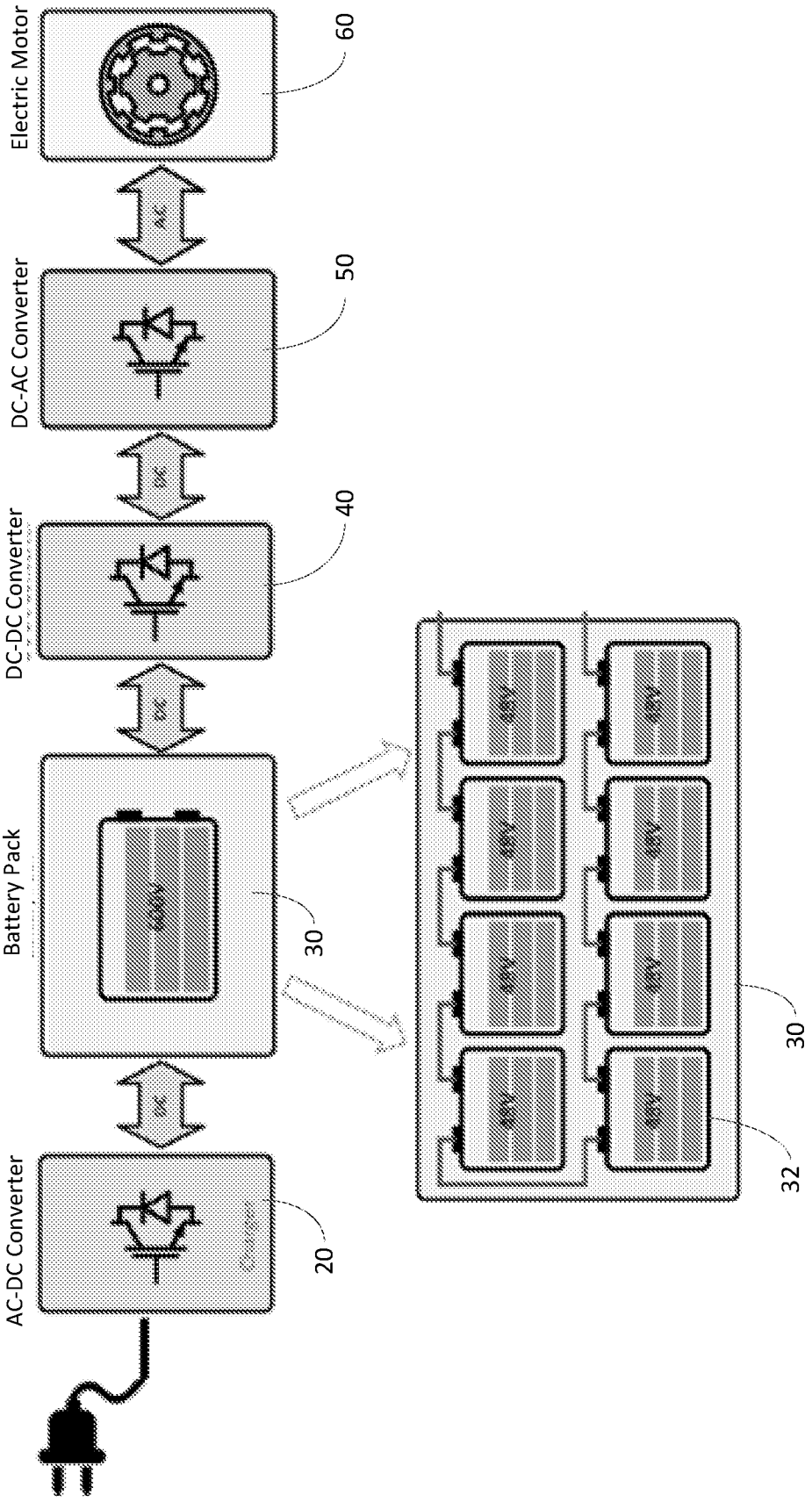

Electric Motor
60
AC
DC-AC Converter
50
DC
DC-DC Converter
40
DC
Battery Pack
30
DC
AC-DC Converter
20
30
32

FIGURE 3A

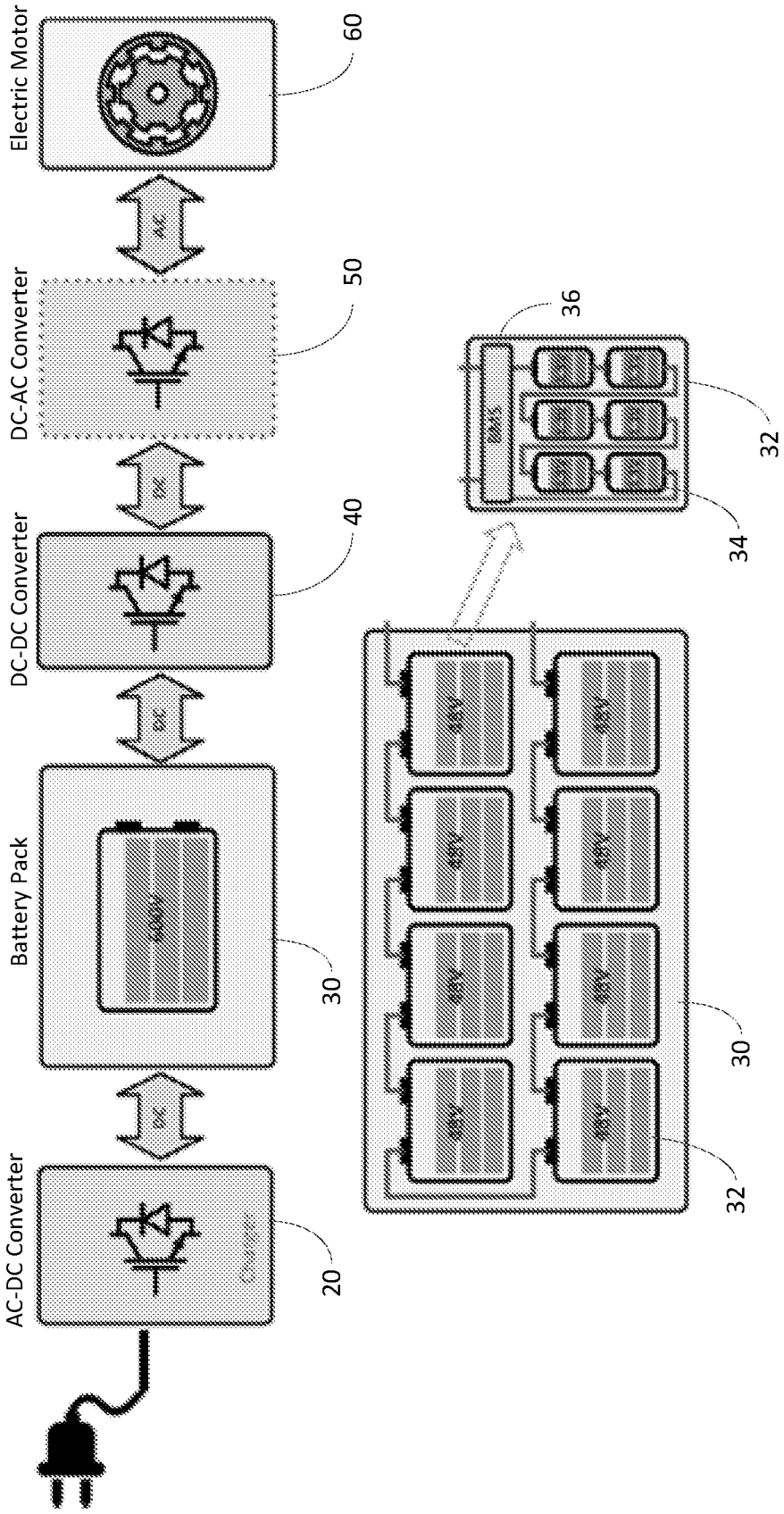

Electric Motor
60
AC
DC-AC Converter
50
DC
DC-DC Converter
40
DC
Battery Pack
30
AC
AC-DC Converter
20
36
32
34
30
32
48V

FIGURE 3B

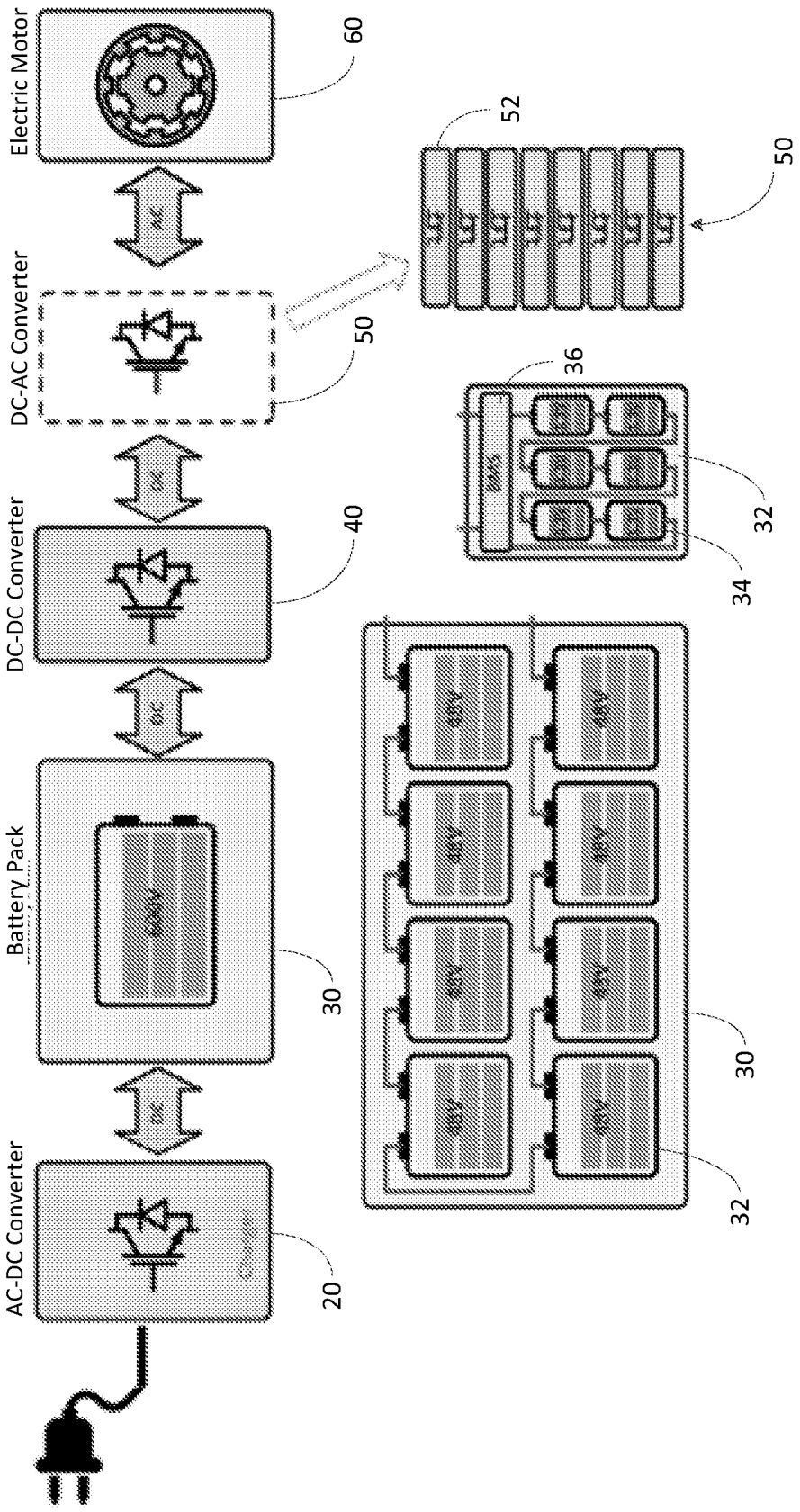

AC-DC Converter
Battery Pack
DC-DC Converter
DC-AC Converter
Electric Motor
20
30
40
50
60
52
36
32
34

FIGURE 3C

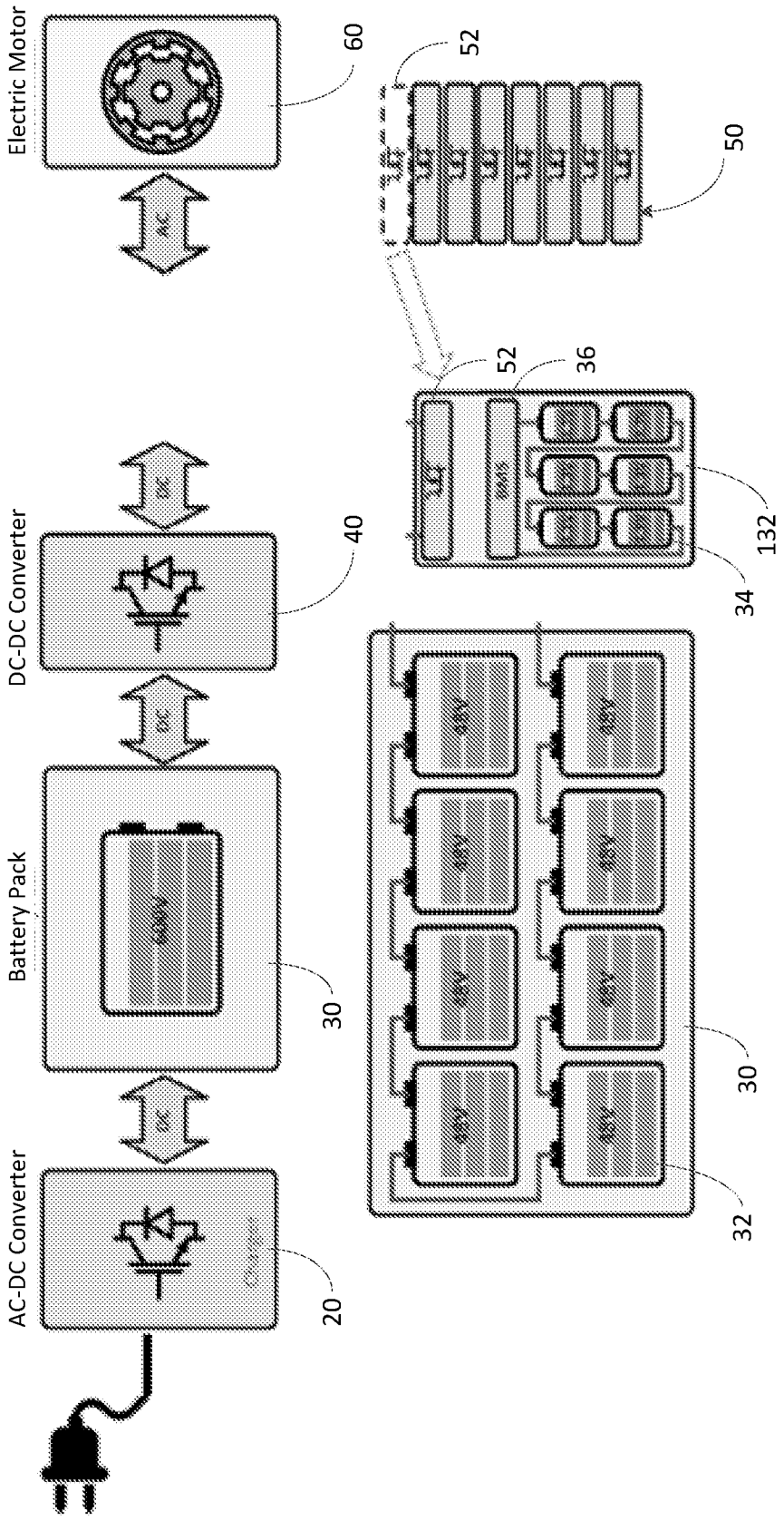

Electric Motor
60
52
50
52
36
132
34
DC-DC Converter
40
Battery Pack
30
AC-DC Converter
20
30
32

FIGURE 3D

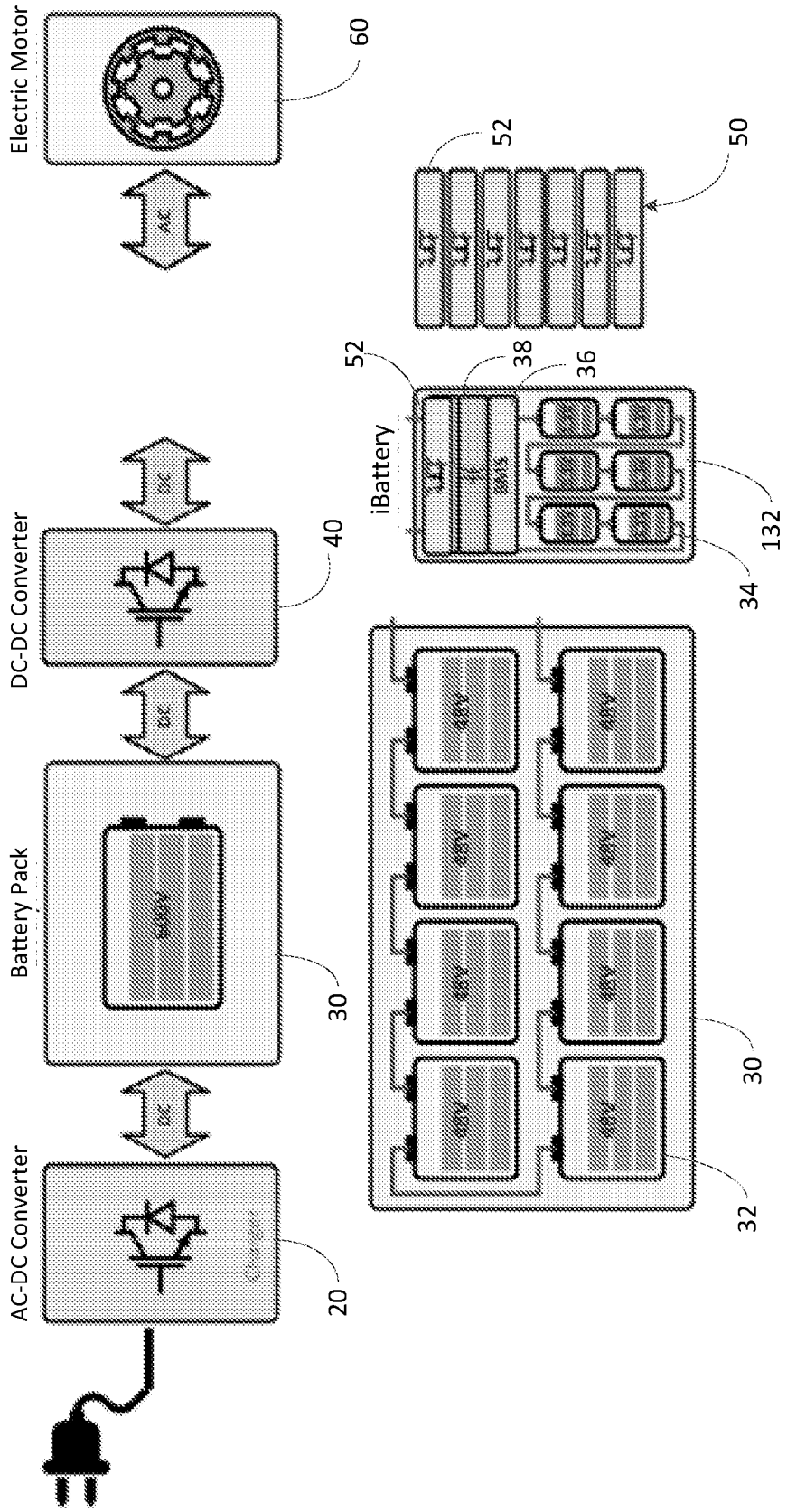

Electric Motor
60
AC
52
50
52
38
36
iBattery
132
34
DC
DC-DC Converter
40
DC
Battery Pack
30
DC
AC-DC Converter
20
30
32

FIGURE 3E

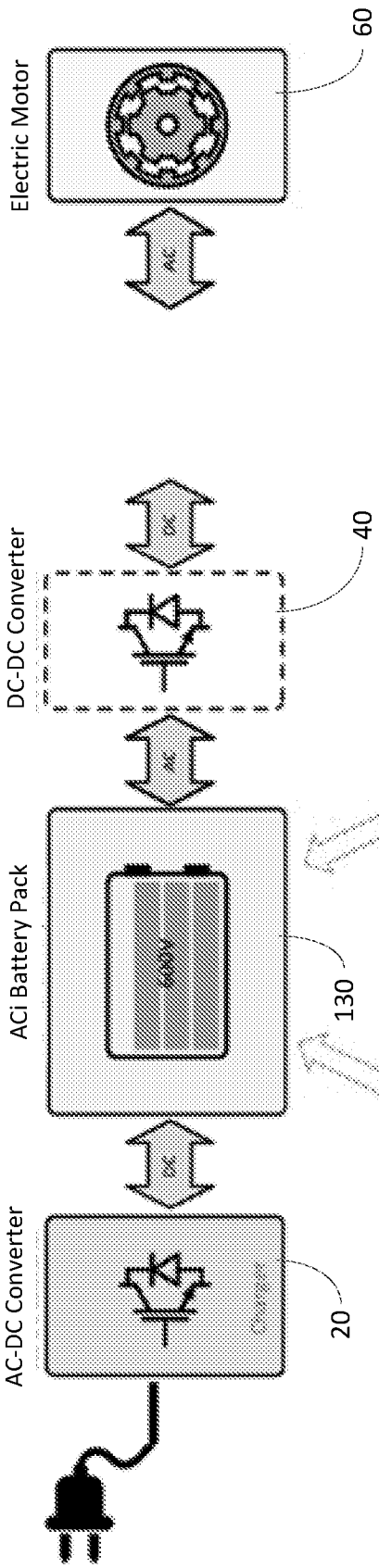


FIGURE 3F

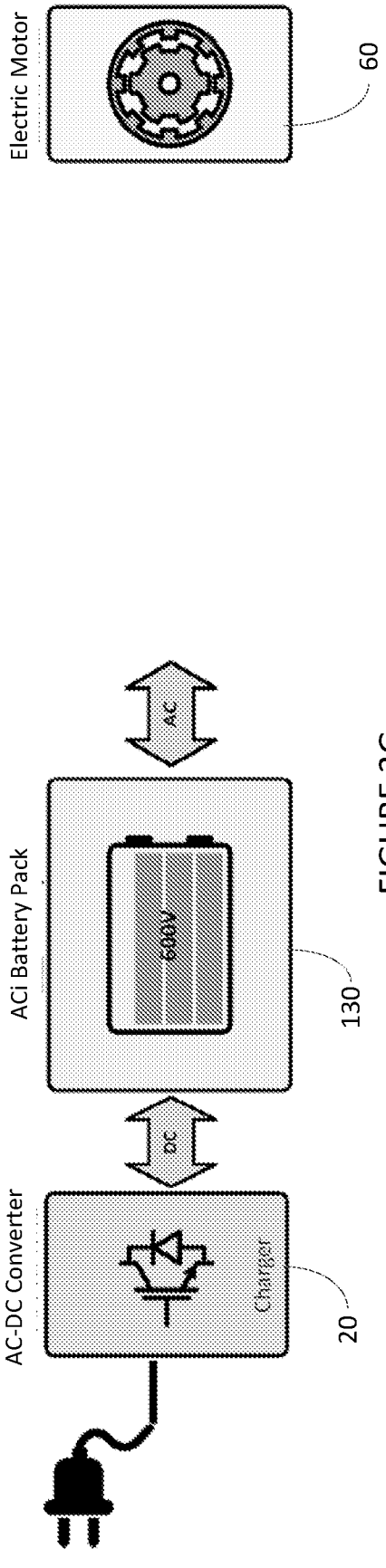


FIGURE 3G

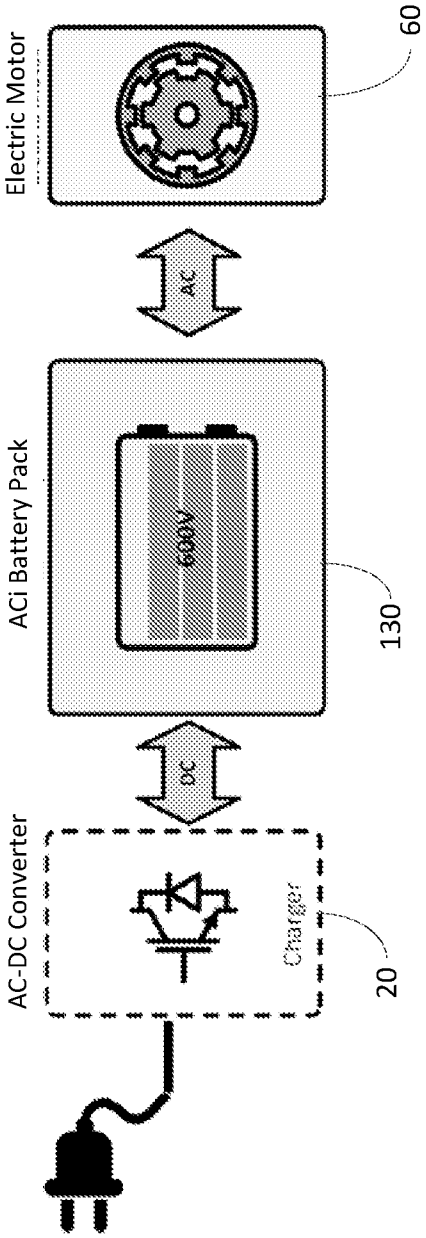


FIGURE 3H

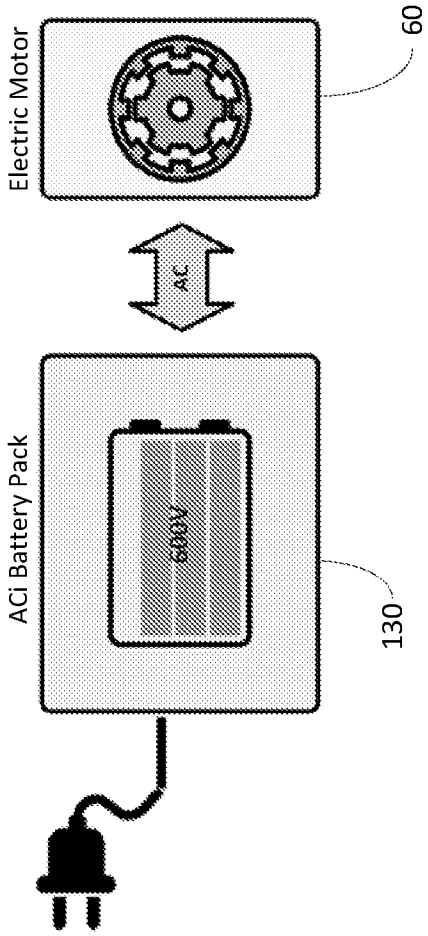


FIGURE 3I

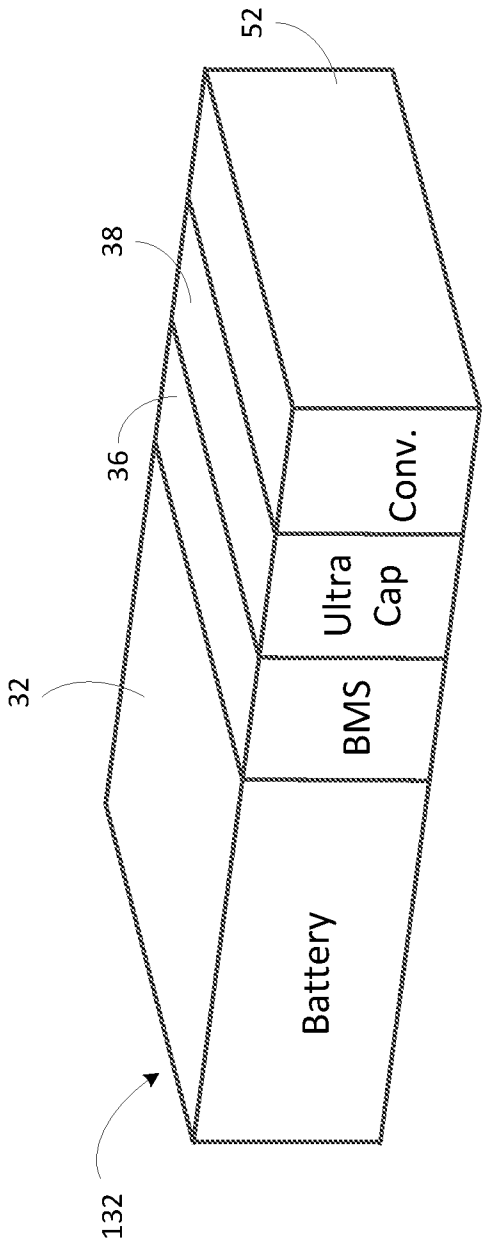


FIGURE 4

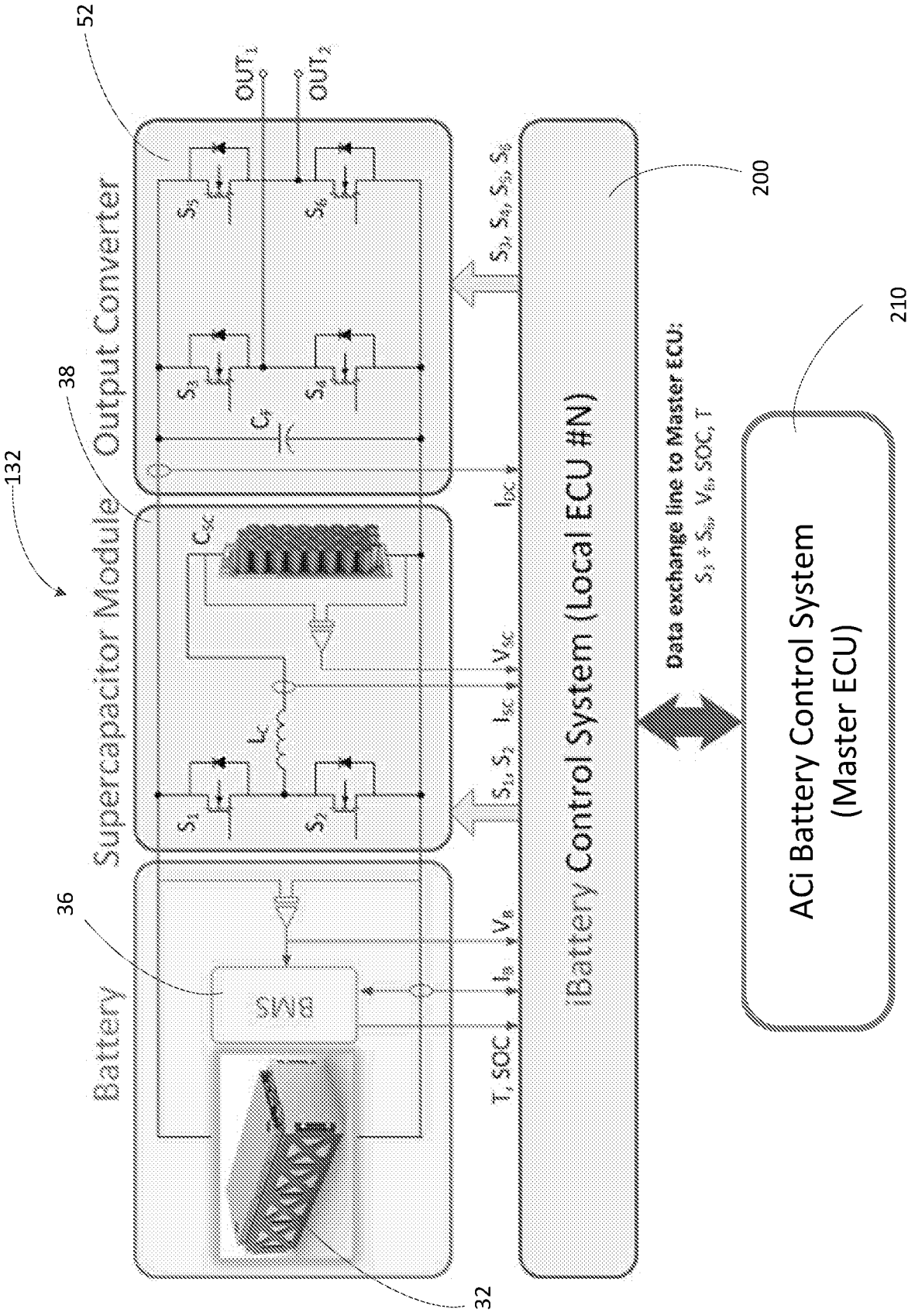

132
52
38
36
32
200
210
Supercapacitor Module Output Converter
Battery
BMS
iBattery Control System (Local ECU #N)
ACi Battery Control System
(Master ECU)
Data exchange line to Master ECU:
$S_1 \div S_6$, V_B, SOC, T
OUT_1
OUT_2
C_F
C_{SC}
L_F
S_1
S_2
S_3
S_4
S_5
S_6
I_{DC}
V_{SC}
I_{SC}
V_B
I_B
T, SOC

FIGURE 5

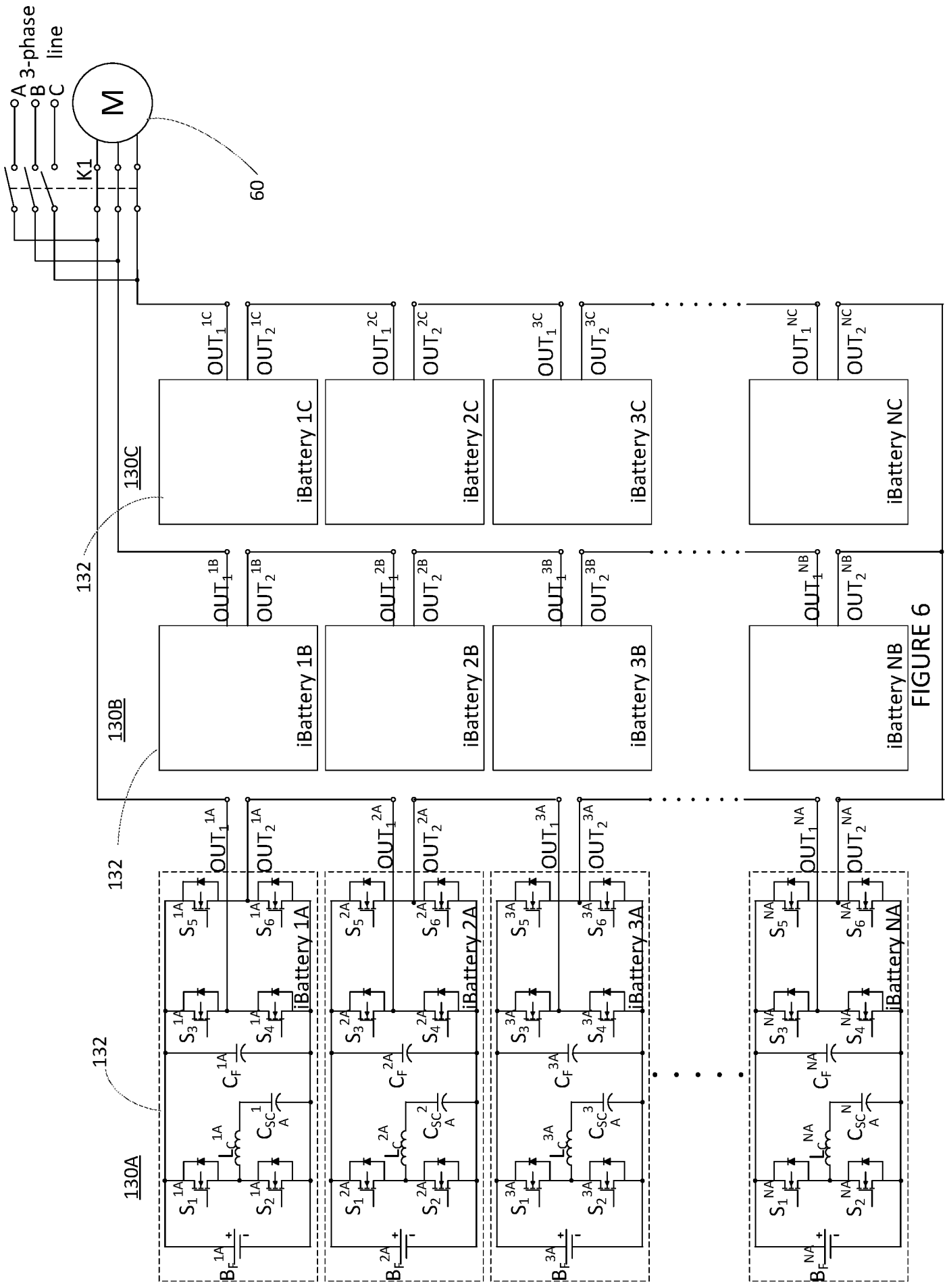

A
B
C
3-phase line
M
K1
60
132
130C
130B
130A
iBattery 1C
iBattery 2C
iBattery 3C
iBattery NC
iBattery 1B
iBattery 2B
iBattery 3B
iBattery NB
iBattery 1A
iBattery 2A
iBattery 3A
iBattery NA

FIGURE 6

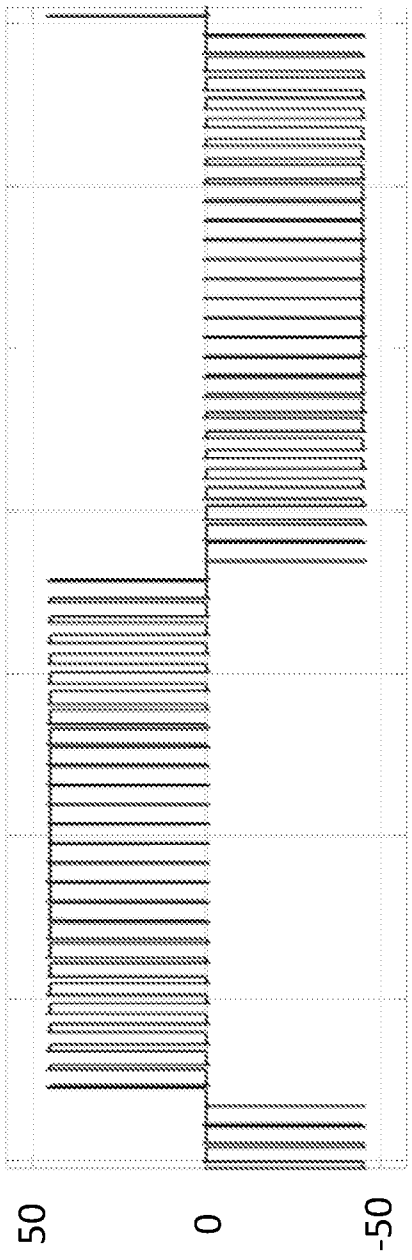


FIGURE 7A

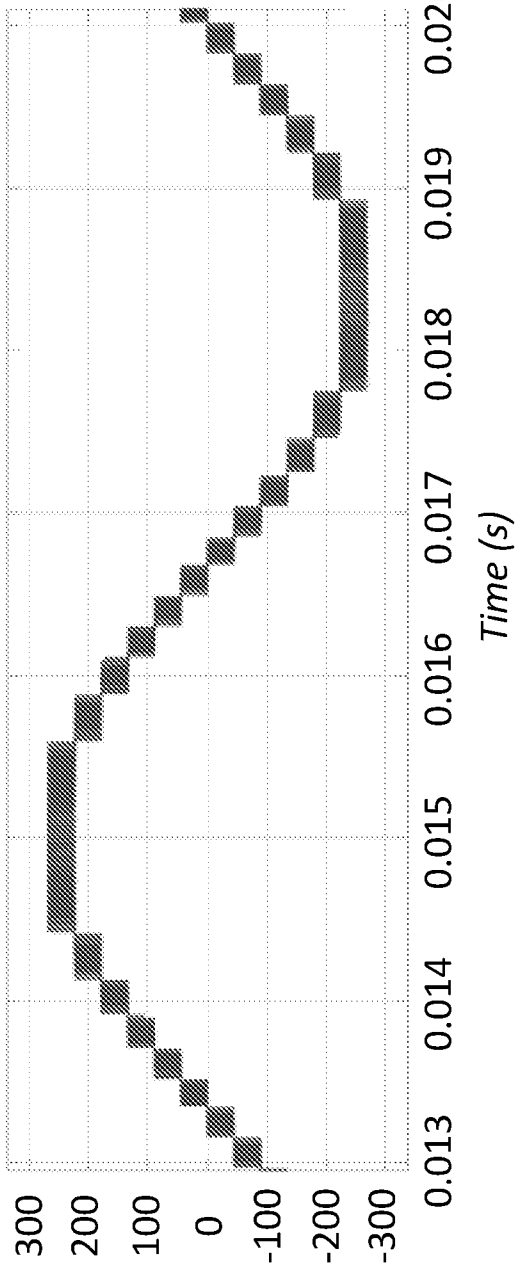


FIGURE 7B

FIGURE 8A

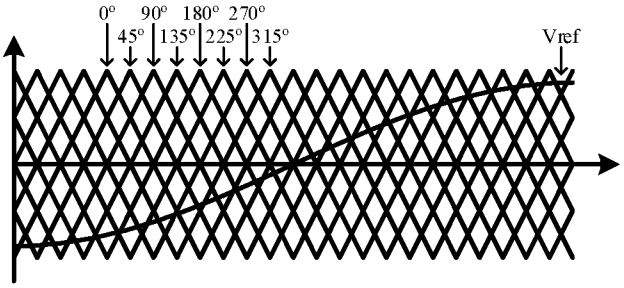


FIGURE 8B

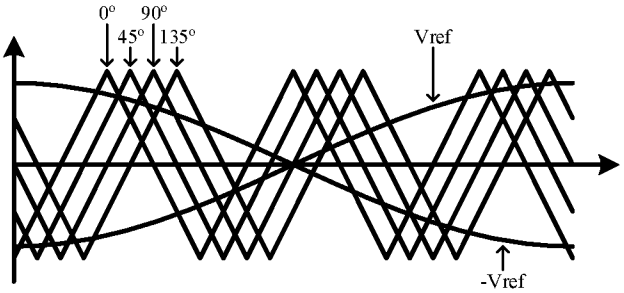


FIGURE 8C

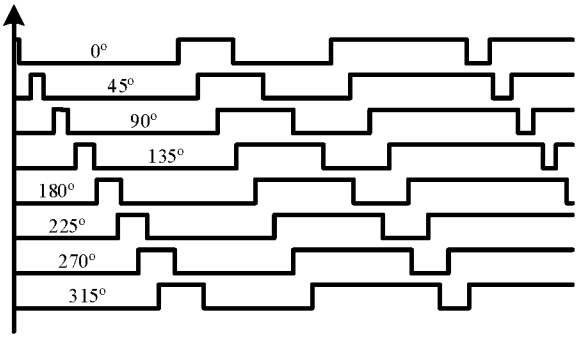
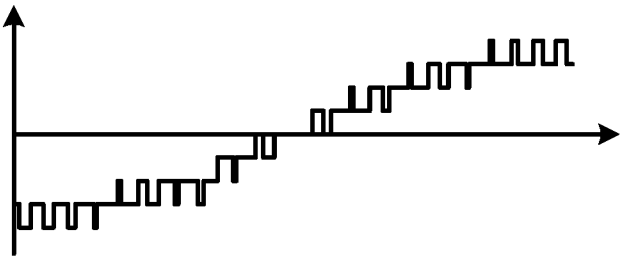


FIGURE 8D



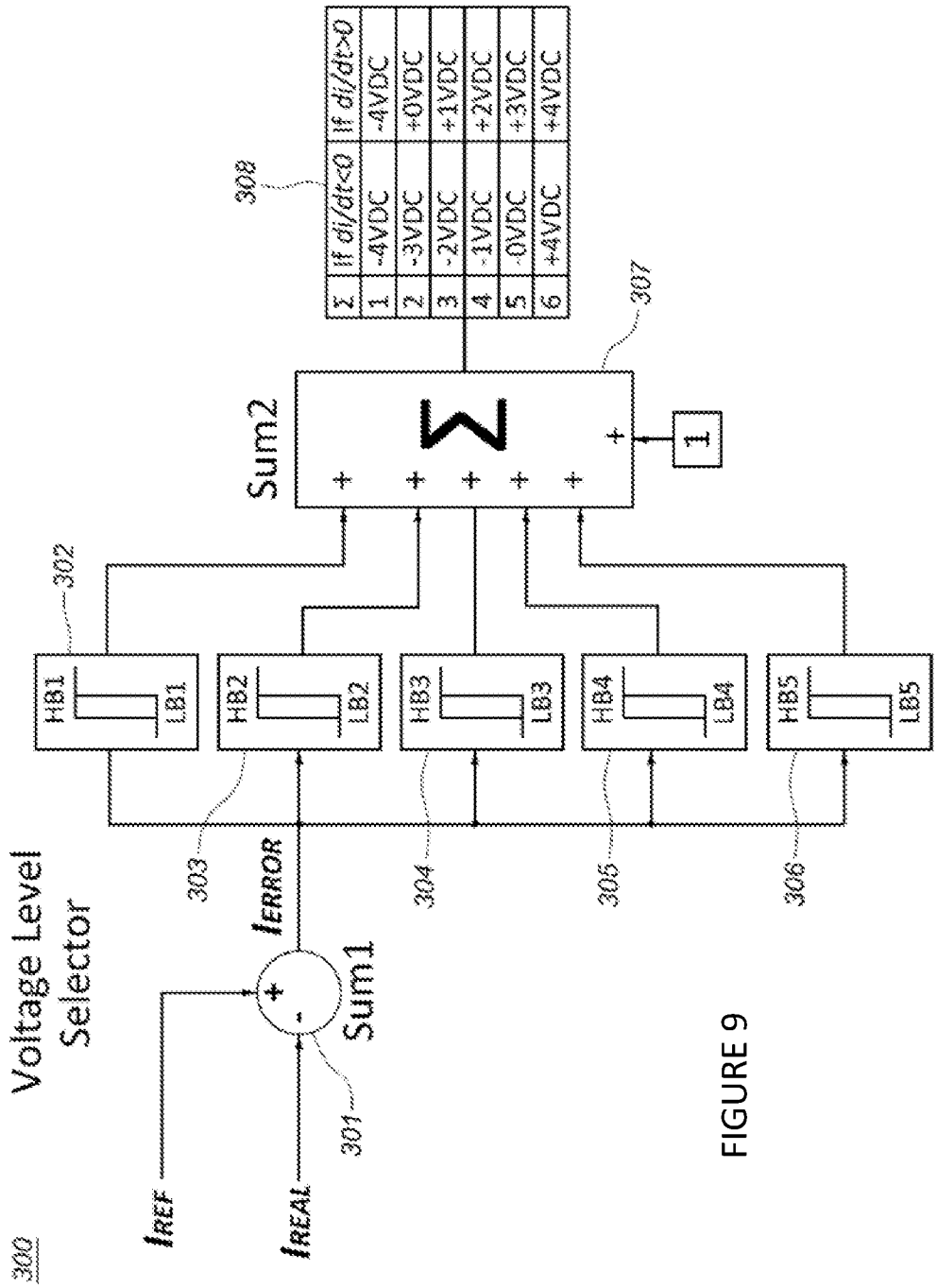

300
Voltage Level Selector
Sum1
Sum2
IREF
IREAL
IERROR
301
302
303
304
305
306
307
308
HB1
LB1
HB2
LB2
HB3
LB3
HB4
LB4
HB5
LB5
1
Σ | If di/dt<0 | If di/dt>0
1 | -4VDC | -4VDC
2 | -3VDC | +0VDC
3 | -2VDC | +1VDC
4 | -1VDC | +2VDC
5 | -0VDC | +3VDC
6 | +4VDC | +4VDC

FIGURE 9

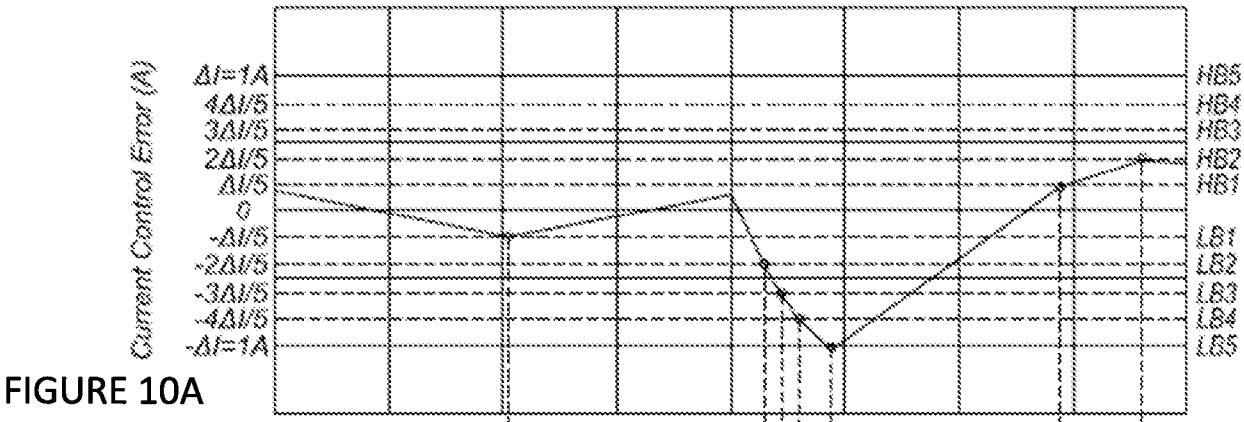


FIGURE 10A

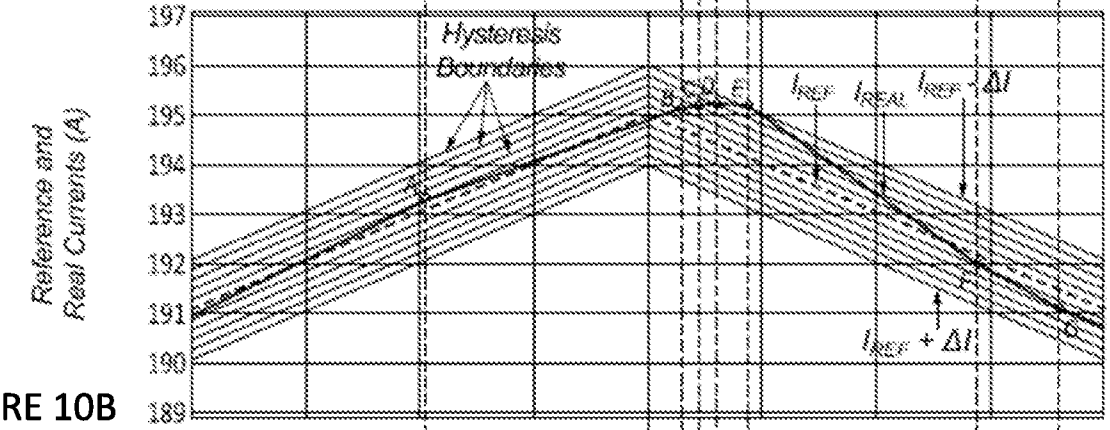


FIGURE 10B

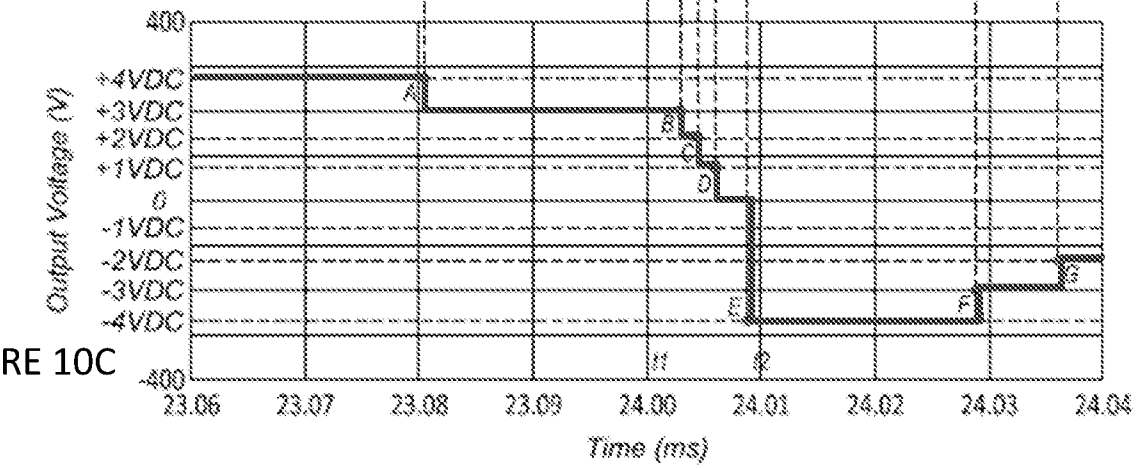


FIGURE 10C

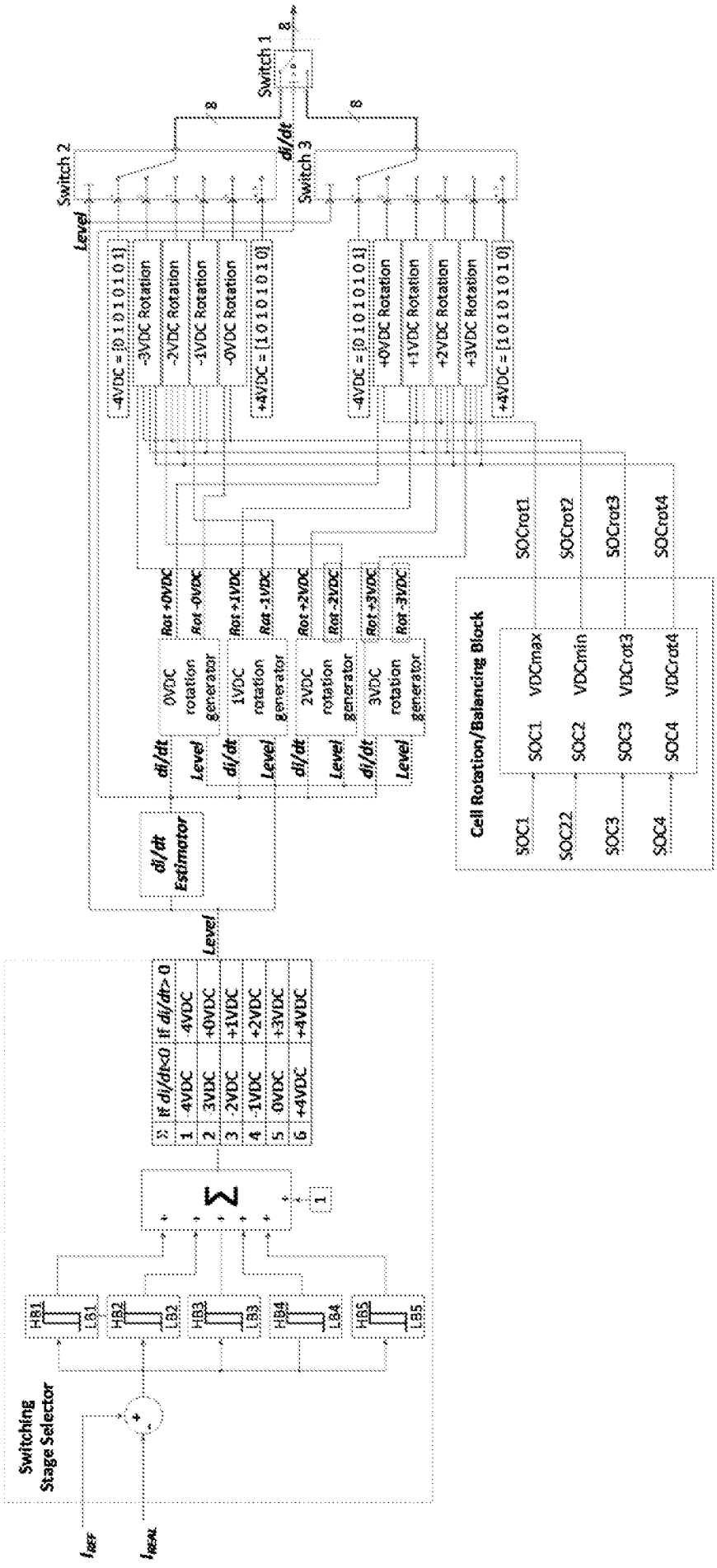

Switching Stage Selector
HB1
HB2
HB3
HB4
HB5
LB1
LB2
LB3
LB4
LB5
Σ
1
Level
di/dt
Estimator
0VDC rotation generator
1VDC rotation generator
2VDC rotation generator
3VDC rotation generator
Rot +0VDC
Rot -0VDC
Rot +1VDC
Rot -1VDC
Rot +2VDC
Rot -2VDC
Rot +3VDC
Rot -3VDC
Switch 1
Switch 2
Switch 3
-4VDC = [0 1 0 1 0 1 0 1]
-3VDC Rotation
-2VDC Rotation
-1VDC Rotation
-0VDC Rotation
+4VDC = [1 0 1 0 1 0 1 0]
+0VDC Rotation
+1VDC Rotation
+2VDC Rotation
+3VDC Rotation
Cell Rotation/Balancing Block
SOC1
SOC2
SOC3
SOC4
VDCmax
VDCmin
VDCrot3
VDCrot4
SOCrot1
SOCrot2
SOCrot3
SOCrot4
Σ
If di/dt<0
If di/dt> 0
-4VDC
+0VDC
+1VDC
+2VDC
+3VDC
+4VDC
-3VDC
-2VDC
-1VDC
0VDC
IREF
IREAL

FIGURE 11

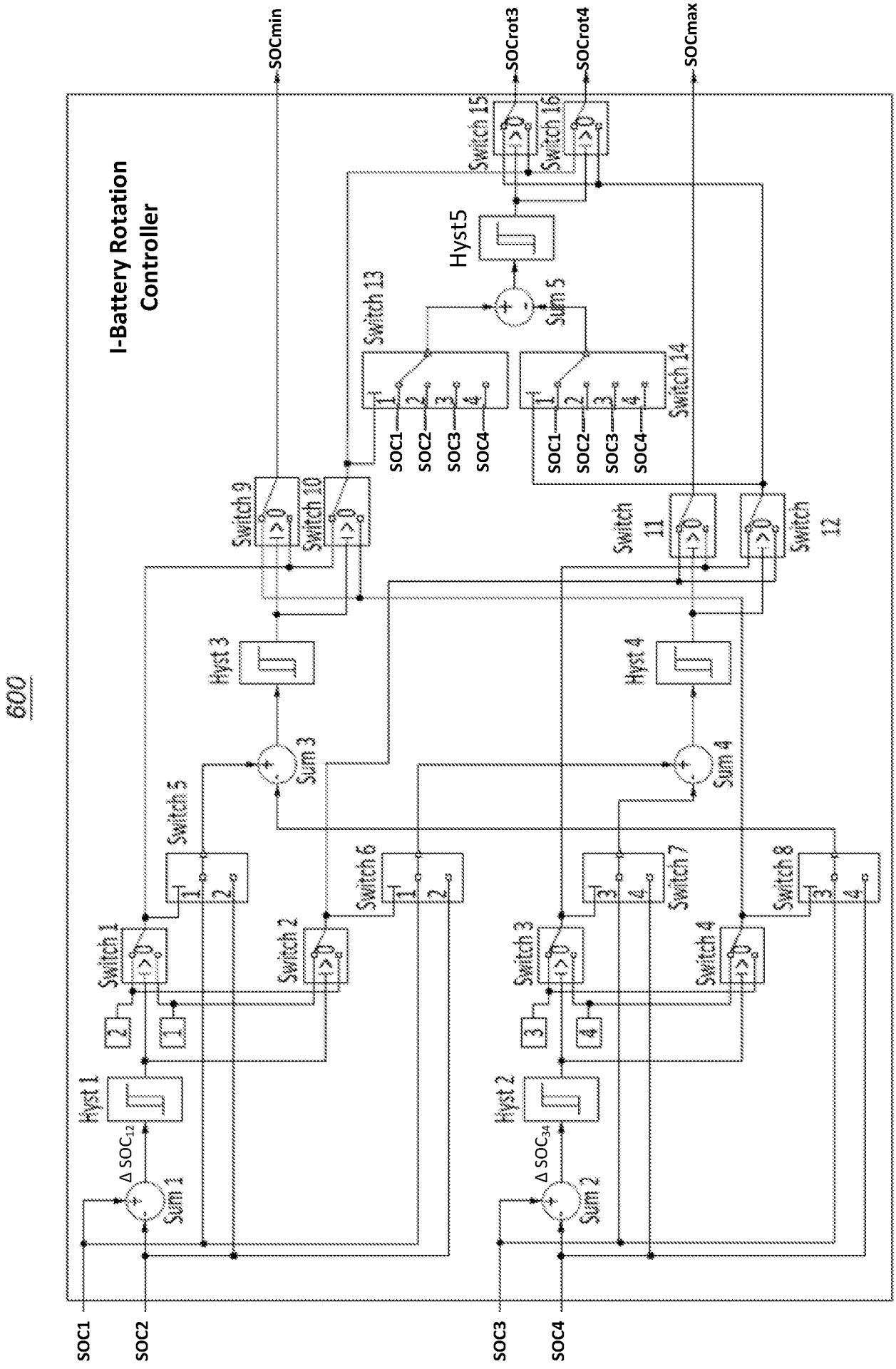

600
I-Battery Rotation Controller
SOCmin
SOCrot3
SOCrot4
SOCmax
Switch 15
Switch 16
Hyst5
Sum 5
Switch 13
Switch 14
SOC1
SOC2
SOC3
SOC4
Switch 9
Switch 10
Switch 11
Switch 12
Hyst 3
Hyst 4
Sum 3
Sum 4
Switch 5
Switch 6
Switch 7
Switch 8
Switch 1
Switch 2
Switch 3
Switch 4
Hyst 1
Hyst 2
Δ SOC12
Δ SOC34
Sum 1
Sum 2

FIGURE 12

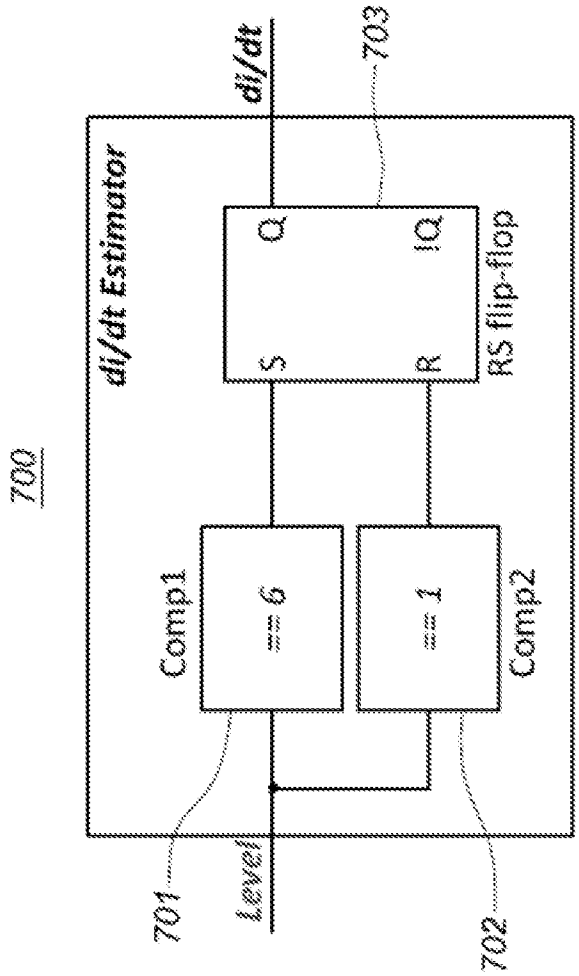

700
di/dt Estimator
di/dt
703
Q
!Q
S
R
RS flip-flop
Comp1
== 6
== 1
Comp2
701
Level
702

FIGURE 13

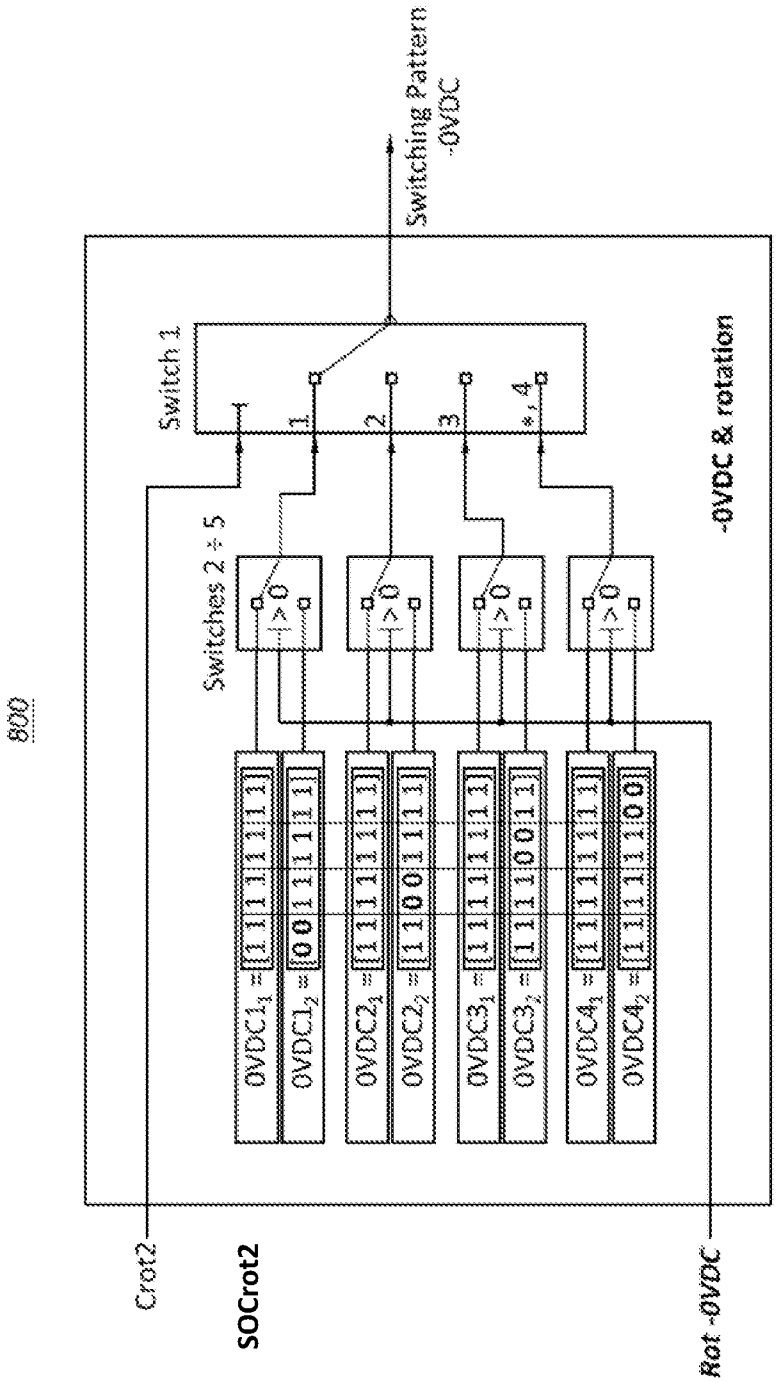

800
Switching Pattern
-0VDC
Switch 1
1
2
3
*.4
Switches 2 ÷ 5
-0VDC & rotation
0VDC1₁ = [1 1 1 1 1 1 1 1]
0VDC1₂ = [0 0 1 1 1 1 1 1]
0VDC2₁ = [1 1 1 1 1 1 1 1]
0VDC2₂ = [1 1 0 0 1 1 1 1]
0VDC3₁ = [1 1 1 1 1 1 1 1]
0VDC3₂ = [1 1 1 1 0 0 1 1]
0VDC4₁ = [1 1 1 1 1 1 1 1]
0VDC4₂ = [1 1 1 1 1 1 0 0]
Crot2
SOCrot2
Rot -0VDC

FIGURE 14A

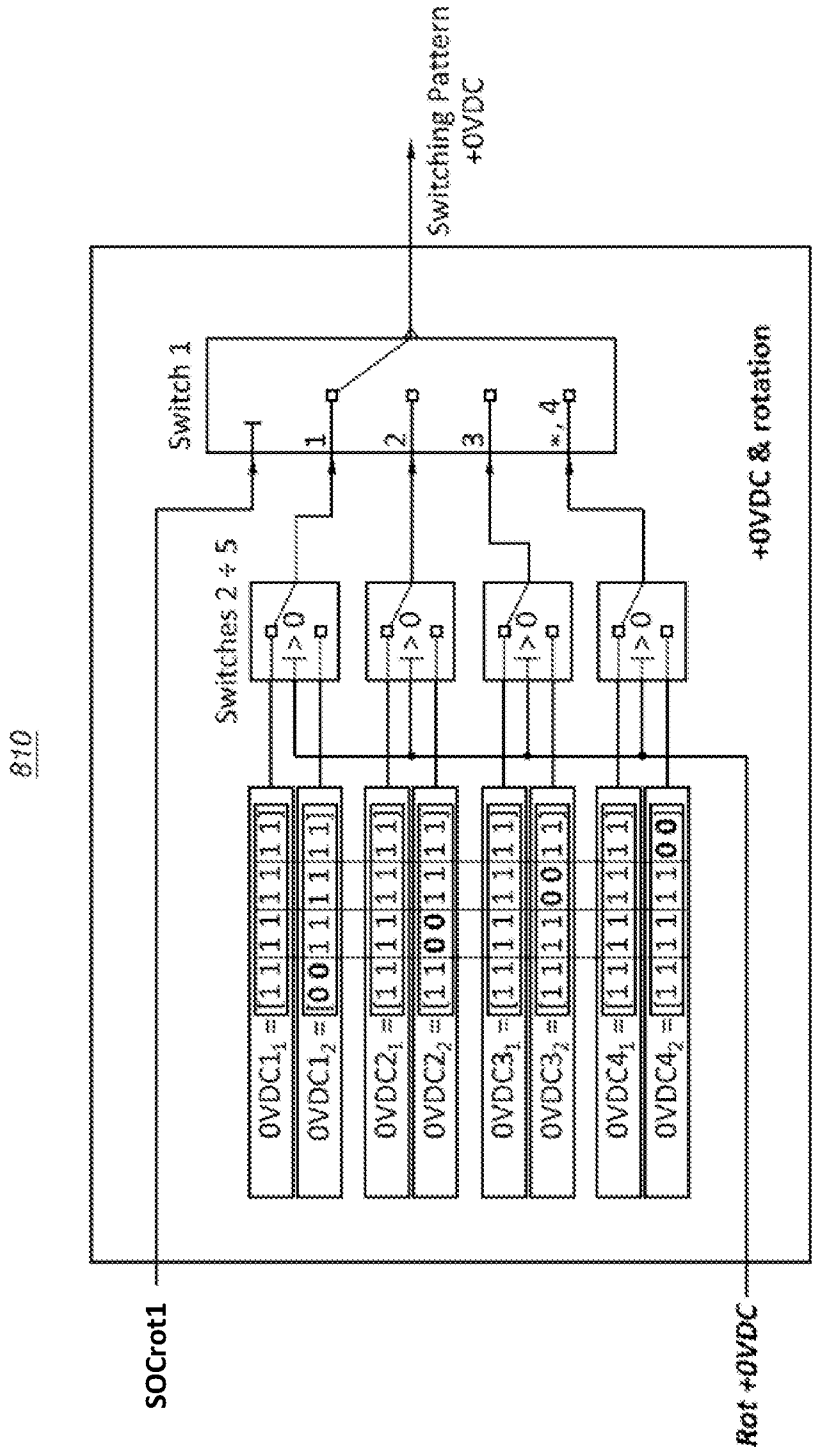

810
SOCrot1
Rot +0VDC
+0VDC & rotation
Switching Pattern
+0VDC
Switch 1
Switches 2 ÷ 5
1
2
3
*, 4
0VDC1₁ = [1 1 1 1 1 1 1 1]
0VDC1₂ = [0 0 1 1 1 1 1 1]
0VDC2₁ = [1 1 1 1 1 1 1 1]
0VDC2₂ = [1 1 0 0 1 1 1 1]
0VDC3₁ = [1 1 1 1 1 1 1 1]
0VDC3₂ = [1 1 1 1 0 0 1 1]
0VDC4₁ = [1 1 1 1 1 1 1 1]
0VDC4₂ = [1 1 1 1 1 1 0 0]

FIGURE 14B

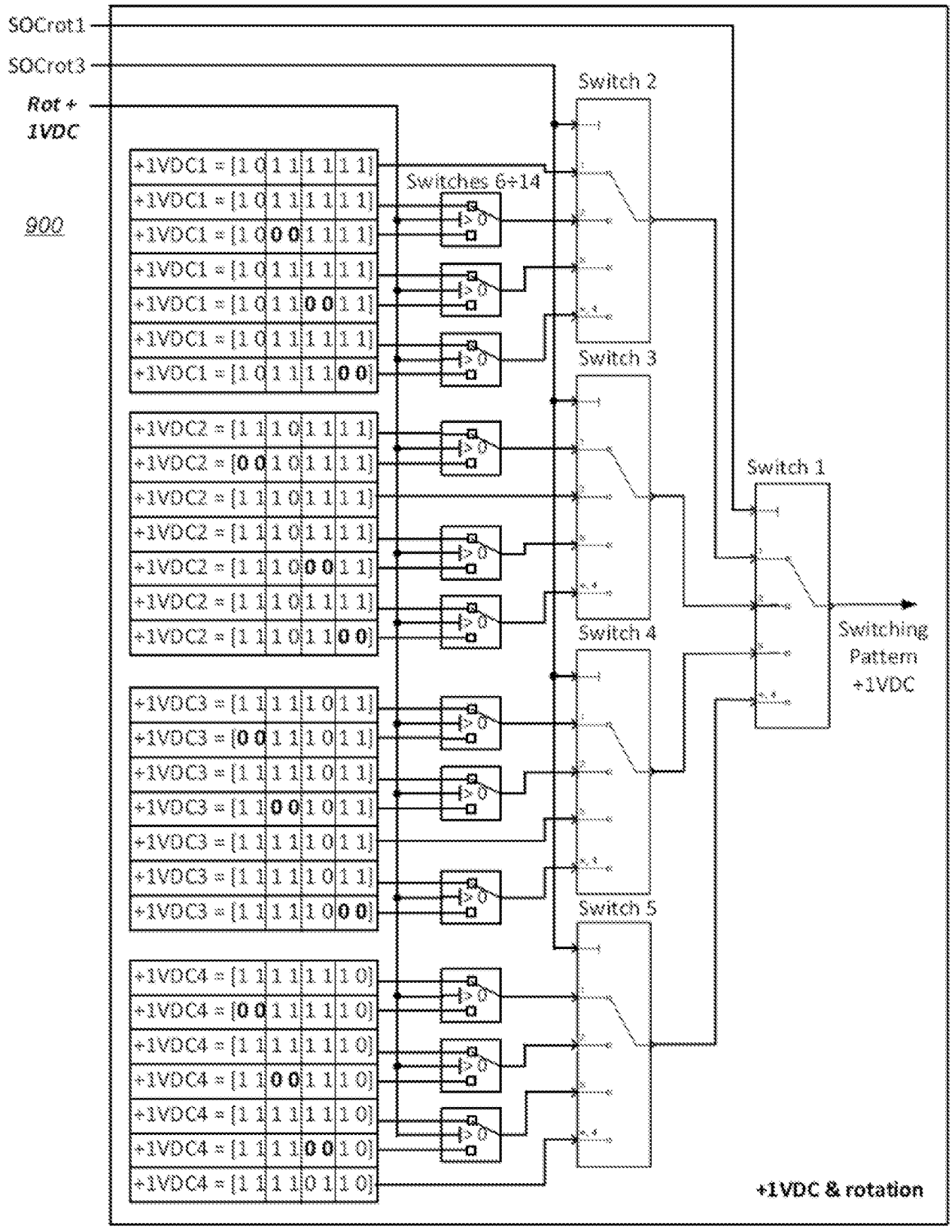

SOCrot1
SOCrot3
Rot + 1VDC
900
+1VDC1 = [1 0 1 1 1 1 1]
+1VDC1 = [1 0 1 1 1 1 1]
+1VDC1 = [1 0 0 0 1 1 1]
+1VDC1 = [1 0 1 1 1 1 1]
+1VDC1 = [1 0 1 1 0 0 1]
+1VDC1 = [1 0 1 1 1 1 1]
+1VDC1 = [1 0 1 1 1 1 0]
+1VDC2 = [1 1 1 0 1 1 1]
+1VDC2 = [0 0 1 0 1 1 1]
+1VDC2 = [1 1 1 0 1 1 1]
+1VDC2 = [1 1 1 0 1 1 1]
+1VDC2 = [1 1 1 0 0 0 1]
+1VDC2 = [1 1 1 0 1 1 1]
+1VDC2 = [1 1 1 0 1 1 0]
+1VDC3 = [1 1 1 1 1 0 1]
+1VDC3 = [0 0 1 1 1 0 1]
+1VDC3 = [1 1 1 1 1 0 1]
+1VDC3 = [1 1 0 0 1 0 1]
+1VDC3 = [1 1 1 1 1 0 1]
+1VDC3 = [1 1 1 1 1 0 1]
+1VDC3 = [1 1 1 1 1 0 0]
+1VDC4 = [1 1 1 1 1 1 0]
+1VDC4 = [0 0 1 1 1 1 0]
+1VDC4 = [1 1 1 1 1 1 0]
+1VDC4 = [1 1 0 0 1 1 0]
+1VDC4 = [1 1 1 1 1 1 0]
+1VDC4 = [1 1 1 0 0 1 0]
+1VDC4 = [1 1 1 1 0 1 0]
Switches 6÷14
Switch 2
Switch 3
Switch 4
Switch 5
Switch 1
Switching Pattern +1VDC
+1VDC & rotation

FIGURE 15A

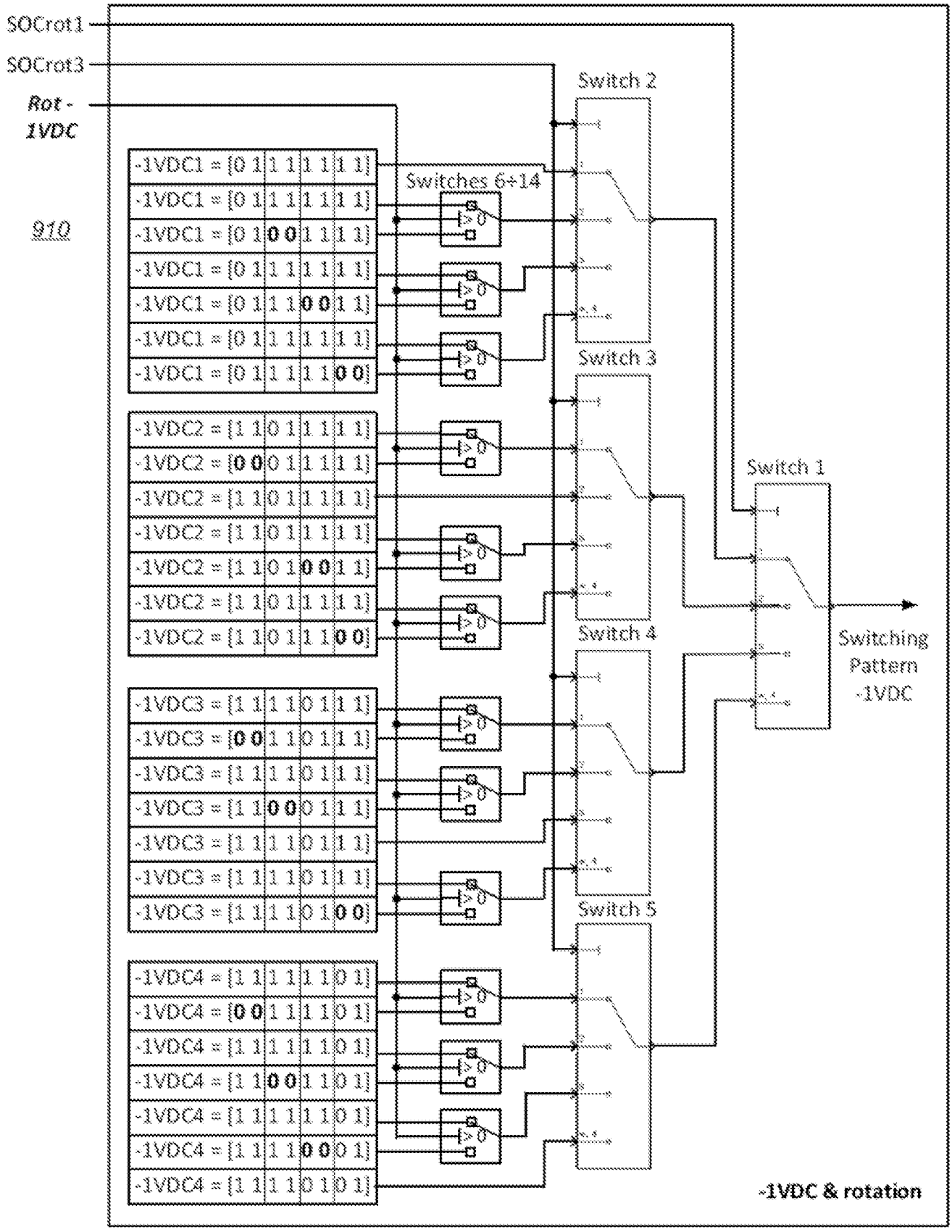

SOCrot1
SOCrot3
Rot - 1VDC
910
-1VDC1 = [0 1 1 1 1 1 1 1]
-1VDC1 = [0 1 1 1 1 1 1 1]
-1VDC1 = [0 1 0 0 1 1 1 1]
-1VDC1 = [0 1 1 1 1 1 1 1]
-1VDC1 = [0 1 1 1 0 0 1 1]
-1VDC1 = [0 1 1 1 1 1 1 1]
-1VDC1 = [0 1 1 1 1 1 0 0]
-1VDC2 = [1 1 0 1 1 1 1 1]
-1VDC2 = [0 0 0 1 1 1 1 1]
-1VDC2 = [1 1 0 1 1 1 1 1]
-1VDC2 = [1 1 0 1 1 1 1 1]
-1VDC2 = [1 1 0 1 0 0 1 1]
-1VDC2 = [1 1 0 1 1 1 1 1]
-1VDC2 = [1 1 0 1 1 1 0 0]
-1VDC3 = [1 1 1 1 0 1 1 1]
-1VDC3 = [0 0 1 1 0 1 1 1]
-1VDC3 = [1 1 1 1 0 1 1 1]
-1VDC3 = [1 1 0 0 0 1 1 1]
-1VDC3 = [1 1 1 1 0 1 1 1]
-1VDC3 = [1 1 1 1 0 1 1 1]
-1VDC3 = [1 1 1 1 0 1 0 0]
-1VDC4 = [1 1 1 1 1 1 0 1]
-1VDC4 = [0 0 1 1 1 1 0 1]
-1VDC4 = [1 1 1 1 1 1 0 1]
-1VDC4 = [1 1 0 0 1 1 0 1]
-1VDC4 = [1 1 1 1 1 1 0 1]
-1VDC4 = [1 1 1 1 0 0 0 1]
-1VDC4 = [1 1 1 1 0 1 0 1]
Switches 6÷14
Switch 2
Switch 3
Switch 4
Switch 5
Switch 1
Switching Pattern -1VDC
-1VDC & rotation

FIGURE 15B

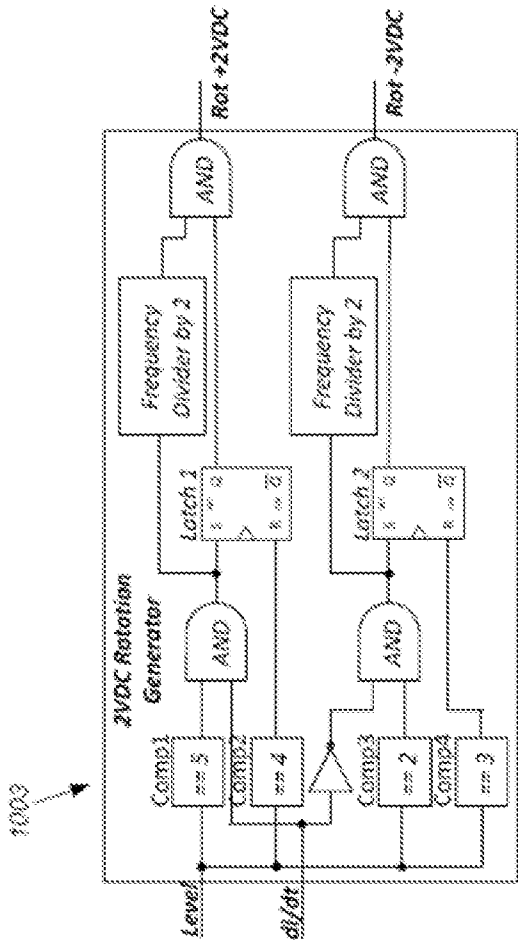


FIGURE 16C

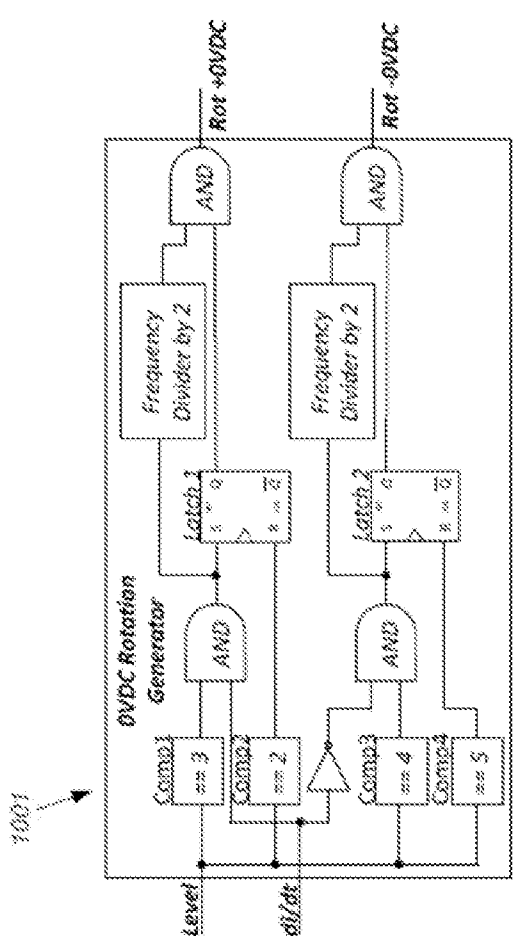


FIGURE 16A

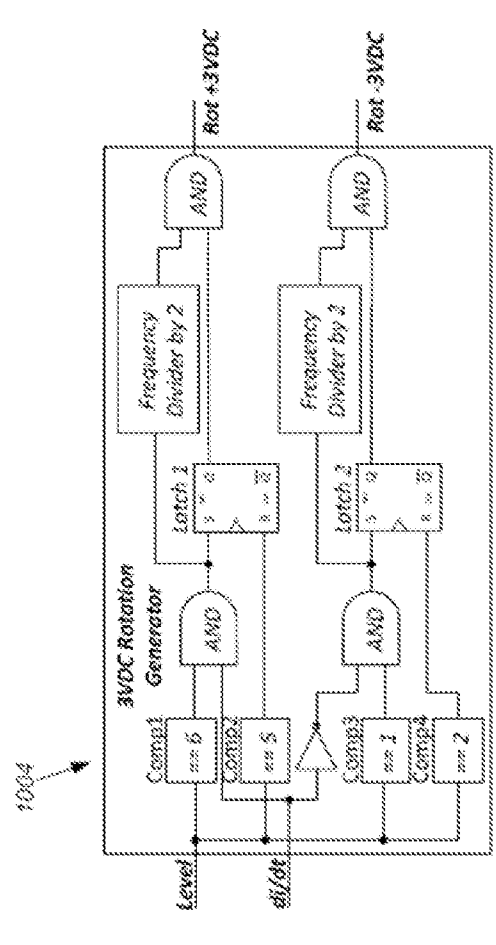


FIGURE 16D

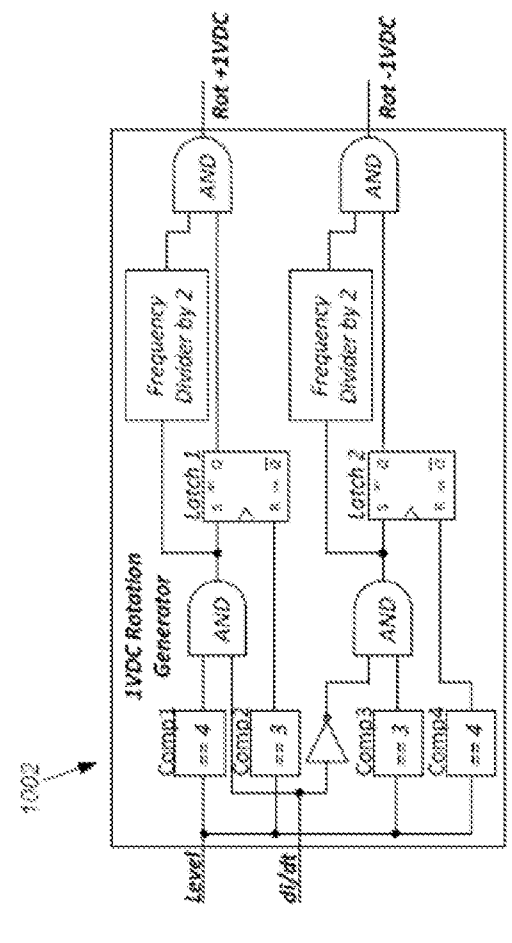


FIGURE 16B

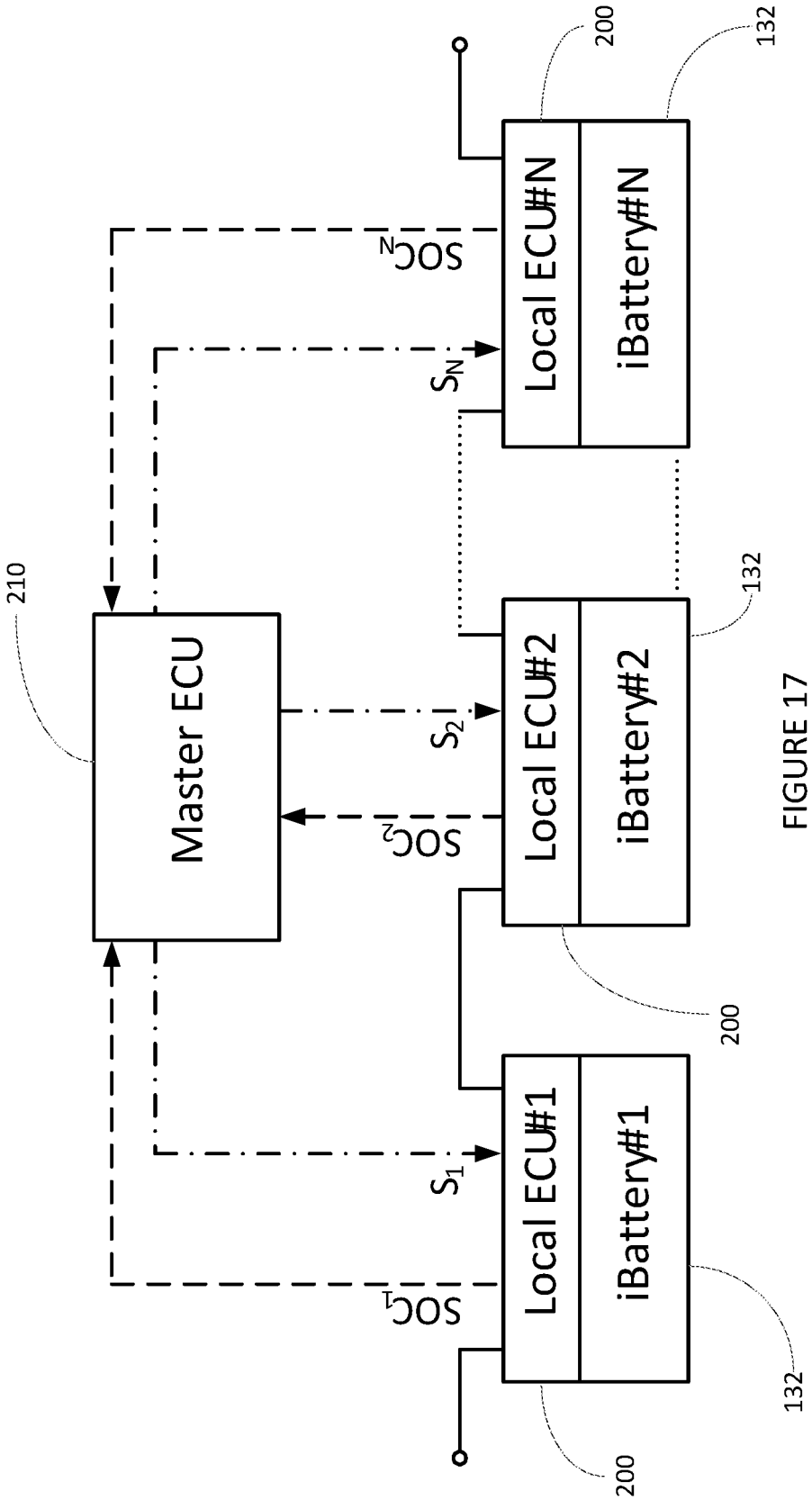

Master ECU
210
Local ECU#N
iBattery#N
Local ECU#2
iBattery#2
Local ECU#1
iBattery#1
200
132
S_N
S_2
S_1
SOC_N
SOC_2
SOC_1

FIGURE 17

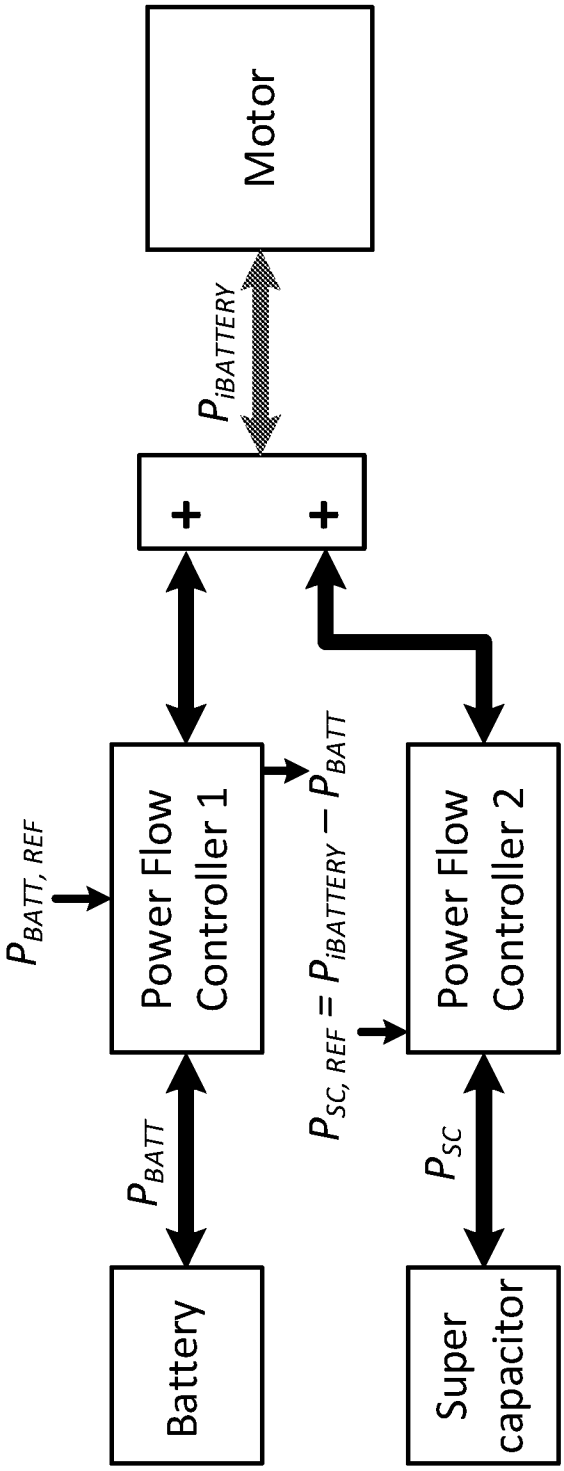

Motor
$P_{iBATTERY}$
+
+
Power Flow Controller 1
Power Flow Controller 2
$P_{BATT, REF}$
$P_{SC, REF} = P_{iBATTERY} - P_{BATT}$
P_{BATT}
P_{SC}
Battery
Super capacitor

FIGURE 18

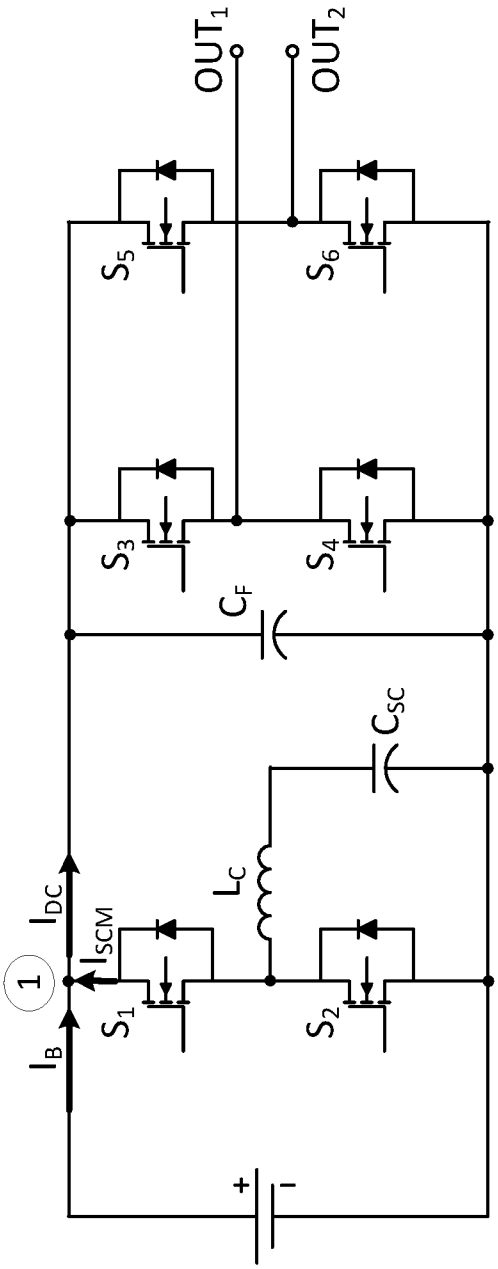


FIGURE 19

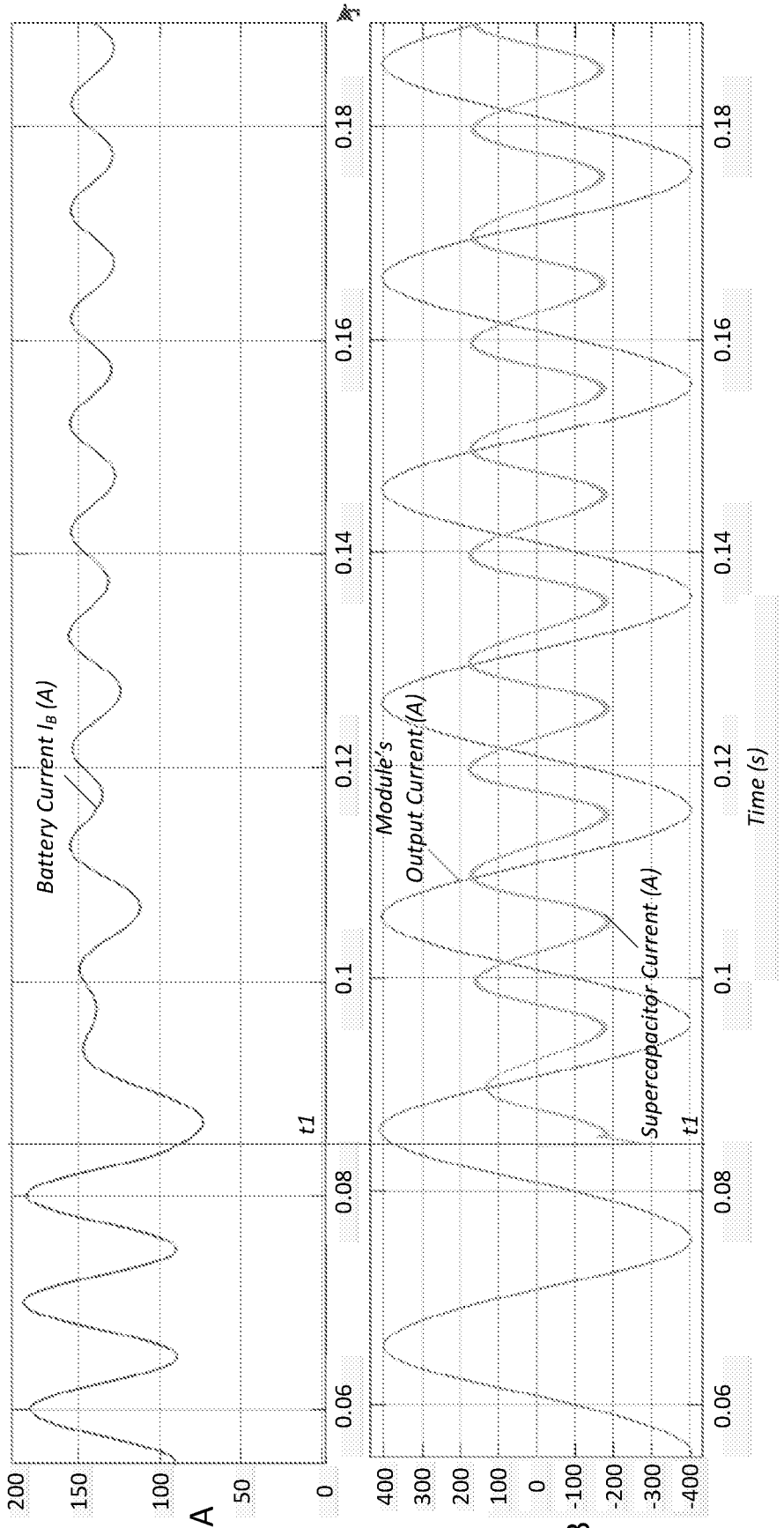


FIGURE 20A

FIGURE 20B

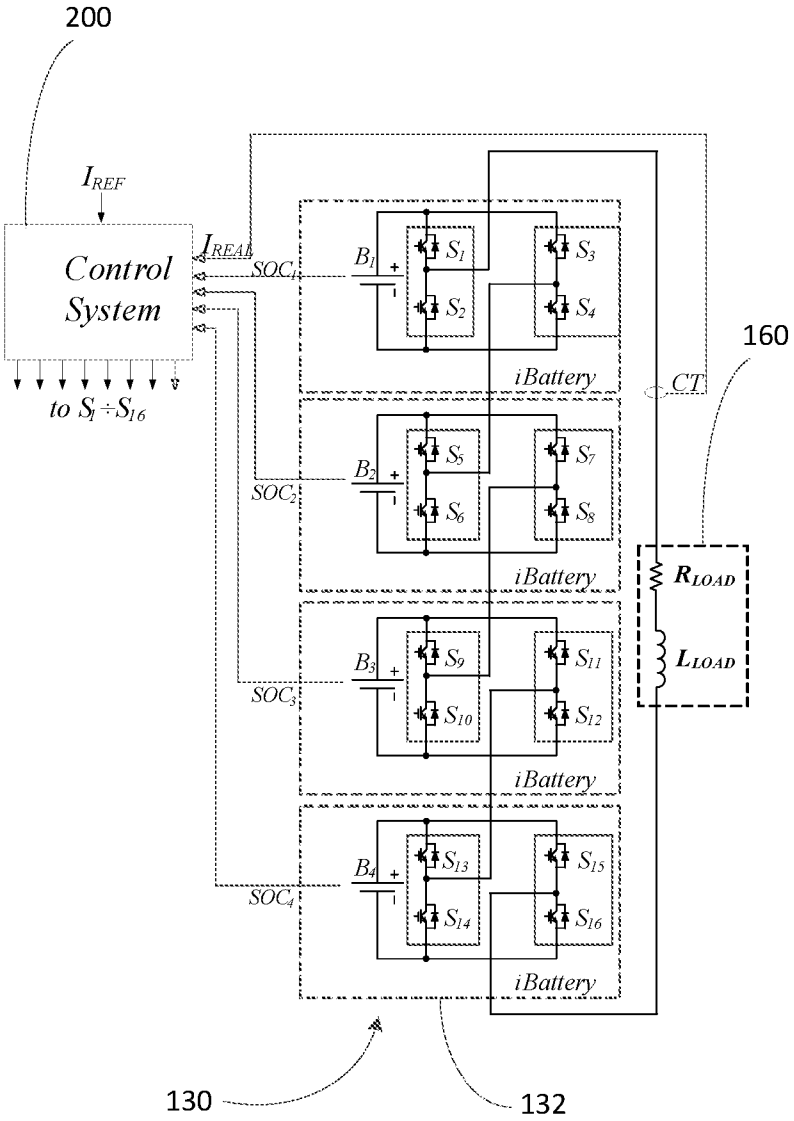

200
I_{REF}
Control System
I_{READ}
SOC_1
SOC_2
SOC_3
SOC_4
to $S_1 \div S_{16}$
B_1
B_2
B_3
B_4
S_1
S_2
S_3
S_4
S_5
S_6
S_7
S_8
S_9
S_{10}
S_{11}
S_{12}
S_{13}
S_{14}
S_{15}
S_{16}
iBattery
iBattery
iBattery
iBattery
CT
160
R_{LOAD}
L_{LOAD}
130
132

FIGURE 21

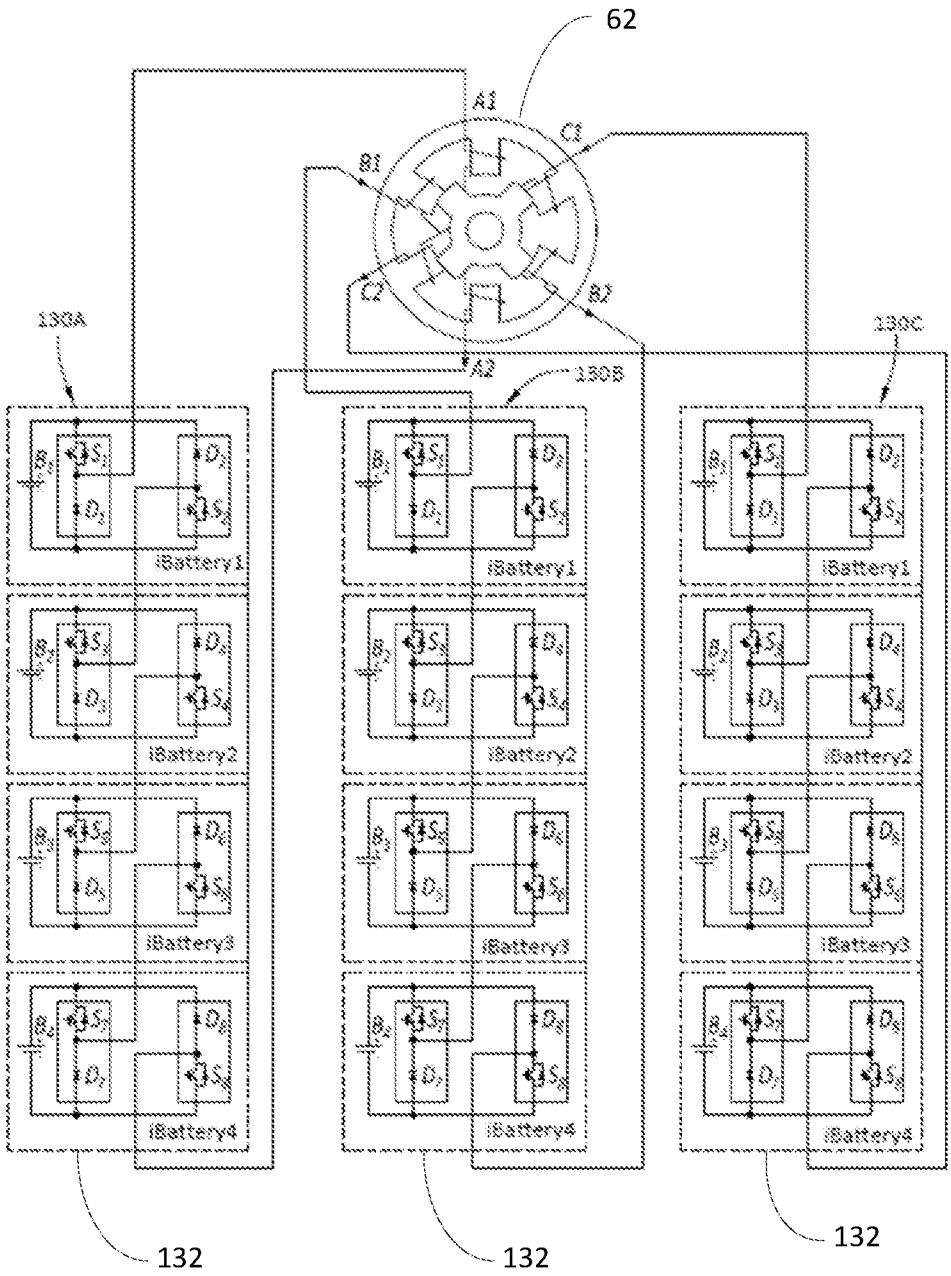

62
A1
B1
C1
C2
B2
A2
130A
130B
130C
iBattery1
iBattery2
iBattery3
iBattery4
132
132
132

FIGURE 22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US19/23695

A. CLASSIFICATION OF SUBJECT MATTER

IPC - B60K 17/34, 17/356; B60L 58/10, 58/18 (2019.01)

CPC - B60K 17/34, 17/356, 7/0007; B60L 58/10, 58/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y -- A	US 2008/0245593 A1 (KIM, R) 9 October 2008; abstract, figure 2, paragraphs [0024], [0026]-[0028], [0031], [0044], claims 1, 9	1, 3 -- 4, 5, 7-11 -- 14
X -- Y	US 2011/0140533 A1 (ZENG, X et al.) 16 June 2011; figure 1A, paragraph [0032], claim 1	16 -- 17-21
X -- Y	CA 2 810 369 A1 (PROTERRA INC) 8 March 2012; figure 6, paragraphs [0031]-[0037], claim 1	22 -- 17, 23-26
Y -- A	US 2009/0311891 A1 (LAWRENCE, R et al.) 17 December 2009; figures 1, 3, 4, paragraphs [0013]-[0016], [0018], [0019]	4, 5, 8-10 -- 6
Y	US 6,064,180 A (SULLIVAN, M et al.) 16 May 2000; column 2, line 50-column 4, line 2, claim 1	7, 18
Y -- A	US 9,444,275 B2 (HUANG, Q et al.) 13 September 2016; column 6, lines 1-17, column 7, lines 8-18, column 16, lines 40-43, claim 1	8, 10, 19-21 -- 6

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 July 2019 (10.07.2019)	12 AUG 2019
Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US19/23695

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN 204156591 U (WUHAN ENERGY ELECTRONIC CO LTD) 11 February 2015; see machine translation	9, 20, 25
Y	CN 201789411 U (RONGXIN POWER ELECTRONIC CO LTD) 6 April 2011; see machine translation	10, 21, 23, 26
Y -- A	EP 2 290 799 A1 (CONVERTEAM TECHNOLOGY LTD) 2 March 2011; paragraphs [0014]-[0016]	11 -- 12, 13
Y	US 7,091,701 B2 (TURNER, G et al.) 15 August 2006; figure 5, column 6, lines 31-54	24-26
A	US 2016/0183451 A1 (MEAN GREEN PRODUCTS, LLC) 30 June 2016; the entire document	1-14
A	US 2012/0074949 A1 (KEPLEY, K et al.) 29 March 2012; the entire document	1-14
A	US 2010/0298957 A1 (SANCHEZ ROCHA, J et al.) 25 November 2010; the entire document	1-14
A	US 2010/0121511 A1 (ONNERUD, P et al.) 13 May 2010; the entire document	1-14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US19/23695

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 15
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
Group I: Claims 1-14; Group II: Claims 16-26

-***-Continued within extra sheet-***-

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US19/23695

-***-Continued from Box No. III Observations where unity of invention is lacking -***-

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-14 are directed towards an electric vehicle.
Group II: Claims 16-26 are directed towards an intelligent battery module.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

The special technical features of Group I include at least wherein: a chassis, three or more wheels operably coupled to the chassis, one or more electric motors operably coupled to the three or more wheels, one or more intelligent modular battery packs operably coupled to the one or more motors, and a control system operably coupled to the one or more battery packs and the one or more motors, which are not present in Group II.

The special technical features of Group II include at least wherein a cascaded architecture comprising a plurality of inter-connected intelligent battery modules; an integrated low voltage converter/controller with peer-to-peer communication capability, an embedded ultra-capacitor, a battery management system, and a plurality of serially connected set of individual cells; a battery with an integrated BMS, a supercapacitor module operably coupled to the battery, and an output converter operably coupled to the battery and the supercapacitor module, which are not present in Group I.

The common technical features shared by Groups I-II are an intelligent battery module. However, these common features are previously disclosed by US 2013/0252033 A1 to BOCEK, P et al. (hereinafter "BOCEK"). BOCEK discloses an intelligent battery module (an intelligent battery pack module; claim 1 of BOCEK).

Since the common technical features are previously disclosed by the BOCEK reference, these common features are not special and so Groups I-II lack unity.