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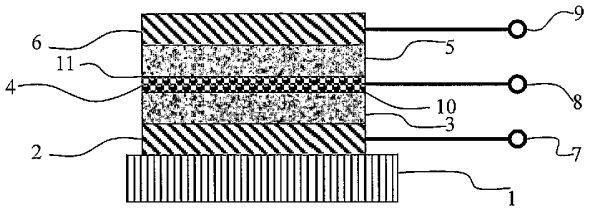
(54) Title: THREE-TERMINAL ELECTRICAL BISTABLE DEVICES



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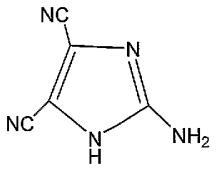

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(57) Abstract: A three terminal electrical bistable device that includes a tri-layer composed of an electrically conductive mixed layer sandwiched between two layers of low conductivity organic material that is interposed between a top electrode and a bottom electrode. The conducting mixed layer serves as the middle electrode. The device includes two memory cells composed of electrode/organic layer/mixed layer, where the interfaces between the electrically conductive mixed layer and the low conductivity organic layer exhibit bistable behavior.

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THREE-TERMINAL ELECTRICAL BISTABLE DEVICES

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to electronic memory cells and switches. More particularly, the present invention involves three-terminal electronic memory and switching devices that utilize two organic memory cells or switching elements that exhibit electrical bistable behavior.

2. Description of Related Art

[0002] The publications and other reference materials referred to herein to describe the background of the invention and to provide additional details regarding its practice are hereby incorporated by reference. For convenience, the reference materials are numerically referenced and identified in the appended bibliography.

[0003] Devices with electrical bistability have been widely studied because they can be used as switches and memory elements, which are important for digital electrical instruments since they have two states of different conductivity. The reversible resistance switching process that occurs in inorganic thin films has engendered strong interest and much work has been done in this field. Recently, organic electrical switching and memory devices have attracted more attention because of the distinct advantages of organic materials, such as light weight, mechanical flexibility, etc. (1-11).

[0004] Organic bistable devices (OBD) and their electrical switching and memory effect have previously been reported (5-8). These devices include five thin films that form an organic/metal-nanocluster/organic triple layer that is sandwiched between two electrodes. When the voltage on the device is larger than a critical voltage, the device switches from a high impedance state (OFF state) to a low impedance state (ON state) and remains in the ON state until a negative voltage is applied. Recently, it was found that the metal-nanocluster layer can be formed by co-evaporation of metal and organic materials, instead of simply depositing the metal at slow deposition rate (8). We found

that the devices fabricated in this way are highly reproducible. For convenience, in this specification we sometimes refer to the (middle) mixed layer as the metal-nanocluster layer.

[0005] Most memory devices based on conductance change are detected by measuring the device current. From application point of view, the memory cell should be as small as possible, such as in the micrometer or sub-micrometer scale, in order to achieve a high density of data storage. In this case, the current through the memory cell may be too small to be distinguished conveniently to determine whether the device is in ON state or OFF state. This issue may be overcome by increasing the ON state current of the device.

SUMMARY OF THE INVENTION

[0006] In accordance with the present invention, we provide another approach to solve the issues set forth above by demonstrating a three-terminal OBD (3-T OBD), which is realized by wiring-out the metal-nanocluster layer of the OBD as the middle electrode. The ON and OFF state of the device can be read out by measuring the potential of the third terminal of a biased device, which is independent of the device area.

[0007] In accordance with the present invention, electrical bistable devices are provided that are convertible between low resistance (impedance) states and high resistance (impedance) states. The electrical bistable devices are well suited for use as electrical switching and memory devices. The electrical bistable devices of the present invention include a tri-layer that is composed of a mixed layer of a high conductivity material and low conductivity organic material that is sandwiched between layers of low conductivity organic material. The tri-layer is sandwiched between two electrodes. The two electrodes and the mixed layer are connected to three terminals to provide for switching of the device between various low resistance states and high resistance states by application of suitable electrical voltages between the terminals. The three-terminal configuration allows one to switch the device between up to four different high and low resistance states.

[0008] As a feature of the present invention, the mixed layer is composed of a low conductivity organic material and a sufficient amount of a high conductivity material to render the mixed layer electrically conductive. The mixed layer includes a first side and a second side. The first layer of low conductivity organic material is located on the first side of the tri-layer. A first interface is formed where the first layer of low conductivity organic material and mixed layer meet. The first layer of low conductivity organic material includes a first electrode side that is located opposite the first interface. A second layer of low conductivity organic material is located on the second side of the mixed layer and forms a second interface where the second layer and mixed layer meet. The second layer of low conductivity organic material includes a second electrode side that is located opposite the second interface. A first electrode is attached to the first electrode side of the first layer of low conductivity organic material and a second electrode is attached to the second electrode side of the second layer of low conductivity organic material.

[0009] The high conductivity material used to form the mixed layer can be a metal, conductive oxide, conducting polymer or organic conductor. The low conductivity organic material used in forming the mixed layer can be an organic semi-conductor or organic insulator. The low conductivity material and the high conductivity material are mixed together in amounts to provide a layer that is electrically conductive. However, as a feature of the invention, the interfaces between the layers of low conductivity organic material and the electrically conductive mixed layer exhibit electrical bistable behavior. Therefore, each unit cell of the dual-memory cell has one interface to the nanocluster and can behave as one individual memory cell.

[00010] The electrical bistable devices may be used to form a wide variety of memory devices and switches wherein a memory input element is provided for applying voltage to the bistable interfaces to convert the bistable interfaces between low electrical resistance states and high electrical resistance states. Memory devices may further include a memory read-out element, which provides an indication of whether the bistable interfaces are in the low or high electrical resistance states.

[00011] As one feature of the present invention, the memory input element includes a terminal (T1) attached to the first electrode (bottom electrode), a terminal (T3) attached to the middle mixed layer (middle electrode) and a terminal (T2) attached to the second electrode (top electrode). The portion between the bottom electrode (T1) and middle electrode (T3) is defined as the bottom part of the 3-T OBD, and the portion between middle electrode (T3) and top electrode (T2) is defined as top part of the 3-T OBD. It was discovered that application of an appropriate voltage between the bottom electrode (T1) and the middle electrode (T3) provided conversion in electrical resistance of that bottom part of the 3-T OBD Likewise, when an appropriate voltage was applied between the top electrode (T2) and the middle electrode (T3), the electrical resistance of the top part of the 3-T OBD was also converted. This particular feature allows the device to be switched between four possible states by applying voltage pulses between the two pairs of terminals (T1-T3 and T2-T3). This type of a device may be used to provide double data storage density.

[00012] When the top part (top-electrode/top-organic/metal-nanocluster) and the bottom part (metal-nanocluster/organic/bottom-electrode) are not electrically the same, caused by interface formation, the potential difference of the middle electrode can be detected for a biased device (less than switching voltage) between the ON state and the OFF state. The 3-T OBDs can be read out by measuring the potential of the middle electrode, which is independent of device area. Hence the reading of 3-OBDs is still effective as the memory cell shrinks to micro or sub-micro scale. It was also found that the electrical contact between the top electrode/top organic layer and the bottom organic layer/bottom electrode is different which causes the two parts of the 3-terminal OBDs to be electrically asymmetric, with the result being a large increase of the potential of the middle electrode during switching ON process.

[00013] The above discussed and many other features and attendant advantages of the present invention will become better understood by reference to the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[00014] FIG. 1 (a) is a diagram of a three-terminal electrical bistable device (3-T OBD) in accordance with the present invention showing a co-evaporated middle layer and the measurement setup. FIG. 1(b) depicts the chemical structure of AIDCN.

[00015] FIG. 2 is a graph showing current (I) – voltage (V) characteristics of an exemplary 3-T OBD in accordance with the present invention recorded during the switching on process and the ON state measured through top and bottom electrode.

[00016] Fig. 3 is the bias dependence of the potential drops on the top part (top-electrode/top-organic/mixed-layer) (U_{top}) and the bottom part (mixed-layer/bottom-organic/bottom-electrode) (U_{bottom}) of a three-terminal OBD (left Y-axis) and the device current (right Y axis).

[00017] FIG. 4 is a graph showing the typical I-V characteristics of a strip of mixed layer material measured at the two ends of the strip in accordance with the present invention where the mixed middle thin film has a size of 10 mm by 3 mm and thickness of 200 Å.

[00018] FIG. 5a is a graph showing the I-V curve of an exemplary 3-T OBD in accordance with the present invention and the potential drop of the top part of the 3-T OBD (U_{top}) during sweeping from 0 to 3 volts during the switch-on process and in the ON state. FIG. 5b is a graph showing the change of the resistance of top part and bottom part of the 3-T OBD during the switch-on process and in the ON state.

[00019] FIG. 6 is a graph showing the results of a stress test of the ON and OFF states of a three-terminal (3-T) OBD in accordance with the present invention that was biased at 1 volt. The device state was read out by measuring the potential drop of the top part of the 3-T OBD (U_{top})..

[00020] FIGS. 7a and 7b are graphs showing the results of cyclic write-read-erase-read tests of an exemplary three-terminal 3-T OBD in accordance with the present invention. The upper curve is the voltage biased on the device and the bottom curve is the potential drop on the top part of the 3-T OBD. The voltage for write, erase and read is 2.5 volts, -1.5 volts and 1 volt, respectively. In order to use a logarithmic axis for the potential drop

across the top part of the 3-T OBD, the current of erasing process is an absolute value. FIG. 7a is the beginning of the cyclic test while FIG. 7b is that recorded after 21 hours of continual testing.

DETAILED DESCRIPTION OF THE INVENTION

[00021] The present invention is an improvement over the high-performance organic or electrical bistable devices that utilize an organic/metal/organic configuration as the bistable structure which is sandwiched between two aluminum electrodes (5,6). The present invention is also an improvement over organic or electric bistable devices where the tri-layer is composed of metal nanoclusters separated by thin oxide layers (8).

[00022] In accordance with the present invention, electrical bistable devices are provided that may be used as a three-terminal organic memory or switching device. The devices have a basic structure where a triple layer (organic layer / mixed layer (metal:organic) / organic layer) is sandwiched between two electrodes. The two electrodes and the wired-out mixed (metal:organic) layer are the three terminals of the device. When the applied voltage on the device is larger than a critical voltage, the device switches from a high impedance state (OFF state) to a low impedance state (ON state) and remains in the ON state until a negative voltage is applied. When the device is biased between the two electrodes, the voltage is observed between the middle mixed layer and the electrodes. We found that for some 3-T OBDs, the potential drop of the top part and the bottom part are not equal. We found that most of the voltage biased on the device drops on the bottom part of the 3-T OBDs, especially when the device is in the OFF state. We further found that the potential drop across the top part of the 3-T OBDs increases dramatically when the device switches from the OFF state to the ON state. Consequently, the state (ON/OFF) can be known from the potential drop across the top part when the device is biased between the top and bottom electrode.

[00023] A 3-terminal organic electrical bistable device (3-T OBD) in accordance with the present invention is shown generally in FIG. 1(a). The 3-T OBD that was fabricated on an insulating substrate 1, includes a mixed middle layer (electrically conductive) 4 that

is sandwiched between a first (top) layer of low conductivity organic material 5 and a second (bottom) layer of low conductivity organic material 3. The mixed middle layer 4 is shown in the form of a layer. However, it will be understood that the mixed middle layer can be provided in any number of different shapes. Mixed middle layers in the form of a thin layer or film are preferred since fabrication techniques for forming thin films are well known. The 3-T OBD further includes a first (top) electrode 6 and a second (bottom) electrode 2.

[00024] The 3-T OBD includes interfaces 10 and 11 located between the mixed middle layer 4 and the organic layers 3 and 5, respectively. The interfaces 10 and 11 exhibit contact resistance that can be changed by charges stored at the interfaces. The 3-T OBD is connected to an electronic control unit (not shown) via electrical terminals 7, 8 and 9. The control unit is capable of providing an electrical voltage bias across any two pair of electrodes 2, 4 and 6 to convert both of the bistable interfaces between low resistance and high resistance states or to convert just one of the interfaces between low resistance and high resistance states. In addition, the control unit is capable of, among other things, measuring the potential of the middle electrode 8 or current to determine the electrical resistance of the device.

[00025] As shown in FIG. 1(a) the terminals 7, 8, and 9 may be used to apply a voltage bias (V_{bias}) across the entire tri-layer to a grounded electrode 6 with the voltage being measured (V_{meas}) at terminal 8. Alternately, the connections 7, 8 and 9 may be used as terminals T1, T3 and T2, respectively. In this exemplary configuration, bias voltages may be applied between T1-T3 and T2-T3, which allows one to individually convert the bottom part (2,3,4) and the top part (4,5,6) of the 3-T OBDs between the high and low resistance states.

[00026] The mixed middle layer 4 includes a low conductivity organic material and an amount of high conductivity material that renders the mixed layer electrically conductive. The incorporation of the high conductivity material into the low conductivity organic material can be accomplished in a number of different ways. The two materials are preferably co-evaporated to form a molecular solution where the mixed layer does not have distinct phases or where there are nanoparticles of high conductivity material

dispersed throughout the low conductivity organic material. The amount of low conductivity organic material and high conductivity material are also chosen such that an electrically bistable interface is formed when the mixed layer is formed on a layer of low conductivity organic material or where a layer of low conductivity organic material is formed on the mixed layer.

[00027] Suitable high conductivity materials include metals, such as aluminum, copper and silver. Other suitable metals can be high work function metals such as gold, nickel and middle work function metals such as magnesium and indium. Low work function metals may also be used such as calcium and lithium. Metal alloys of the above metals (e.g., lithium/aluminum alloys) may also be used as the high conductivity material. Conductive oxides such as metal oxides are also suitable. Conducting polymers such as 3,4-polyethylenedioxy-thiophenepolystyrene-sulfonate (PEDOT) or doped polyaniline are also suitable high conductivity material. Organic conductors such as buckminster fullerene may also be used as the high conductivity material.

[00028] Suitable low conductivity organic materials include organic semiconductors and organic insulators. Exemplary organic semiconductors include small molecular organic materials such as 2-amino-4,5-imidazoledicarbonitrile (AIDCN); tris-8-(hydroxyquinoline)aluminum (Alq); 7,7,8,8-tetracyanoquinodimethane (TCNQ); 3-amino-5-hydroxypyrazole (AHP). Oligomers such as polyanaline may also be used. Organic insulators include polymers such as polystyrene (PS), polycarbonate (PC), polymethylmethacrylate (PMMA), polyolefines, polyesters, polyamides, polyimides, polyurethanes, polyaccetals, polysilicones and polysulfonates. In addition semiconducting polymers may be utilized. Exemplary semiconducting polymers include poly(phenylene vinylene) (PPV), polyfluorene (PF), polythiophene (PT), poly(paraphenylene) (PPP) and their derivatives as well as copolymers. The same low conductivity organic materials that are used in forming the mixed layer 12 may also be used to make the layers 14 and 16.

[00029] If desired, the above low conductivity (insulating) polymers may be doped with selective dopants such as charge blocking or trapping material, electron and hole transport material, and luminescent material. Charge blocking material include 2,9-

dimethyl-4,7-diphenyl-1,10-phenanthroline (Bathocuproine, or BCP); electron transporting materials include tris-(8-hydroxyquinolinolato) aluminum (Alq3) and its derivatives, such as tris-(4-methyl-8-hydroxyquinolinolato) aluminum (Almq3); hole transporting materials include N,N-diphenyl-N,N-bis(3-methylphenyl)-1, 1-diphenyl-4,4 diamine (TPD) and N,N-diphenyl-N,N-bis(1-naphthylphenyl)-1, 1-diphenyl-4,4 diamine (NPB); luminescent material include 4,4-N,N-dicarbazole-biphenyl (CBP). With regards to the electrodes 15 and 17, conventional electrode material such as aluminum, copper, and other electrode metals, including alloys, may be used. Conducting metal oxides, such as indium tin oxide (ITO), indium oxide and other metal oxides are also suitable electrode material. In addition, conducting polymers such as PEDOT and doped polyanaline may be used.

[00030] The high conductivity material and low conductivity organic material may be combined in numerous different ways to form mixed layers in accordance with the present invention that are electrically conductive and which form interfaces with layers of low conductivity organic material that exhibit a reversible transition between high and low electrical resistance states (bistable behavior). For example, the two materials may be co-evaporated to form a single phase mixed layer or a mixed layer in which nanoparticles of high conductivity material are dispersed in the low conductivity organic material. Such deposition procedures are known. The amounts of low conductivity and high conductivity material may be varied to achieve the desired electrical conductivity in the body of the mixed layer and bistable behavior at the interfaces with the layers of low conductivity organic materials. A 1:4 volume ratio of low conductivity to high conductivity material is preferred. However, the volume ratio of low conductivity to high conductivity material may be varied depending upon the particular materials being used and provided that the mixed layer is electrically conductive and also forms electrically bistable interfaces with low conductivity organic materials.

[00031] As mention above, the mixed layer may be in the form of a two-phase system where nanoparticles or molecular clusters of high conductivity material are dispersed throughout the low conductivity material. The nanoparticles and molecular clusters preferably have an average particle size of between 1 to 50 nm. The formation of such

mixed layers may be accomplished using conventional evaporation techniques known in the electronic fabrication art for forming thin layers containing nanoparticles dispersed in a solid matrix.

[00032] Examples of practice are as follows:

[00033] The devices of the present invention can be made using fabrication processes that are similar to what has been previously reported (5,6). A glass substrate (See FIG. 1) is cleaned using a routine procedure. First, the pre-cleaned glass substrate is sonicated in detergent, followed by sonication in deionized water, sonication in acetone and then sonication in isopropanol. The cleaned glass substrate is then baked in an oven at about 80°C to prepare for fabrication. The five layers of the 3-T OBD are deposited layer by layer by thermal evaporation at high vacuum (pressure of the evaporator is below 2.0 x 10^{-6} Torr) without breaking the vacuum.

[00034] The low conductivity organic material and the high conductivity metal material used in this example were 2-amino-4,5- imidazoledicarbonitrile (AIDCN) and aluminum (Al), respectively. First, a 650Å Al film was deposited on the cleaned glass substrate at a deposition rate of 3 Å/s to form the bottom or second electrode (17). Then, a 400 Å thick film of AIDCN was deposited (0.5 Å/s) to form the bottom organic layer (16). Then, a mixed layer 12 composed of Al and AIDCN was deposited by co-evaporation. The bistable layer 12 was 200 Å thick. The deposition rate of Al and AIDCN for the middle bistable layer 12 was 0.4 Å/s and 0.1 Å/s, respectively. Then, another 450 Å thick film of AIDCN was deposited at a rate of 0.5 Å/s to form the upper organic layer 14. Finally, an 800 Å thick film of Al was deposited at a rate of 2 Å/s to form the top or first electrode 15. The cross-sectional area of the top and bottom electrodes 17 and 15 was 0.4 mm^2, which is the size of 3-T OBD's set forth in this example.

[00035] In order to study the mechanism of 3-T OBD's and investigate the potential distribution of the device, we wired out the middle layer 4 during device fabrication. When the mixed middle layer 4 was deposited on the bottom AIDCN layer 3, it was also deposited on an extra bottom electrode for wiring it out and a strip of the mixed film was deposited on the glass substrate at the same time for study of the mixed film itself.

[00036] The thicknesses of the thermally evaporated organic and metal thin films were monitored by a quartz crystal calibrated with Dektak IIA. Current-voltage curves reported here were measured with a HP 4155B semiconductor parameter analyzer. The curves of the cyclic write-read-erase-read test and stress test were characterized by two Keithley 2400 Series Sourcemeters (one for biasing the voltage, another one for measuring the potential drop) that were controlled by a computer. All electrical measurements were done in ambient condition.

[00037] Typical I–V curves for a 3-T OBD are shown in FIG. 2. During the first forward bias scan from -1.5 to 3 volts, the device shows a very low current in the low-voltage range, indicating the device is in the OFF state. At a critical voltage (it is 2 volts here), the current has a sharp increase of several orders of magnitude, indicating the device has had a transition from the OFF state to the ON state. However, the I–V curve recorded in the second bias scan is totally different from that observed in the first bias scan. Even in the low-voltage range, the device shows a very high current, indicating that the device remains in the ON state. When the device is switched to the ON state, it remains in that state even when the power is off. The OFF state can be recovered by applying a reverse bias, which means that this kind of device is ideal for memory applications.

[00038] When we measured the I-V curves of the exemplary 3-T OBD, a sweeping voltage was biased between the top Al electrode 9 and bottom Al electrode 2 and the change in potential of the middle mixed layer 4 was observed at same time. The I-V curves and the changing potential drop on the top part (4,5,6) (U_{top}) and the bottom part (2,3,4) (U_{bottom}) during the switch-on process of a device are shown in FIG. 3.

[00039] In FIG. 3, the common electrode for biasing and measurement is the top Al electrode 6, so the potential measured is the voltage drop across the top part (4,5,6) (defined as U_{top}). U_{top} increases from 0.2 mV to 1V when the device transitions from the OFF state to the ON state at around 2.5 volts. The potential drop of the bottom part (2,3,4) (defined as U_{bottom}) can be obtained by subtracting U_{top} from the biased voltage. U_{bottom} changes very smoothly while sweeping the voltage, but decreases slightly more when the device switches from the OFF state to the ON state. When the device in the OFF state,

almost all of the voltage on the device drops on the bottom part (2,3,4). In the ON state, the values of U_{top} and U_{bot} are of the same order and comparable.

[00040] To further confirm this point, the common electrode was also selected for the bottom Al electrode 2 during the measurement. A similar result was also observed.

[00041] The I-V curve of the middle mixed layer alone on a glass substrate is shown in FIG. 4. The size of the thin film or layer is 10mm by 3 mm. The layer was deposited on glass when the mixed middle layer 4 was deposited on the bottom AIDCN film 3 during fabrication of the exemplary device. The thickness of the isolated mixed layer was also 200 Å. The I-V curve in FIG. 4 is a perfect straight line, which means the middle mixed layer shows ohmic behavior. The resistance of the layer is about 79 KΩ. From this, we can see that the conductivity of the mixed middle layer 4 is quite large, the potential measured by wiring out the middle layer is reliable and the potential drop on the mixed middle layer 4 can be ignored.

[00042] FIG. 5 shows the current through the 3-T OBD, U_{top} and the resistance of the top part (4,5,6) and bottom part (2,3,4) during the switch-on process and the ON state. In FIG. 5a, during the first sweep (squares), the current through the 3-T OBD and the potential drop of the top part (4,5,6) sharply increase three orders at the same time when the sweeping voltage increases to 2 volts and the 3-T OBD is switched on. During the second sweep (circles), the 3-T OBD remains in the ON state and the current and U_{top} are much higher compared to the OFF state. It is clear that the changes in current and U_{top} are synchronous in the OFF and ON state.

[00043] The resistance of the top part (4,5,6) and bottom part (2,3,4) is obtained by dividing U_{top} and U_{bottom} by the current. The resistance-voltage curves of the top part (4,5,6) and bottom part (2,3,4) calculated from the data of FIG. 5a are shown in FIG. 5b, where the open curves (open squares and circles) show the resistance change of the top part (4,5,6) and solid curves (solid squares and circles) show the change of the bottom part (2,3,4). From FIG. 5b, one can see that when the 3-T OBD is in the OFF state, the resistance of the bottom part (2,3,4) (defined as R_{bottom}) is about 5 orders larger than the resistance of the top part (4,5,6) (defined as R_{top}). This is the reason why U_{top} is very small and most of the voltage is dropped at the bottom part (2,3,4) in the OFF state.

When the 3-T OBD switches from OFF to ON, both R_{bottom} and R_{top} decrease sharply, but R_{bottom} decreases about 4 orders while R_{top} only decreases 1 order of magnitude. In the ON state, R_{bot} is about 50 times greater than R_{top}, so U_{top} increases sharply during the transition of 3-T OBD from the OFF state to the ON state. When the 3-T OBD remains in the ON state, $R_{bot\ tom}$ and R_{top} have no obvious change while sweeping the voltage. From FIG. 5, it is apparent that the decreasing of R_{bottom} plays a more important role for the switching of the 3-T OBD.

[00044] Although the thickness of the bottom and top AIDCN layers (3 and 5) is identical, R_{bottom} is much bigger than R_{top} in the ON state and OFF state. The probable reason is that the interfaces of the two AIDCN layers are different. When the mixed middle layer 4 was deposited on the bottom AIDCN layer, a few Al atoms penetrated the bottom AIDCN layer because of the low deposition rate and the co-deposition with AIDCN. As a result, the interface between the bottom AIDCN layer 16 and the mixed middle layer 4 is not clear. When the top electrode 6 was deposited, a lot of Al atoms penetrated in the top AIDCN layer 5 due to the high deposition rate. The morphology of the bottom Al electrode 2 is flatter than the mixed middle layer 4, which is another reason for the uneven potential distribution. The mixed middle layer 4 plays an important role in the 3-T OBD and we believe that the middle mixed layer is "nano-structured" meaning that nanoparticles of Al are dispersed in the AIDCN. The reason for the large decrease of R_{bottom} when the device is switched ON is probably due to charges stored at the nano-particles in the mixed middle layer 4. This results in some charges being induced in the AIDCN layer near the middle and the contact resistance at interfaces 10 and 11 are reduced which results in the device being switched to the ON state.

[00045] As is apparent from the above example, a new type of 3-T OBD with three terminals has been created in accordance with the present invention. The top electrode 6, bottom electrode 2 and the electrically conductive mixed middle layer 4 are attached to the three terminals 9, 7 and 8 of the 3-T OBD , which act as ground, control and read terminal, respectively. Top electrode 9 is just the common electrode for biasing and measuring the voltage. The bottom electrode 2 is used to control the state of the 3-T OBD (bias a voltage to switch ON/OFF the device) and bias the small voltage read the

state (ON/OFF) of the device, as shown in FIG. 1a. The readout of the three-terminal 3-T OBD is different than the previous two-terminal OBD. A low level voltage (100 mV magnitude in the ON state and below 1 mV in the OFF state) is needed in order to read (measure) the state of the device, while a low level current (1 μA in the ON state and below 10 nA in the OFF state) is needed for the two-terminal OBD. Because a 100 mV voltage is easier to measure than a 1 μA current and the fabrication technology for these two kinds of OBD is the same, the three-terminal OBD in accordance with the present invention is more practical.

[00046] In order to study the stability of the device in the on and OFF state, a constant small voltage is biased on the device. U_{top} is recorded to monitor the state of the 3-T OBD when the 3-T OBD stays in the on or OFF state. FIG. 6 shows the stress test of the ON state and OFF state of the exemplary three-terminal 3-T OBD biased at 1 volt. The inset of FIG. 6 shows the switch-on process and the ON state of the device. The switch-on voltage for this three-terminal 3-T OBD is 2.0 volts. In FIG. 6, U_{top} in the ON state is 3 orders bigger than in the OFF state. It can be seen that there is no significant degradation of the device in either the on or OFF state during the three-hour stress test, which is indicative that both states are stable.

[00047] In FIG. 7, we present the rewritable data-storage application of the exemplary three terminal 3-T OBD. The device was biased by a multi-step voltage to: 1) switch on (write): 2) read, switch off (erase); and 3) read it. The voltage for write, erase and read is 2.5 volts, -1.5 volts and 1 volt, respectively. The ratio of U_{top} in the on and OFF state is about 10^3 during the test. At the beginning, the success ratio of the cycle (write-read-erase-read) is almost 100 %. After 21 hours of continual testing, the device still worked very well. The ratio was still near 100%, but U_{top} in the OFF state increased 1.5 orders from 0.1 mV to 10 mV. This indicates that the device degraded during the test since the test was operated in air. It should be noted that the time scale used in FIG. 7 is due to the inherent limitation of the test instrument and program.

[00048] The bistable device 10 may also be used to provide double data storage density when the terminals T1, T2 and T3 are connected as set forth in FIG. 1. This terminal configuration sets up two cells (T1-T3) and (T2-T3) in which the interfaces between the

mixed layer and layers of low conductivity organic material exhibit electrical bistable characteristics. This means both cells have a 0 state and a 1 state. As a result the bistable device 10 can have 4 different state described by (*n*,*m*), where *n* represents the state of the T1-T3 cell, and *m* represents the state of T2-T3 cell. The four states are: (0,0), (1,1), (0,1) and (1,0). As is well known, the various states of the device can be controlled by applying voltage pulses between T1-T3 and T2-T3, respectively. This dual cell operation provides for the doubling of the data storage density of the device.

[00049] The principle of operation of this type of dual cell device is based at least in part on the interfaces 19 and 21 between the bistable layer 12 and organic layers 14 and 16. For example, if the device is at the (0,0) state, one can apply a writing voltage pulse to the T1-T3 cell. This results in that charge being stored within that portion of the bistable layer at the interface layer 19. Consequently, it causes the T1-T3 cell to be in the ON-state (1). Since no voltage is applied to the T2-T3 cell, the interfacial layer 21 still remains in the OFF-state (0). Because there are barriers between metallic metal-nanoclusters cores, the stored charge within the metal-nanoclusters layer on the interfacial layer or interface 19 remains in place provided no further negative bias is applied to the interfacial layer 19 via the T1-T3 terminals. Hence, the two cells, T1-T3 and T2-T3 can work independently without interference from each other. One can obtain this double data storage density simply by wiring out the bistable device 10 (T1, T2 and T3) as shown in FIG. 1.

[00050] As is apparent from the above examples, the potential distribution in the organic bistable device with the organic/metal:organic/organic triple layer structure sandwiched between two electrodes (FIG. 1) is asymmetric. When the device switches from the OFF state to the ON state, the potential drop on the top part (4,5,6) has a sharp jump while the potential drop on the bottom part (2,3,4) has a small change. The reason is that the resistance of the bottom part (2,3,4) decreases several orders when the device is switched on.

[00051] Having thus described exemplary embodiments of the present invention, it should be noted by those skilled in the art that the within disclosures are exemplary only and that various other alternatives, adaptations and modifications may be made within the scope of the present invention. Accordingly, the present invention is not limited to the above preferred embodiments and examples, but is only limited by the following claims.

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CLAIMS

What is claimed is:

1. An electrical bistable device comprising:

an electrically conductive mixed layer comprising a first side and a second side, said mixed layer comprising a low conductivity material and a sufficient amount of a high conductivity material wherein said mixed layer is electrically conductive;

a first layer of low conductivity material located on said first side of said mixed layer, said first layer of low conductivity material having a first electrode side;

a second layer of low conductivity material located on said second side of said mixed layer, said second layer of low conductivity material having a second electrode side;

a first electrode attached to said first layer of low conductivity material at said first electrode side;

a second electrode attached to said second layer of low conductivity material at said second electrode side.

a first interface located on the first side of said mixed layer where said first layer of low conductivity material and said mixed layer meet, said first interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage between the said first electrode and the said mixed layer; and

a second interface located on the second side of said mixed layer where said second layer of low conductivity material and said mixed layer meet, said second interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage between the said second electrode and said mixed layer.

2. An electrical bistable device according to claim **1** wherein said low conductivity material is selected from the group consisting of organic semiconductors and organic insulators.

3. An electrical bistable device according to claim 1 wherein said high conductivity material is selected from the group consisting of metals, metal oxides, conducting polymers and organic conductors.

4. An electrical bistable device according to claim 1 wherein said electrically conductive mixed layer is formed by condensing vapors comprising said high conductivity material and said low conductivity material together to form said electrically conductive mixed layer.

5. A method for making a bistable device comprising the steps of:

providing a bottom electrode;

forming a layer of low conductivity organic material on said bottom electrode;

forming an electrically conductive mixed layer on said layer of low conductivity material, said electrically conductive mixed layer comprising a low conductivity material and a sufficient amount of a high conductivity material such that said mixed layer is electrically conductive and wherein an electrically bistable interface is formed between said layer of low conductivity material and said electrically conductive mixed layer;

forming a second layer of low conductivity material on said electrically conductive layer wherein a second electrically bistable interface is formed between said electrically conductive layer and said second layer of low conductivity material; and

forming a top electrode on said second layer of low conductivity material.

6. A method for making an electrical bistable device according to claim 5 wherein said low conductivity material is selected from the group consisting of organic semiconductors and organic insulators.

7. A method for making an electrical bistable device according to claim **5** wherein said high conductivity material is selected from the group consisting of metals, metal oxides, conducting polymers and organic conductors.

8. A method for making an electrical bistable device according to claim **5** wherein said electrically conductive mixed layer is formed by condensing vapors of said high conductivity material and said low conductivity material together to form said electrically conductive mixed layer.

9. A method comprising the step of applying a sufficient electrical voltage between the first and second electrodes of the bistable device according to claim **1** to convert both said first interface and said second interface between said high resistance state and said low resistance state.

10. A method comprising the step of applying a sufficient electrical voltage between the first electrode and the electrically conductive mixed layer of said electrical bistable device according to claim **1** to convert said first interface between said high resistance state and said low resistance state.

11. A method comprising the step of applying a sufficient electrical voltage between the second electrode and the electrically conductive mixed layer of said electrical bistable device according to claim **1** to convert said second interface between said high resistance state and said low resistance state.

12. A memory device comprising:

an electrically conductive mixed layer comprising a first side and a second side, said mixed layer comprising an low conductivity material and a sufficient amount of a high conductivity material wherein said mixed layer is electrically conductive;

a first layer of low conductivity material located on said first side of said mixed layer, said first layer of low conductivity material having a first electrode side;

a second layer of low conductivity material located on said second side of said mixed layer, said second layer of low conductivity material having a second electrode side;

a first interface located on the first side of said mixed layer where said first layer of low conductivity material and said mixed layer meet, said first interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage to said first interface,

a second interface located on the second side of said mixed layer where said second layer of low conductivity material and said mixed layer meet, said second interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage to said second interface;

a first electrode attached to said first layer of low conductivity material at said first electrode side;

a second electrode attached to said second layer of low conductivity material at said second electrode side;

a memory input element for applying a voltage to said first electrode, said second electrode and/or said electrically conductive mixed layer to convert said first interface and/or said second interfaces between said low electrical resistance state and said high electrical resistance state; and

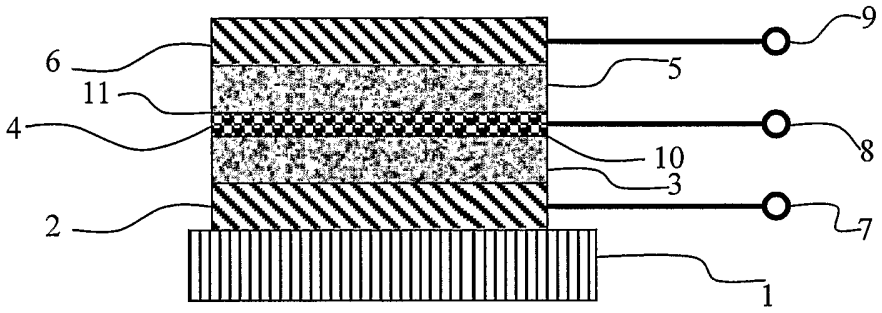
a memory readout element which provides and indication of whether said first interface and/or said second interface is in said low electrical resistance state or said high electrical resistance state.

13. A memory device according to claim **12** wherein said low conductivity material is selected from the group consisting of organic semiconductors and organic insulators.

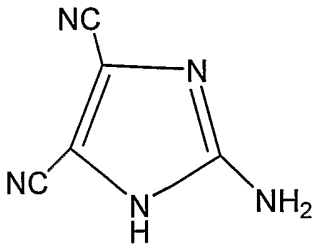
14. A memory device according to claim **12** wherein said high conductivity material is selected from the group consisting of metals, metal oxides, conducting polymers and organic conductors.

15. A memory device according to claim **12** wherein said electrically conductive mixed layer is formed by condensing vapors of said high conductivity and low conductivity materials together to form said electrically conductive mixed layer.

16. A method for operating a memory device according to claim **12** comprising the step of applying a sufficient electrical voltage to said memory input element to convert said first interface and/or said second interface between said high resistance state and said low resistance state.



(a)



(b)

Fig. 1

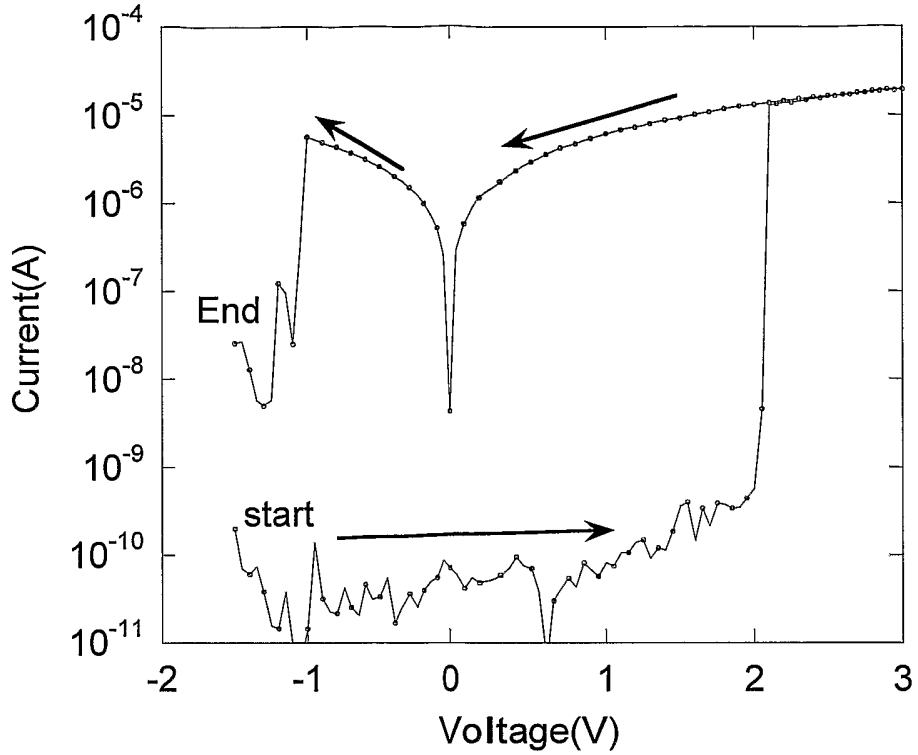

Current(A)
Voltage(V)
End
start
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
-2
-1
0
1
2
3

Fig. 2

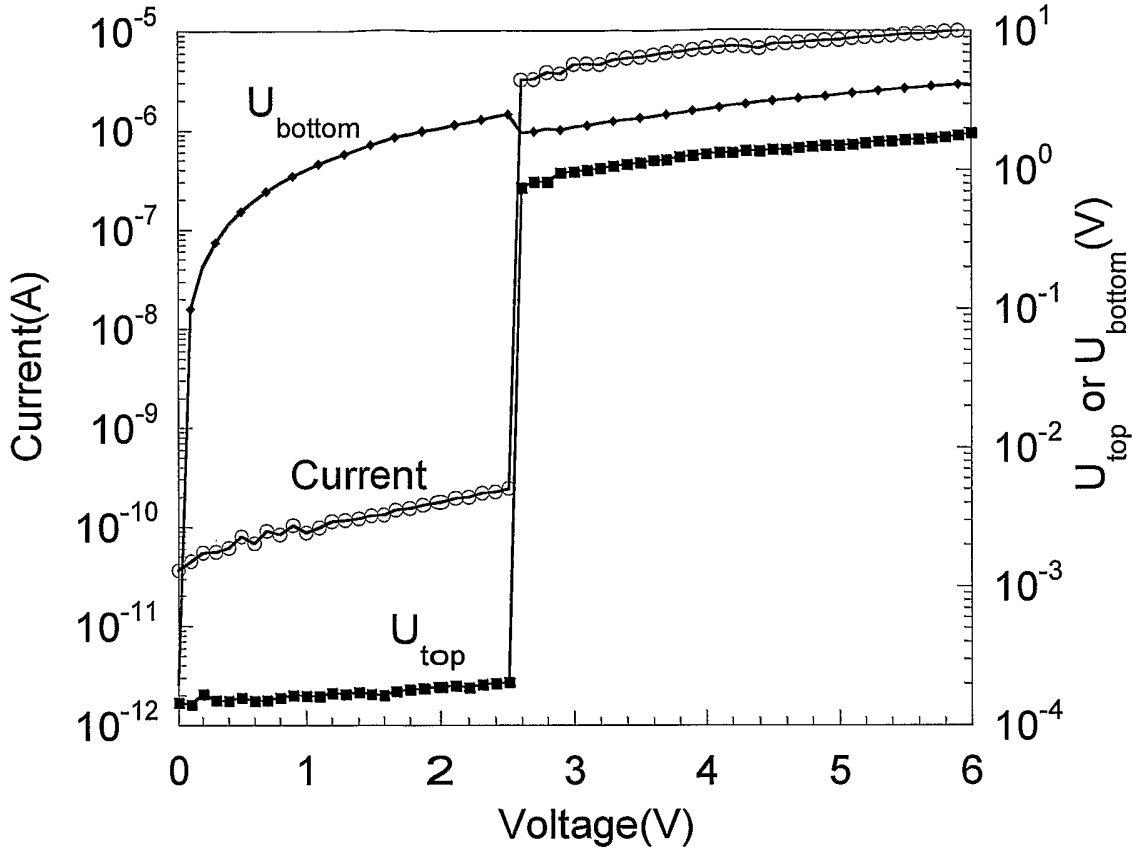

Current(A)
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
U_{bottom}
Current
U_{top}
0
1
2
3
4
5
6
Voltage(V)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
U_{top} or U_{bottom}(V)

Fig. 3

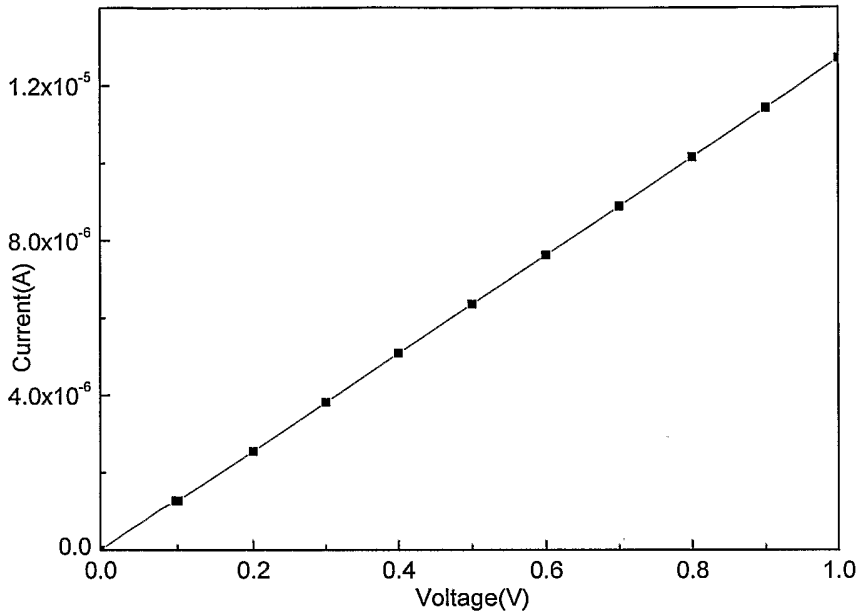


Fig. 4

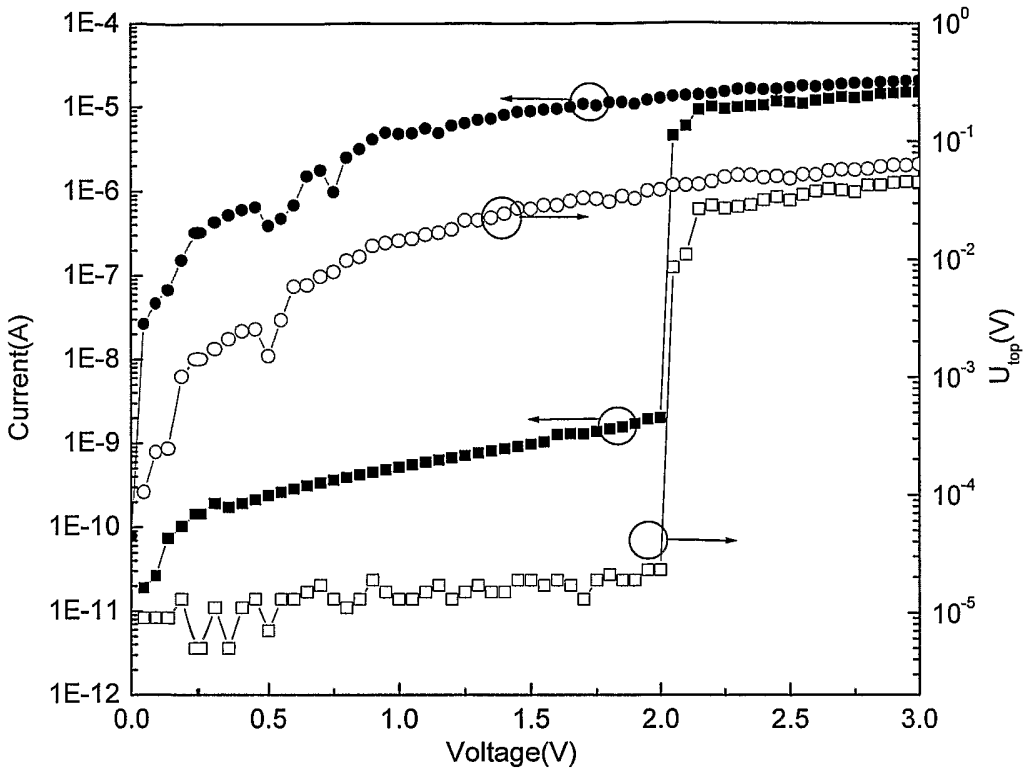

1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
1E-12
Current(A)
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
U_{top}(V)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Voltage(V)

Fig. 5(a)

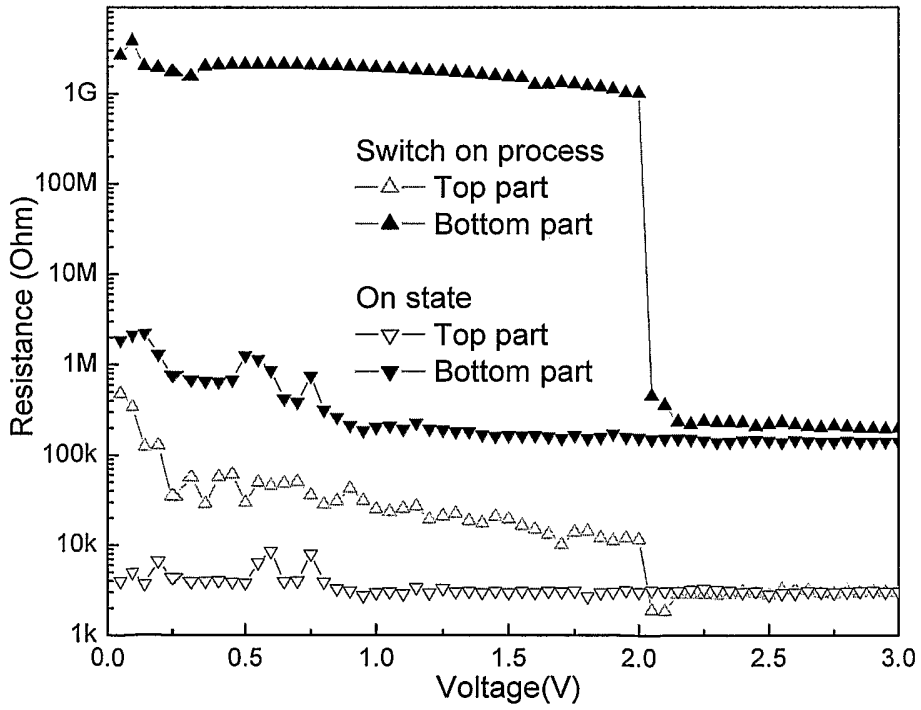

1G
100M
10M
1M
100k
10k
1k
Resistance (Ohm)
Switch on process
Top part
Bottom part
On state
Top part
Bottom part
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Voltage(V)

Fig. 5(b)

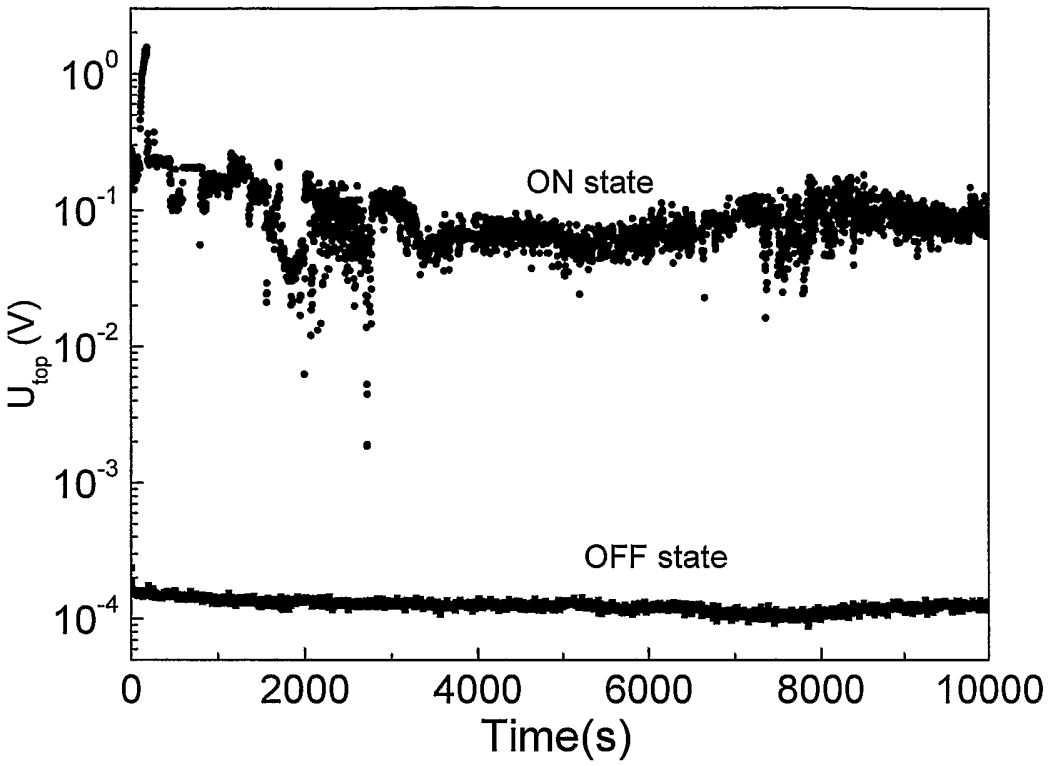

10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
U_{top} (V)
ON state
OFF state
0
2000
4000
6000
8000
10000
Time(s)

Fig. 6

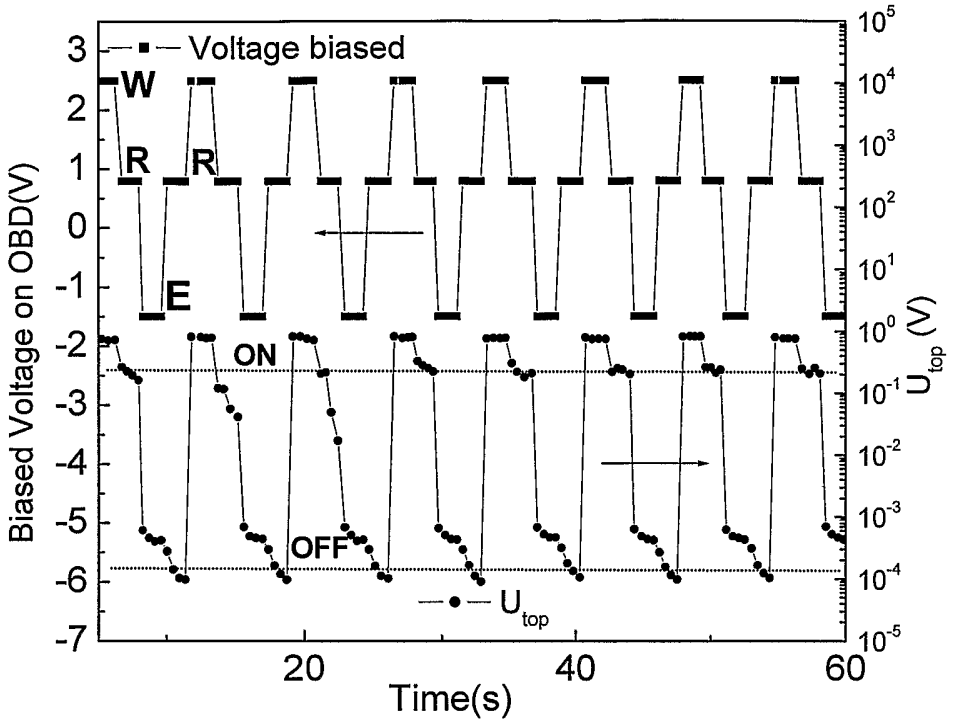

Voltage biased
W
R
R
E
ON
OFF
U_{top}
Biased Voltage on OBD(V)
U_{top} (V)
Time(s)
3
2
1
0
-1
-2
-3
-4
-5
-6
-7
10^5
10^4
10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
20
40
60

Fig.7(a)

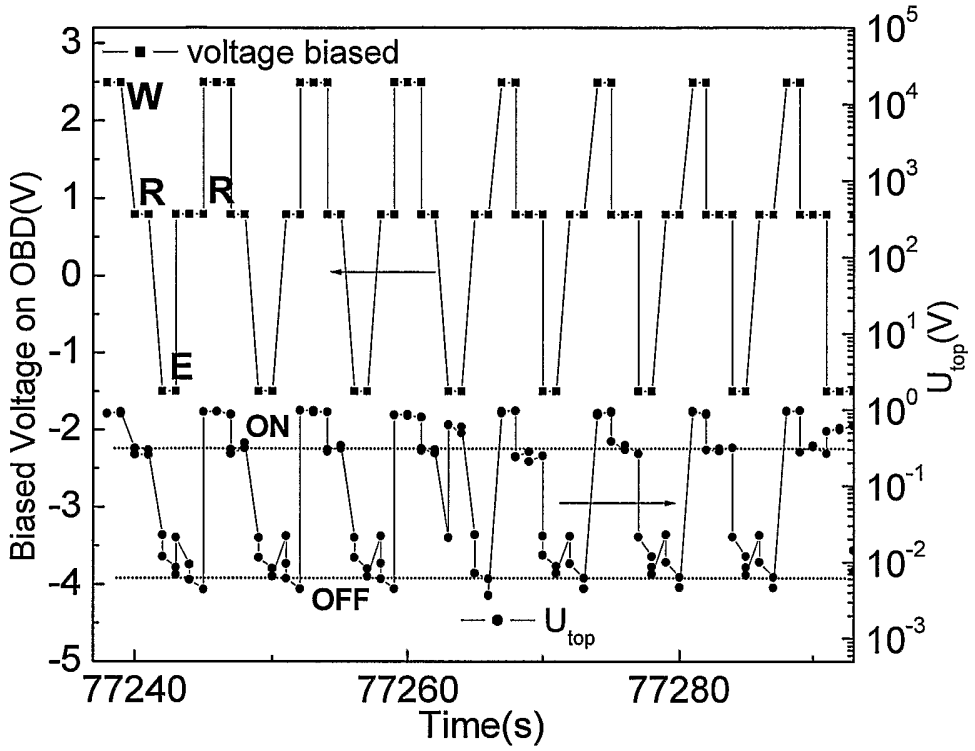

voltage biased
W
R
R
E
ON
OFF
U_{top}
Biased Voltage on OBD(V)
U_{top}(V)
Time(s)
3
2
1
0
-1
-2
-3
-4
-5
77240
77260
77280
10^5
10^4
10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}

Fig. 7(b)