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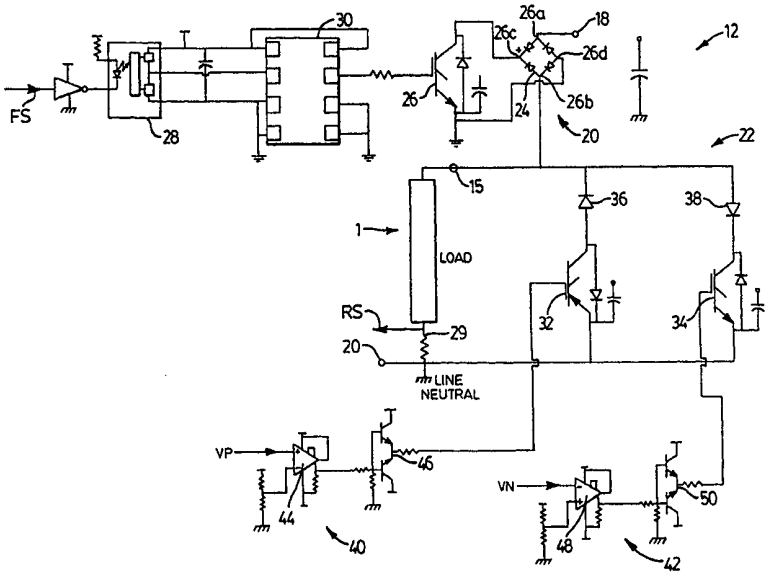
(54) Title: APPARATUS FOR DIMMING A FLUORESCENT LAMP WITH A MAGNETIC BALLAST




(57) Abstract

A current controlled dimmer for controlling the output intensity of a fluorescent lamp with a magnetic ballast. The current controlled dimmer generates an AC current which follows the shape of the AC line voltage for the fluorescent lamp. The light intensity output of the fluorescent lamp is controlled by varying the amplitude of the AC current. The AC current is generated using a pulse width modulator (PWM) to modulate the AC line voltage. The current controlled dimmer (10) utilizes a feedback control loop which applies proportional and integral (PI) control to the PWM modulation. In another embodiment of the current controlled dimmer, the AC current is generated by rectifying the AC line voltage and modulating the rectified voltage by a pulse width modulator (PWM) into positive and negative cycles to generate a 60 Hz AC current signal.

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TITLE: APPARATUS FOR DIMMING A FLUORESCENT LAMP WITH A MAGNETIC BALLAST

## FIELD OF THE INVENTION

The present invention relates to a dimmer for fluorescent lighting systems, and more particularly to a dimmer which controls the AC current from the power line to vary the output intensity of a fluorescent lamp having a magnetic ballast.

## BACKGROUND OF THE INVENTION

One way of controlling escalating energy costs is by limiting energy consumption. In a modern office building, the principle energy consumers are lighting and heating and cooling. To conserve energy, the thermostat is "turned back" and the lighting is reduced during non-office hours. Reducing the energy consumption from lighting essentially involves dimming the lamps or turning off selected lamps. To conserve energy during non-office hours, most banks of lamps on a floor are turned off, with a few banks of lamps being left on to provide some lighting for security. The other approach to conserving energy consumption involves dimming the fluorescent lamps during non-office hours. As a result of being dimmed less power is consumed, while at the same time a minimum light level is maintained for security purposes.

In a typical office building the lighting system comprises banks or groups of fluorescent lamps. A fluorescent lamp is a type of lamp in which light is generated by fluorescence. The most common form of fluorescent lamp comprises a gas-discharge tube which

contains a low-pressure gas such as mercury. The inner surface of the tube is coated with phosphor and when a current passes through the tube a discharge results and the ultraviolet radiation produced strikes the phosphor which then emits visible radiation. To start the discharge, i.e. turn on the lamp, the current must be provided at a sufficiently high voltage level, and typically a form of ballast circuit is utilized to produce the discharge current.

Compared to incandescent lamps, fluorescent lamps present special problems with respect to dimming. Various solutions have been proposed for dimming fluorescent lamps, including a magnetic ballast, an electronic ballast, and an electronically tapped voltage transformer.

The magnetic ballast solution produces a high voltage when there is no discharge in the lamp (i.e. the lamp is not conducting) and also feeds a "cathode heater circuit". When the arc (i.e. discharge) starts in the tube, the voltage at the output of the secondary winding on the ballast collapses to a level which is necessary to sustain the arc. The ballast absorbs, i.e. through its inductance, the excess voltage from the power source. There have been several dimmers proposed in the art based on the variation of the voltage controlling the discharge in the lamp, but none of these solutions have achieved any commercial success.

Another type of known dimmer for fluorescent lamps is based on an electronic ballast. The electronic ballast generates a rectified DC voltage from a power source and injects a resonant current into the lamp tube.

The resonant current has a relatively high frequency (typically 20 kHz) and as a result special tubes are required for the fluorescent lamps. Each lamp requires an electronic ballast. The electronic ballast is modified for dimming control by providing a variable DC voltage.

In view of the shortcomings with the state of art devices, there remains a need for a dimmer for use with fluorescent and other types of gas discharge lamps.

## BRIEF SUMMARY OF THE INVENTION

The present invention provides a current controlled dimmer for fluorescent lamps. The current controlled dimmer generates a feedback controlled current signal output with a waveshape which follows the voltage drive signal for the lamp. By varying the amplitude of the current output signal, the output intensity of the fluorescent lamp can be decreased (i.e. dimmed) or increased (i.e. intensified). According to the invention, the voltage drive signal across the lamp electrodes (i.e. ballast) is kept constant and a constant heating current is maintained so that the lamp can respond almost instantaneously to an increase in the amplitude of the current signal.

In accordance with the present invention, the current signal output is obtained by modulating the AC line (i.e. drive) voltage to generate an AC current signal. The current controlled dimmer utilizes a feedback control loop which applies proportional/integral (PI) control to the PWM control signal to superimpose a fast response (e.g. 2 kHz) over the steady state base chopping rate. Advantageously, this feature eliminates noticeable flicker in the lamp

output. The generated AC current signal output has a quasi-sinusoidal waveform which follows the sinusoidal voltage waveform over the range of operation.

In one aspect, the present invention provides an apparatus for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, the apparatus comprises: (a) means for coupling an AC supply voltage to the magnetic ballast for energizing the ballast to produce a discharge in the gas discharge lamp; (b) means for generating an intensity level signal for setting the output intensity level for the lamp; (c) switch means for switching the AC supply voltage to generate an AC current for powering the gas discharge lamp, the switch means being responsive to a chopping control signal for varying the amplitude of the AC current and thereby varying the output intensity of the lamp; (d) controller means for controlling the switch means, the controller means including a pulse width modulator for generating the chopping control signal, the pulse width modulator having means responsive to the intensity level signal for generating the chopping control signal with a duty cycle derived from the intensity level signal.

In another aspect, the present invention provides an apparatus for controlling the output intensity level of a gas discharge lamp having a magnetic ballast or a group of lamps each having a magnetic ballast and being connected to a single protection device such as a circuit breaker or fuse, the apparatus comprising: (a) means for coupling an AC voltage to the magnetic ballast for energizing the ballast to produce a discharge in the gas discharge lamp; (b) means for generating an intensity level signal for setting the output intensity level for the lamp; (c) switch

means for switching the AC voltage to generate an AC current for powering the gas discharge lamp, the switch means being responsive to a chopping control signal; (d) controller means for controlling the switch means, the controller means having means responsive to the intensity level signal and including a pulse width modulator for generating the chopping control signal and the chopping control signal having a duty cycle derived from the intensity level signal.

In yet another aspect, the present invention provides a method for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, the method comprising the steps of: (a) applying a voltage to the magnetic ballast for energizing the ballast and producing a discharge in the gas discharge lamp; (b) modulating the voltage to produce an alternating current for powering the gas discharge lamp, the alternating current having a controllable waveshape substantially following a reference signal; (c) generating an intensity level signal from the reference signal for setting the output intensity of the lamp; (d) varying the modulation of the voltage in response to an error signal, the error signal comprising the difference between the intensity level signal and a feedback current signal, so that the output intensity level of the gas discharge lamp follows the reference signal.

In another aspect, the present invention provides a method for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, the method comprising the steps of: (a) applying a voltage to the magnetic ballast for energizing the ballast and producing a discharge in the gas discharge lamp; (b) modulating the

voltage signal to produce an alternating current with a variable magnitude for powering the gas discharge lamp; (c) inputting an intensity level signal for setting the output intensity level of the lamp; (d) varying the modulation of the voltage in response to the intensity level signal to change the magnitude of the alternating current and thereby vary the output intensity of the gas discharge lamp.

In another aspect, the present invention provides, an apparatus for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, the apparatus comprises: (a) means for coupling an AC supply voltage to the magnetic ballast for energizing the ballast to produce a discharge in the gas discharge lamp; (b) means for generating an intensity level signal for setting the output intensity level for the lamp; (c) switch means for switching said AC supply voltage to generate an AC current for powering the gas discharge lamp, the switch means being responsive to a chopping control signal for varying the amplitude of the AC current and thereby varying the output intensity of the lamp; (d)controller means for controlling the switch means, the controller means including means responsive to the intensity level signal for generating a chopping control signal with a duty cycle derived from the intensity level signal.

Advantageously, the current controlled dimmer according to the present invention provides the following beneficial features. Current control of the lamp output suppresses flicker which results in a steady light emission from the lamp. The constant light emission, in turn, produces a perceived brighter output even though the lamp is powered at a lower level. Operation at less than full power (e.g. 80%) improves the operating life of the ballast

in the lamp by reducing excess heating. Furthermore, the balancing of the current signal also reduces overheating in the ballast and eliminates harmonics. It has been found that the injection of even order harmonics can be particularly detrimental to the longevity of the ballast in a fluorescent lamp. In addition, the slight lag in the current feedback produces a phase advance in the current signal which allows the power factor to be maintained above 0.9.

## BRIEF DESCRIPTION OF THE DRAWINGS

Reference will now be made to the accompanying drawings which show, by way of example, preferred embodiments of the present invention, and in which:

Fig. 1 shows in block diagram a current controlled dimmer for a fluorescent lamp;

Figs. 2(a) to 2(f) are timing diagrams for signals associated with the current controlled dimmer of Fig. 1;

Fig. 3 is a schematic diagram of a power stage for the current controlled dimmer of Fig. 1;

Fig. 4 is a schematic diagram of a firing logic stage for the current controlled dimmer of Fig. 1;

Fig. 5 is a schematic diagram of a control circuit stage for the current controlled dimmer of Fig. 1;

Fig. 6 is a block diagram of a current controlled dimmer according to another embodiment of the present invention;

Fig. 7 is a schematic diagram of a power and driver stage for the current controlled dimmer of Fig. 6;

Fig. 8 is a schematic diagram of a PWM gate generation stage for the current controlled dimmer of Fig. 6;

Fig. 9 is a schematic diagram of proportional-integral control stage for the current controlled dimmer of Fig. 6;

Fig. 10 is a schematic diagram of a lockout circuit for the current controlled dimmer of Fig. 6;

Fig. 11 is a schematic diagram of an open-loop current controlled dimmer according to another embodiment of the present invention;

Fig. 12 is a schematic diagram of the current controlled dimmer of Fig. 11 with a feedback control loop;

Fig. 13 is a schematic diagram showing the relationship between exemplary modulation pattern curves and a voltage half cycle for the current controlled dimmer according to the present invention; and

Figs. 14(a) and 14(b) are schematic diagrams showing alternative implementations for circuitry in the current controlled dimmer.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As will now be described, the present invention comprises a current controlled dimmer as shown in Fig. 1 and denoted generally by reference 10. The current controlled dimmer 10 according to the invention generates a current signal which follows the shape of the AC drive or line voltage signal for a fluorescent lamp. The light intensity output of the fluorescent lamp is controlled by varying the amplitude of the current signal. The current signal is generated by using a pulse width modulator (PWM) to modulate the AC line voltage. The current controlled dimmer 10 utilizes a feedback control loop which applies proportional/integral (PI) control to the PWM control signal to superimpose a fast response (i.e. 2 kHz) over the steady state base chopping rate.

As will be familiar to those skilled in the art, a fluorescent light or lamp assembly 1 (Fig. 1) typically comprises a magnetic ballast 2 and a pair of glass tubes 3 and 4. The glass tubes 3 and 4 are typically filled with mercury vapour and have a phosphorescent coating on the inside surface. Excitation of an electrode in each of the glass tubes 3,4 with a high voltage causes ionization of the mercury vapour and the emission of ultraviolet light. The ultraviolet light activates the fluorescent coating on the inside surface of the glass tubes 3 and 4. More specifically, the electrons emitted by the electrode collide with electrons in the outer rings of the mercury atoms and ultraviolet radiation is produced. The ultraviolet radiation, in turn, acts on phosphor crystals applied to the inside of the glass wall to produce light. The electrode is connected in series to the magnetic ballast 2. The ballast 2 comprises an iron-core inductive element which provides the required high starting voltage

for energizing the electrode while limiting the operating current.

Reference is now made to Fig. 1 which shows in block diagram form a current controlled dimmer 10 for use with a fluorescent light or lamp assembly 1 or a group of lamp assemblies, shown individually as 1a, 1b,... 1n. Each lamp assembly 1 includes a pair of fluorescent tubes 3 and 4, and the magnet ballast 2. The lamp assemblies 1 are connected in parallel to the current controlled dimmer 10 and dimmer 10 is provided for each circuit breaker (not shown) which is connected to a group of lamp assemblies 1. For example, for a 15 Ampere circuit breaker (not shown) ten to twelve lamp assemblies 1 (nominally rated at 1 Ampere each) would be connected to single current controlled dimmer 10. As will be described, the current controlled dimmer 10 according to the present invention varies the amplitude of the current to the magnetic ballast 2 in order to control output intensity of the fluorescent tubes 3 and 4 in the lamp assembly 1.

As shown in Fig. 1, the current controlled dimmer 10 comprises a power stage 12, a firing stage 14, and a control circuit 16. The ballast 2 in the lamp assembly 1 is coupled to a live output terminal 19 from the power stage 12, and the return or neutral line 20 for the AC supply or line voltage. The power stage 12 is powered by AC line or supply voltage which is connected to live 18 and neutral 20 terminals. The AC line voltage is typically 110 or 220 Volts RMS.

Reference is made to Fig. 3, which shows the power stage 12 in greater detail. The power stage 12 comprises an AC switching stage 20 and an output stage 22.

The AC switching stage 20 switches the AC line voltage through the load, i.e. lamp assembly 1, in response to a modulation or chopping control signal FS which is generated by the firing logic stage 14 (Fig. 4). The output stage 22 controls the cycling of the current signal through the magnetic ballast 2 (Fig. 1) as will be described below.

The AC switching stage 20 comprises a full-wave bridge rectifier 24 and an insulated gate bipolar transistor (IGBT) 26. In known manner, the bridge rectifier 24 comprises four diodes D which are connected in a bridge configuration to form two pairs of nodes or junctions 26a,26b and 26c,26d. The AC line voltage from terminal 18 is applied to node 26a, and the other node 26b forms the live output terminal 19 which is connected to the live terminal of the ballast 2 (Fig. 1). The return terminal in the ballast 2 is coupled to the neutral return terminal 20 through a shunt resistor 29. The shunt resistor 29 provides a shunt current output signal RS which is utilized by the control circuit 16 as will be described below. The other pair of nodes 26c,26d are connected across the collector and emitter of the IGBT 26. The transistor 26 functions as the actuator for the AC switch 20 (i.e. bridge 24). The base of the transistor 26 receives a chopping or modulation control signal FS from the firing logic stage 14. To allow for a floating power supply, the modulation control signal FS is coupled through an opto-isolator 28. The output of the opto-isolator 28 is coupled to the base of the IGBT 26 through a driver 30, such as the IR2121. The driver 30 provides 0 to +15V offset for the modulation control signal FS for turning the IGBT 26 ON and OFF. The emitter of the IGBT 26 is connected to isolated ground. When the modulation or chopping control signal FS is HIGH, the IGBT 26 is ON and

thus the AC switch 20 is closed, and a current derived from the AC line voltage will flow through the bridge 24 into the magnetic ballast 2 in the lamp assembly 1. Conversely, when the modulation control signal FS is LOW, the IGBT 26 is turned OFF and the AC switch 20 is opened. However, while the AC switch 20 is opened, a free-wheeling path across the load (i.e. the magnetic ballast 2 in the lamp 1) has to be established, and the AC current through the load is modulated with the AC switch 20.

As shown in Fig. 3, the output stage 22 comprises a PNP insulated gate bipolar transistor 32 and a NPN insulated gate bipolar transistor 34. The PNP IGBT 32 together with a diode 36 are coupled across the load (i.e. magnetic ballast 2) as shown. Similarly, the NPN IGBT 34 and diode 38 are also coupled across the magnetic ballast 2. The emitters of both the IGBT's 32, 34 are coupled to the neutral line 20 which serves as the common ground for the dimmer 10. The IGBT's 32, 34 and associated diodes 36, 38 provide free-wheeling paths when the AC switch 20 is open. Since the magnetic ballast 2 comprises an inductive load, a path must be provided to remove the energy stored in the ballast 2 when the switch 20 is open. The IGBT 34 and diode 38 provide a free-wheeling path for the negative cycle of the AC, and the IGBT 32 and diode 36 provide a path for the positive cycle. Each of the IGBT's 32, 34 are actuated by respective drive circuits 40, 42. The drive circuit 40 receives a voltage logic control signal VP generated by the firing logic stage 14, and the drive circuit 40 receives a voltage logic control signal VN, also from the firing logic stage 14. The drive circuit 40 comprises a level shifter 44 for producing a ± 15V output. The level shifter 44 includes a push-pull output circuit 46 which is coupled to the base of the IGBT 32. Similarly,

the other drive circuit 42 comprises a level shifter 48 for producing a ±15V output and includes a push-pull circuit 50 coupled to the base of the IGBT 34. To turn ON the IGBT 32, -15V is applied to the base, whereas +15V is applied to the base to turn ON the other IGBT 34.

Referring still to Fig. 3, the insulated gate bipolar transistors 32, 34 and diodes 36, 38 which provide the free-wheeling paths in the output stage 22 may be replaced by the free-wheel circuits 35a, 35b shown in Fig. 14(a). The implementation of which will be apparent to those skilled in the art.

Reference is next made to Fig. 4 which shows the firing logic stage 14 in more detail. As described above, the firing logic stage 14 generates the modulation or chopping control signal FS. The modulation control signal FS controls the actuation of the AC switching stage 20 which in turn controls the amplitude of the AC current signal applied to the magnetic ballast 2 in the lamp assembly 1 or assemblies 1a to 1n. In addition to the modulation signal FS, the firing logic stage 14 generates the voltage logic control signals VP and VN.

As shown in Fig. 4, the firing logic stage 14 comprises a voltage pulse generator circuit 100, a current pulse generator circuit 102, a pulse width modulator circuit 104, a dimmer level circuit 106, and an output logic circuit 108.

The voltage pulse generator circuit 100 generates the voltage logic control signals VP and VN described above for the power stage 12. The logic control signals VP and VN are derived from the AC line voltage signal as shown in

Figs. 2(c) and 2(d). The logic control signal VP corresponds to the positive cycle of the AC line voltage $V_{AC}$, and the logic control signal VN corresponds to the negative cycle of the AC line voltage $V_{AC}$. As shown in Fig. 4, the voltage pulse generator circuit 100 comprises a signal transformer 110 having a primary coupled to the AC line voltage $V_{AC}$. The output from the secondary of the transformer 110 is coupled to a voltage follower 112 through a voltage divider 113. The voltage follower 112 provides a synchronizing voltage signal. As shown in Fig. 4, the output from the voltage follower 112 feeds a first comparator 114 and invertor 116 which generate the positive voltage logic control signal VP for the voltage waveform $V_{AC}$ (Fig. 2(a)). The voltage follower 112 also feeds a second comparator 118 and invertor 120 which generate the negative voltage logic control signal VN for the voltage waveform $V_{AC}$ (Fig. 2(a)). The voltage logic control signals VP and VN from the generator circuit 100 provide inputs to the output logic circuit 108.

The other inputs to the output logic circuit 108 comprise a positive current logic control signal CP and a negative current logic control signal CN. The current logic control signals CP and CN are used by the output logic circuit 108 to generate the modulation control signal FS (as will be described below). The current logic control signals CP and CN are derived from a conditioned current feedback signal CFB which is received at input 122 from the control circuit 16. Referring to Fig. 5, the conditioned current feedback signal CFB is derived from the shunt current output signal RS from the shunt resistor 29 (Fig. 2). The shunt current signal RS represents the current flowing in the load, i.e. the magnetic ballast 2. As shown in Fig. 5, the conditioned current feedback signal CFB is

generated by first converting the shunt current RS into a voltage signal using a current-to-voltage converter 200. The output from the current-to-voltage converter 200 is amplified by a non-inverting amplifier 202 with an adjustable gain set by a potentiometer 203. The output from the amplifier 202 is filtered by a second order Butterworth filter 204 comprising amplifiers 205, 206 configured as shown in Fig. 5. The output from the filter 204 is fed to another inverting amplifier 208 which is configured with a level shifter comprising a potentiometer 209 for correcting offset in the conditioned current feedback signal CFB. In the present embodiment, the peak value of the current signal CFB is set to approximately 5 Volts.

Referring back to Fig. 4, the current pulse generator circuit 102 comprises a first comparator 124 and inverter 126 and a second comparator 128 and inverter 130. The conditioned current feedback signal CFB from the control circuit 16 is coupled to the input of each comparator 124, 128. The first comparator 124 and inverter 126 are configured to generate the logic control signal CP for the positive half-cycle of the AC current waveform $I_{AC}$ as shown in Fig. 2(e). Similarly, the second comparator 128 and inverter 130 are configured to generate the logic control signal CN for the negative half-cycle of the AC current waveform $I_{AC}$ as shown in Fig. 2(f). The configuration of the comparators 124, 128 will be within the understanding of those skilled in the art. The logic control signals CP and CN are used by the output logic circuit 108 as will be described below.

Referring again to Fig. 4, the pulse width modulator circuit 104 generates a pulse width modulation

signal PWM which is used by the output logic circuit 108 to generate the chopping or modulation control signal FS. The pulse width modulator circuit 104 comprises a pulse width modulation generator 132. Preferably, the generator 132 is implemented using a commercially available PWM generator chip, as will be familiar to one skilled in the art. In known manner, the PWM generator 132 is configured to produce a 20kHz frequency for the pulse width modulation signal PWM. A potentiometer 133 is included for adjusting the output frequency of the generator 132. The pulse width or duty cycle of the pulse width modulation signal PWM is determined by a pulse width modulation level control signal PWMlev. The control signal PWMlev is generated by the control circuit 16 as will now be described.

Referring to Fig. 5, the control circuit 16 generates the modulation level control signal PWMlev from the conditioned current feedback signal CFB and a demand adjust signal $V_{ADJ}$. The demand adjust signal $V_{ADJ}$ represents the desired output level for the lamp assembly 1. The demand adjust signal $V_{ADJ}$ may be set manually or automatically, for example, under computer control as part of lighting control system for an office building or plant. As shown in Fig. 5, the demand adjust signal $V_{ADJ}$ is set using a manually adjustable potentiometer 210. The potentiometer 210 is connected to the output of a rectifier 111 (Fig. 4) which is coupled across the secondary of the transformer 110 (Fig. 4) to generate a rectified voltage reference signal ~V. The output, i.e. wiper, of the potentiometer 210 is coupled to a voltage follower or unity gain buffer 212 which provides the output for the demand adjust signal $V_{ADJ}$. It will be appreciated that the demand adjust signal $V_{ADJ}$ comprises a rectified sinusoidal signal derived from the AC line voltage $V_{AC}$ through the transformer

110 and rectifier 111 (Fig. 4) the amplitude of which is manually controlled by the potentiometer 210. Alternatively, the voltage reference signal ~V may be derived from sinusoidal signal tapped from the transformer 110 and controlled by a variable gain amplifier (not shown) via a microcontroller interface (not shown). In another variation, a sinusoidal signal locked to the AC line voltage $V_{AC}$ is generated utilizing a variable amplitude output signal from a microcontroller. As shown in Fig. 5, the demand adjust signal $V_{ADJ}$ forms one input to an error circuit 214. The other input to the error circuit 214 is derived from the conditioned current feedback signal CFB as will now be described.

As shown in Fig. 5, the conditioned current feedback signal CFB is fed into a precision rectifier 216 which comprises two operational amplifiers 218, 222 and diodes 220a, 220b configured in known manner. The output signal from the rectifier 216 is conditioned by a voltage follower or unity gain buffer 224 to produce a load current output signal ~C and also provide isolation. The load current output signal ~C provides the other input to the error circuit 214. The error circuit 214 comprises an operational amplifier 215 which is configured in known manner to produce an output signal comprising the sum of the rectified signal CFB and the demand adjust signal $V_{ADJ}$. The output of the error circuit 214 provides an error signal Err which represents the difference between the desired demand, i.e. signal $V_{ADJ}$, and the actual load current, i.e. signal ~C.

Referring to Fig. 5, the error signal Err from the error circuit 214 is fed to a proportional/integral (P/I) feedback control loop indicated generally by

reference 225. The feedback control loop 225 comprises two branches: an integral control branch 226 and a proportional control branch 228. The integral controller 226 provides a long time constant and is intended to control the steady state level of the sinusoidal waveform. The integral controller 226 generates a DC base voltage which represents the steady state PWM modulation rate for the pulse width modulation generator 132. The proportional controller 228, on the other hand, is used to correct errors between the desired demand and the actual load current. The proportional controller 228 provides the dynamic modulation signal which directs the pulse width modulation generator 132 to produce the desired sinusoidal shape for the AC current signal $I_{AC}$. The outputs from the integral controller 226 and the proportional controller 228 are mixed with a ramped signal ~P to generate the pulse width modulation level control signal PMWlev.

As shown in Fig. 5, the proportional controller 228 comprises first 230 and second 232 inverting amplifiers. The first inverting amplifier 230 includes a potentiometer 231 for adjusting the gain on the error signal Err. The second inverting amplifier 232 further conditions the error signal Err and produces an error output signal which is enabled by (i.e. summed with) the ramped signal ~P generated by the start-up chopping enable block 106 (Fig. 4). The sum of the error output signal and the signal ~P are applied to the negative input of a PWM mixer 234 which is implemented with a differencing amplifier. As shown in Fig. 5, the positive input of the differencing amplifier 234 receives the output from the steady state integral controller 226.

Referring back to Fig. 4, the signal ~P is derived from a chopping (i.e. dimmer) enable signal $C_{enable}$ which is generated by a switch SW1. The chopping enable signal $C_{enable}$ is active LOW and chopping is enabled when the switch SW1 is open. When the switch SW1 is closed, the chopping enable signal $C_{enable}$ is pulled HIGH, and the modulation control signal FS is disabled (by the output logic 108 as will be described below) so that the full AC line voltage $V_{AC}$ is applied to the lamp assembly 1. The signal ~P is generated by utilizing an integrator 134 to slowly ramp the chopping enable signal $C_{enable}$. As shown in Fig. 4, the ramped signal ~P from the integrator 134 is coupled to the negative input of the differencing amplifier 234 (Fig. 5) through a unity gain buffer or voltage follower 136.

Referring to Fig. 5, the integral controller 226 provides integral control for steady state conditions by generating a DC base voltage which corresponds to the steady PWM rate for the PWM generator 132. The integral controller 226 comprises a first inverting amplifier 236, a second inverting amplifier 238, and an integrator 240. The error signal Err (i.e. the difference between the demand setting $V_{ADJ}$ and the actual load current signal ~C) is applied to the first amplifier 236 which includes a potentiometer 237 for adjusting the gain. The error signal Err is further conditioned by the second amplifier 238 before being applied to the integral controller 226. The amplifiers 236, 238 and the integrator 240 are configured in known manner using operational amplifiers and discrete components as will be within the understanding of those skilled in the art. The output of the integrator 240 is buffered by a voltage follower 242 and coupled to the positive input of the differencing amplifier 234 through a

level shifter 244 which allows the level of the integrated error signal Err to be adjusted. As shown in Fig. 5, the level shifter 244 comprises an operational amplifier 246 configured as a unity gain amplifier with a potentiometer 248 coupled to the non-inverting input of the op-amp 246. The pulse width modulation level control signal PWMlev is generated by the PWM mixer 234 as the difference between the steady state error signal (i.e. the output of the integral controller 226) and the sum of the ramped chopped enable signal ~P and the instantaneous error signal (i.e. the output of the proportional controller 228). The pulse width modulation level control signal PWMlev is fed to the PWM generator 132 through a buffer 138. It will be appreciated that the pulse width modulation level signal PWMlev provides an input signal which controls the duty cycle of the pulse width modulation signal PWM under steady state and error conditions.

Referring to Fig. 4, the output logic circuit 108 generates the chopping control signal FS from the voltage logic control signals VP and VN, the current logic control signals CP and CN, and the pulse width modulation signal PWM from the PWM generator 132. In this aspect, chopping or modulation of the AC voltage signal $V_{AC}$ is only allowed when the voltage and current cycles have the same polarity. This condition is fulfilled by logically AND'ing the respective voltage logic control signals VP, VN and the current logic control signals CP, CN. As shown in Fig. 4, the output logic circuit 108 includes an AND logic gate 140 to logically AND the positive voltage logic control signal VP and the positive current logic control signal CP, and another AND gate 142 to logically AND the negative voltage VN and current CN logic control signals. The outputs of the two AND gates 140, 142 are logically OR'd by OR gate

144 so that either condition, i.e. positive polarity or negative polarity, enables generation of the chopping control signal FS. The output of the OR gate 144 is logically AND'd by gate 146 with the output of another AND gate 148. The output of gate 148 comprises the pulse width modulation signal PWM which is enabled by the chopping enable signal $C_{enable}$. Accordingly, the chopping control signal FS is only active when the voltage and current signals have the same polarity and the chopping enable is active.

Referring still to Fig. 4, the output logic circuit 108 includes a delay circuit denoted generally by 109. The delay circuit 109 serves to force a minimum delay for the turn-off time of IGBT 26. As shown in Fig. 4, the delay circuit 109 comprises a delay generator 150 and an AND gate 152. The delay generator 150 is triggered by the rising edge of the output from the AND gate 146. The output from the AND gate 146 is inverted by inverter 154 and provides one input to the AND gate 152. The other input is the delayed output signal from the delay generator 150. Accordingly, the chopping control signal FS is delayed by the generator 150 for a predetermined period. The delay period is based on the turn-off time for the IGBT 26 and for the present embodiment is set at 5 $\mu$sec.

In operation, the dimming function is enabled by opening the switch SW1 (Fig. 4) and manually setting the demand or dimming level for the light assembly 1 using the potentiometer 210 (Fig. 5). In response to the opening of the switch SW1, chopping is enabled by the chopping enable signal $C_{enable}$, and the demand level setting $V_{ADJ}$ is converted into a pulse width modulation level PWMlev (Fig. 5) for the pulse width generator 132 (Fig. 4). The pulse width

generator 132, in turn, generates an output signal PWM with the appropriate duty cycle. The pulse width modulation signal PWM is mixed with the output of OR gate 144 (derived from the voltage logic control signals VP, VN and the current logic control signals CP, CN) so that chopping only occurs when the cycles in the AC voltage $V_{AC}$ and AC current $I_{AC}$ signals (Fig. 2(a)) have the same polarity. In this way, the resulting AC current signal $I_{AC}$ (Fig. 2(b)) is quasi-sinusoidal and essentially tracks the AC voltage $V_{AC}$. If there is a change in the demand or an error between the demand level and the actual load current, the control circuit 16 adjusts the pulse width modulation level PWMlev (Fig. 5) which in turn adjusts the chopping control signal FS. Advantageously, the current controlled dimmer 10 substantially reduces noticeable flicker in the lamp output, and the quasi-sinusoidal shape of the current reduces harmonics which are potentially harmful to the magnetic ballast 2. In addition, the delay introduced by the proportional/integral feedback control loop 225 (Fig. 5) results in a high power factor, typically 0.9 or better.

Another embodiment of a current controlled dimmer according to the present invention is shown in Fig. 6 and depicted generally by reference 300. The current signal is generated by rectifying the AC line voltage and modulating the rectified voltage by a PWM (Pulse Width Modulator) into positive and negative cycles to generate a 60 Hz AC current signal. Referring to Fig. 6, the current controlled dimmer 300 comprises a power output stage 301, a pulse width modulation (PWM) gate generation stage 302, a proportional and integral (P/I) controller stage 303, a reference demand circuit 304, and a lockout circuit 305.

The power output stage 301 is coupled to the fluorescent lamp assembly 1 (or group of lamp assemblies 1a to 1n) and provides the drive voltage and current. The power output stage 301 comprises an IGBT output drive circuit 310. The IGBT output drive circuit 310 includes four insulated gate bipolar transistors (IGBT's), denoted individually as 314, 316, 318, 320, which are connected in an H-bridge configuration as will be familiar to those skilled in the art. The first pair of IGBT's 314, 316 are driven by a first IGBT driver 315, and the second pair of IGBT's 318, 320 are driven by a second IGBT driver 319. The drivers 315, 319 may be implemented using a commercially available device such as the IR2110 as will be familiar to one skilled in the art. The bridge for the output drive circuit 310 is supplied from a rectified non filtered line voltage ~V. The rectified line voltage ~V is generated by a line synchronization circuit 312 as shown in Fig. 8.

Referring to Fig. 8, the line synchronization circuit 312 comprises a transformer 322, having a secondary with a center-tap 323, and a rectifier 324. As shown in Fig. 8, the bridge rectifier 324 is connected across the secondary winding and the center-tap 323 is coupled to neutral. The transformer 322 receives the AC line or drive voltage $V_{AC}$ which is rectified by the bridge rectifier 324 to produce the rectified line voltage ~V which powers the IGBT bridge in the output drive circuit 310.

Referring to Fig. 6, the PWM gate generation stage 302 comprises a pulse width modulation circuit 332, a group firing pulse circuit 334, and a soft start circuit 336, in addition to the line synchronization circuit 312. As shown in Fig. 8, the line synchronization circuit 312

includes a square wave generator circuit 326 for generating a square wave signal which is locked to the 60 Hz line voltage $V_{AC}$ and has a minimum dead zone. The square wave generator 326 is implemented in known manner and comprises a comparator 327 which is coupled to the output of the transformer 322 through a voltage follower 328 and with a level shifter 329. The comparator 327 includes a potentiometer 330 for adjusting the dead zone.

The PWM modulation circuit 332 provides PWM modulation for generating the AC current signal for the light assembly 1. The PWM modulation circuit 332 as shown in Fig. 8 is implemented in a similar fashion to the PWM generator 132 (as described above for Fig. 4) using a PWM generator 333 such as the commercially available SG3526 device. The PWM generator 333 is configured to provide a minimum OFF time for the IGBT blocking conditions. The modulation frequency is set to 20 kHz in order to be above the audible level.

The group firing pulses circuit 334 reconstructs a positive group signal +Group and a negative group signal -Group as shown in Fig. 6. The group firing pulses circuit 334 receives the square wave output and square wave inverted output from the square wave generator 326. An implementation for the group firing pulses circuit 334 is shown in Fig. 8.

The soft start circuit 336 is also shown in Fig. 8. The soft start circuit 336 generates a soft start enable signal 337. On power-up or upon energizing the AC supply line $V_{AC}$, the soft start circuit 336 generates the enable signal 337 which serves to disable all signals for the dimmer 300 until the appropriate power supply levels

are reached. As shown in Fig. 8, the enable signal 337 is logically AND'd with the PWM modulation signal by AND gate 339. The soft start circuit 336 also synchronizes the zero crossing of the voltage to start firing the IGBT pairs in the output drive circuit 310 only at low voltages.

Reference is next made to Fig. 9, which shows the proportional and integral (P/I) controller stage 303 in greater detail. The P/I controller 303 comprises an error circuit 342, a load current feedback circuit 344, an integral control loop 346 for the steady state PWM, a proportional control loop 348, and a PWM mixer 350. The error circuit 342 receives an input from the reference demand circuit 304 and another input from the load current feedback circuit 344. The reference demand circuit 304 generates a rectified sinusoidal demand adjust signal $V'_{ADJ}$ having a magnitude corresponding to the desired current in the load (i.e. magnetic ballast 2). The demand adjust signal $V'_{ADJ}$ provides a reference signal from which the magnitude and waveform shape for the AC current waveform $I_{AC}$ is derived. The reference demand circuit 304 is implemented in a fashion similar as the circuitry for the demand adjust signal $V_{ADJ}$ described above for Fig. 5.

The load current feedback circuit 344 monitors the load current (i.e. the current in the magnetic ballast 2) and is shown in greater detail in Fig. 9. The load current feedback circuit 344 includes a current transformer 352 which provides an output indicative of the load current. The output current from the transformer 352 is filtered by a capacitor 354 to reject the high frequency noise components while still maintaining a bandwidth of 5 kHz. The filtered signal is conditioned by an amplifier 356 and rectified by a precision rectifier circuit 358.

The precision rectifier 358 comprises operational amplifiers 360, 362 and diodes 364, 366 which are configured in known manner. The level of the rectified signal is conditioned further and the level adjusted before being outputted as a load current signal $C_{load}$ for the error circuit 342. The error circuit 342 generates an error signal Err which is the difference between the actual load current (i.e. signal $C_{load}$) and the desired demand setting (i.e. signal $V'_{ADJ}$).

The integral controller 346 generates a DC base voltage which represents the steady state PWM modulation rate for the PWM modulation circuit 332. As shown in Fig. 9, the integral controller 346 comprises an integrator stage and a clamping circuit which adjusts the level of the DC base voltage signal to a level which is compatible with the PWM chip 333 (Fig. 8). The integral controller 346 is implemented in a similar fashion to the integral controller branch 226 described above with reference to Fig. 5. The PWM mixer 350 mixes the outputs from the integral controller 346 and the proportional controller 348 and generates an output signal PWM which set the modulation level for the PWM modulation circuit 332.

The proportional controller 348 generates a signal which is the error signal Err amplified to an optimum gain level. The output of the proportional controller 348 provides the dynamic modulation signal which directs the PWM modulation circuit 332 to produce the desired sinusoidal shape for the AC current signal. The proportional controller 348 is implemented in a similar fashion to the proportional controller 228 described above with reference to Fig. 5.

The lockout circuit 305 detects a recovery current in the IGBT bridge 311 (Fig. 7) and locks out the control signals from the group firing pulses circuit 334 which, in turn, control the IGBT drivers 315 and 319 (Fig. 7) in the driver. It will be appreciated that the purpose of the lockout circuit 305 is to prevent "shoot through" in the IGBT bridge 311 by allowing recovery currents. The lockout circuit 305 is implemented as shown in Fig. 10.

Reference is next made to Fig. 11, which shows a single ballast current controlled dimmer 401 according to another embodiment of the present invention. The current controlled dimmer 401 shown in Fig. 11 is intended primarily for use with a single magnetic ballast 402, i.e. one fluorescent lamp assembly 401 comprising the magnetic ballast 402 and a pair of fluorescent tubes. By equipping each ballast 402 with a single ballast current controlled dimmer 401, each individual ballast 402 may be individually controlled in a multiple ballast (lamp) installation.

As shown in Fig. 11, the current controlled dimmer 401 comprises an AC switching stage 410, a firing stage 412, and an output stage 414.

The AC switching stage 410 comprises a full-wave bridge rectifier 420 and an insulated gate bipolar transistor (IGBT) 422. The bridge rectifier 420 comprises four diodes which are connected in a bridge configuration to form an AC branch 424 and a DC branch 426. One terminal of the DC branch 424 is connected to the collector of the IGBT 422 and the other terminal is connected to the emitter of the IGBT 422. For the AC branch 424, one terminal is connected to the AC supply voltage (i.e. terminal 18), and

the other terminal is connected to the load, i.e. input terminal of the magnetic ballast 402.

As shown in Fig. 11, the output stage 414 comprises a first capacitor 428, a resistor 429 and a second capacitor 430. The capacitor 428 and the resistor 429 are connected in series and coupled in parallel across the ballast 402. The resistor 429 and the capacitor 428 provide a parallel load for the ballast 402 which permits free-wheeling when the AC supply voltage to the ballast 402 is turned off during the chopping interval. The capacitor 428 provides energy transfer for the inductive energy stored in the magnetic ballast 402. The resistor 429 limits the current stress in the capacitor 428 and the ballast 402 when the full AC supply or line voltage is applied during the ON interval in the chop cycle. During the OFF interval, the voltage on the ballast 402 decreases and there is an inrush of current into the capacitor 428, i.e. free-wheeling.

The firing stage 412 comprises a pulse width modulator 432 and a driver chip or integrated circuit 434, such as the IR2121. The pulse width modulator 432 generates a pulse width modulated output signal 433. The output signal 433 has a variable duty cycle which is set by a chop voltage signal derived from a potentiometer 436. The pulse width modulated output signal 433 is logically AND'd by logic gate 438 with a chop enable signal 435 and inverted by an inverter 442 to produce a modulation or chopping control signal 413. The chop enable signal 435 is active HIGH and produced by a chop enable switch 440. When the chop enable signal 435 is set LOW, the current dimmer 401 is disabled and the lamp is operated at full intensity. The chopping control signal 413 is applied to the input of

the driver 434. The driver 434 provides 0 to +15V offset to the chopping control signal 413 for turning the IGBT 422 ON and OFF. When the chopping control signal 413 is HIGH, the IGBT 422 is ON and thus the AC switch 410 is closed, and a current derived from the AC line voltage will flow through the bridge 420 into the magnetic ballast 402 in the lamp assembly. Conversely, when the chopping control signal 413 is LOW, the IGBT 422 is turned OFF and the AC switch 410 is opened, and a free-wheeling path across the load, i.e. the magnetic ballast 2, is established by the resistor 429 and capacitor 428 connected in parallel with the ballast 402.

In experimental testing, it has been found that the open loop current controlled dimmer 401 provides an output intensity control range from full 100% power to 20% power before there is any noticeable flicker for a single ballast (i.e. lamp) arrangement. Advantageously, the implementation for the open loop current controlled dimmer 401 is simplified and requires a single +15 Volt power supply, a single IGBT 422 and bridge 420.

The open loop current dimmer 401 may be extended to control the output intensity of multiple lamp assemblies connected in parallel. For such an arrangement, a capacitance value of 0.75 $\mu$F for the capacitor 428 for each magnetic ballast 402 (connected in parallel) was found to be sufficient, and the need for the resistor 429 is eliminated because of the natural damping of the circuit. In experimental testing for multiple ballasts 402 (i.e. lamp assemblies), the open loop current dimmer 401 was found to provide output intensity control over the range of 100% (full power) to 70% output before therefore was any noticeable flicker in the light output.

Reference is next made to Fig. 12 which shows another embodiment of a current controlled dimmer 404 according to the present invention. The current controlled dimmer 404 is similar to the dimmer 401 of Fig. 11 with the addition of a feedback control loop or circuit denoted generally by reference 405. The current controlled dimmer 404 with feedback control circuit 405 is suitable for controlling a number of ballasts (i.e. lamp assemblies) connected in parallel and shown individually as 402a,... 402N.

As shown in Fig. 12, a capacitor 428' is connected in parallel across the ballasts 402. The capacitor 428' has a capacitance value of 0.75 $\mu$F for each ballast 402, i.e. N x 0.75 $\mu$F. The capacitor 428' provides a free-wheeling path for the inductive energy stored in the magnetic ballast(s) 402 during the OFF intervals in the chopping cycle.

Referring to Fig. 12, the IGBT 422 is turned ON and OFF, i.e. chopped, by a chopping or modulation control signal FS. The chopping control signal FS is generated by the pulse width modulator generator 432. The chopping control signal FS output from the PWM generator 432 is coupled to the driver 434 through a buffer 450 and an opto-isolator 452. The buffer 450 is implemented using a discrete NPN transistor. The opto-isolator 452 is provided to allow for a floating power supply, and the output of the opto-isolator 452 is coupled to the base of the IGBT 26 through the driver chip 434. The driver chip 434 provides a 0 to +15V offset for the modulation control signal FS for turning the IGBT 422 ON and OFF.

The feedback control circuit 405 is implemented in similar fashion to the control circuit 16 described above with reference to Fig. 5. As shown in Fig. 12, the control circuit 16 comprises an amplifier 502, a filter and rectifier circuit 504, an error circuit 514, a manual demand (i.e. output intensity) adjust circuit 512, a proportional/integral feedback loop 525, and a PWM mixer 534. The proportional/integral feedback loop 525 comprises an integral control branch 526, and a proportional control branch 528.

The control circuit 16 generates a pulse width modulation level control signal PWMlev which determines the pulse width or duty cycle of the modulation control signal FS. The modulation level control signal PWMlev is derived from a feedback current RS which flows in a shunt resistor 529. The feedback current RS is amplified and conditioned by the amplifier 502 and the filter and rectifier circuit 504 and provides one input to the error circuit 514. The amplifier 502 has an adjustable gain and is implemented in a similar fashion to the amplifier 202 described above in Fig. 5. The filter and rectifier circuit 504 is implemented in a similar fashion to the filter and rectifier 204 described above in Fig. 5. The other input to the error circuit 514 is the demand adjust signal $V_{ADJ}$, which represents the desired output level for the lamp(s). The error circuit 514 produces an error signal Err which represents the difference between the actual intensity output (i.e. the feedback current RS) and the desired demand adjust level $V_{ADJ}$. The error circuit 514 is implemented in a similar fashion to the error circuit 204 described above in Fig. 5.

The error signal Err is fed to a proportional/integral feedback control loop 525, and in particular the integral control branch 526 and the proportional control branch 528. The integral controller 526 is implemented in a similar fashion to the integral controller 226 described above in Fig. 5 and provides a long time constant and is intended to control the steady state level of the sinusoidal waveform. The integral controller 526 generates a DC base voltage which represents the steady state PWM modulation rate for the pulse width modulation generator 432. The proportional controller 528, on the other hand, is used to correct errors between the desired demand and the actual load current. The proportional controller 528 provides the dynamic modulation signal which directs the pulse width modulation generator 432 to produce the desired sinusoidal shape for the AC current signal $I_{AC}$. The proportional controller 528 is implemented in a similar fashion to the controller 228 described above in Fig. 5. The PWM mixer 534 mixes the outputs from the integral controller 526 and the proportional controller 528 with a minimum PWM offset signal ~P to generate the pulse width modulation level control signal PMWlev. The PWM mixer 534 is implemented in a similar fashion to the PWM mixer 234 described above in Fig. 5.

Advantageously, the current controlled dimmer with feedback control 404 utilizes only a single AC switching element and provides a free wheeling path (through the capacitor 428') which is static. By utilizing a static free wheeling path, the likelihood of a short circuit through the output stage 414' is minimized and the need for trip circuits and synchronization signals is eliminated. Advantageously, this reduces the component

count and subsequent cost of the current controlled dimmer 404.

In experimental testing, it has been found that the current controlled dimmer 404 with feedback control provides an output intensity control range from full 100% power to 65% power before there is any noticeable flicker for multiple ballast(s), i.e. lamps. Below 65% output, a slight flickering was noticeable with possible tube drop outs. However, with the addition of the feedback control loop 405, the total power output will match the desired output level (i.e. demand adjust level), and if one tube drops out, the other tubes compensate as their individual lumen output is increased to the total power output level. Advantageously, the current controlled dimmer 404 provides smooth continuous control of the lumen output in a multiple lamp arrangement.

Reference is made again to Fig. 11, which also shows another embodiment for the single ballast current controlled dimmer 401. As shown in Fig. 11, circuitry inside the broken outline box 450, namely, the pulse width modulator 432, the potentiometer 436, the logic gate 438 and inverter 442, and the chop enable switch 440, are replaced by a microcontroller. The microcontroller is suitably programmed to generate the modulation or chopping control signal 413 for the AC switching stage 410. As will be described below, the microcontroller is programmed to provide predictive open loop control which is implemented in the form of a look-up table. The predictive look-up table provides appropriate duty cycle levels for the pulse width modulation of the AC supply voltage applied to the ballast to generate the AC current signal which controls

the intensity (i.e. output) of the fluorescent lamp assembly.

For the single ballast current controlled dimmer 401, the predictive open loop control comprises modulation of the duty cycle over each half cycle of the AC voltage that is being applied to the magnetic ballast 402. Fig. 13 shows the relationship, over a half cycle, between the duty cycle of the modulated voltage applied to the magnetic ballast and the angular degrees of the input line voltage. The duty cycle is set to 100% (i.e. FULL ON) at and after the zero crossing of the line voltage, and is maintained at 100% for the first part (501)of the half cycle. The magnitude of the duty cycle is then decreased sharply, as shown for curve A in Fig. 13, and is maintained at a minimum value near the middle half (502) of the half cycle. A gradual increase in the duty cycle is performed in the second half (503) of the half cycle until 100% magnitude is reached. The 100% magnitude duty cycle is then maintained until the end of the half cycle.

Referring still to Fig. 13, curve A shows a typical pattern for the duty cycle modulation that is used for a 34 Watt Cool White type of fluorescent bulb. This pattern is derived from observations of the PWM signal in the closed loop configuration for the current controlled dimmer 404 described above with reference to Fig. 12. The pattern of curve A is stored in the form of a look-up table in memory for the microcontroller and the microcontroller uses the look-up table to generate the chopping control signal 413 for the AC switching stage 410 in the single ballast current controlled dimmer 401 of Fig. 11. To provide an increased dimming level, each point in curve A is multiplied by a scaling factor to produce curve B.

These points are then used to generate a chopping control signal for an increased dimming level. Similarly, to provide a decreased dimming level, each point in curve A is multiplied by another scaling factor to produce curve C, and these points are used to generate the chopping control signal. The appropriate modulation pattern (e.g. curve B) is generated by the microcontroller in response to a user input (e.g. a switch input).

Referring again to Fig. 11, the AC switch 410 may be modified with an AC switch configuration 411 as shown in Fig. 14(b). The switch configuration 411 comprises two transistors Q9 and Q10 and two anti-parallel diodes D6 and D7 and the implementation is readily apparent to one skilled in the art.

The present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Therefore, the presently discussed embodiments are considered to be illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

**WHAT IS CLAIMED IS:**

1. An apparatus for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, said apparatus comprising:

(a) means for coupling an AC supply voltage to the magnetic ballast for energizing the ballast to produce a discharge in the gas discharge lamp;

(b) means for generating an intensity level signal for setting the output intensity level for the lamp;

(c) switch means for switching said AC supply voltage to generate an AC current signal for powering the gas discharge lamp, said switch means being responsive to a chopping control signal for varying the amplitude of the AC current signal and thereby varying the output intensity of the lamp;

(d) controller means for controlling said switch means, said controller means including a pulse width modulator for generating said chopping control signal, said pulse width modulator having means responsive to said intensity level signal for generating said chopping control signal with a duty cycle derived from said intensity level signal.

2. The apparatus as claimed in claim 1, wherein said controller means includes a current feedback control loop comprising means for generating a load current signal indicative of the current flowing in the ballast and means for adjusting said chopping control signal based on the difference between the intensity level signal and the load current signal.

3. An apparatus for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, said apparatus comprising:

(a) means for coupling an AC supply voltage to the magnetic ballast for energizing the ballast to produce a discharge in the gas discharge lamp;

(b) means for generating an intensity level signal for setting the output intensity level for the lamp;

(c) switch means for switching said AC supply voltage to generate an AC current for powering the gas discharge lamp, said switch means being responsive to a chopping control signal for varying the amplitude of the AC current and thereby varying the output intensity of the lamp;

(d) controller means for controlling said switch means, said controller means including means responsive to said intensity level signal for generating a modulation control signal, and said controller means further including a pulse width modulator for generating said chopping control signal, said pulse width modulator having means responsive to said modulation control signal for generating said chopping control signal with a duty cycle derived from said intensity level signal.

4. The apparatus as claimed in claim 3, wherein said controller means includes a current feedback control loop comprising means for generating a load current signal indicative of the current flowing in the ballast and means for adjusting said modulation control signal based on the difference between the intensity level signal and the load current signal.

5. The apparatus as claimed in claim 3, wherein said intensity level signal comprises a sinusoidal signal derived from said AC supply voltage.

6. The apparatus as claimed in claim 4, wherein said means for adjusting said modulation control signal comprises a proportional integral controller having an integral control loop and a proportional control loop, said integral control loop including means for generating a steady state control signal corresponding to a steady state pulse width modulation rate for said pulse width modulator, and said proportional control loop including means for generating an error signal based on the difference between the intensity level signal and the load current signal.

7. The apparatus as claimed in claim 6, wherein said integral control loop includes means for introducing a delay so that said AC current lags said AC supply voltage to produce a power factor of approximately 0.9.

8. The apparatus as claimed in claim 4, wherein said switch means comprises a bridge rectifier and a transistor, said bridge rectifier having an input port for receiving said AC supply voltage, an output port coupled to the magnetic ballast of the gas discharge lamp, and a control port, said transistor having an emitter, a base, and a collector, the emitter and the collector of said transistor being coupled to said control port for actuating said bridge rectifier in response to said chopping control signal being applied to the base of said transistor.

9. A method for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, said method comprising the steps of:

(a) applying a voltage to the magnetic ballast for energizing the ballast and producing a discharge in the gas discharge lamp;

(b) modulating the voltage to produce an alternating current for powering the gas discharge lamp, said alternating current having a controllable waveshape substantially following a reference signal;

(c) generating an intensity level signal from said reference signal for setting the output intensity of the lamp;

(d) varying the modulation of the voltage in response to an error signal, said error signal comprising the difference between said intensity level signal and a feedback current signal, so that the output intensity level of the gas discharge lamp follows said reference signal.

10. The method as claimed in claim 9, wherein said voltage comprises a sinusoidal waveform and said alternating current comprises a similar sinusoidal waveform having essentially the same shape as said voltage waveform.

11. The method as claimed in claim 9, wherein said step of modulating further includes the step of introducing a delay between said alternating current and said voltage to produce a power factor of at least 0.9.

12. The method as claimed in 11, wherein said step of modulating said voltage comprises pulse width modulation.

13. A method for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, said method comprising the steps of:

(a) applying a voltage to the magnetic ballast for energizing the ballast and producing a discharge in the gas discharge lamp;

(b) modulating the voltage signal to produce an alternating current with a variable magnitude for powering the gas discharge lamp;

(c) inputting an intensity level signal for setting the output intensity level of the lamp;

(d) varying the modulation of the voltage in response to said intensity level signal to change the magnitude of said alternating current and thereby vary the output intensity of the gas discharge lamp.

14. The method as claimed in claim 13, wherein said voltage comprises a sinusoidal waveform and said alternating current comprises a similar sinusoidal waveform having essentially the same shape as said voltage waveform.

15. The method as claimed in claim 13, wherein said step of modulating further includes the step of introducing a delay between said alternating current and said voltage to produce a power factor of at least 0.9.

16. The method as claimed in 15, wherein said step of modulating said voltage comprises pulse width modulation.

17. An apparatus for controlling the output intensity level of a gas discharge lamp having a magnetic ballast, said apparatus comprising:

(a) means for coupling an AC supply voltage to the magnetic ballast for energizing the ballast to produce a discharge in the gas discharge lamp;

(b) means for generating an intensity level signal for setting the output intensity level for the lamp;

(c) switch means for switching said AC supply voltage to generate an AC current for powering the gas discharge lamp, said switch means being responsive to a

chopping control signal for varying the amplitude of the AC current and thereby varying the output intensity of the lamp;

(d) controller means for controlling said switch means, said controller means including means responsive to said intensity level signal for generating a chopping control signal with a duty cycle derived from said intensity level signal.

18. The apparatus as claimed in claim 17, wherein said means for generating a chopping control signal includes a look-up table for storing a modulation pattern corresponding to a pre-determined intensity level signal.

19. The apparatus as claimed in claim 18, wherein said means for generating a chopping control signal includes scaling means for adapting said modulation pattern to a plurality of intensity level signals.

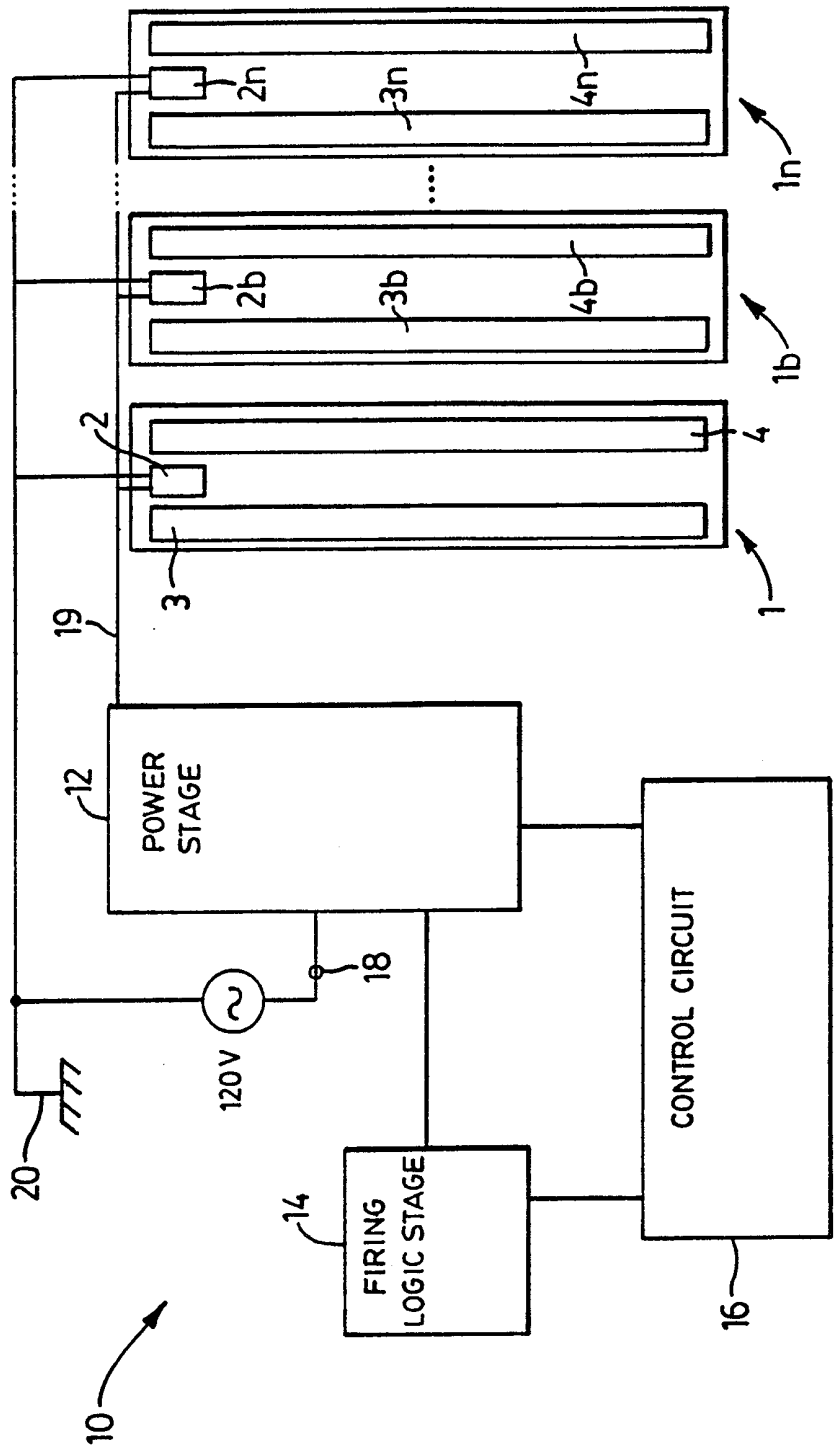
2n
3n
4n
1n
2b
3b
4b
1b
2
4
3
1
19
12
POWER STAGE
18
120 V
20
14
FIRING LOGIC STAGE
CONTROL CIRCUIT
16
10

FIG. 1

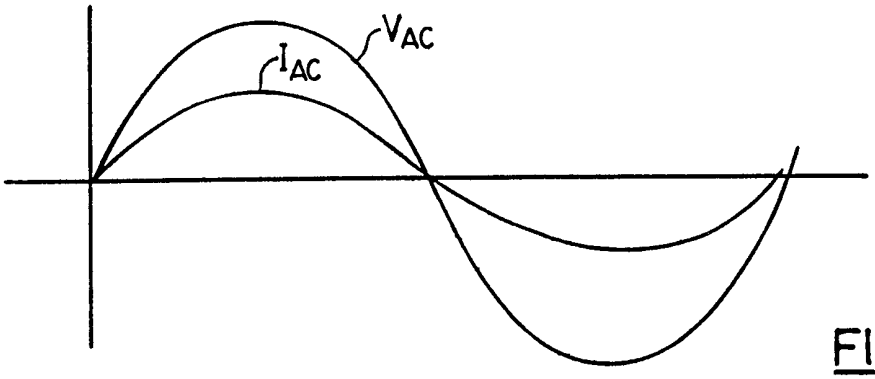


FIG. 2a

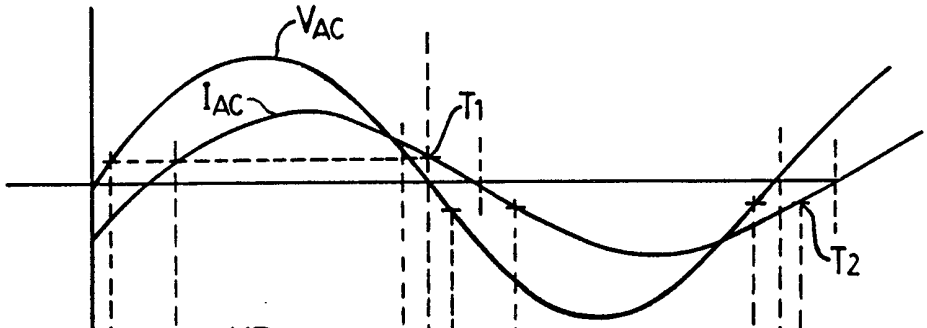


FIG. 2b


FIG. 2c

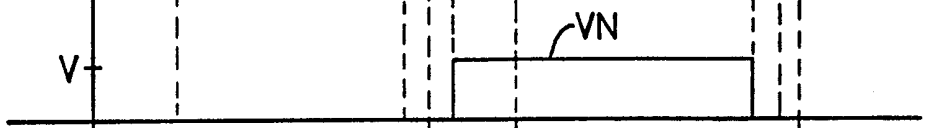


FIG. 2d


FIG. 2e

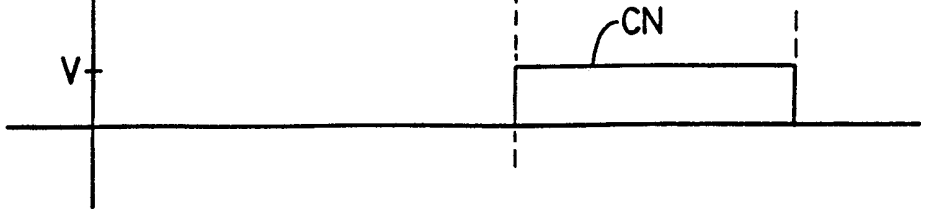


FIG. 2f

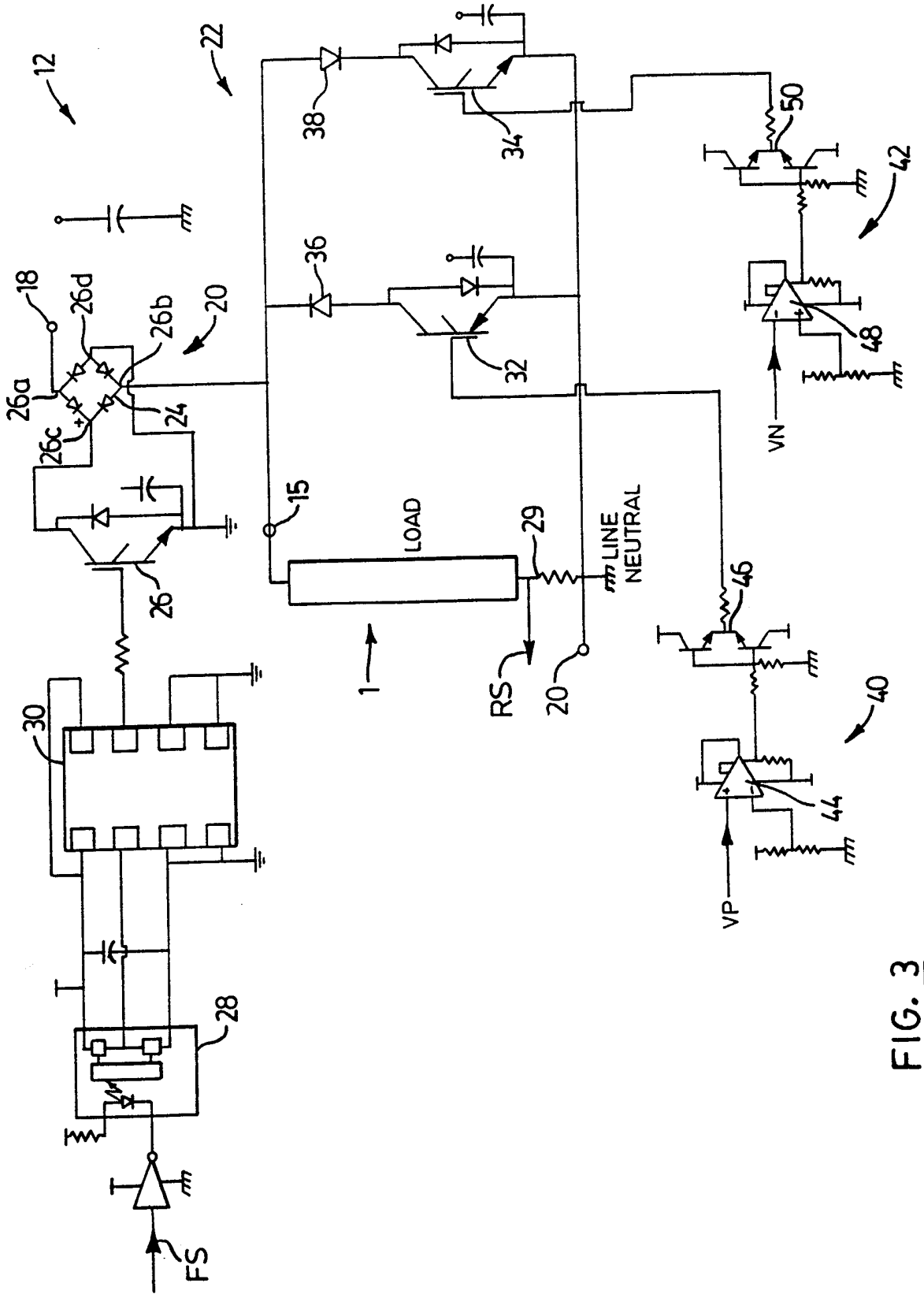
12
22
38
34
50
42
36
18
26d
26b
20
48
32
26a
24
VN
26c
15
LOAD
29
LINE
NEUTRAL
46
26
1
RS
20
40
30
44
VP
28
FS

FIG. 3

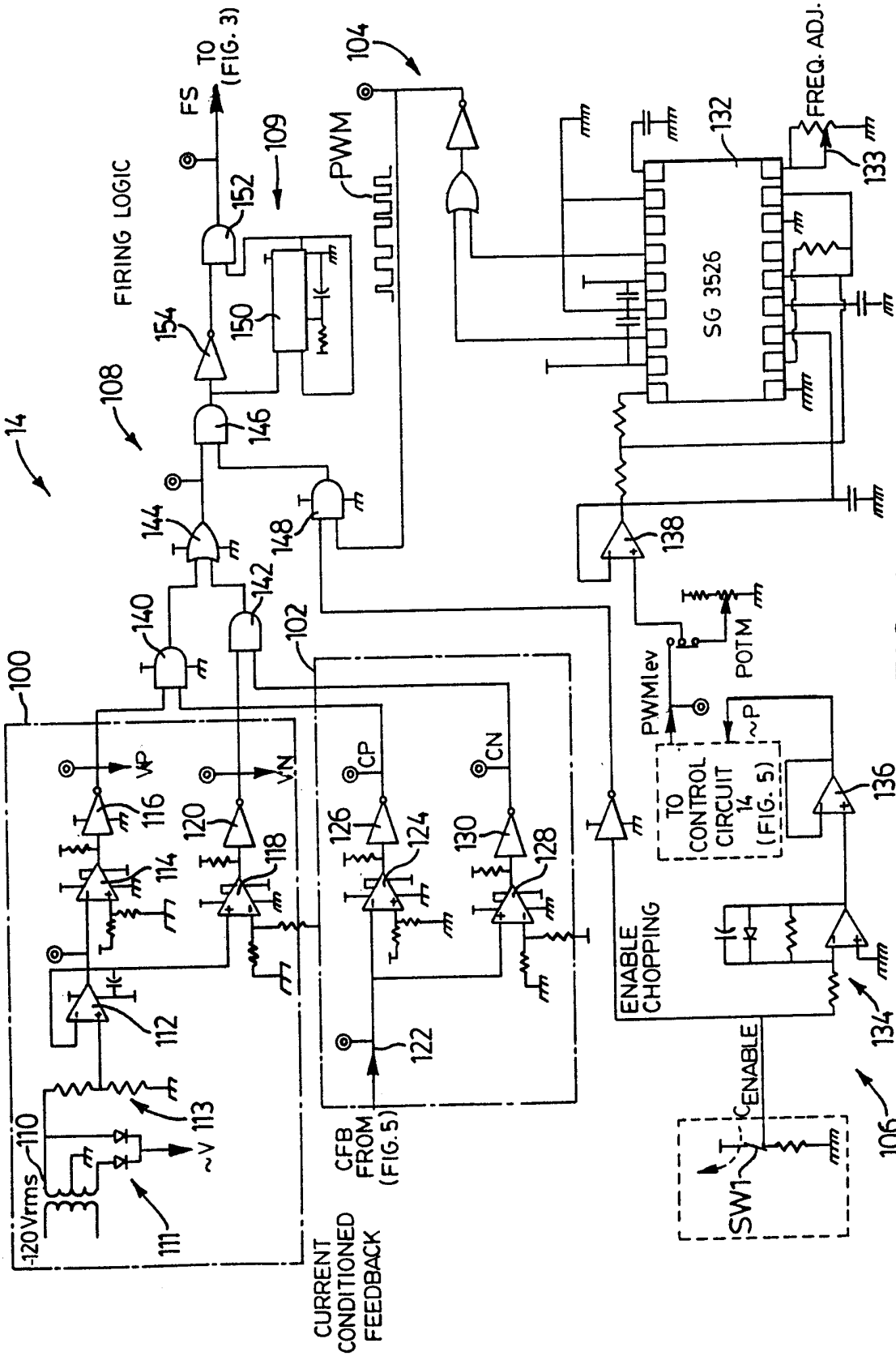
14
100
102
104
106
108
109
110
111
112
113
114
116
118
120
122
124
126
128
130
132
133
134
136
138
140
142
144
146
148
150
152
154
VP
VN
CP
CN
FS
PWM
PWMlev
POTM
ENABLE
CHOPPING
FIRING LOGIC
SG 3526
FREQ. ADJ.
TO (FIG. 3)
TO CONTROL CIRCUIT 14 (FIG. 5)
CFB FROM (FIG. 5)
120Vrms
~V
~P
SW1
CENABLE
CURRENT CONDITIONED FEEDBACK

FIG. 4

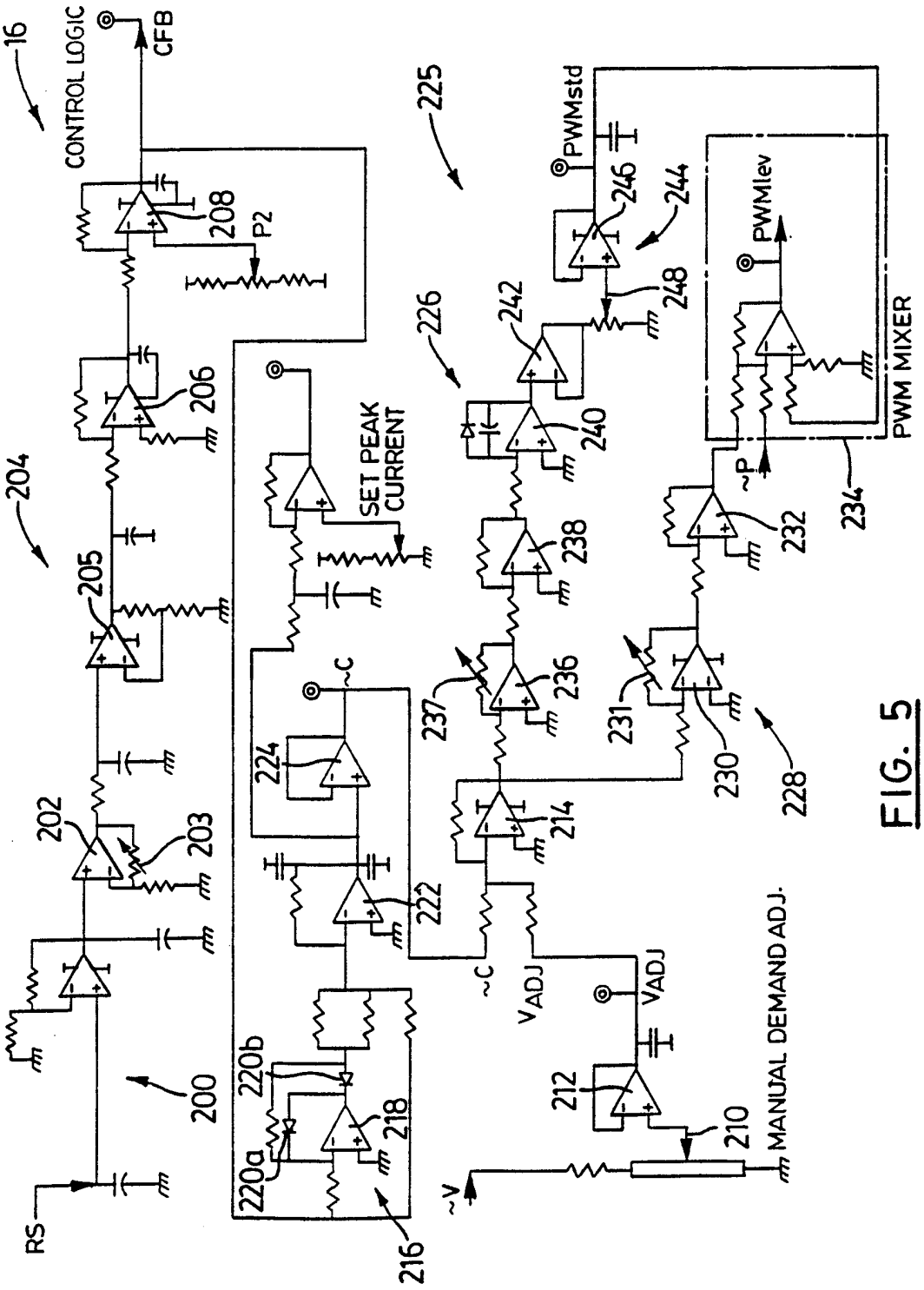
16
CONTROL LOGIC
CFB
208
P2
206
204
205
202
203
200
RS
220a
220b
218
216
224
222
SET PEAK CURRENT
~C
~V
VADJ
VADJ
214
212
210
MANUAL DEMAND ADJ.
225
PWMstd
246
244
248
242
240
226
238
236
237
231
230
228
PWMlev
PWM MIXER
~P
232
234

FIG. 5

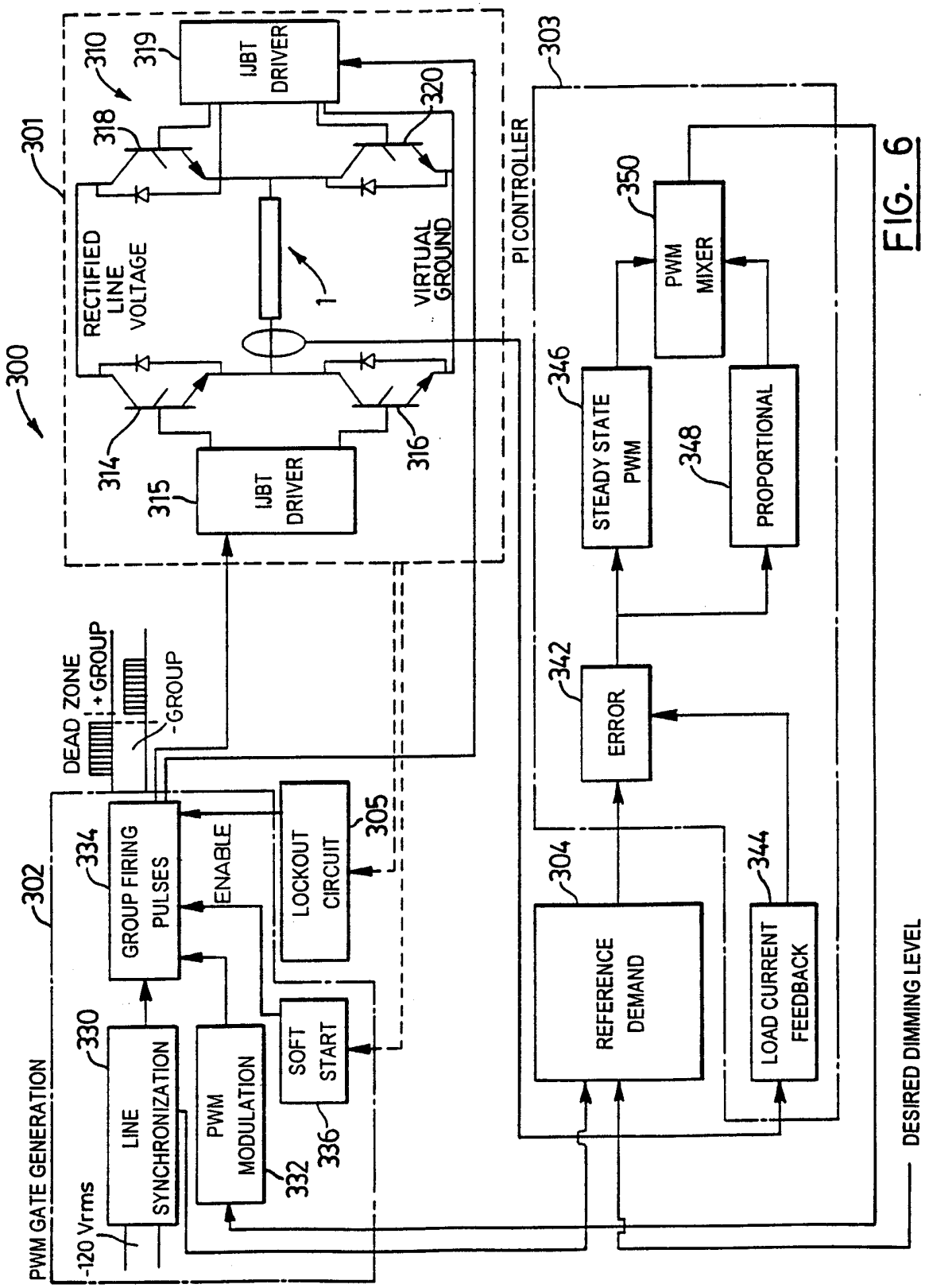
300
301
310
319
IJBT DRIVER
318
320
RECTIFIED LINE VOLTAGE
1
VIRTUAL GROUND
314
315
IJBT DRIVER
316
303
PI CONTROLLER
350
PWM MIXER
346
STEADY STATE PWM
348
PROPORTIONAL
342
ERROR
304
REFERENCE DEMAND
344
LOAD CURRENT FEEDBACK
DESIRED DIMMING LEVEL
DEAD ZONE
+GROUP
-GROUP
302
334
GROUP FIRING PULSES
ENABLE
LOCKOUT CIRCUIT
305
330
LINE SYNCHRONIZATION
PWM MODULATION
SOFT START
336
332
-120 Vrms
PWM GATE GENERATION

FIG. 6

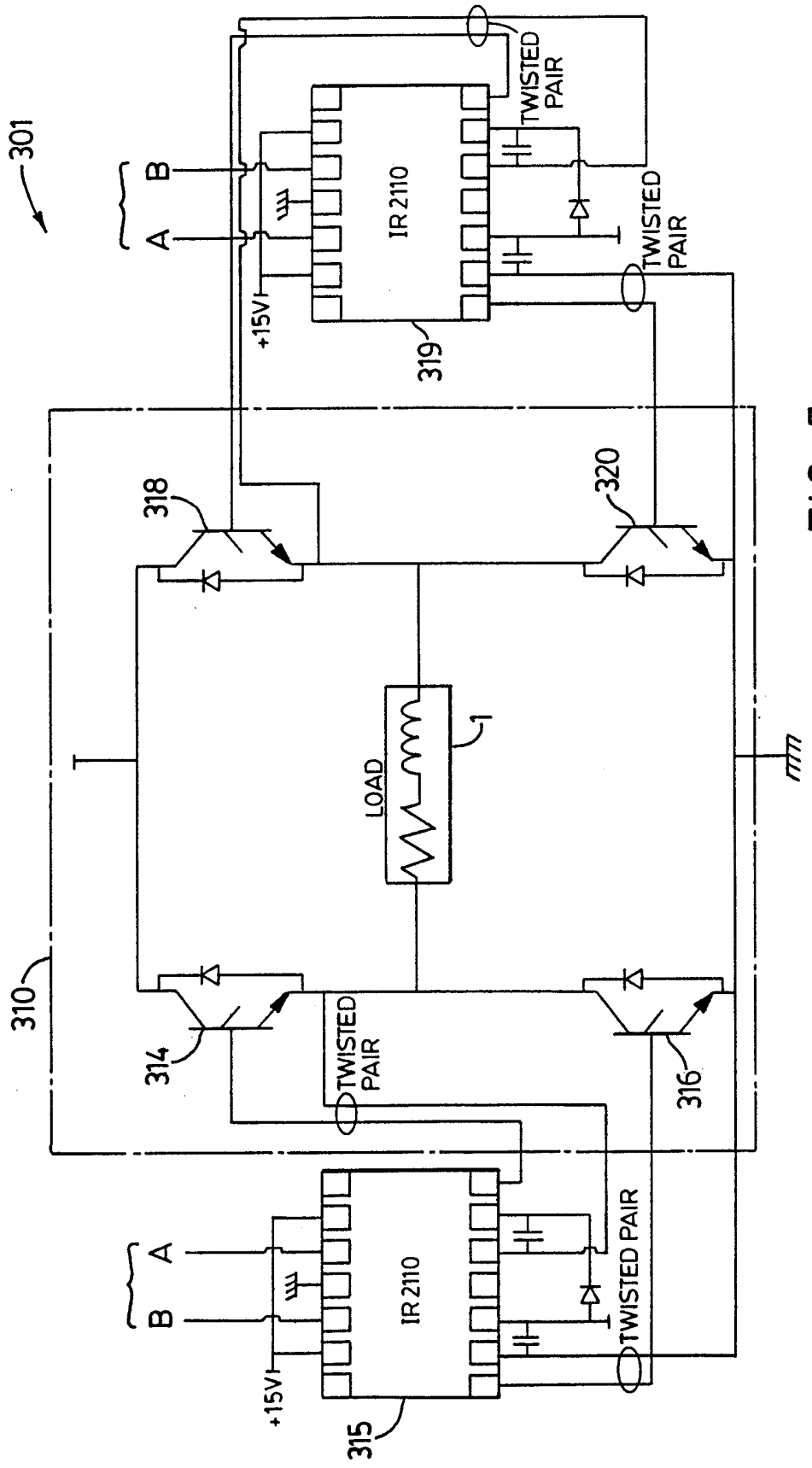
301
A
B
IR 2110
+15V
319
TWISTED PAIR
TWISTED PAIR
318
320
LOAD
L
310
314
316
TWISTED PAIR
TWISTED PAIR
A
B
IR 2110
+15V
315

FIG. 7

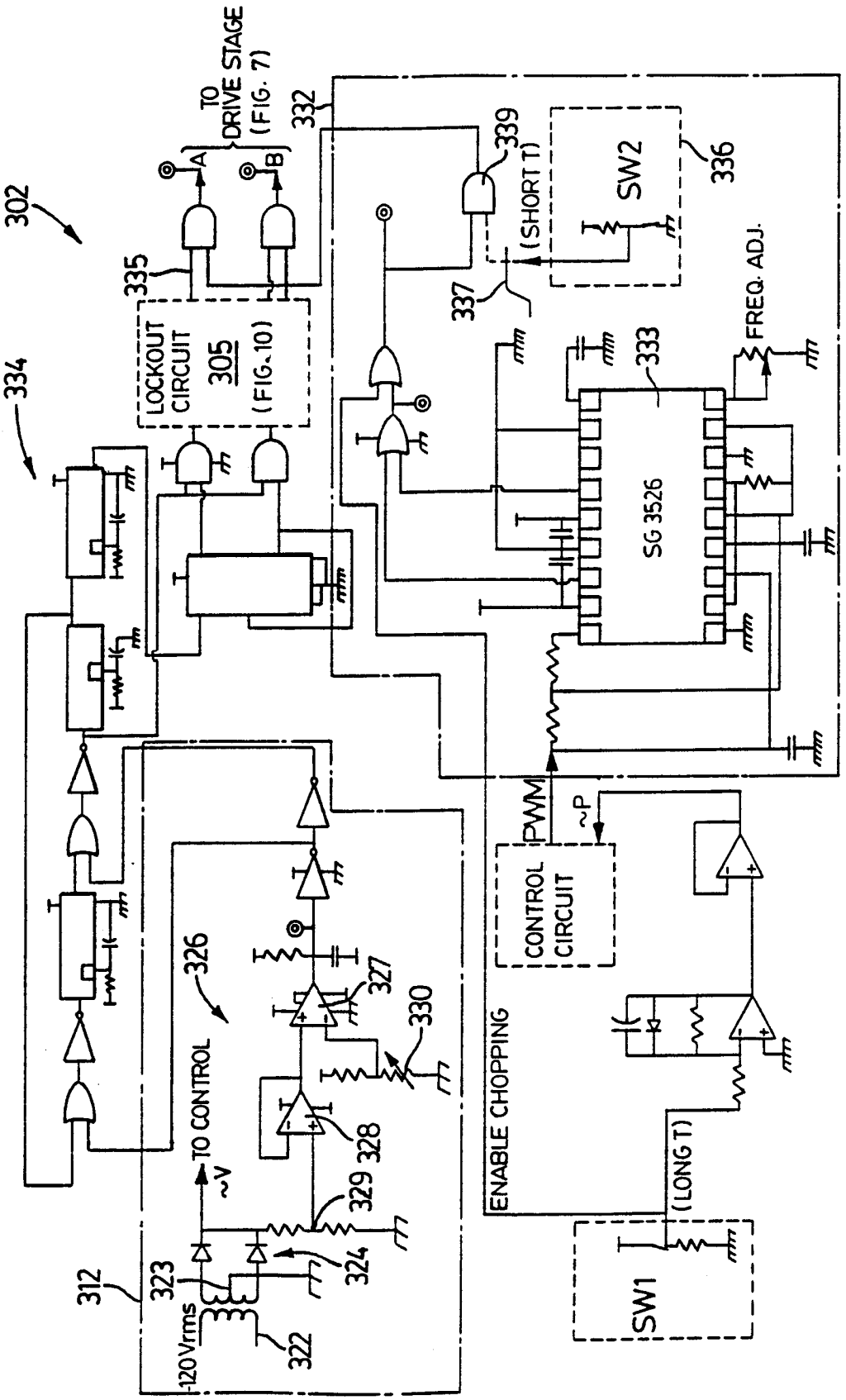
302
334
335
LOCKOUT CIRCUIT 305 (FIG. 10)
TO DRIVE STAGE (FIG. 7)
A
B
332
339
(SHORT T)
337
SW2
336
FREQ. ADJ.
333
SG 3526
PWM
~P
CONTROL CIRCUIT
ENABLE CHOPPING
(LONG T)
SW1
326
327
330
328
329
324
TO CONTROL
~V
312
323
120Vrms
322

FIG. 8

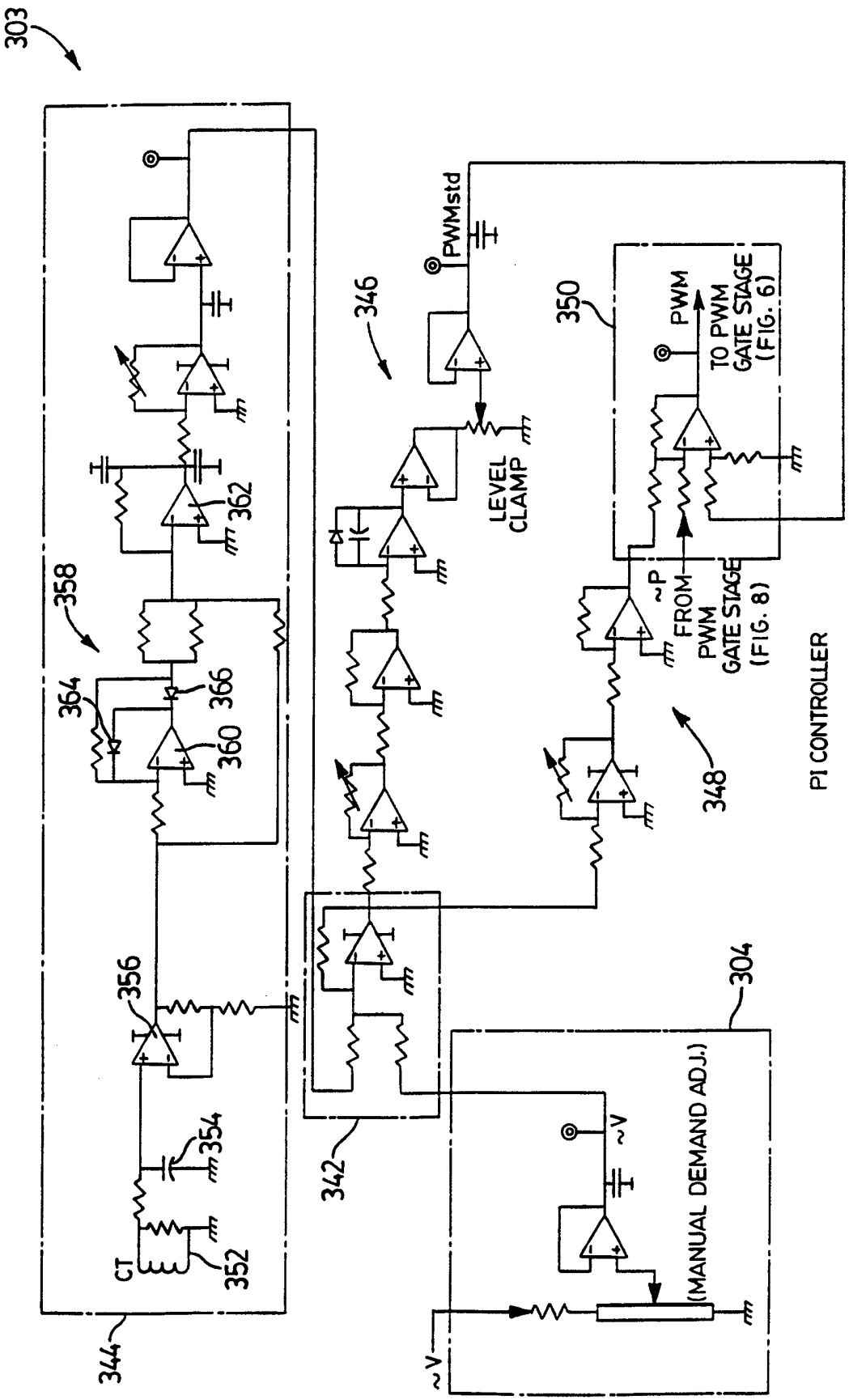
303
PWMstd
346
350
PWM
TO PWM GATE STAGE (FIG. 6)
LEVEL CLAMP
~P FROM PWM GATE STAGE (FIG. 8)
348
PI CONTROLLER
358
364
366
360
362
356
354
CT
352
342
304
~V
(MANUAL DEMAND ADJ.)
~V
344

FIG. 9

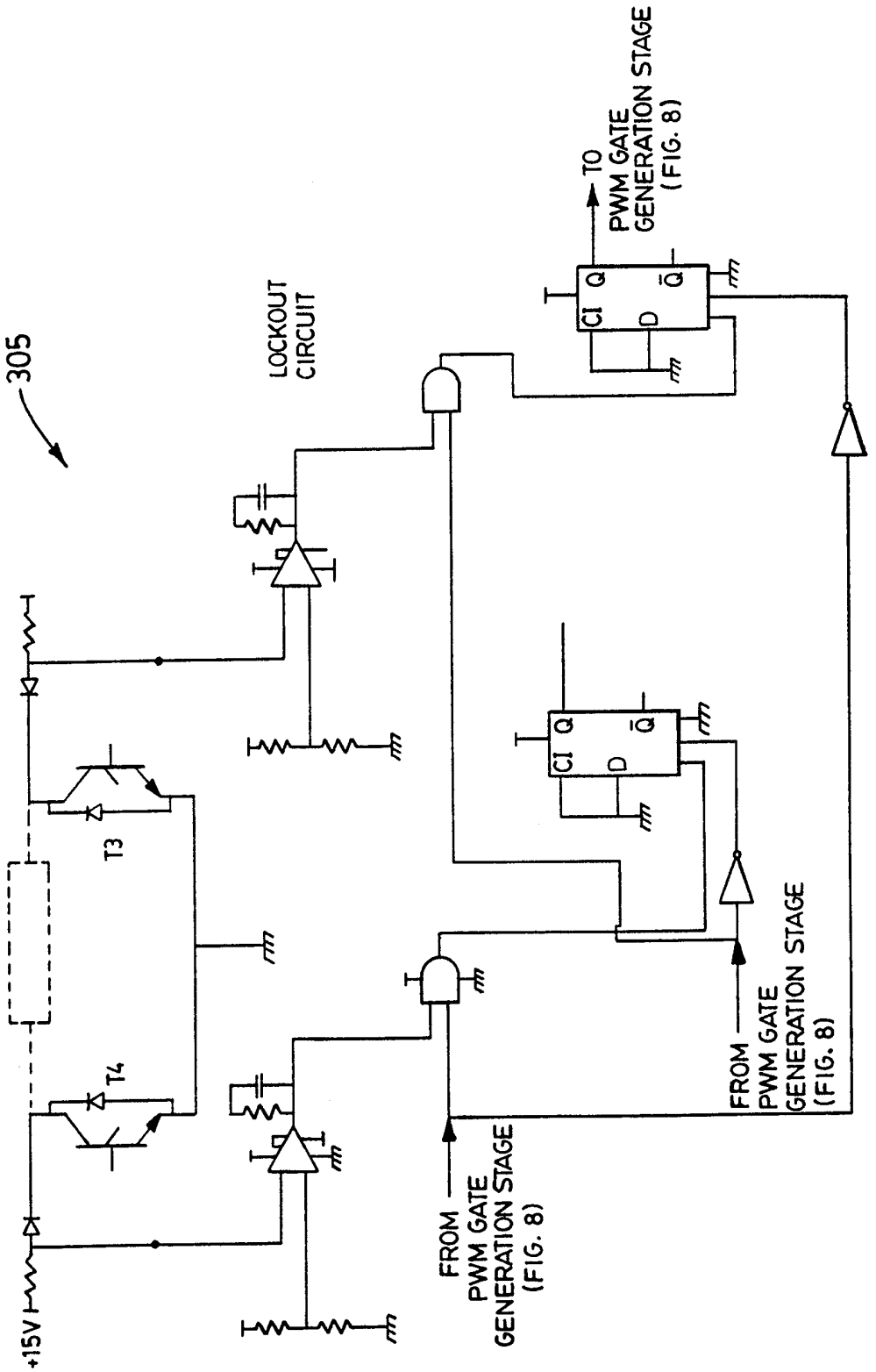
305
LOCKOUT CIRCUIT
TO PWM GATE GENERATION STAGE (FIG. 8)
C1 Q Q̄ D
T3
T4
+15V
FROM PWM GATE GENERATION STAGE (FIG. 8)
FROM PWM GATE GENERATION STAGE (FIG. 8)

FIG. 10

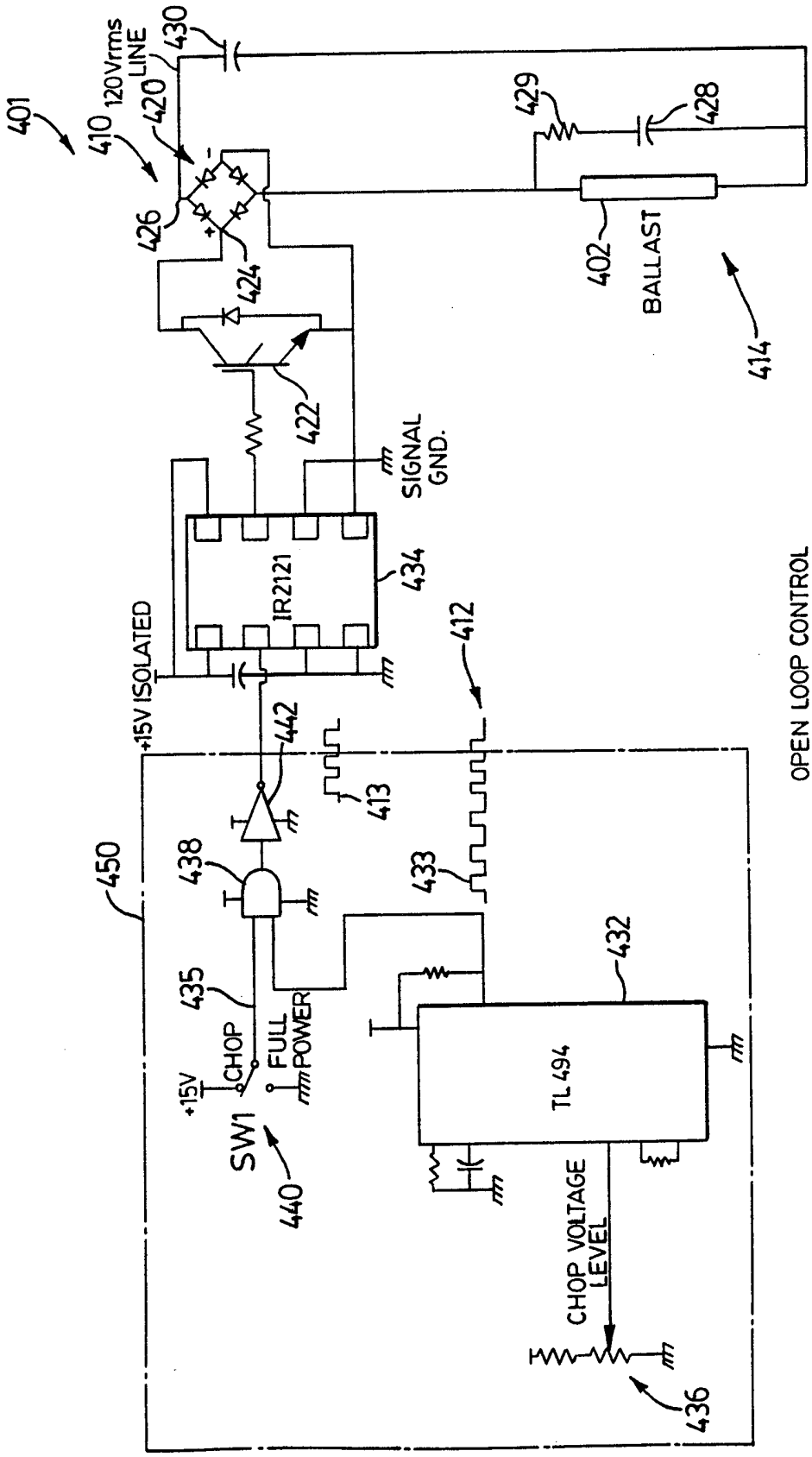
401
410
120Vrms LINE
420
430
426
424
429
428
402
BALLAST
414
422
SIGNAL GND.
IR2121
434
+15V ISOLATED
412
442
413
450
438
433
435
CHOP
FULL POWER
+15V
SW1
440
TL 494
432
CHOP VOLTAGE LEVEL
436
OPEN LOOP CONTROL

FIG. 11

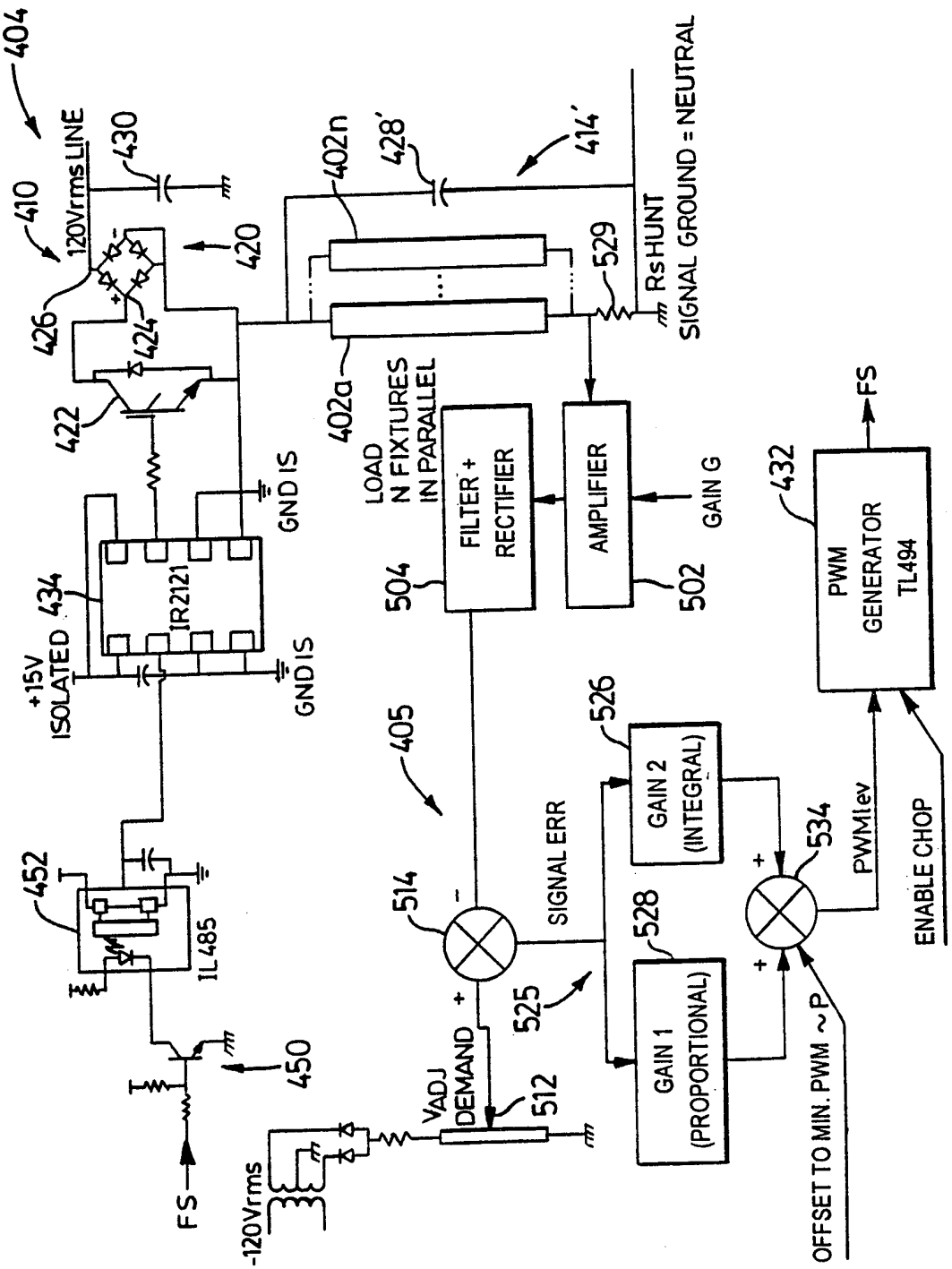
404
410
120Vrms LINE
430
420
426
424
422
402n
428'
414'
529
RsHUNT
SIGNAL GROUND = NEUTRAL
402a
LOAD
N FIXTURES
IN PARALLEL
GND IS
434
IR2121
+15V
ISOLATED
GND IS
504
FILTER +
RECTIFIER
AMPLIFIER
GAIN G
502
432
PWM
GENERATOR
TL494
FS
405
526
GAIN 2
(INTEGRAL)
452
IL485
514
SIGNAL ERR
528
534
PWMlev
ENABLE CHOP
525
GAIN 1
(PROPORTIONAL)
450
VADJ
DEMAND
512
FS
-120Vrms
OFFSET TO MIN. PWM ~P

FIG. 12

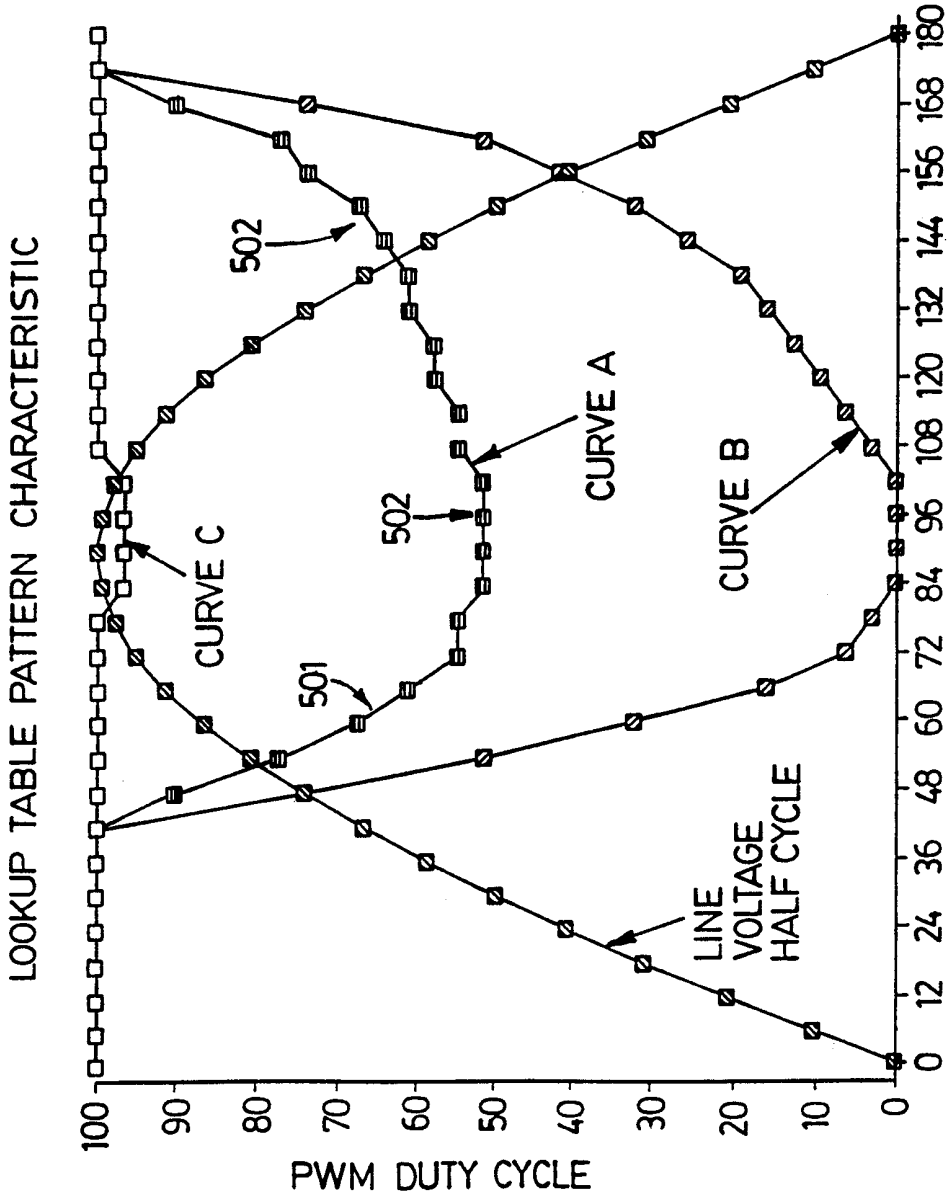
LOOKUP TABLE PATTERN CHARACTERISTIC
PWM DUTY CYCLE
DEGREES FROM ZERO CROSSING
100
90
80
70
60
50
40
30
20
10
0
0
12
24
36
48
60
72
84
96
108
120
132
144
156
168
180
CURVE C
CURVE A
CURVE B
502
502
501
LINE VOLTAGE HALF CYCLE

FIG. 13

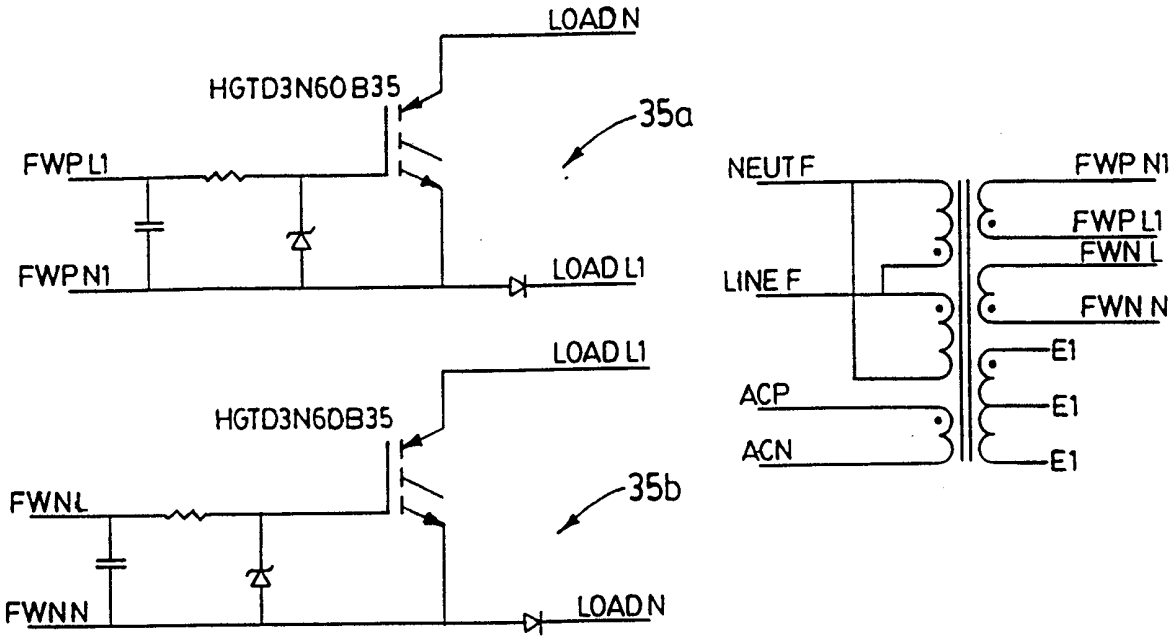


FIG. 14a

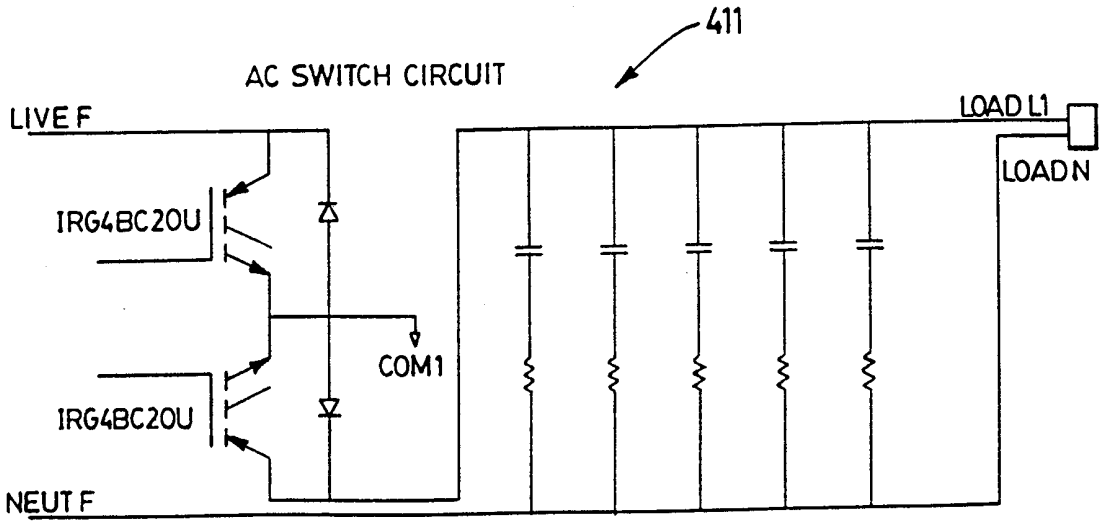


FIG. 14b

# INTERNATIONAL SEARCH REPORT

Inte: onal Application No
PCT/CA 99/00964

**A. CLASSIFICATION OF SUBJECT MATTER**
IPC 7 H05B41/392

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5 500 575 A (IONESCU ADRIAN)<br>19 March 1996 (1996-03-19)<br>column 2, line 66 -column 6, line 20;<br>figures 1-3 | 1-5 |
| X | GB 2 067 318 A (ZUMTOBEL AG)<br>22 July 1981 (1981-07-22)<br>page 3, line 45 -page 5, line 17; figures<br>1-9 | 1-4,8,17 |
| P,X | WO 99 20084 A (AMTECA AG ;MEIER PATRICK<br>(CH); MOSER ROMAN (CH); BURTSCHER HEINZ ()<br>22 April 1999 (1999-04-22)<br>page 5, line 12 -page 9, line 12; figures<br>1-3 | 9,10,13,<br>14,16 |

-/--

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 21 January 2000 | 28/01/2000 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Albertsson, E |

1

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# INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/CA 99/00964

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication,where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5 371 440 A (LIU RUI ET AL)<br>6 December 1994 (1994-12-06)<br>column 2, line 62 -column 5, line 68;<br>figures 1-3 | 9,10,13,<br>14,16 |
| A | EP 0 576 271 A (TOKYO SHIBAURA ELECTRIC CO<br>;TOSHIBA FACTORY AUTOMATION SYS (JP))<br>29 December 1993 (1993-12-29)<br>abstract; figure 1 | 6,7,9,15 |
| A | US 4 640 389 A (KAMAIKE HIROSHI)<br>3 February 1987 (1987-02-03)<br>abstract; figure 11 | 18,19 |
| A | US 4 302 717 A (OLLA ROBERT S)<br>24 November 1981 (1981-11-24) | |
| A | US 4 535 399 A (SZEPESI TAMAS S)<br>13 August 1985 (1985-08-13) | |
| A | US 4 970 437 A (STEVENS CARLILE R)<br>13 November 1990 (1990-11-13) | |
| A | US 3 906 302 A (WIJSBOOM DAN BERNARDUS)<br>16 September 1975 (1975-09-16) | |
| A | DE 42 00 900 A (PHILIPS PATENTVERWALTUNG)<br>17 September 1992 (1992-09-17) | |

1

# INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/CA 99/00964

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 5500575 A | 19-03-1996 | AU 1044895 A | 22-05-1995 |
| | | CA 2175035 A | 04-05-1995 |
| | | EP 0746808 A | 11-12-1996 |
| | | IL 111409 A | 14-08-1997 |
| | | WO 9512157 A | 04-05-1995 |
| | | US 5714847 A | 03-02-1998 |
| GB 2067318 A | 22-07-1981 | AT 374289 B | 15-08-1983 |
| | | AT 234780 A | 15-08-1983 |
| | | AU 581884 B | 09-03-1989 |
| | | AU 4110085 A | 15-08-1985 |
| | | AU 548230 B | 05-12-1985 |
| | | AU 6505780 A | 11-06-1981 |
| | | DE 3044406 A | 27-08-1981 |
| | | ES 497447 A | 16-09-1981 |
| | | GB 2131985 A,B | 27-06-1984 |
| | | AT 768279 A | 15-07-1983 |
| | | AT 374072 B | 15-07-1983 |
| WO 9920084 A | 22-04-1999 | NONE | |
| US 5371440 A | 06-12-1994 | NONE | |
| EP 0576271 A | 29-12-1993 | JP 2790403 B | 27-08-1998 |
| | | JP 6245388 A | 02-09-1994 |
| | | JP 2796035 B | 10-09-1998 |
| | | JP 6311653 A | 04-11-1994 |
| | | JP 6327258 A | 25-11-1994 |
| | | JP 6014465 A | 21-01-1994 |
| | | AU 4140593 A | 06-01-1994 |
| | | CN 1086639 A,B | 11-05-1994 |
| | | DE 69320425 D | 24-09-1998 |
| | | DE 69320425 T | 29-04-1999 |
| | | KR 142026 B | 17-08-1998 |
| | | US 5493485 A | 20-02-1996 |
| US 4640389 A | 03-02-1987 | JP 1618052 C | 12-09-1991 |
| | | JP 2040586 B | 12-09-1990 |
| | | JP 60137789 A | 22-07-1985 |
| | | GB 2153608 A,B | 21-08-1985 |
| | | KR 8904728 B | 25-11-1989 |
| | | SG 5888 G | 17-06-1988 |
| US 4302717 A | 24-11-1981 | NONE | |
| US 4535399 A | 13-08-1985 | DE 3420469 A | 06-12-1984 |
| | | FR 2547128 A | 07-12-1984 |
| | | JP 60013472 A | 23-01-1985 |
| US 4970437 A | 13-11-1990 | NONE | |
| US 3906302 A | 16-09-1975 | NL 7200720 A | 23-07-1973 |
| | | AT 328561 B | 25-03-1976 |
| | | AT 33573 A | 15-06-1975 |
| | | BE 794165 A | 17-07-1973 |
| | | CA 1029432 A | 11-04-1978 |
| | | DE 2263582 A | 26-07-1973 |
| | | FR 2168436 A | 31-08-1973 |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

Int tional Application No
PCT/CA 99/00964

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 3906302 A | | GB 1357313 A | 19-06-1974 |
| | | JP 1123081 C | 12-11-1982 |
| | | JP 48082686 A | 05-11-1973 |
| | | JP 57009200 B | 19-02-1982 |
| DE 4200900 A | 17-09-1992 | NL 9100459 A | 01-10-1992 |