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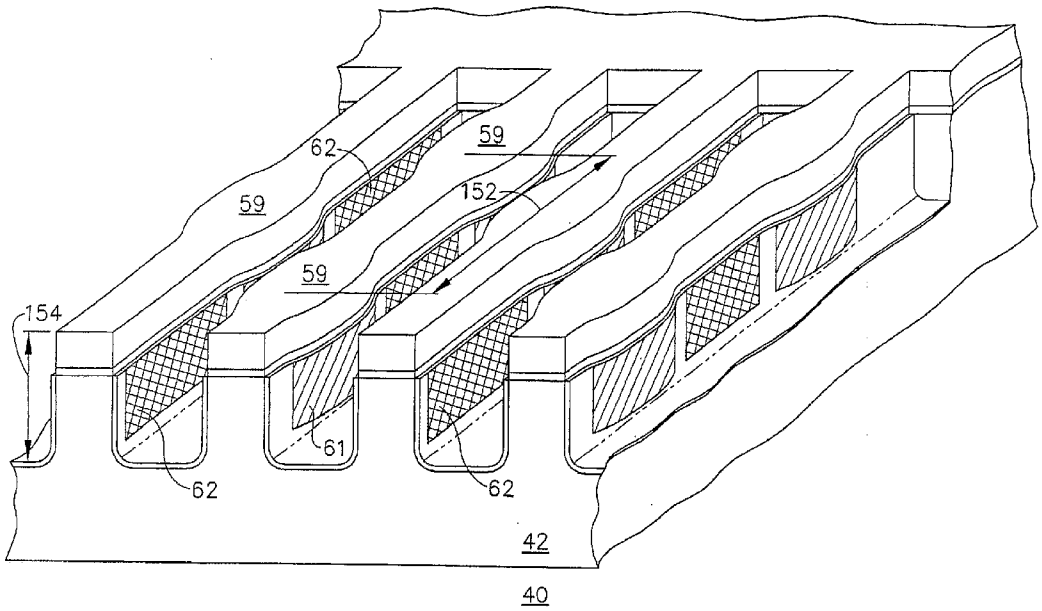
(54) **Title:** VERTICAL EEPROM DEVICE



(57) **Abstract:** A semiconductor device (40), for example an EEPROM, and methods for its fabrication are provided. The semiconductor device comprises a trench (52) formed in the semiconductor substrate (42) and bounded by a trench wall (54, 56) extending from the semiconductor surface (46) to a trench bottom (58). A drain region (61, 94) and a source region (61, 95), spaced apart along the length (152) of the trench, are formed along the trench wall, each extending from the surface toward the bottom. A channel region (62, 97) is formed in the substrate along the trench wall between the drain region and the source region and extending along the length of the trench parallel to the substrate surface. A gate insulator (66) and a gate electrode (68) are formed overlying the channel.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

VERTICAL SEMICONDUCTOR DEVICE

TECHNICAL FIELD OF THE INVENTION

The present invention generally relates to a vertical semiconductor device, and more particularly relates to a vertical MOS device fabricated in the wall of a trench formed in a semiconductor substrate and having a channel along the edge of the trench parallel to the surface of the semiconductor substrate.

BACKGROUND OF THE INVENTION

The majority of present day integrated circuits (ICs) are implemented by using a plurality of interconnected field effect transistors (FETs), also called metal oxide semiconductor field effect transistors (MOSFETs), or simply MOS transistors. An MOS transistor includes a gate electrode as a control electrode and spaced apart source and drain regions between which a current can flow. A control voltage applied to the gate electrode controls the flow of current through a channel between the source and drain electrodes.

ICs are typically fabricated in and on a thin semiconductor substrate having a substantially planar surface. The source and drain regions are spaced apart impurity doped regions ion implanted into the substantially planar surface on opposite sides of the gate electrode which is formed overlying the planar surface. As the complexity of the integrated circuits increases, more and more MOS transistors are needed to implement the integrated circuit function. As more and more transistors are designed into the IC, it becomes important to shrink the size of individual MOS transistors so that the size of the IC remains reasonable and the IC can be reliably manufactured. Shrinking the size of an MOS transistor implies that the minimum feature size, that is, the minimum width of a line or the minimum spacing between lines, is reduced. MOS transistors have now been aggressively reduced to the point at which the gate electrode of the transistor is less than or equal to 90 nanometers (nm) in width. Aggressively shrinking the minimum feature size even further to incorporate more devices in and on the planar substrate surface, however, will incur a significant increase in manufacturing cost, in terms of increased capital expenditures and reduced yield.

Attempts have been made to overcome the problem of packing more and more transistors onto the semiconductor surface by manufacturing vertical transistors. In such attempts, instead of locating each of the source, drain, and channel on the substantially planar surface of the substrate, the vertical transistors are fabricated in trenches that are etched into the surface of the substrate with a source at the bottom of the trench, a drain at the top of the trench near the semiconductor surface, and a channel conducting current along the wall of the trench between the source and the drain. Unfortunately, such attempts have been largely unsuccessful because of problems of isolating one transistor from another and of making the necessary electrical contacts to the vertical transistor elements.

Accordingly, it is desirable to provide a vertical device structure that allow an increase in the number of devices integrated in an IC without requiring a further reduction in minimum feature size. In addition, it is desirable to provide a memory IC based on a vertical transistor structure. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and the foregoing technical field and background.

BRIEF SUMMARY OF THE INVENTION

A vertical semiconductor device and a method for its fabrication are provided. The semiconductor device comprises a trench formed in the semiconductor substrate and bounded by a trench wall extending from the semiconductor surface to a trench bottom. A drain region and a source region, spaced apart along the length of the trench, are formed along the trench wall, each extending from the surface toward the bottom. A channel region is formed in the substrate along the trench wall between the drain region and the source region and extending along the length of the trench parallel to the substrate surface. A gate insulator and a gate electrode are formed overlying the channel.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and wherein FIG. 1-13 illustrate a portion of a semiconductor device and method steps for its fabrication in accordance with various embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description. Terms such as "vertical" and "horizontal" are used herein for descriptive purposes and refer only to orientation with respect to the surface of a substrate (taken to be horizontal), and are not intended to otherwise limit the orientation of the inventive device.

FIGS. 1-13 schematically illustrate a semiconductor memory integrated circuit 40 and method steps for the fabrication of integrated circuit 40 in accordance with various embodiments of the invention. Although the term "MOS device" properly refers to a device having a metal gate electrode and an oxide gate insulator, that term will be used throughout to refer to any semiconductor device that includes a conductive gate electrode (whether metal or other conductive material) that is positioned over a gate insulator (whether oxide or other insulator) which, in turn, is positioned over a semiconductor substrate. In these illustrative embodiments only a small portion of integrated circuit 40 is illustrated. Various steps in the manufacture of MOS devices are well known and so, in the interest of brevity, many conventional steps will only be mentioned briefly herein or will be omitted entirely without providing the well known process details. In this exemplary embodiment integrated circuit 40 is illustrated to be a non-volatile memory circuit such as an electrically erasable programmable read only memory (EEPROM) or a Flash memory, but the invention is also applicable to other semiconductor memory circuits as well as to other ICs, especially those that have a repetitive structure.

A semiconductor memory IC typically includes a memory array or core area and a peripheral area. The core area, in which data is stored, usually, but not necessarily, includes only N-channel MOS (NMOS) transistors and the exemplary embodiment described below will be such an NMOS circuit. The invention is not limited, however, to such single channel embodiments. The peripheral area, which includes support circuitry such as clock circuits, address circuits, I/O circuits, and the like, usually includes complementary MOS (CMOS) transistors. In accordance with an embodiment of the invention, the peripheral circuitry is conventional and is fabricated in substantially the conventional

manner with conventional (not vertical) CMOS transistors. Because the peripheral circuitry is fabricated in conventional manner, the peripheral circuitry and the process steps for fabricating such circuitry will not be illustrated or described except to discuss how such conventional process steps are integrated process for fabricating the core area. Accordingly, the drawing figures will illustrate only (a portion of) the core area of integrated circuit 40.

As illustrated in FIG. 1, fabrication of a semiconductor device in accordance with one embodiment of the invention begins with providing a semiconductor substrate 42. Although other semiconductor materials can be used, the semiconductor substrate is preferably a silicon substrate, either a bulk substrate or a silicon on insulator (SOI) substrate. Without limitation, the semiconductor substrate will generally be referred to herein as a silicon substrate. As used herein, the term "silicon substrate" will be used to encompass the relatively pure monocrystalline silicon materials typically used in the semiconductor industry, either bulk or SOI, as well as silicon admixed with other elements such as germanium, carbon, and the like to form substantially monocrystalline semiconductor material.

In accordance with a preferred embodiment of the invention isolation in the peripheral portion of the IC, preferably shallow trench isolation (STI), is formed first. Because the peripheral isolation is formed in conventional manner, the process steps for its formation will not be described in detail and will not be illustrated in the drawing figures. Although many techniques can be used for forming STI, all such methods generally involve forming a pad oxide and a layer of nitride on the silicon substrate, patterning the nitride and oxide as an etch mask, etching trenches into the surface of the substrate, filling the trenches with an oxide or other insulator, and removing the excess oxide, for example by chemical mechanical planarization (CMP). During the formation of the peripheral isolation the core area is protected by the silicon nitride layer that is left unpatterned over the core area.

As illustrated in cross section in FIG. 1, in accordance with an embodiment of the invention, a thin layer of oxide 44 is formed on surface 46 of the silicon substrate. A layer of silicon nitride 48, having a thickness of about 90 nm is deposited over the layer of oxide. Layer of oxide 44 can be grown by heating the silicon substrate in an oxidizing ambient and layer of silicon nitride 48 can be deposited by low pressure chemical vapor deposition (LPCVD) by the reaction of dichlorosilane and ammonia.

A layer of photoresist 50 is applied over silicon nitride layer 48 and is patterned as illustrated in cross section in FIG. 2. Although not illustrated, the photoresist is left unpatterned and protecting the peripheral area of the IC. Using the patterned photoresist as an etch mask, trenches 52 are etched into the surface of silicon substrate 42 in the core area. Preferably the trenches are anisotropically etched, for example by reactive ion etching (RIE) using a Cl or HBr/O_2 chemistry. The anisotropic etching results in trench walls 54, 56 that are nearly vertical extending from surface 46 to the trench bottom 58. Although not apparent in FIG. 2 (but illustrated in FIG. 4 below) the walls of trenches 52, when viewed along their length, preferably are not straight, but rather are patterned and etched to leave enlarged contact regions 59 in the silicon substrate bordering the trenches. Most preferably, the contact regions are staggered from row to row to increase packing density. "Row" is used here in the context of rows and columns of a memory array. Word lines will eventually be formed along the row direction. The number and length of trenches will be determined by the size of the memory to be fabricated.

After completing the trench etch, photoresist layer 50 is stripped and a thin layer of thermal oxide 60 is grown as an oxide liner on the walls and bottom of the trenches as illustrated in cross section in FIG. 3. One or more layers of thermal oxide (not illustrated) may be grown and subsequently removed by etching before the growth of oxide

60. The growth and stripping of the additional layers of thermal oxide remove etch damage caused by the trench etching. During the growth and stripping the peripheral area is protected by nitride layer 48. Layer 60 removes additional damage caused by the trench etching and prevents implant channeling during subsequent ion implantations. FIG. 4 illustrates, in a partially cut away perspective view, a portion of IC 40 at this stage of the processing. The areas indicated by diagonal shading lines 61 are areas in which source and drain regions will be formed. The areas indicated by cross hatching 62 are areas in which the channel regions of the memory transistors will be formed. Just for clarity of understanding, double headed arrow 152 indicates the length direction of trenches 52, and double headed arrow 154 indicates the depth direction of the trenches.

In conventional CMOS processing ions are implanted into the surface of the substrate to form doped well regions in which the active transistors are formed. In accordance with an embodiment of this invention the well regions are formed in the portions of the substrate forming the walls of trenches 52. Because the core of the IC will be formed of NMOS transistors, P-type ions are implanted through thermal oxide 60 into the substrate forming the walls of the trenches to form P-doped wells 64 as illustrated in cross section in FIG. 5. Because walls 54, 56 are nearly vertical, the ions are implanted at a high tilt angle determined by the depth of the trench and the proximity of the adjacent trench. Multiple implants may be used to tailor the concentration gradient of the dopant in the wells. An additional implant (not illustrated) may also be used to adjust the threshold voltage of the MOS transistors. The implants are then activated by heating, for example by rapid thermal annealing (RTA). As illustrated, the wells are formed on both walls of the trenches so that vertical transistors can be formed in both walls, optimizing the density of transistors in a given unit of surface area.

In accordance with this exemplary embodiment of the invention, specifically if the semiconductor device being fabricated is a non-volatile memory IC, thin thermal oxide 60 is stripped and a thin tunnel oxide 66 is grown on the walls and bottom of trenches 52 as illustrated in cross section in FIG. 6. Preferably tunnel oxide 66 has a thickness of about 8-9 nm. A layer of silicon, either amorphous or polycrystalline but hereinafter referred to as a poly layer, is deposited onto the layer of tunnel oxide. The poly layer is anisotropically etched, for example by RIE, to form poly spacers 68 extending from near the surface of the substrate but below the bottom of nitride layer 48 to the bottom of the trenches. The anisotropic etching removes the poly layer from the bottom of the trenches as well as from the nitride layer 48 and from the peripheral area. In forming a volatile device, the tunnel oxide would be the gate insulator of the MOS transistor and the poly spacer would form the gate electrode. Continuing the process for fabricating a non-volatile memory device, the poly spacers are thermally oxidized to form a layer of oxide 70 having a thickness of about 4-5 nm and a layer of silicon nitride 72 having a thickness of about 8-9 nm is deposited over oxide layer 70.

A layer of photoresist (not illustrated) is applied and patterned to leave the patterned photoresist covering the silicon nitride that is located over the channel regions of the MOS transistors as indicated by cross hatching 62 in FIG. 4. The patterned photoresist is used as an etch mask and the exposed silicon nitride and the poly layer underlying the exposed silicon nitride is etched, preferably in a high pressure isotropic plasma etch. The high pressure etch aids in removing silicon nitride from corners and otherwise difficult to etch areas. After the etch, silicon nitride layer 72 and poly spacer 68 are left covering only the channel regions. The nitride etch is controlled in length so that the bulk of silicon nitride layer 48 remains on the surface of the substrate. Patterned silicon nitride layer 72 and silicon nitride layer 48 are together used as an oxidation mask and a thick thermal isolation oxide 74 is grown on the exposed silicon by heating in an oxidizing ambient. The exposed silicon is the silicon at the bottom 58 of trenches 52 as well as on the

walls 54, 56 of the trench in the areas indicated in FIG. 4 by diagonal shading lines 61. The isolation oxide is grown as a LOCOS oxide. The thermal oxidation process also grows a thin thermal oxide 76 on the surface of patterned silicon nitride layer 72. Thermal oxide 76, together with patterned silicon nitride layer 72 and oxide layer 70 form an oxide-nitride-oxide (ONO) memory film or memory stack on poly layer 68. FIG. 7 illustrates, in a partially cut away perspective view, a portion of integrated circuit 40 at this stage of the processing.

Another layer of silicon, either amorphous or polycrystalline but hereinafter referred to as poly silicon, is deposited to a thickness of about 200 nm. The poly silicon layer is doped N-type, and preferably is deposited as a doped layer. The doping can be phosphorus or arsenic, but preferably is phosphorus. A layer of photoresist (not illustrated) is applied over the layer of poly silicon and is patterned as an etch mask for the layer of poly silicon. The poly silicon layer is etched using the patterned photoresist layer as an etch mask to form top contact or control gate 78 for memory transistors formed on wall 54 of trench 52 and top contact or control gate 80 for memory transistors formed on wall 56 of trench 52. The patterned photoresist layer also protects a contact area 82 coupled to control gate 78 and a contact area 84 coupled to control gate 80, with both contact area 82 and 84 located on the surface of nitride layer 48. The etching of the poly silicon layer, which can be done as an anisotropic etch such as a RIE, leaves the poly silicon on the sidewall of trench 52, but removes the poly silicon from all horizontal surfaces (except for contact areas 82 and 84) including the bottom of the trench and horizontal surfaces in both the core and peripheral areas. The patterned photoresist layer is removed and a further photoresist layer (again not illustrated) is applied and patterned. This further photoresist layer is patterned to protect all of the poly silicon except the poly silicon on the wall at the ends of the trenches. Using the patterned photoresist as an etch mask, the exposed poly silicon is etched to form a gap 86 at the end of each trench physically and electrically separating poly silicon control gate 78 from poly silicon control gate 80. FIG. 8 illustrates, in a partially cut away perspective view, a portion of integrated circuit 40 at this stage of the processing. The poly silicon forming control gates 78 and 80 extends along the length of trench 52 on the walls of the trench, and at the end of the trench extends up and onto the horizontal surface of nitride layer 48 to form contacts 82 and 84. In this and later figures, for ease of illustration, the three ONO layers are illustrated by a single layer 85.

Having completed a much of the core area of IC 40, the process now continues by processing a portion of the peripheral area. Again, as these process steps are conventional, they need not be described or illustrated in detail. A layer of oxide 90 is deposited over the entire structure, in part to protect the core area from subsequent process steps to be performed in the peripheral area. The layer of oxide is photolithographically patterned to remove the oxide from the peripheral area while leaving the oxide covering and masking the core area. Using the patterned oxide as an etch mask, silicon nitride layer 48 is removed from the peripheral area. Until now, the silicon nitride layer has been masking the peripheral area from many of the process steps performed in the core area. After removing the silicon nitride layer, N-wells and P-wells are formed in the peripheral area in conventional manner to form the necessary substrate regions for the fabrication of CMOS peripheral transistors. Any remaining oxide is removed from the peripheral area, the surface of the peripheral area is cleaned, and a gate oxide layer is grown. The gate oxide layer, preferably having a thickness of 3-6 nm, will form the gate insulator of both the PMOS and the NMOS transistors of the peripheral circuitry. A layer of polycrystalline silicon having a thickness of about 150-200 nm is deposited overlying the layer of gate insulator. The layer of polycrystalline silicon is preferably deposited as an undoped polycrystalline layer and is subsequently doped with conductivity determining impurities during the formation of source and drain regions. The layer of polycrystalline silicon is patterned to form the gate electrodes of both the PMOS and the NMOS transistors of the peripheral circuitry. The portion of this polycrystalline silicon layer overlying the core area is etched and totally removed, either as part of

the gate electrode forming etch step or in a separate etch step. The core area is protected by photoresist and source and drain extensions are ion implanted for first the PMOS transistors and then for the NMOS transistors of the periphery circuitry.

A layer of silicon nitride 92 is deposited to a thickness of about 90 nm. A layer of photoresist (not illustrated) is applied over the layer of silicon nitride and is photolithographically patterned to leave the photoresist covering all of the peripheral area and overlying the substrate between the trenches in the core area. Using the patterned photoresist as an etch mask, layer of silicon nitride 92 and layer of oxide 90 are etched to remove the nitride and oxide from the patterned poly silicon 78 and 80 and to leave the nitride and oxide overlying the substrate between the trenches as illustrated in FIG. 9.

The layer of patterned photoresist is removed and another layer of photoresist (not illustrated) is applied and patterned. The layer of patterned photoresist covers the peripheral area and all of the core area except for a portion of each of contact regions 59. The patterned photoresist is used as an etch mask and layer of nitride 92, layer of oxide 90 and layer of nitride 48 exposed in the contact regions are etched to form an opening 93 as illustrated in cross section in FIG. 10 to allow a subsequent ion implantation into the contact regions. FIG. 10 illustrates a cross section through only one of contact regions 59. Recall that the contact areas are also the regions along the length of the trench in which isolating oxide 74 was grown.

The layer of patterned photoresist is removed and another layer of photoresist (not illustrated) is applied and patterned to leave the photoresist covering and protecting all of the core area. With the core area protected, nitride layer 92 is anisotropically etched to form spacers on the sidewalls of the gate electrodes in the peripheral area. After forming the spacers, the PMOS transistors are masked with photoresist and N-type ions are implanted to form the source and drain regions of the NMOS transistors in the peripheral area. The N-type ions are also implanted into the exposed portions of contact regions 59 in the core area to form drain regions 94 and source regions 95 alternating in the substrate along the length of trench 52 as illustrated in top view in FIG. 11. Channels 97 of the MOS transistors exist along the walls of the trench between the source and drain regions. In operation, current flows through the channel between the source and drain regions in a direction along the length of the trench. Isolation oxide 74 separates each channel from adjacent channels. The NMOS transistors and the core area are then masked with photoresist and P-type ions are implanted to form the source and drain regions of the PMOS transistors in the peripheral area. Following the implantations, the patterned photoresist is patterned and the implants are annealed, for example by RTA. Drain regions 94 and source regions 95, formed in the substrate bounding trenches 52, extend from the surface of the substrate to the bottom of the trench as illustrated in FIG. 12 which shows an exemplary drain region in cross section.

Any residual oxide is removed from the implanted regions including the gate electrodes and also from the poly silicon forming control gates 78 and 80 and contact area 82 and 84, for example by etching in dilute hydrofluoric acid. A silicide forming metal such as cobalt is blanket deposited and heated, for example by RTA, to form a metal silicide (not illustrated) in those locations where the metal is in contact with silicon. The metal silicide forms on the source regions, drain regions, and gate electrodes of the peripheral transistors and on the contact regions 59 forming contacts to source and drain regions 94 and 95, control gates 78 and 80 and contact areas 82 and 84 in the core area. The silicide forming metal that is not in contact with exposed silicon does not react during the RTA and can be removed, for example by washing in a H_2O_2/H_2SO_4 or HNO_3/HCl solution. After silicidation a layer of oxide is blanket deposited to a thickness great enough to fill trenches 52. The excess oxide can be removed and the upper surface of the

oxide layer is planarized, for example by CMP. Contact openings are etched through the planarized oxide to expose the surface of drain regions 94, source regions 95, and contact areas 82 and 84. Contact openings are also formed in the peripheral area to allow electrical contact to source and drain regions and to gate electrodes as necessary for the circuit function being implemented.

As illustrated in top view in FIG. 13, a layer of metal is deposited on the surface of the planarized oxide layer and is patterned to form bit lines 102, source lines 104, and word line contacts 106. Bit lines 102 electrically contact drain regions 94, source lines electrically contact source lines 95, and word line contacts 106 electrically contact control gates 78 and 80. The metal lines can be aluminum, copper, alloys of those metals, or other conductive materials commonly used for interconnection on a semiconductor integrated circuit. Although not illustrated, plug structure may be used to directly contact the metal silicide and fill the contact openings. The plug structure may include, for example, sequential layers of titanium, titanium nitride, and tungsten as is well known. The metal lines would then electrically contact the plug structure. Although the bit lines, source lines, and word lines are all illustrated to be on a single level, it may be advantageous, for optimum layout reasons, to form the bit lines and source lines in one layer of metal and to form the word lines in another layer of metal separated from the bit lines by a layer of inter level dielectric.

Integrated circuit 40 can be completed with the conventional back end of line processing which, being conventional, will not be described herein.

While at least one exemplary embodiment has been presented in the foregoing detailed description, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or exemplary embodiments are only examples, and are not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing the exemplary embodiment or exemplary embodiments. It should be understood that various changes can be made in the function and arrangement of elements without departing from the scope of the invention as set forth in the appended claims and the legal equivalents thereof.

CLAIMS

What is claimed is:

1. A semiconductor memory device [40] comprising:

a semiconductor substrate [42] having a surface [46];

a trench [52] etched into the surface of the substrate and having a first wall [54] and a second wall [56] extending away from the surface and having a bottom [58] at the extremity of the first wall and the second wall;

a first drain region [94] and a second drain region [94] formed in the semiconductor substrate along the first wall [54] and a third drain region [94] and a fourth drain region [94] formed in the semiconductor substrate along the second wall [56], each drain region extending from proximate the surface [46] toward the bottom [58];

a first source region [95] formed in the semiconductor substrate along the first wall [54] between and spaced apart from the first drain region and the second drain region and a second source region [95] formed in the semiconductor substrate along the second wall [56] between and spaced apart from the third drain region and the second drain region, each source region extending from proximate the surface [46] toward the bottom [58];

a first channel region [97] formed in the semiconductor substrate along the first wall [54] between the first drain and the first source, a second channel region [97] formed in the semiconductor substrate along the first wall [54] between the first source and the second drain, a third channel region [97] formed in the semiconductor substrate along the second wall [56] between the third drain region and the second source, and a fourth channel region [97] formed in the semiconductor substrate along the second wall [56] between the second source region and the fourth drain;

a first gate electrode [68] overlying the first channel, a second gate electrode [68] overlying the second channel, a third gate electrode [68] overlying the third channel, and a forth gate electrode [68] overlying the fourth channel;

a first word line [106] coupled to the first gate electrode and the second gate electrode and a second word line [106] coupled to the third gate electrode and the fourth gate electrode; and

a first bit line [102] coupled to the first drain region and the third drain region and a second bit line [102] coupled to the second drain region and the fourth drain region.

2. The semiconductor memory of claim 1 further comprising a first isolation oxide [74] grown at the bottom of the trench.

3. A semiconductor device [40] comprising:

a semiconductor substrate [42] having a surface [46];

a trench [52] formed in the semiconductor substrate and bounded by a trench wall [54, 56] extending from the surface to a bottom [58];

a drain region [94] formed in the substrate along the trench wall and extending from the surface [46] toward the bottom [58];

a source region [95] formed in the substrate along the trench wall and extending from the surface [46] toward the bottom [58];

a channel region [97] formed in the substrate along the trench wall between the drain region [94] and the source region [95] and extending parallel to the surface [46];

a gate insulator [66] overlying the channel; and

a gate electrode [68] overlying the gate insulator.

4. The semiconductor device of claim 3 further comprising a drain contact [59] formed at the surface and electrically contacting the drain region [94]; and a source contact [59] formed at the surface and electrically contacting the source region [95].

5. The semiconductor device of claim 3 further comprising a localized oxide [74] grown at the bottom [58].

6. A semiconductor device [40] comprising:

a semiconductor substrate [42] having a surface [46];

a trench [52] etched into the substrate and extending in a direction [152] along the surface, the trench bounded by a first wall [54] and a second wall [56];

a first MOS transistor formed along the first wall [54] comprising a first source [95], a first drain [94], and a first channel [97] extending in the direction [152] between the first source and the first drain; and

a second MOS transistor formed along the second wall [56] comprising a second source [95], a second drain [94], and a second channel [97] extending in the direction [152] between the second source and the second drain.

7. The semiconductor device of claim 6 wherein the first wall [54] and the second wall [56] extend into the substrate [42] to a bottom [58] and wherein the semiconductor device further comprises an isolation oxide [74] grown at the bottom of the trench and electrically isolating the first MOS transistor from the second MOS transistor.

8. The semiconductor device of claim 7 wherein the first source [95] and the first drain [94] each extend from the surface [46] toward the bottom [58] along the first wall [54] and the second source [95] and the second drain [94] each extend from the surface [46] toward the bottom [58] along the second wall [56].

9. The semiconductor device of claim 8 further comprising contact areas [59] to the first source, first drain, second source and second drain, each of the contact areas located on the surface [46].

10. The semiconductor device of claim 6 further comprising:

a first gate electrode [78] overlying the first channel, extending along the first wall, and having a first portion [82] overlying the substrate; and

a second gate electrode [80] overlying the second channel, extending along the second wall, and having a second portion [84] overlying the substrate.

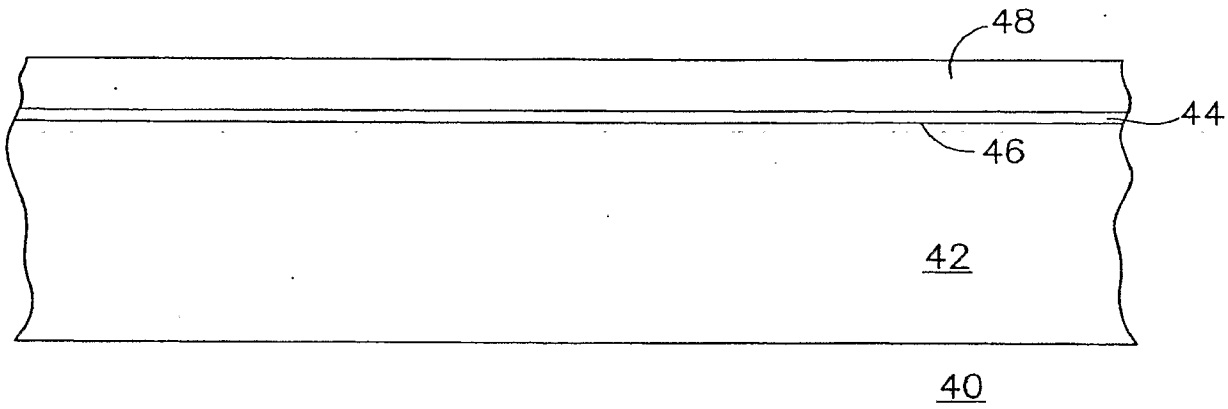

FIG. 1

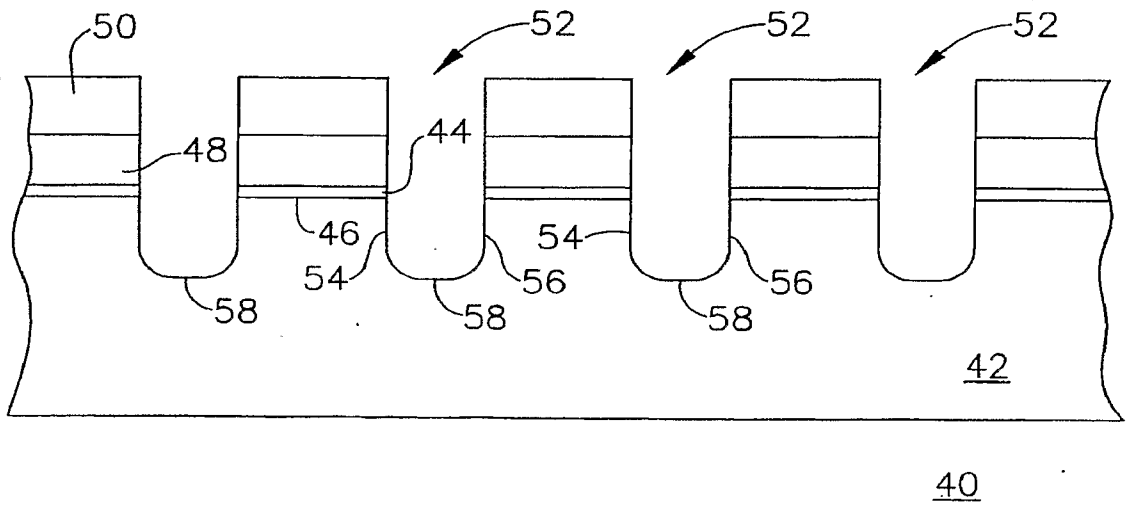

FIG. 2

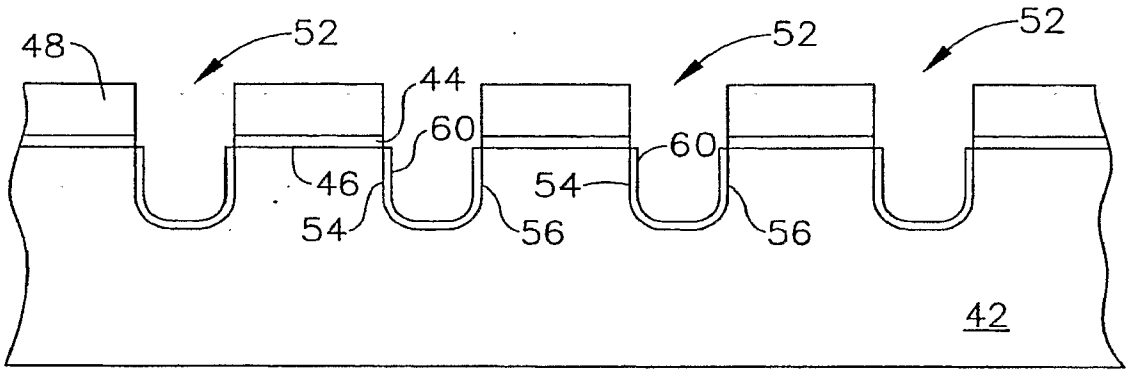

FIG. 3

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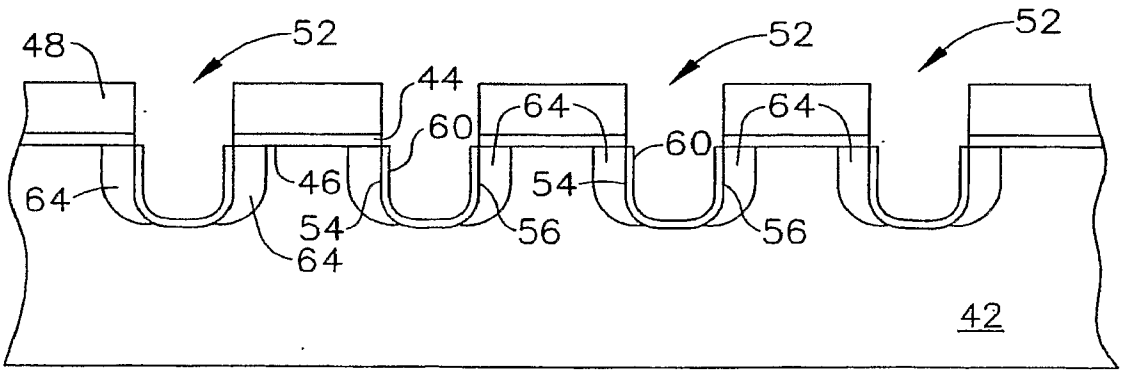

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FIG. 5

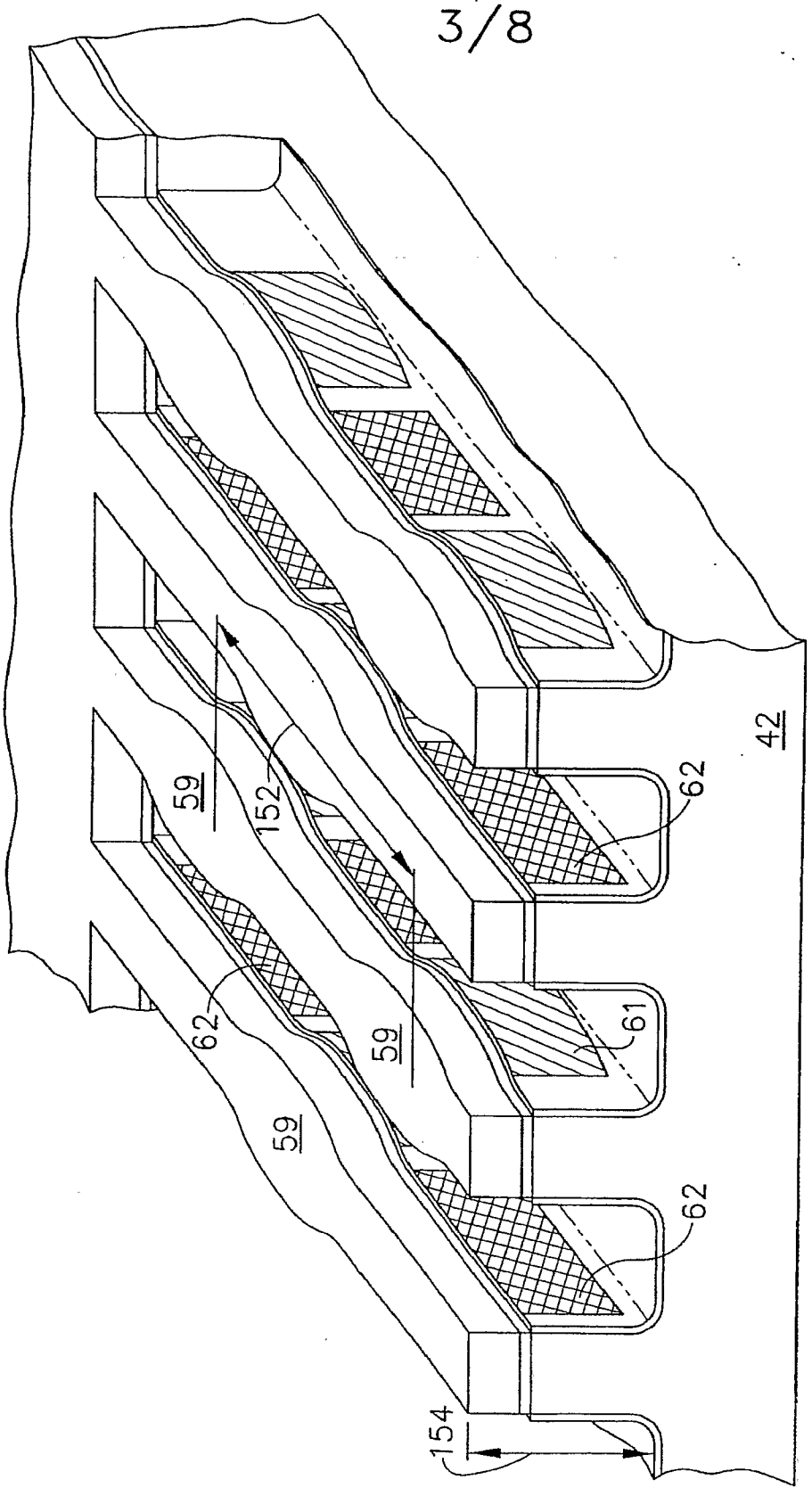

FIG. 4

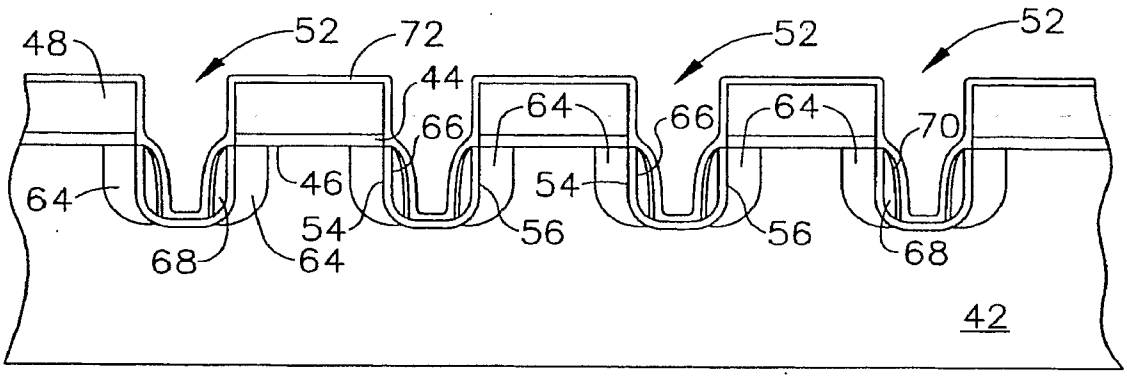

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FIG. 6

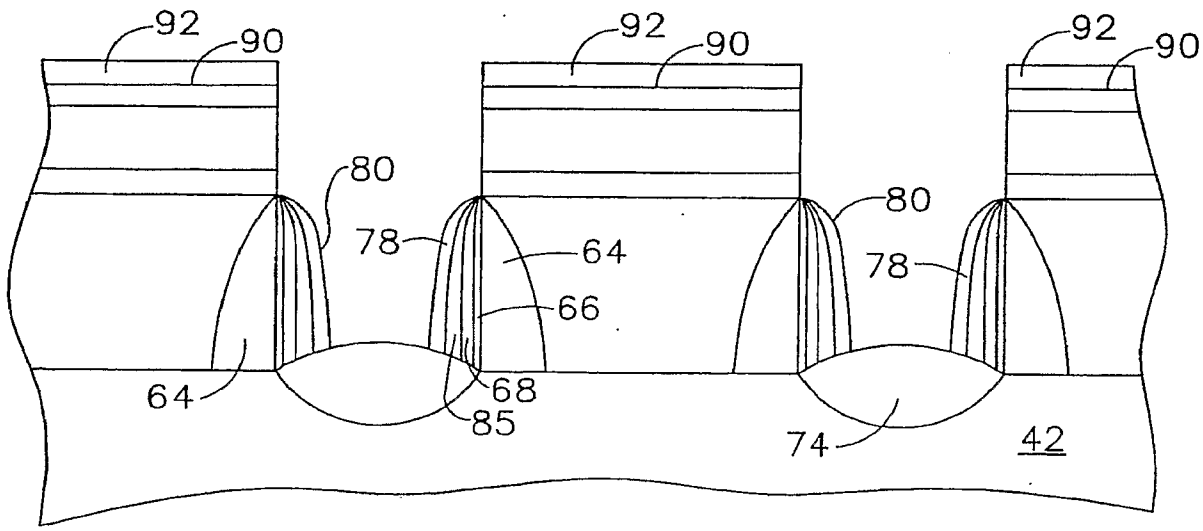

FIG. 9

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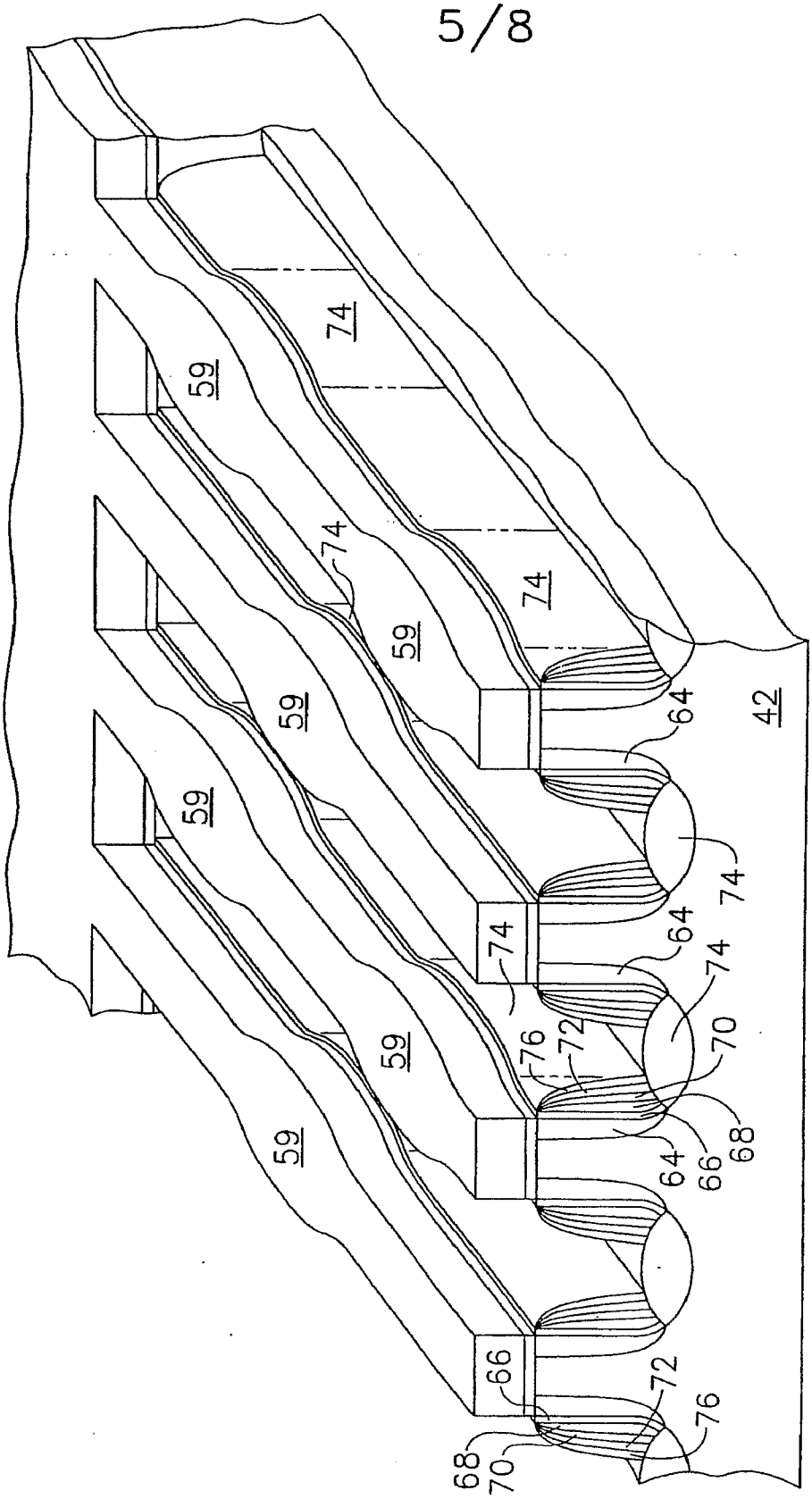

FIG. 7

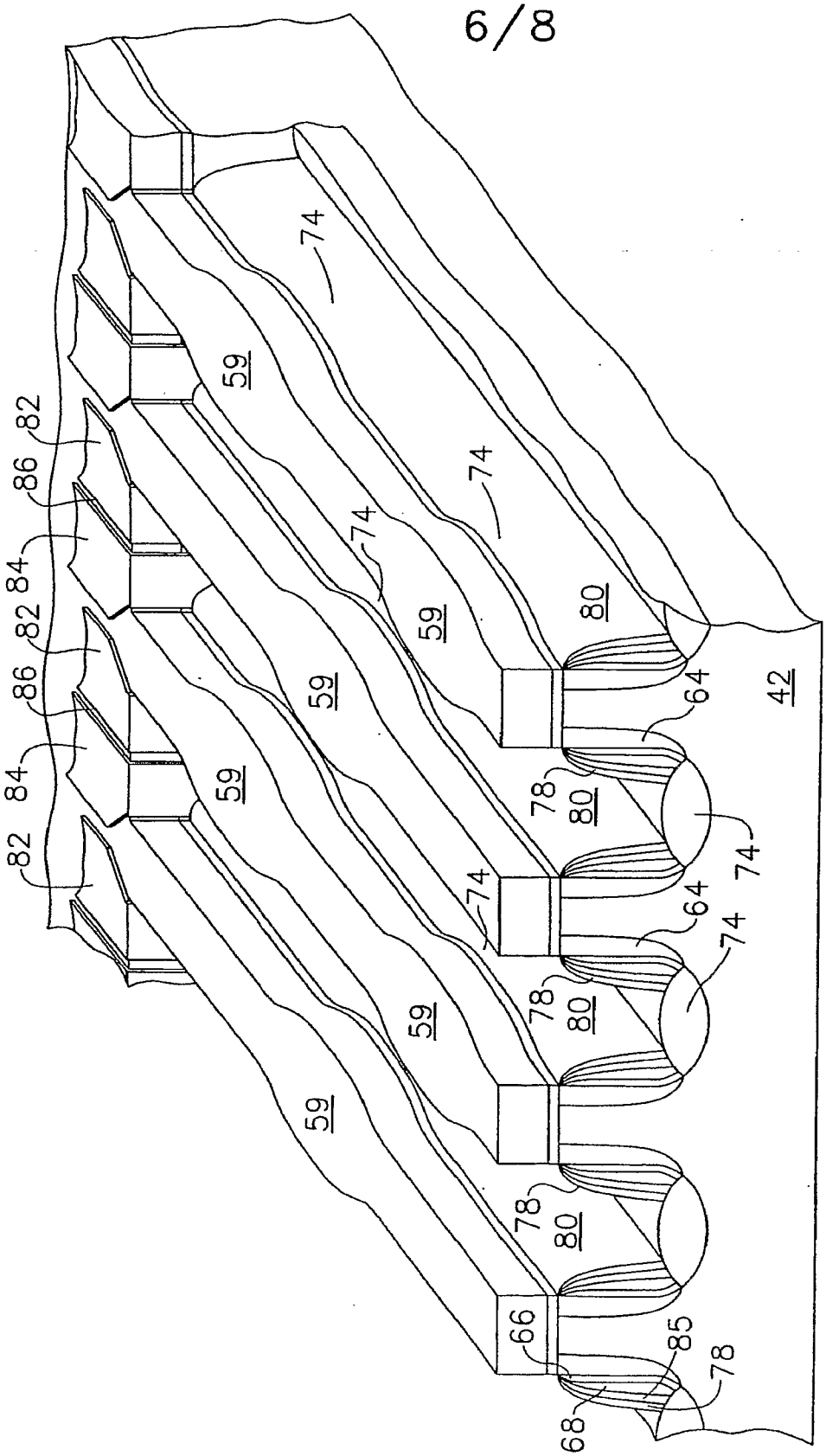

FIG. 8

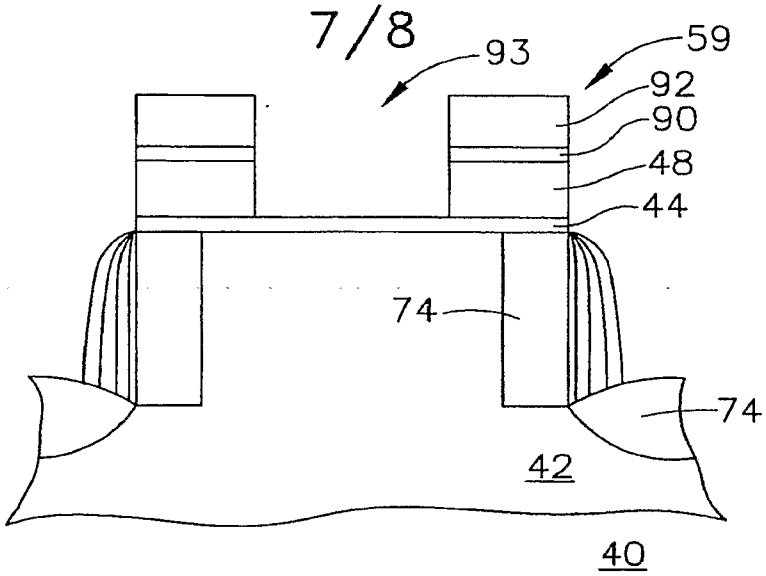
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FIG. 10

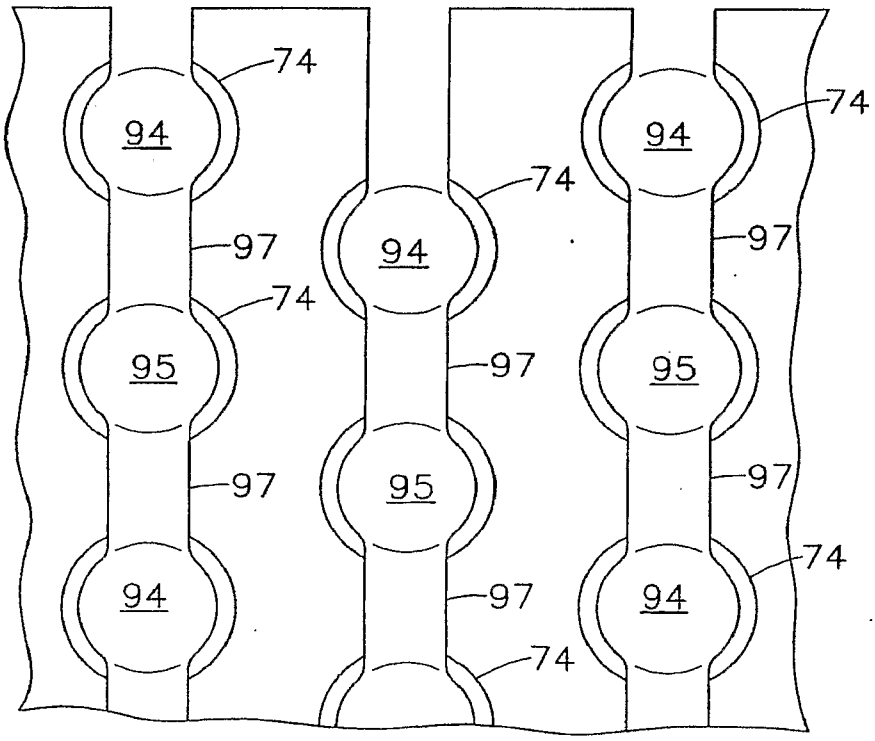
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FIG. 11

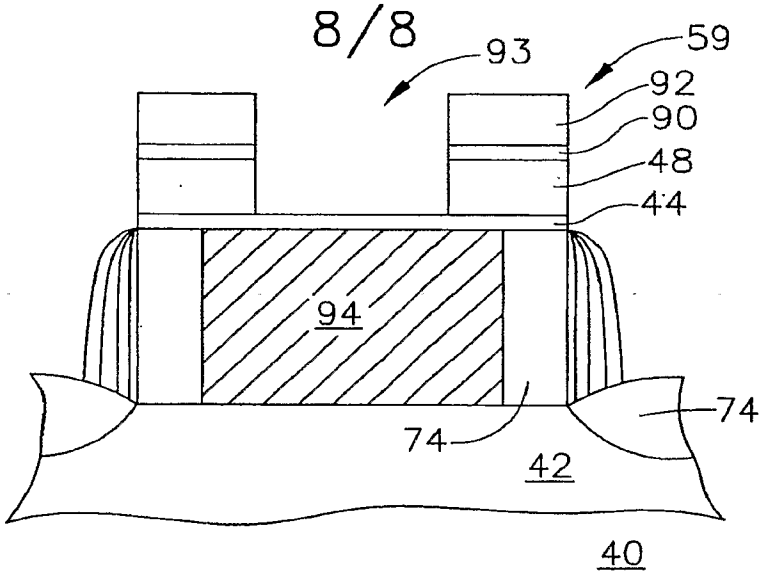
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FIG. 12

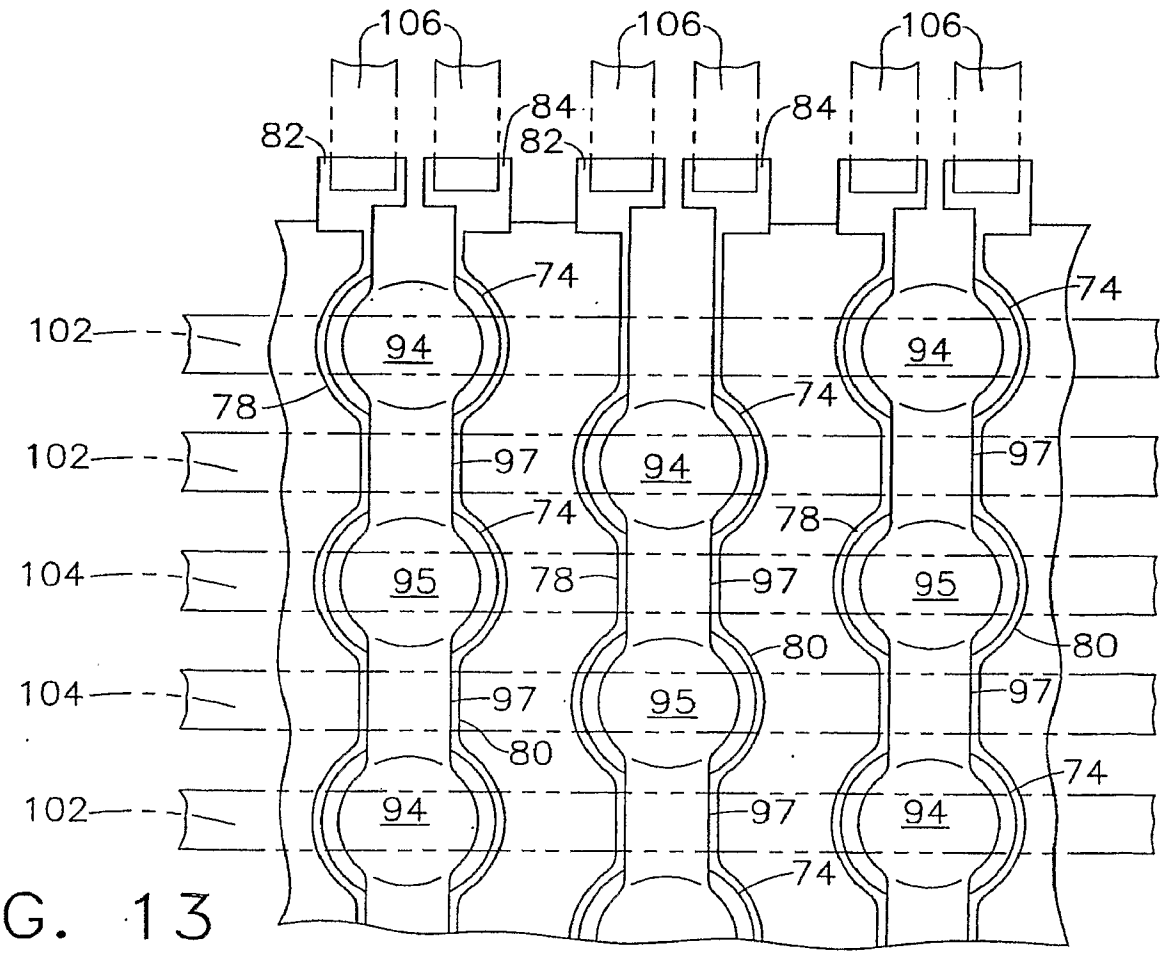
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FIG. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/006715

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/336 H01L21/8247 H01L27/115 H01L29/788
ADD. H01L27/105 H01L27/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/232472 A1 (SAKUI KOJI [JP] ET AL) 25 November 2004 (2004-11-25) paragraphs [0016], [0017], [0093] - [0127]; figures 1-34,45	1-10
X	JP 07 045797 A (TOKYO SHIBAURA ELECTRIC CO) 14 February 1995 (1995-02-14) the whole document	1-10
X	WO 03/096425 A (INFINEON TECHNOLOGIES AG [DE]; HOFMANN FRANZ [DE]; SPECHT MICHAEL [DE]) 20 November 2003 (2003-11-20) page 3, line 4 - page 6, line 30; figures 1-5	1-10

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
21 August 2007	28/08/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Neumann, Andreas

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/006715

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5 804 854 A (JUNG SUNG MUN [KR] ET AL) 8 September 1998 (1998-09-08) figure 4	
A	US 6 831 310 B1 (MATHEW LEO [US] ET AL) 14 December 2004 (2004-12-14) figure 12	

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Information on patent family members

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