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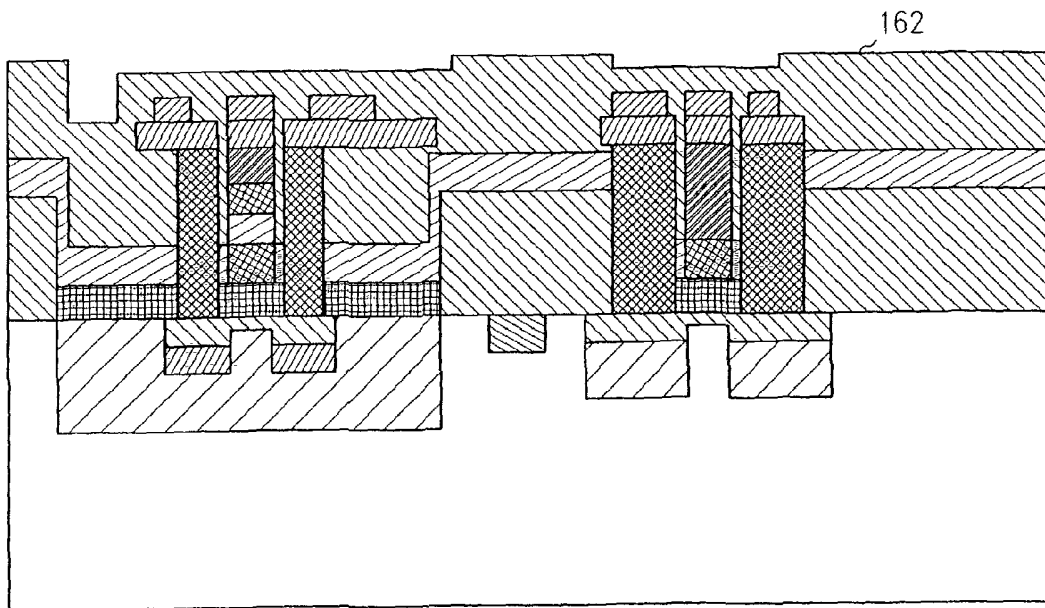
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(54) Title: SILICON CARBIDE MICROELECTROMECHANICAL DEVICES WITH ELECTRONIC CIRCUITRY



(57) Abstract: A method of forming electronics and microelectromechanical on a silicon carbide substrate having a slow etch rate is performed by forming circuitry on the substrate. A protective layer is formed over the circuitry having a slower etch rate than the etch rate of the silicon carbide substrate. Microelectromechanical structures supported by the substrate are then formed. The circuitry comprises a field effect transistor in one embodiment, and the protective layer comprises a heavy metal layer.



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Silicon Carbide Microelectromechanical Devices With Electronic Circuitry

Related Application

This application claims the benefit of priority under U.S.C. 119(e) to U.S. Provisional Patent Application Serial No. 60/362,618, filed on March 8, 2002, which is incorporated herein by reference.

Government Funding

The invention described herein was made with U.S. Government support under Grant Number ECS-9875206 awarded by National Science Foundation. The United States Government has certain rights in the invention.

Field of the Invention

The present invention relates to forming devices on silicon carbide, and in particular to monolithically integrating microelectromechanical devices with electronic circuitry on silicon carbide.

Background of the Invention

Microelectromechanical devices (MEMS) are currently being formed on silicon substrates with integrated circuitry. However, silicon based circuitry is not well suited to harsh environments. More and more applications or MEMS devices are being considered for harsh environments, and there is a need for a more robust combination of MEMS and circuitry that can withstand high temperatures.

Summary of the Invention

Microelectromechanical (MEMS) devices with electronic circuitry are formed on a common silicon carbide substrate. MEMS devices are fabricated as part of a silicon carbide electronics process enabling formation of bulk

piezoresistive strain sensing regions or surface micromachined electrostatic sensing regions.

In one embodiment, the electronic circuitry process includes temperature compensated metal-oxide semiconductor (MOS) devices for signal conditioning and system control by programmable digital function via non-volatile memory
5 for custom, programmable logic.

Leveraging off of the unique material properties of silicon carbide, a platform for the fabrication of monolithically integrated microelectromechanical devices with electronic circuitry is established. Processing steps enable not only
10 the fabrication of the structural and electronic parts individually, but also the monolithic integration of these parts onto the same substrate.

In one embodiment, electronics are partially fabricated, a protective layer is formed, and then MEMS structures and remaining electronics are formed. There are several options for the MEMS structures including a bulk
15 micromachining process yielding membranes or bossed membranes or cantilevers with or without proof masses and a surface micromachining process with two structural layers for planar structures. The transducer action in this process for converting mechanical motion into electrical signals arise from either piezoresistive strain sensing regions in the bulk process or from electrostatic
20 sensing from the surface micromachined process.

The electronics portion of the process includes MOS structures, compensated for high-temperature operation, that can be used as analog amplifiers or signal control circuitry. In addition, non-volatile memory structures are fabricated to provide digital and logic functions for
25 programmability.

In a further embodiment, one or more silicon carbide microelectromechanical device is integrated with electronic circuitry on a common silicon carbide substrate. The MEMS device is fabricated as part of the silicon carbide electronics process, allowing bulk piezoresistive strain sensing
30 regions or surface micromachined electrostatic sensing regions to be formed

from MEMS elements ranging bulk micromachined to surface micromachined structures. The electronic circuitry process includes temperature compensated MOS circuits for signal conditioning and system control by programmable digital function via non-volatile memory for custom, programmable logic.

5

Brief Description of the Drawings

FIG.s 1A, 1B, 1C, 1D, 1E, 1F 1G, 1H, 1I, 1J, 1K, 1L, 1M, and 1N are cross section

representations of the formation of electronics and MEMS devices on a
10 silicon carbide substrate.

FIG. 2 is a block diagram of options for forming different structures.

FIG. 3 is a cross section showing the formation of electronics following formation of a protective layer.

FIG. 4 is a cross section showing bulk micromachining following formation of a
15 protective layer.

FIG.s 5A, 5B, 5C, 5D and 5E are cross sections showing surface micromachining following formation of a protective layer.

20

Detailed Description of the Invention

In the following description, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These
25 embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the scope of the present invention. The following description is, therefore, not to be taken in a limited sense, and the scope of the present
30 invention is defined by the appended claims.

Monolithic integration of microelectromechanical devices (MEMS) and electronics on silicon has been successfully implemented over the past several years. However, such devices normally fail in harsh environmental conditions. Devices formed on SiC fare much better in harsh environments, but it has proven
5 difficult to integrate such devices with electronics.

A major challenge in integration of SiC based MEMS with electronics involves processing. Due to SiC's inertness to most wet etch chemistry employed in silicon CMOS processes, plasma based deep reactive ion etching (DRIE) may be employed to form the MEMS structure. This provides a unique
10 challenge during electronic device integration due to the damage that a long DRIE process can cause in electronic devices and circuits. Maintaining a metal oxide semiconductor interface where a metal oxide semiconductor field effect transistor (MOSFET) gate resides is important to the success of creating a usable
15 MOSFET. It must be protected during the process while forming the MEMS structure.

In one embodiment, a protective layer such as electroplated heavy metals is formed over the electronic circuitry. Because of the slow etch rates of SiC, oxide based protective layers may etch too quickly to do the job. The protective layer is on the order of 10s of microns of nickel in one embodiment. The layer
20 thickness is limited to ensure successful use lift off. Other heavy metals can be used. A sacrificial masking material that will survive longer than the etch rate of the SiC bay also be used. In one embodiment, the sacrificial layer has an etch rate on the order or 1 micrometer per minute in a flourinated plasma. SF₆, CF₄ or a wet etch in a hot bath of ammonia is used for the etch. In a further
25 embodiment, through holes in a desired shape facilitating formation of MEMS devices are cut in the SiC substrate prior to formation of circuitry.

A method is disclosed for integrating one or more silicon carbide microelectromechanical (MEMS) devices with electronic circuitry on a common silicon carbide substrate. The MEMS device is fabricated as part of the silicon
30 carbide electronics process allowing bulk piezoresistive strain sensing regions or

surface micromachined electrostatic sensing regions to be formed. In one embodiment, the electronic circuitry process includes temperature compensated MOS for signal conditioning and system control by programmable digital function via non-volatile memory for custom, programmable logic.

5 Leveraging off of the unique material properties of silicon carbide, a platform for the fabrication of monolithically integrated microelectromechanical devices with electronic circuitry is established. The material properties of silicon carbide presents many fabrication challenges. To address these challenges a unique and novel process sequence has been developed along with
10 unique processing steps to enable not only the fabrication of the structural and electronic parts individually, but also the monolithic integration of these parts onto the same substrate. Methods developed for silicon substrates do not simply transfer to silicon carbide. A different approach in fabrication is required to develop these structures.

15 In one embodiment, electronics are partially fabricated followed by the MEMS structures and remaining electronics. There are several options for the MEMS structures including a bulk micromachining process yielding membranes or bossed membranes or cantilevers with or without proof masses and a surface micromachining process with two structural layers for planar structures. The
20 transducer action in this process for converting mechanical motion into electrical signals arise from either piezoresistive strain sensing regions in the bulk process or from electrostatic sensing from the surface micromachined process.

 The electronics portion of the process includes MOS structures, compensated for high-temperature operation, that can be used as analog
25 amplifiers or signal control circuitry. In addition, non-volatile memory structures are fabricated to provide digital and logic functions for programmability.

 In a further embodiment, one or more silicon carbide microelectromechanical devices are integrated with electronic circuitry on a
30 common silicon carbide substrate. The MEMS devices are fabricated as part of

the silicon carbide electronics process, allowing bulk piezoresistive strain sensing regions or surface micromachined electrostatic sensing regions to be formed from MEMS elements ranging bulk micromachined to surface micromachined structures. The electronic circuitry process includes temperature compensated

5 MOS for signal conditioning and system control by programmable digital function via non-volatile memory for custom, programmable logic.

A detailed fabrication flow for monolithic integration of SiC MEMS with SiC electronic devices and circuits process follows. Using this process functional

10 electronic devices and circuits may be formed that operate at approximately 280°C as well as MEMS structures. The process allows for the MEMS structure to be fabricated at the beginning, intermediate, or at the very end of the process flow. If the MEMS component is fabricated prior to any electronic device processing, care must be taken to ensure that the MEMS structures are not

15 damaged during the ion implant activation thermal cycle (1600°C for 30 minutes). Ideally, the MEMS structure will be fabricated immediately following all ion implantations and high temperature activation steps. Further, the MEMS structure can also be fabricated after all of the electronic devices are processed. In this case, a thick protective passivation dielectric is deposited on top of the

20 electronics. Since long duration DRIE steps are used to form the MEMS structures, circuit layout may require considerable attention and thought prior to fabrication. For example, a layout is arranged such that that finished devices and circuits are protected from the high energy plasma by the ~ 15 microns thick nickel DRIE mask.

Further electronic devices which may be formed include P-N and Schottky

25 diodes, MOS and MIM capacitors, N and P-enhancement MOSFETs, N-type normally on depletion NMOSFETs, and signal conditioning amplifier circuitry to process data taken from the MEMS structure. These devices and circuits may be functional up to approximately 280°C or higher. Further MEMS structures include bulk micro-machined circular diaphragm pressure/acceleration sensor

30 with piezoresistors used for strain sensing.

The following is an example of process flow for fabricating the silicon carbide electronics and MEMS structures as shown in FIG.s 1A through 1U.

FIG. 1A shows a single-crystal silicon carbide substrate 100 that is used
5 to start the process. In one embodiment, an approximately 3 micrometer
epitaxial layer of SiC is formed on the wafer to provide a base substrate prior to
circuit formation. The epitaxial layer can be doped to a desired concentration.
In further embodiments, ion implantation is used to dope the substrate to a
desired concentration.

10 The substrate 100 surfaces are conditioned by solvent clean and acid clean. In
one embodiment, at least one surface 100 is so conditioned. A registration mark
103 is etched into the substrate for alignments between different mask steps.
Multiple such marks may be used. The surface 100 is patterned for formation of
P wells 104. P-type dopants are introduced via ion implantation or selective
15 epitaxy to define the P wells. The substrate surface is then patterned again for
forming N wells. N-type dopants are introduced via ion implantation or
selective epitaxy to define N Wells 106. Surface 100 is then patterned for
introduction of P-type dopants via ion implantation or selective epitaxy to define
P+ Regions 108 for a PFET device. Surface 100 is then patterned for
20 introduction of N-type dopants via ion implantation or selective epitaxy to define
N+ Regions at 106 for a NFET device.

A threshold adjustment implant for MOSFETS is then performed as
indicated at 110 and 112. The threshold adjustment implant allows for the
lowering of the threshold
25 voltages of enhancement MOSFETs as well as the realization of normally on
depletion mode MOSFETs. Then, a field dielectric layer 114 is deposited, which
is then patterned to define active areas as indicated in FIG. 1B. A layer of gate
dielectric 116 is thermally grown or deposited and patterned as seen in FIG. 1C.
A polysilicon layer, doped or undoped, or other gate electrode material, is

deposited at 118. A gate electrode layer is patterned to form Gate1 at 118 in FIG. 1D.

In FIG. 1E, a layer of dielectric 120 is thermally grown or deposited. A polysilicon layer, doped or undoped, or other gate electrode material, is deposited. Gate electrode layer is patterned to form Gate2 at 124.

As seen in FIG. 1F, P+ and/or N+ ohmic contact formation is then performed following different options. In a first option, a same metal 128, 130 is deposited for P+ and N+ contacts respectively, followed by one annealing step. In an alternative, the same metal is actually a combination of metals suitable for forming contacts. In a second option, metal is deposited for P+ and N+ contacts in separate steps, followed by one annealing step. In a third option, metal is deposited and an anneal is performed for P+ and N+ contacts in separate steps all as represented at 128 and 130 respectively.

A layer of dielectric 134 is deposited as seen in FIG. 1G. Vias to Poly Silicon gates are shown in FIG. 1H. Dielectric layer 134 is then patterned and etched to define source/drain vias, Gate1 via 136 and Gate2 via at 138 as seen in FIG. 1H. The vias are filled with metal 140 as seen in FIG. 1I. A metal1 layer 144 is deposited, patterned and etched as seen in FIG. 1J. A layer of dielectric 148 is then deposited. The dielectric layer is patterned and etched to define Inter-Metallic Vias 150 as seen in FIG. 1K. The Inter-Metallic Vias are filled with metal 154 as seen in FIG. 1L. A Metal2 layer 160 is then deposited, patterned and etched as seen in FIG. 1M. This layer serves as a further interconnect level. A layer of dielectric 162 is then deposited as seen in FIG. 1N. Dielectric 162 is thick, and serves as a protection layer to inhibit degradation of the electronic devices formed beneath it in response to etching of MEMS structures.

As seen in FIG. 2, there are several options available following the dielectric deposition. Box 210 illustrates the ability to select and option. A first option, Option A 220 is followed if only electronics formation is needed. An Option B 230 is followed if surface-micromachined MEMS structures with

electronics are to be included. Option C 240 is followed if bulk-micromachined MEMS structures with electronics are to be included. A further option 250 utilizes two or more of the options, such as use of Option B then Option C if both bulk- and surface-micromachined structures are desired.

5 Option A is shown in the cross sections of FIG. 3. Option A is utilized for the formation of electronics only. Dielectric is patterned and etched to define Pad Cuts 310. Deeper cuts to the substrate may also be made, making it possible to contact the substrate directly. This can be useful for example in forming Schottky Barrier diodes etc.

10 Option B is shown in the cross section of FIG. 4 showing Bulk Micromachining. A second, or backside mask is used to pattern a backside 410 of the substrate. A backside etch is then performed to form openings 415 and 420. A first side 425 of the substrate is then patterned using a topside mask. A topside etch is then performed to provide through holes 430 opening to backside 15 410 through opening 420. A released structure 433 is formed by such etches. In one embodiment, various released structures include cantilever, beams with mass, or bossed structures. Dielectric is patterned and etched to define Pad Cuts 435. Vestiges of metal layer 160 remain after such etching.

20 It should be noted that the dimensions illustrated in the figures are not to scale and some features are shown much larger with reference to others to enhance visibility of them. In one embodiment, the substrate is approximately 100 to 300 micrometers thick, while the layers formed on top of the substrate are approximately 3 to 5 microns thick. P wells 104 are approximately 1 micron thick, and opening 415 extends to approximately 50 micrometers of the top of 25 the substrate. These dimensions are for example only, and may be modified significantly without departing from the invention.

30 Option C for Surface Micromachining is shown in FIG.s 5A-5E. A top passivation and sacrificial dielectric layer 510 are deposited on top of a patterned metal ground plane 515 as seen in FIG. 5A. The metal layer is formed on top of an insulator dielectric such as SiO₂. A via 520 or multiple vias are formed as by

etching to the metal ground plane 515 following patterning. A first structural layer 525 is deposited and patterned, followed by a deposition of a second sacrificial oxide 530 as seen in FIG. 5B. A via or vias 535 to the first structural layer 525 is formed after patterning in FIG. 5C. A second structural layer 540 is deposited and patterned in FIG. 5D. Pad Cuts are defined and the sacrificial layer 510 is etched to simultaneously release structures 525 and 540.

One example of a devices constructable using this fabrication process is intelligent microsystems for high acceleration, high-g load, and high temperature applications.

10 In one fabrication example, the process is started with a 1' diameter, Cree, Inc. research grade n-type 6H-SiC (3.5° off from 0001 direction) wafer is utilized. The wafer contains an ~5 micron thick n-type ($n_d=2.9 \times 10^{15} \text{ cm}^{-3}$) epitaxial layer. A non-self aligned process is adopted for the electronics fabrication in one embodiment. Ion implantations at 600°C (P-well, N+, and P+ implants) and room temperature (threshold adjustment implant) are used to form the P-well, N+, and P+ regions as well as to adjust the threshold voltage of the normally-on depletion mode NMOSFETs. The dose and energy of the implant species used in one embodiment follow. Many other dose and energy levels may be utilized due to the protection provided by the protection layer. Such doses and energy levels may be varied to obtain different desired device characteristics.

P+ (Aluminum): $2.2 \times 10^{14} \text{ cm}^{-2}$ @ 40keV, $3.4 \times 10^{14} \text{ cm}^{-2}$ @ 80keV, $4 \times 10^{14} \text{ cm}^{-2}$ @ 130keV, and $1 \times 10^{15} \text{ cm}^{-2}$ @ 210keV.

25 N+ (Nitrogen): $4 \times 10^{15} \text{ cm}^{-2}$ @ 30keV, $6 \times 10^{15} \text{ cm}^{-2}$ @ 65keV, $8 \times 10^{15} \text{ cm}^{-2}$ @ 115keV, and $1.4 \times 10^{16} \text{ cm}^{-2}$ @ 190keV.

P-Well (Boron): $3.75 \times 10^{12} \text{ cm}^{-2}$ @ 15keV, $6.3 \times 10^{12} \text{ cm}^{-2}$ @ 35keV, $9.3 \times 10^{12} \text{ cm}^{-2}$ @ 70keV, $1.44 \times 10^{13} \text{ cm}^{-2}$ @ 125keV, $2.69 \times 10^{13} \text{ cm}^{-2}$ @ 230keV, and $6 \times 10^{13} \text{ cm}^{-2}$ @ 360keV.

30 N-Threshold Adjusting Implant (Nitrogen): $1 \times 10^{12} \text{ cm}^{-2}$ @ 23keV, $1.5 \times 10^{12} \text{ cm}^{-2}$ @ 58keV, $2 \times 10^{12} \text{ cm}^{-2}$ @ 110keV, and $3.8 \times 10^{12} \text{ cm}^{-2}$ @ 190keV.

After ion implantation and a subsequent RCA clean, a thin (~200Å) layer of silicon dioxide is thermally grown and stripped off via HF dip. A blanket “implant activation” is done at 1600⁰C for 30 minutes in argon ambient. Following a second RCA clean, a combination of grown (at 1150⁰C for 2 hours) and deposited (at 800⁰C) gate oxidation is used to form a gate dielectric with total thickness of 750Å. P+ doped poly silicon is used to form the gate electrode. Aluminum and titanium are used to form ohmic contacts to the P+ and N+ regions respectively, and platinum is used as the interconnect metal for both metal levels.

Claims

1. A method of forming electronics and microelectromechanical on a silicon carbide substrate having a slow etch rate, the method comprising:
forming circuitry on the substrate;
forming a protective layer over the circuitry having a slower etch rate than the etch rate of the silicon carbide substrate; and
forming a microelectromechanical structure supported by the substrate.
2. The method of claim 1 wherein the circuitry comprises a field effect transistor.
3. The method of claim 1 wherein the protective layer comprises a heavy metal layer.
4. The method of claim 3 wherein the protective layer is electroplated.
5. The method of claim 3 wherein the protective layer has an etch rate of approximately 1 micrometer per minute.
6. The method of claim 3 wherein the protective layer comprises nickel.
7. The method of claim 1 wherein the protective layer is formed approximately 10 micrometers thick.
8. The method of claim 1 wherein the microelectromechanical structure comprises a sensor.
9. The method of claim 1 wherein the microelectromechanical structure is selected from the group consisting of piezoresistive strain sensors and electrostatic sensing regions.

10. The method of claim 1 wherein the circuitry comprises temperature compensated MOS devices.
11. The method of claim 10 wherein the circuitry functions at temperatures at or above 280 °C.
12. The method of claim 11 and further comprising growing an epitaxial layer of SiC on top of the substrate.
13. The method of claim 11 and further comprising implanting impurities in the substrate by ion implantation.
14. The method of claim 1 wherein the circuitry is formed prior to the protective layer and the microelectromechanical structure.
15. The method of claim 1 wherein the protective layer is formed prior to forming the microelectromechanical structure.
16. The method of claim 1 wherein portions of the microelectromechanical structure are formed prior to forming the circuit.
17. A method of forming a device on a silicon carbide substrate, the method comprising:
 - forming wells for a field effect transistor using ion implantation or selective epitaxy;
 - adjusting a threshold for the field effect transistor;
 - forming electrodes for the field effect transistor;
 - forming ohmic contacts;
 - defining source/drain, and multiple gate vias;

forming inter-metallic vias;
forming a protective metal layer;
forming a layer of dielectric over the protective metal layer;
forming microelectromechanical devices after formation of the protective metal layer.

18. The method of claim 17 wherein the microelectromechanical devices are formed on a side of the substrate opposite the side on which the transistor is formed.

19. The method of claim 17 wherein the protective layer is electroplated.

20. The method of claim 17 wherein the protective layer has an etch rate of approximately 1 micrometer per minute.

21. The method of claim 17 wherein the protective layer comprises nickel.

22. The method of claim 17 wherein the protective layer is formed approximately 10 micrometers thick.

23. The method of claim 17 wherein the microelectromechanical structure comprises a sensor.

24. The method of claim 17 wherein the microelectromechanical structure is selected from the group consisting of piezoresistive strain sensors and electrostatic sensing regions.

25. The method of claim 17 wherein the circuitry comprises temperature compensated MOS devices.

26. The method of claim 17 and further comprising growing an epitaxial layer of SiC on top of the substrate.
27. A method of forming a device on a silicon carbide substrate, the method comprising:
- forming wells for a field effect transistor using ion implantation or selective epitaxy;
 - adjusting a threshold for the field effect transistor;
 - forming electrodes for the field effect transistor;
 - forming ohmic contacts;
 - defining source/drain, and multiple gate vias;
 - forming inter-metallic vias;
 - forming a protective metal layer;
 - forming a layer of dielectric over the protective metal layer;
 - forming vias to a metal ground plane;
 - forming structural layers; and
 - releasing the structural layers.
28. A device formed on a silicon carbide substrate, the device comprising:
- circuitry formed on the substrate;
 - vestiges of a protective layer over the circuitry having a slower etch rate than the etch rate of the silicon carbide substrate; and
 - a microelectromechanical structure supported by the substrate.

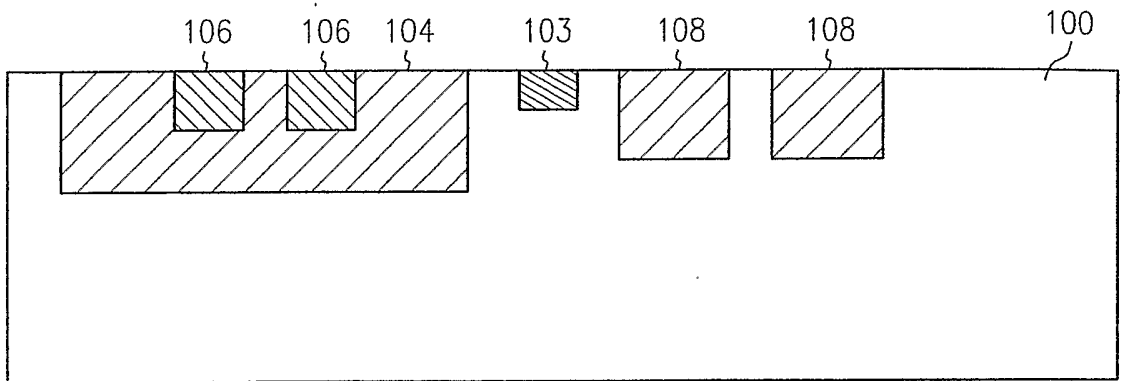


FIG. 1A

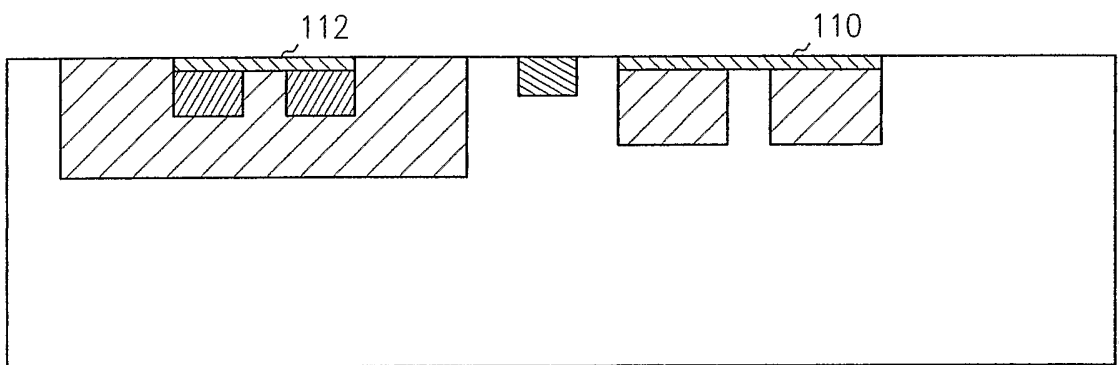


FIG. 1B

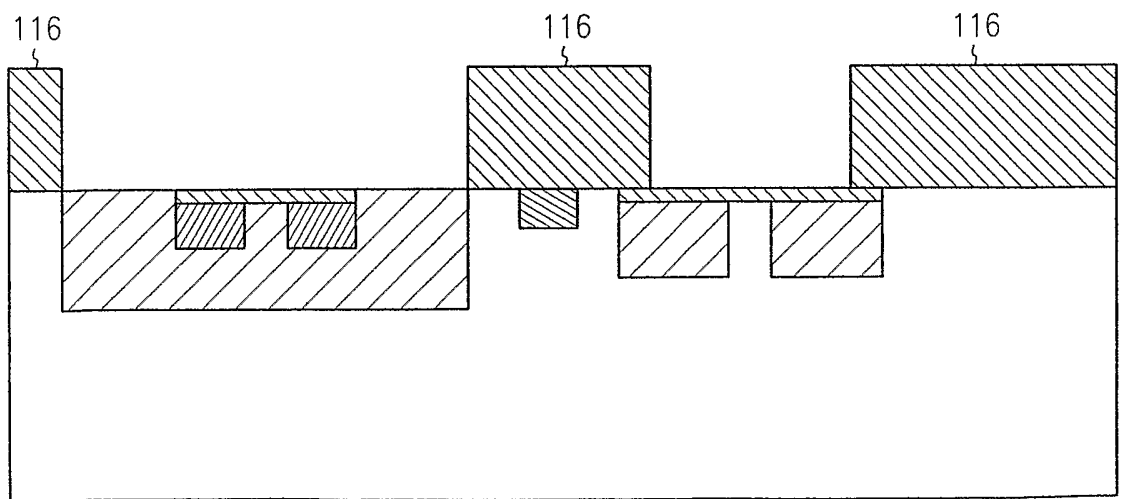


FIG. 1C

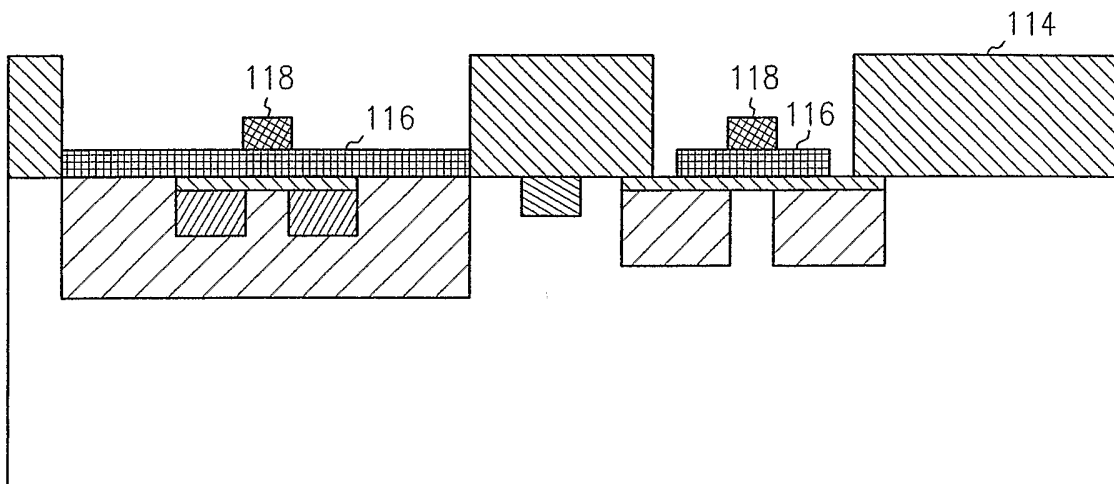


FIG. 1D

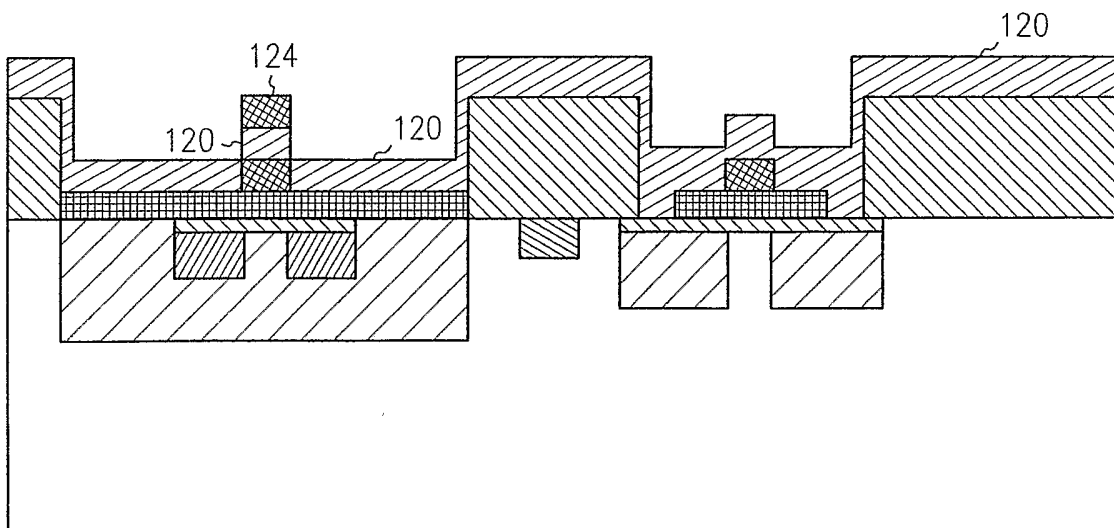


FIG. 1E

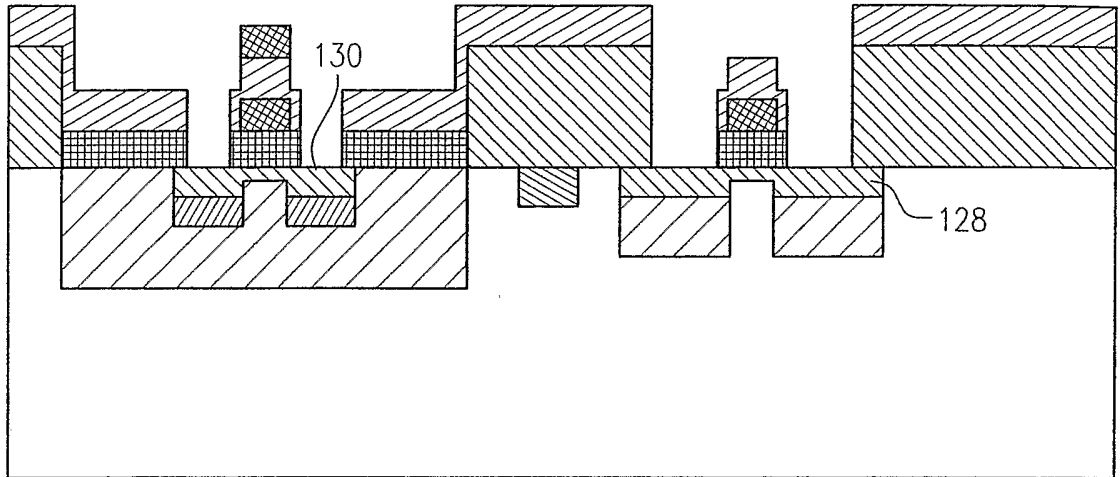


FIG. 1F

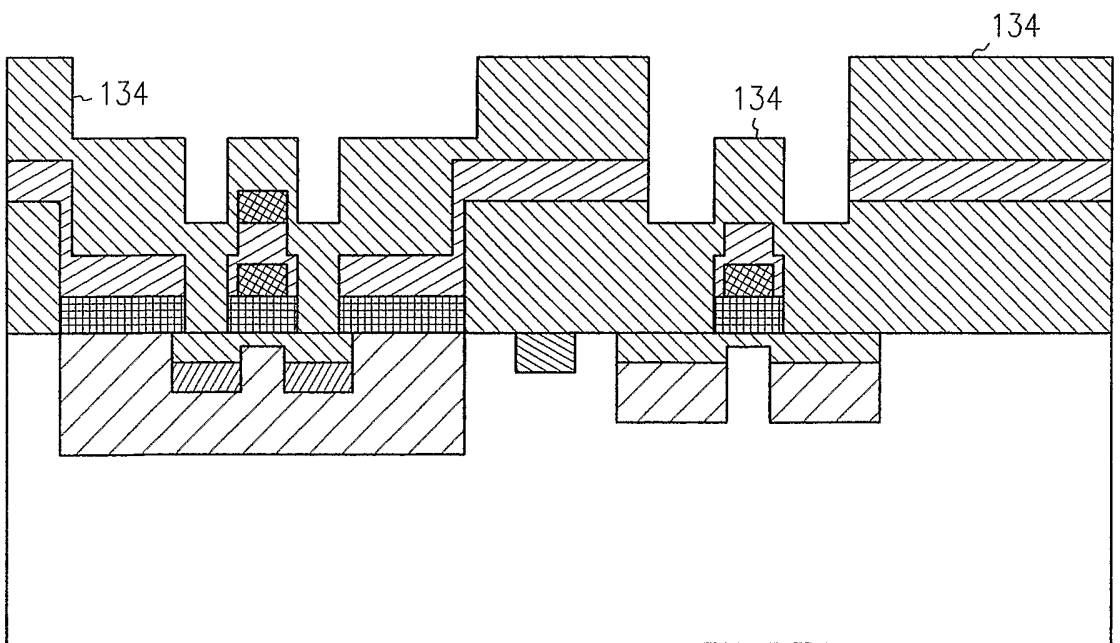


FIG. 1G

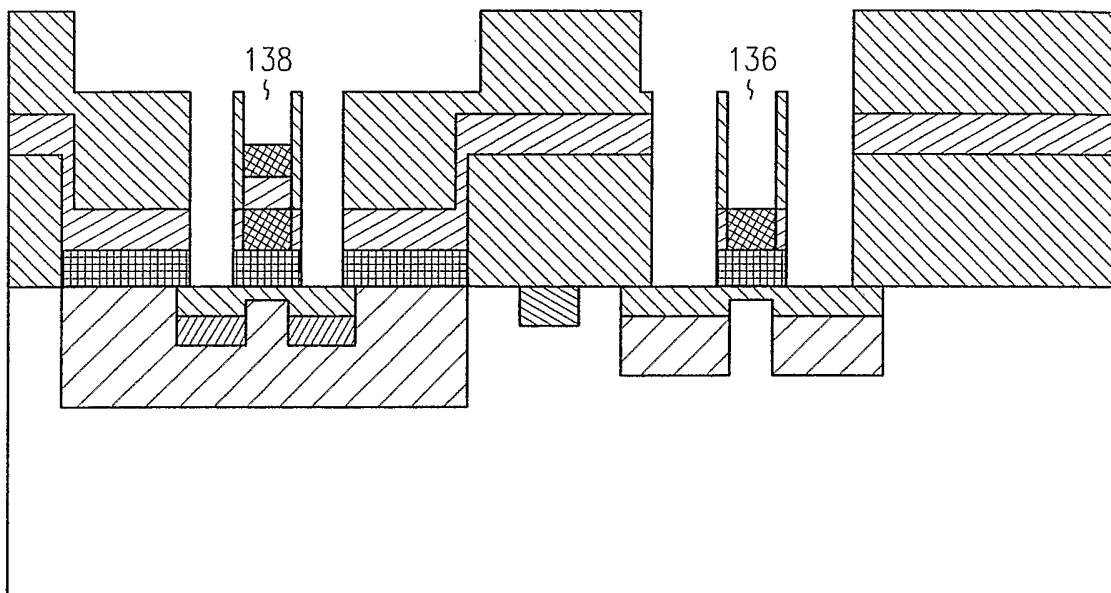


FIG. 1H

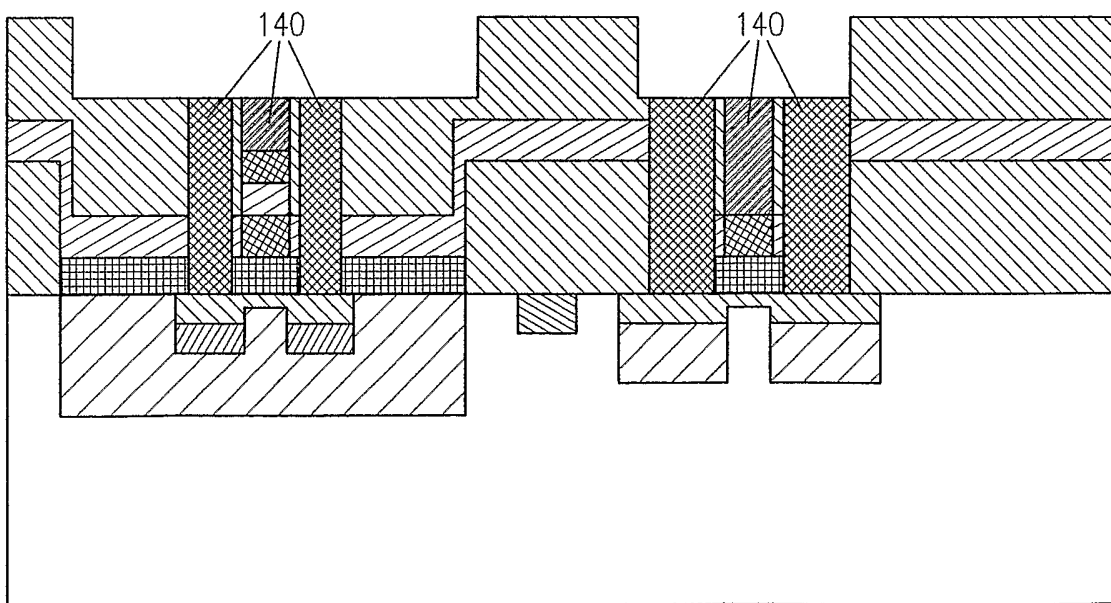


FIG. 1I

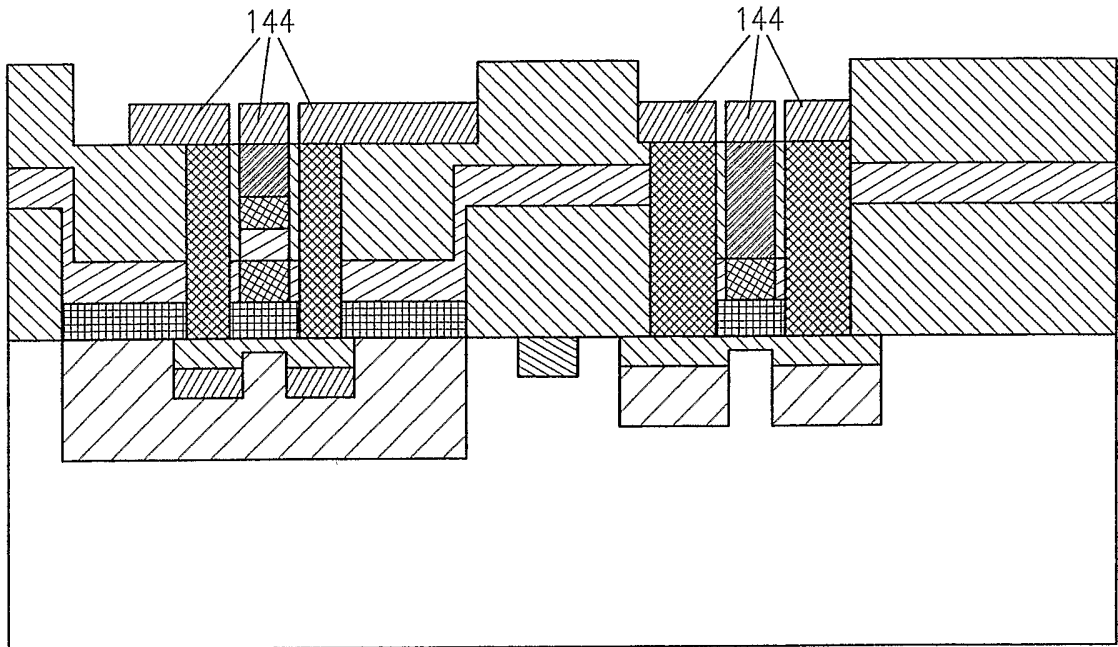


FIG. 1J

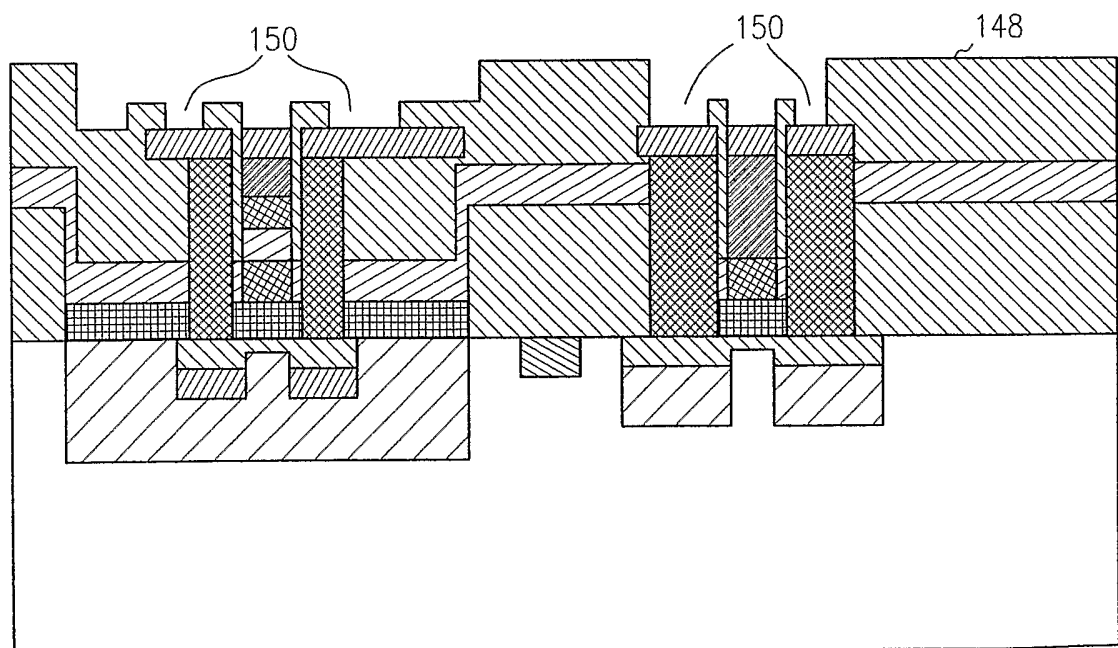


FIG. 1K

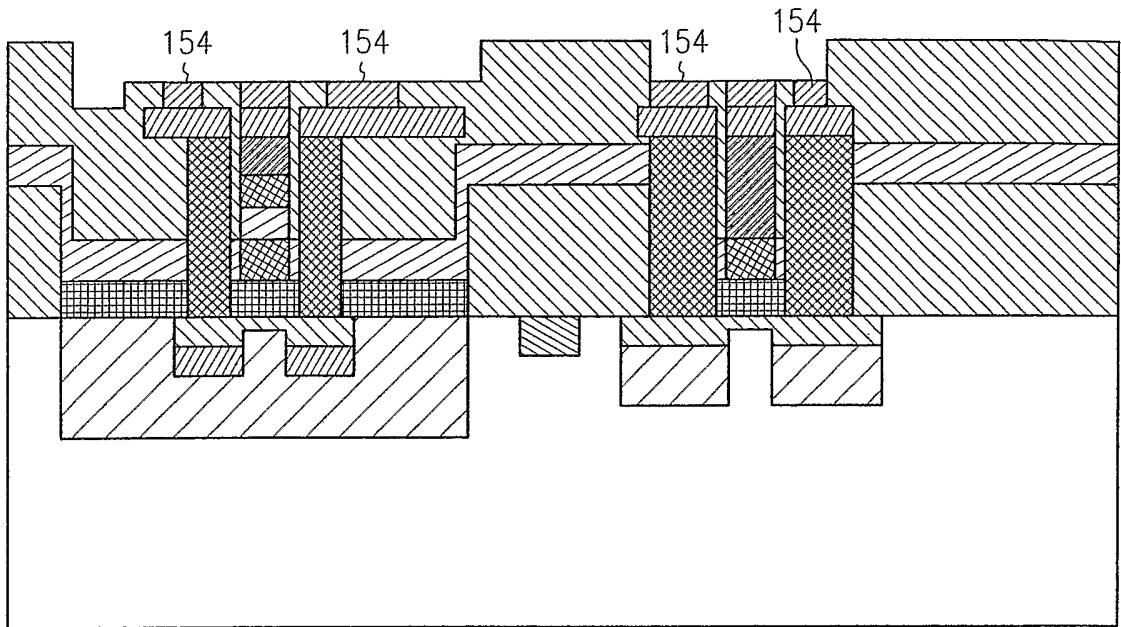


FIG. 1L

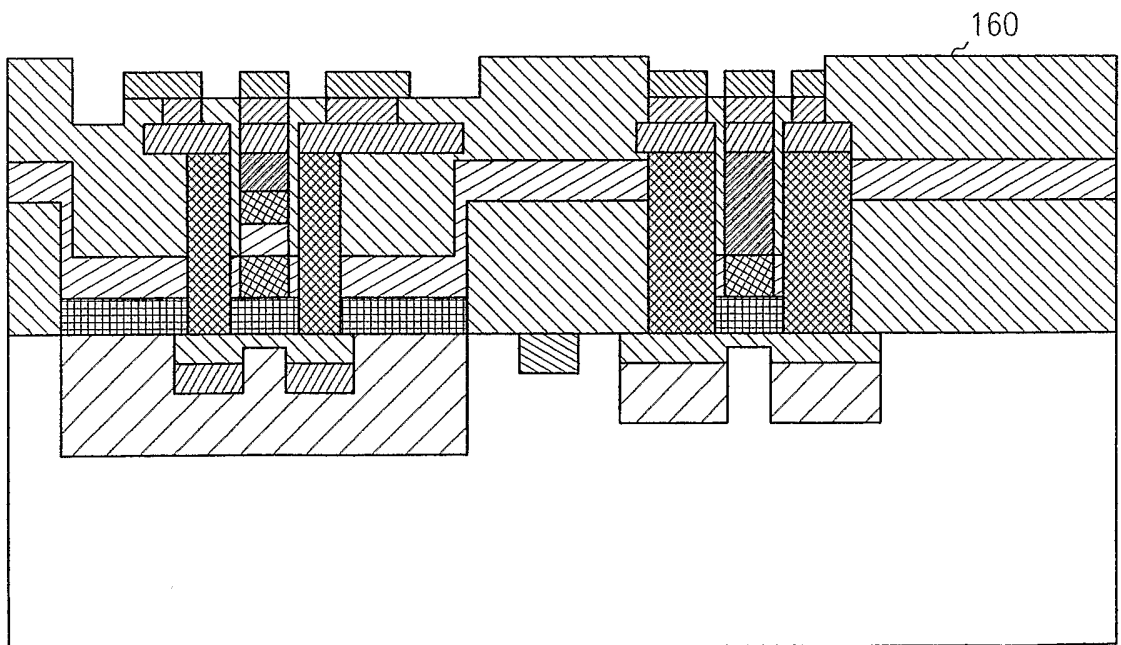


FIG. 1M

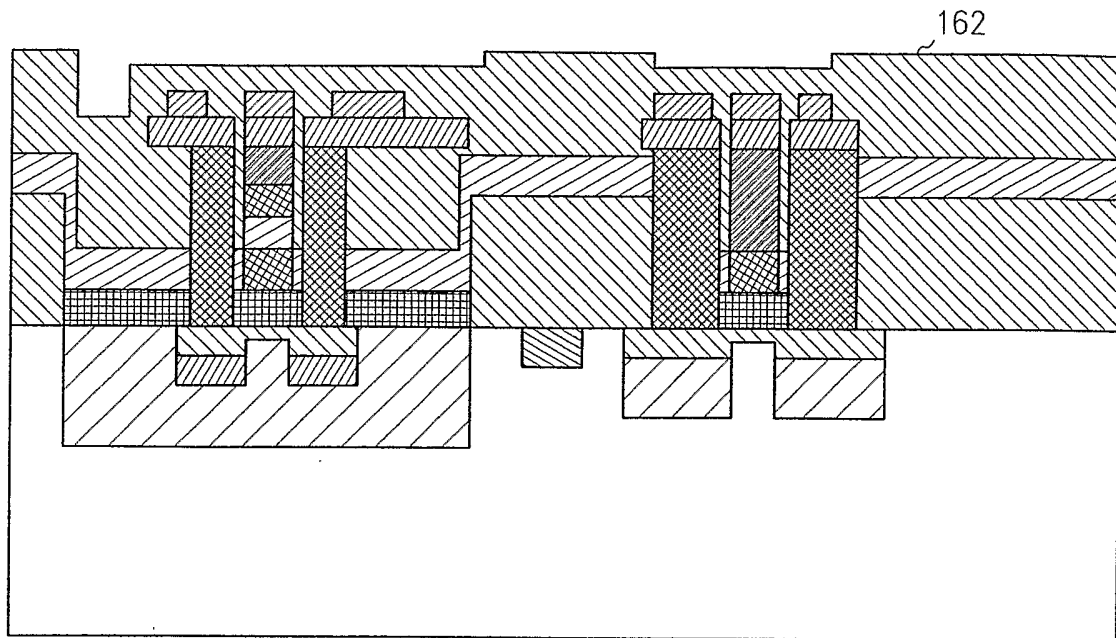


FIG. 1N

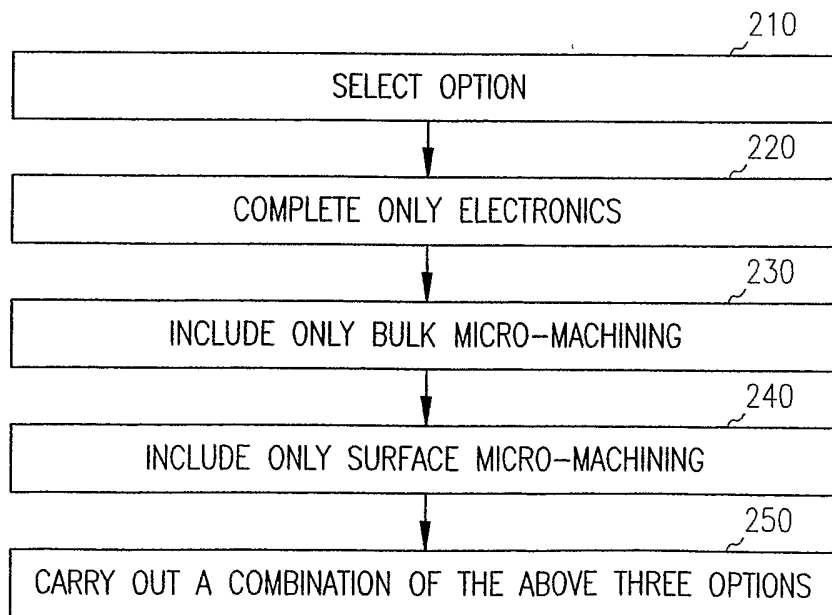


FIG. 2

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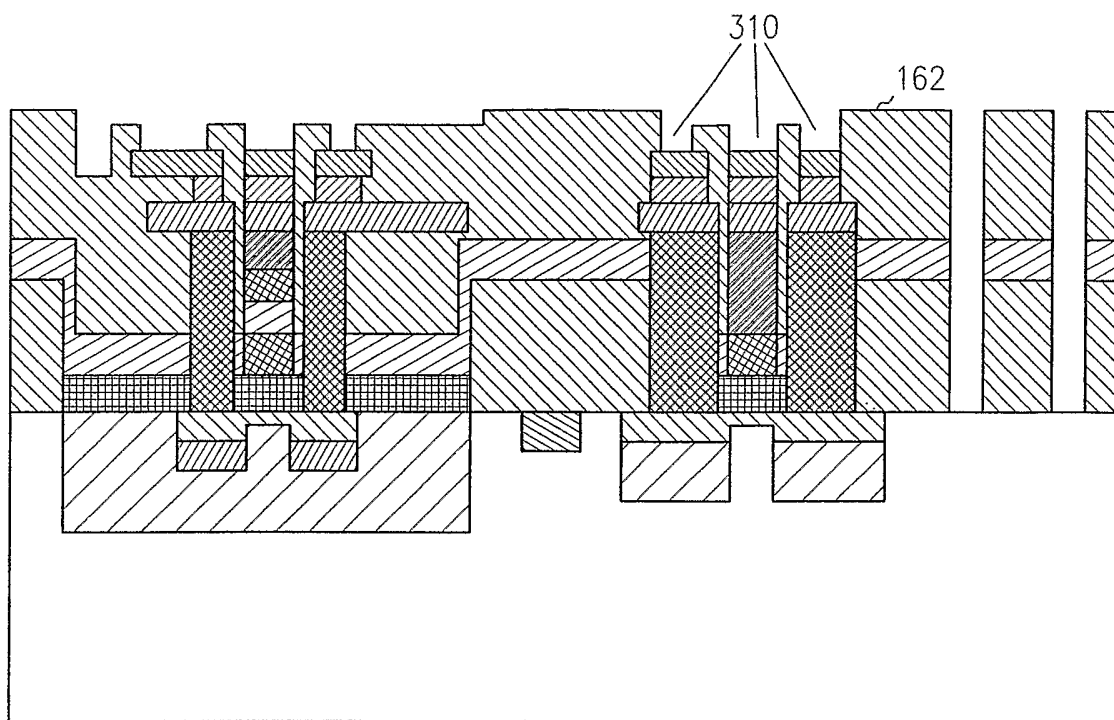


FIG. 3

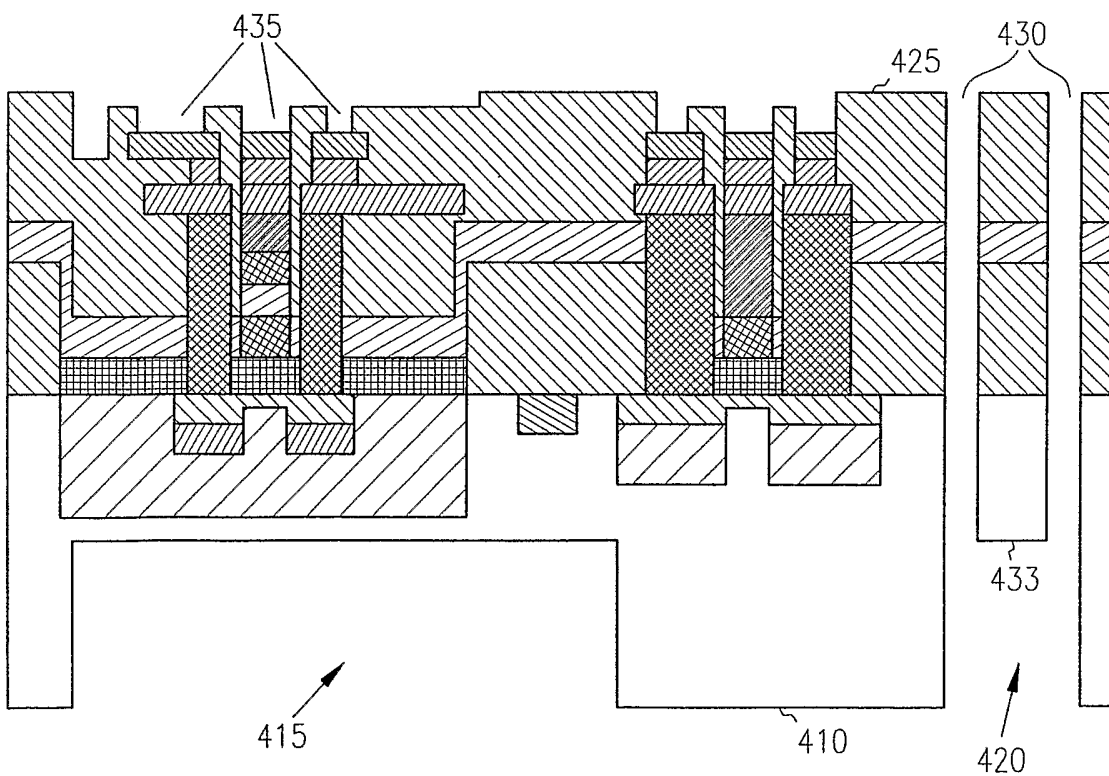


FIG. 4

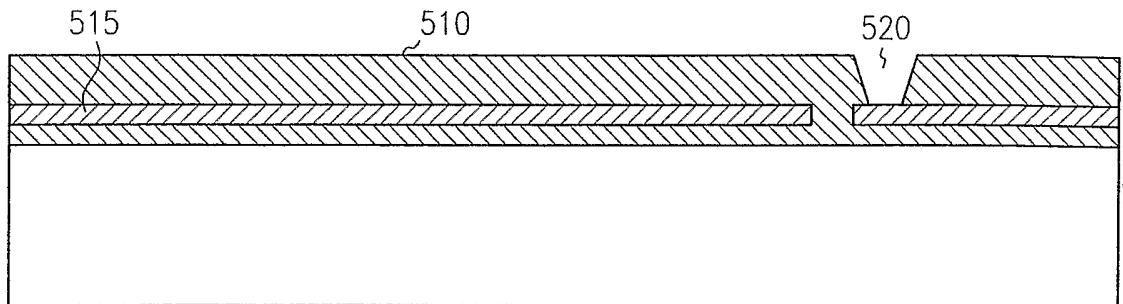


FIG. 5A

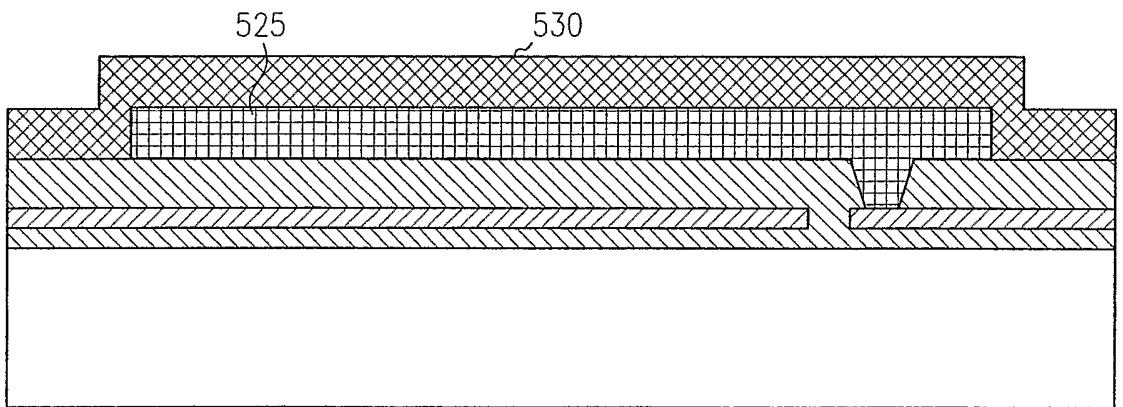


FIG. 5B

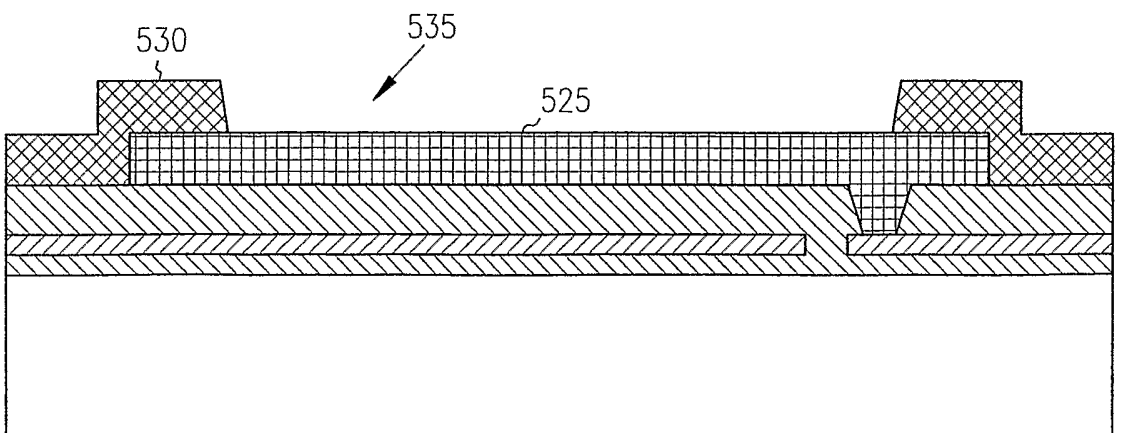


FIG. 5C

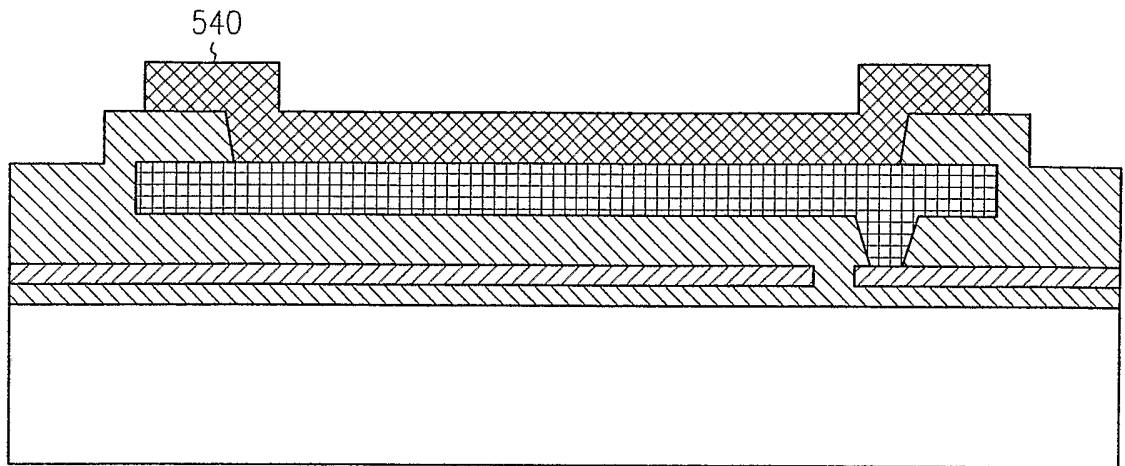


FIG. 5D

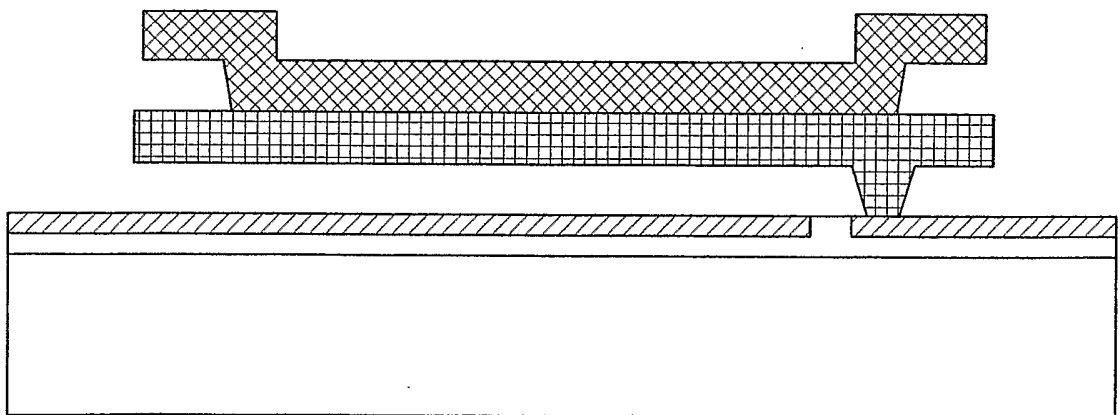


FIG. 5E