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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L	A2	(11) International Publication Number: WO 96/13055 (43) International Publication Date: 2 May 1996 (02.05.96)

(21) International Application Number: PCT/US95/12808

(22) International Filing Date: 13 October 1995 (13.10.95)

(30) Priority Data:
08/322,769 13 October 1994 (13.10.94) US

(71) Applicant: NATIONAL SEMICONDUCTOR CORPORATION [US/US]; 1090 Kifer Road, M/S 16-135, Sunnyvale, CA 94086-3737 (US).

(72) Inventors: CHEN, Andrea, Shu-hui; 140 W. Dana Street, Mountain View, CA 94041 (US). LO, Randy, Hsiao-Yu; 3779 Acapulco Drive, Campbell, CA 95008 (US). TAKIAR, Hem; 1544 Blackfoot Drive, Fremont, CA 94539 (US).

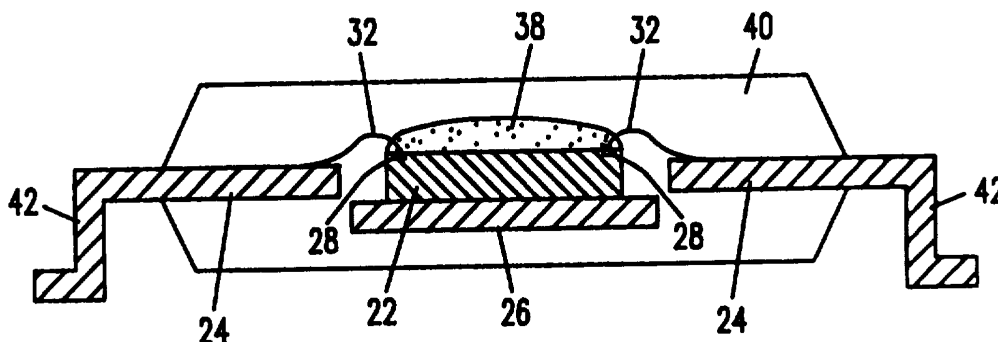
(74) Agent: CONSER, Eugene; National Semiconductor Corporation, 1090 Kifer Road, M/S 16-135, Sunnyvale, CA 94086-3737 (US).

(81) Designated States: DE, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: PLASTIC ENCAPSULATION OF IC DEVICE BY TWO LEVEL EPOXY ENCAPSULATION

(57) Abstract



A two level epoxy encapsulated integrated circuit device with improved high temperature characteristics is disclosed. The arrangement is particularly useful in packaging integrated circuits having aluminum die pads that are electrically connected to other components using gold bonding wires. A non-brominated epoxy topping is applied over the top surface of the die taking special care to encapsulate the intermetallic gold/aluminum bond regions. A second level encapsulation involving a transfer molding compound is then performed to form an exterior plastic package. The resulting package has reduced intermetallic growth and improved high temperature storage life and operational reliability.

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PLASTIC ENCAPSULATION OF IC DEVICE BY TWO LEVEL EPOXY ENCAPSULATION

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FIELD OF THE INVENTION

This invention relates generally to integrated circuit epoxy encapsulated plastic packaging. More particularly it relates to the use of a two level encapsulation arrangement wherein an inner glob-type topping formed from a non-brominated/non-antimony epoxy
10 material is provided to reduce gold-aluminum intermetallic growth in integrated circuit packages.

BACKGROUND OF THE INVENTION

One of the most popular techniques of packaging an integrated circuit is by
15 encapsulation (plastic packages). Typically, packaging an integrated circuit using plastic encapsulation involves mounting a die on a support member such as a die attach pad of a lead frame; electrically coupling the die to associated wiring traces such as leads in a lead frame; and then overmolding the die and portions of the wiring trace with a transfer molding compound to form a protective plastic package.

20 A common method used for electrically coupling an integrated circuit die to its associated wiring trace in semiconductor packaging is wire bonding. Bonding wires are typically made of gold (Au) wherein one end of the bonding wire has a gold ball bond that attaches to the contact region on the die. The contact region on the die typically has an aluminum (Al) bond pad for making electrical contact with the gold ball of the bonding wire.

The metallurgical bond between the gold ball bond and aluminum bond pad will be referred to as an intermetallic contact region from this point on. The second end of the bonding wire is then attached to an associated wiring trace, lead tip, bond pad or the like that is arranged to electrically connect the integrated circuit to another component.

It has been found that the intermetallic contact region is particularly susceptible to intermetallic growth which can result in bond degradation and possible electrical failure of the package. This seems to be a particular problem with gold-aluminum bonds and does not seem to occur as much in other intermetallic bonds such as gold-copper or gold-silver bonds. In packages that contain lead frames, intermetallic growth at the bonding wire-lead frame contact region is usually not a problem since lead frames are typically formed from copper that is spot plated with silver because gold better adheres to silver and produces a good quality bond.

One place where intermetallic growth frequently occurs is during high temperature storage testing. Elevated temperatures combined with the presence of certain substances such as bromine or antimony tend to accelerate intermetallic growth in the contact regions. Bromine and antimony have very good flame retardant characteristics and are frequently used in conventional epoxy transfer molding compounds in order to meet flame retardant guidelines.

A problem seen during the transfer molding process is the wire sweep or wire wash problem in which the bonding wires have a tendency to move, and possibly contact one another during the injection molding thereby shorting out the leads. The wire wash problem is particularly noticeable when fairly viscous transfer molding compounds are used during the encapsulation process. An effective measure taken to counter this occurrence is glob-topping that is applied to form a hardened protective barrier over the entire bonding wire region as schematically shown in Fig. 1a. The glob-topping used in this instance may be any suitable material including a non-brominated epoxy material that contains essentially no bromine, antimony or their compounds thereof. Such materials are commonly referred to as non-flame retardant epoxies. Such a method for glob topping is disclosed in Weiler et al. co-pending application Serial No. 08/225,900 entitled: Plastic Encapsulated Integrated Circuit Package

Having Protective Barrier for Its Bonding Wires and Method filed 04/11/94 which is incorporated by reference herein in its entirety. Fig. 1a is a diagrammatic cross sectional view of a die and lead frame assembly 2 that has had glob-topping 4 applied over the entire die 6 and bonding wires 8. The die 6 is attached to a die attach pad 12 that is supported by support arms (not shown) connected to the lead frame 10. Fig. 1b shows the glob-topped integrated circuit assembly 2 that has been overmolded with a transfer molding compound to form the exterior plastic package 16.

A similar type coating sometimes applied over the die and bonding wires is silicone, which is used for stress relief. Silicone has a relatively high thermal expansion as compared to the silicon die but imparts less stress on the die during thermal expansion since it is very soft and tends to act like a cushion. Silicone does not contain flame retardants but has the undesirable properties of having very limited structural and mechanical integrity unlike other materials, such as epoxy encapsulants, which can stand alone in chip-on-board applications. They also exhibit poor adhesion to molding compounds unlike epoxies. Silicone, because of its relatively high thermal expansion coefficient, tends to sweep the bonding wires into contact with each other during thermal excursions and silicone also possesses a much lower modulus than epoxies thus is very soft. Thermal excursions and transfer molding pose shear stress on the both the pad structure and ball bond which may result in bond pull or separated contacts. For the above and other reasons other materials, such as epoxies, are preferable to silicone for use in semiconductor packages.

A solution used in the past to reduce intermetallic growth was to eliminate gold-aluminum intermetallic bonds altogether in semiconductor packages. This yielded higher reliability but was much more costly because it required an expensive new Fab and assembly processes. Another approach was to try to control the concentration of intermetallic growth inducing substances at the source of the epoxy supply. The supplying manufacturer would try to reduce the concentration level of these substances by, for example, introducing ion scavengers and by "cleaning" up the overall manufacturing process. Voltage tests were then

performed on the packages since intermetallic growth resulted in increased resistance thus yielding lower voltage readings. If the tests proved unsatisfactory, subsequent iterations of the cleansing process and compound formulations may have had to have been evaluated. This can be a tediously time consuming and costly process to endure. A much more efficient and less 5 costly way to reduce Au-Al intermetallic growth at the semiconductor packaging stage is needed. Accordingly, it is a general objective of the present invention to provide a method and apparatus that reduces Au-Al intermetallic growth and allows for improved high temperature and operational reliability.

SUMMARY OF THE INVENTION

To achieve the foregoing and other objects and in accordance with the purpose of the present invention, an integrated circuit packaging arrangement for reducing gold-aluminum intermetallic growth is described. The arrangement provides improved high temperature storage life. In a method aspect of the invention, a die having a plurality of aluminum bond pads is mounted on a support member. The bond pads are then electrically coupled to associated wiring traces using a plurality of gold bonding wires. Each bonding wire is bonded at a first end to an associated aluminum bond pad and the second end is bonded to an associated wire trace. The connection between the gold bonding wire and the aluminum bond pad defines an intermetallic contact region. A non-brominated epoxy topping material that contains essentially no bromine, antimony or oxide compounds thereof, is then applied over the intermetallic contact regions of the die. The epoxy topping material is applied only on the surface of the die that contains the bond pads and does not overflow the die or encapsulate the entire bonding wires. The die, bonding wires and the non-brominated epoxy topping material are then overmolded with a flame retardant epoxy transfer molding compound to form an exterior plastic package.

The support member can be a variety of supporting structures on which a die can be mounted such as, a substrate, a circuit board, a die attach pad of a lead frame, etc. The wiring traces may take the form of conductive traces laid down on (or within) a substrate, traces on a circuit board, bond pads of an adjacent die, other circuit components within a package, leads of a lead frame etc. In one preferred embodiment, the epoxy topping is soft cured until it has gelled but not fully hardened before overmolding, although fully curing the epoxy topping yields acceptable results. The topping tends to "shield" the contacts from the brominated transfer molding compound used to form the exterior plastic package. In another embodiment, the transfer molding compound includes at least one of bromine, antimony, and compounds thereof.

In a separate apparatus aspect of the invention, a packaged integrated circuit that has reduced intermetallic growth that results in improved high temperature storage life is described. The packaged integrated circuit includes a die mounted on a support member, with the die containing a plurality of aluminum bond pads. A plurality of gold bonding wires are provided
5 with each bonding wire having a first end that is electrically connected to an associated bond pad thereby defining an intermetallic contact region and a second end electrically connected to an associated wiring trace. A non-brominated epoxy topping material is disposed over the top surface of the die and the intermetallic contact regions such that the epoxy encapsulant does not overflow the die or encapsulate the entire bonding wires. A transfer molding compound
10 overmolds the die, the bonding wires and the topping material to form an exterior plastic package.

Advantages of the present invention include improved high temperature storage life, unaltered external appearance and package performance from conventional plastic packages, and a package that continues to meet flame retardant requirements. Another advantage is that the
15 invention can also be used in any plastic package for a variety of products.

The two level encapsulated package of the present invention is superior to a device encapsulated with either just the transfer molding compound or the non-brominated epoxy encapsulant alone since, in combination, the molding compound provides the device with good flame retardant capabilities while the epoxy topping gives high temperature reliability.
20 Improved elevated temperature performance allows for greater reliability and high ambient temperature operation (>150 °C) which is particularly desirable in areas such as the automotive market and other high temperature environments.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention, together with further objects and advantages thereof, may best be understood by reference to the following description taken in conjunction with the
5 accompanying drawings in which:

Fig. 1a is a diagrammatic cross sectional illustration of a glob-top epoxy applied to a die, bonding wires, and lead frame assembly to prevent wire wash.

Fig. 1b is a diagrammatic cross sectional illustration the assembly in Fig. 1a that is
10 molded with a transfer molding compound to form an exterior package.

Figs. 2a-2d show diagrammatic cross sectional illustrations of the encapsulation process in the present invention. Fig. 2a shows a die attached to a die attach pad of a lead frame.

Fig. 2b is a diagrammatic cross sectional illustration of the assembly in Fig. 2a that has been wire bonded.

15 Fig. 2c is a diagrammatic cross sectional illustration of the assembly in Fig. 2b with a non-brominated epoxy applied over the top surface of the die and intermetallic contact regions.

Fig. 2d is a diagrammatic cross sectional illustration of the assembly in Fig. 2c encapsulated with a conventional transfer molding compound.

Fig. 3 is a top view of a die showing the aluminum die pads.

20 Fig. 4 is an illustration of a second embodiment where the non-brominated epoxy is applied only over the intermetallic contact regions.

Fig. 5 is a diagrammatic top view of the die in Fig. 4 wire bonded to a lead frame.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following figures referenced to are not drawn to scale but are used to illustrate the general structure of the device. Referring initially to Fig. 2d, a packaged integrated circuit having a two level epoxy encapsulation of its integrated circuit in accordance with a first
5 embodiment of the present invention will be described. The package includes a die 22 having aluminum bond pads 28, a lead frame 24, gold bonding wires 32 arranged to electrically connect the bond pads to the lead frame, a non-brominated epoxy topping 38 that covers the intermetallic regions on the top surface of a die 22, and a plastic encapsulation transfer molding compound 40. It should be noted that the non-brominated epoxy topping 38 is applied only to
10 the top surface of the die 22 and does not overflow over the edge yet is applied in such a manner that the gold-aluminum intermetallic contact regions defined where the gold bonding wires 32 attach to the aluminum bond pads are completely covered.

The means that supports the die is referred to herein as a support member and can be any suitable supporting structures. By way of example, substrates, circuit boards, heat
15 spreaders, and die attach pads. Likewise, the term wiring traces is used in this context to include any suitable structure that the bonding wires may be adhered to. By way of example, conductive traces or any contacts laid down on a substrate or circuit board, circuit components within a package, bond pads on adjacent dies, or leads on adjacent leads of a lead frame are all contemplated. Referring next to Fig. 2a, a method of packaging a die in accordance with a first
20 embodiment of the present invention will be described. In the embodiment shown, a die 22 is affixed to a die attached pad 26. The die attach pad 26 may be supported by support arms (shown as 56 in Fig. 5) attached to the lead frame 24. The lead frame may be a conventional lead frame constructed, by way of example, out of copper or a copper alloy because of their relatively good conductivity and cost effectiveness. The lead frame may be stamped out of a
25 sheet of conducting material or it can be etched in a process that is well known in the industry.

Referring next to Fig. 2b, the die 22 is electrically coupled to a lead frame 24 through the use of bonding wires 32. It should be noted that other conventional bonding methods such as tape automated bonding (TAB) are possible as well. Bonding wires 32 are made of a conductive material such a gold because of its excellent conductivity and ability to bond well.
5 To improve bonding to copper lead frames, silver may be spot plated on the lead tips. The first end of the bonding wire is metallurgically bonded with the bond pad 28 on the die 22. Suitable wire bonding techniques are well known to those skilled in the art and are widely used in the industry today. By way of example ball bonding and stitch bonding are appropriate.

Fig. 2c shows the assembly of Fig 2b after a non-brominated epoxy material 38 applied
10 over the top surface of the die 22. Particular care is taken to cover the intermetallic contact regions. The non-brominated epoxy is also referred to as a non-flame retardant, as opposed to brominated materials which are present in typical transfer molding compounds formulated to meet the UL 94V-0 package flame retardant requirement. Brominated materials in this context includes, in addition to bromine, antimony and compounds thereof such as derivative oxides
15 such as antimonytrioxide or antimonypentoxide, for example. By way of example, suitable non-brominated epoxy materials include non-flame retardant epoxies available from companies such as Dexter Electronic Materials of Industry, California and Sumitomo Bakelite Corp., which have been found to work well. In order to provide adequate protection, the topping material must at least cover the ball bond-bond pad intermetallic contact region but may also
20 cover the entire die surface as shown in the Fig. 2c.

Flame retardants or brominated materials tend to accelerate intermetallic growth, which is especially prominent at elevated temperatures, in bonds between gold and aluminum. By way of example, some brominated compounds have been seen to induce intermetallic growth after around 1000 hours of high temperature testing at about 150°C to 175°C. Brominates and
25 antimony play a catalytic role in inducing a degradative reaction that converts the gold rich intermetallic into $AuAl_5$ among other byproducts. Continued intermetallic growth weakens the bonds resulting in increased resistivity or potential electrical failure of the package. Moisture

induced degradation is also a significant issue. Degradation of the gold wire-aluminum bond pad intermetallic bond is accelerated by moisture at relatively low temperatures 150-160°C, leading to loss of bond strength after around 500 hours of testing. Non-brominated epoxy topping is also effective in protecting against moisture induced degradation, as well.

5 For applications where heat dissipation is an important issue, the encapsulant can include a highly thermally conductive filler which, combined with high Tg compound, can be very effective in conducting heat away from the die. The conductive filler utilized in conduction with a heat spreader, for example, can be used effectively with high performance, high heat generating IC's. Following the application of the topping, the device is then baked to "gel" or
10 "soft cure" the encapsulant. Of course the appropriate soft curing time will depend on the material used as the topping. When the aforementioned epoxies are used, baking in the range of 110°C to 150°C, and preferably around 125°C for about several minutes works well. To achieve optimum results, the epoxy should not be fully cured at this point. This permits the encapsulant to somewhat "harden" around the intermetallic contact areas prior to the transfer
15 molding process. Acceptable results are also obtained if the epoxy topping is fully cured prior to the transfer molding step.

Fig. 2d shows a cross sectional view of the unit in Fig. 2c that has been molded with a conventional flame retardant transfer molding compound 40 to form an exterior plastic package. This second level transfer molding technique is practiced widely and is well known to those
20 skilled in the art. The lead frame has been formed into legs 42 that attach and electrically connect the IC to the circuit board. The resulting package yields considerably improved high temperature storage life and looks and performs in a comparable or superior manner as a standard plastic IC package. The package of the present invention also maintains the UL 94V-0 flame retardant rating.

25 Fig. 3 shows a top view of a typical die illustrating the aluminum bond pads 48 along the four outer edges of the top surface of the die. In this quad configuration, it may not be necessary to apply the non-brominated epoxy over the entire surface of the die but in a manner

such that the bond pads are covered. Other arrangements of bond pads, for example, in a grid pattern throughout the entire surface of the die or portions thereof are possible thus the application of the non-brominated epoxy over the entire surface makes sense. Fig. 4 shows a second embodiment where the die is sufficiently large enough such that the non-brominated 5 epoxy can be applied in a "ring" over the intermetallic regions of the die 22, illustrated without bonding wires for simplicity, as described above. Further embodiments of the present invention that include spot application of individual bond pads when separation is large or irregularly spaced are possible, so long as the intermetallic regions are covered.

Fig. 5 shows a top view of the die in Fig. 4 wire bonded 32 to a conventional lead 10 frame 24 with non-brominated epoxy encapsulation material 50 applied over the intermetallic regions in accordance with the second embodiment. It should be pointed out that the epoxy does not cover a major portion of the bonding wires 32 or any of the lead frame. Rather it is only deposited within the periphery of the die 22. This embodiment is then processed exactly as embodiment one in that a second level encapsulation of a transfer molding compound is 15 performed to form the plastic package. There is no visible exterior difference from conventional packages and the alterations made by the invention are impervious to the customer. This two level encapsulation prove beneficial in several aspects over conventional plastic packages. Performance gain due to improved heat conduction of the encapsulant is possible. However, more importantly, the package provides improved high temperature storage life resulting in 20 longer operational lifetime of the device.

Although two embodiments of the present invention have been described in detail, it should be understood that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. While this invention has been described in terms of a Quad Flat Package, it should also be understood that the invention can 25 be applied to other types of packages as well. Particularly, the method described can be used in a multi-chip packages where multiple dies are coupled and bonded together within a single package. Similarly, the method is applicable to hybrid packages in which multiple components

such as resistors, capacitors, or other circuit elements are coupled and bonded to the die/dies within a single package. These multi-component packages may be electrically coupled in various ways including using gold bonding wires bonded to aluminum bond pads in which this invention would be pertinent. It should be noted that the same type of improvement may be
5 found in both ball bonding and stitch bonding procedures. Therefore the present examples are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims.

What is claimed is:

CLAIMS

1. A method of packaging an integrated circuit comprising the steps of:

(a) mounting a die on a support member wherein the die has a plurality of aluminum

5 bond pads;

(b) electrically coupling the bond pads to associated wiring traces by using a plurality of gold bonding wires wherein each bonding wire having a first end that is bonded to an associated aluminum bond pad and a second end bonded to a lead of an associated wire trace, the connection between the gold bonding ball of first end of the bonding wire to the

10 aluminum bond pad defines an intermetallic contact region; and

(c) applying a non-brominated epoxy topping material, that contains essentially no bromine, antimony or oxide compounds thereof, over the intermetallic contact regions of the die wherein the epoxy topping material is applied only on the surface of the die that contains the bond pads and does not overflow the die or encapsulate the entire bonding wires; and

15 (d) overmolding the die, the bonding wires and the non-brominated epoxy topping material with epoxy transfer molding compound to form an exterior plastic package.

2. A method as recited in claim 1 wherein the support member is a wherein the support member is a die attach pad.

3. A method as recited in claim 1 wherein the support member is a substrate or

20 circuit board.

4. A method as recited in claim 1 wherein the wiring trace is a lead frame.

5. A method as recited in claim 1 wherein the wiring trace includes bonding pads of adjacent dies or circuit components, and includes electrical connections there between the aforementioned.

6. A method as recited in claim 1 wherein the non-brominated epoxy topping material is non-flame retardant.

7. A method as recited in claim 1 wherein the non-brominated epoxy topping material is applied only over the intermetallic contact regions on the die.

8. A method as recited in claim 1 further comprising the step of soft curing the non-brominated epoxy topping material after it has been applied to the die and before the overmolding step.

9. A method as recited in claim 8 wherein the soft curing is accomplished by baking at a temperature in a range of approximately 110°C to 150°C until the topping is soft cured.

10. A method as recited in claim 1 further comprising the step of fully curing the non-brominated epoxy topping material after it has been applied to the die and before the overmolding step.

11. A method as recited in claim 1 wherein the transfer molding compound is a flame retardant material that includes at least one of bromine, antimony, or compounds thereof.

12. A packaged integrated circuit comprising:

(a) a die mounted on a support member, the die having a plurality of aluminum bond pads;

(b) a plurality of gold bonding wires each having a first end that is electrically connected to the bond pad thereby defining an intermetallic contact region;

(c) a plurality of wiring traces each electrically connected to a second end of an associated bonding wire;

5 (d) a non-brominated epoxy topping material, that contains essentially no bromine, antimony, or oxide compounds thereof, the topping material being disposed over the top surface of the die and the intermetallic contact regions such that the epoxy encapsulant does not overflow the die or encapsulate the entire bonding wires;

(e) a transfer molding compound that overmolds the die, the bonding wires and the
10 topping material to form an exterior plastic package.

13. A packaged integrated circuit as recited in claim 12 wherein the support member is a die attach pad.

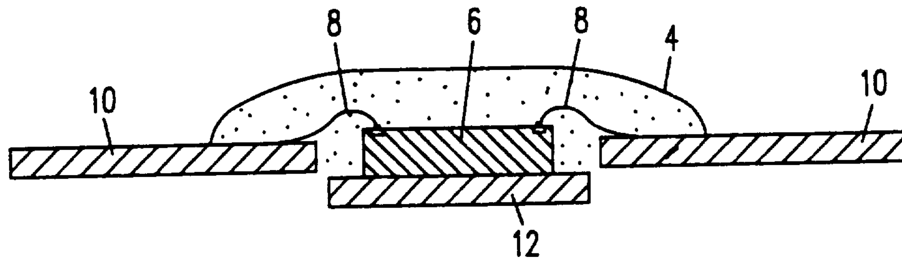
14. A packaged integrated circuit as recited in claim 12 wherein the support member includes a substrate or circuit board.

15 15. A packaged integrated circuit as recited in claim 12 wherein the wiring trace is a lead frame.

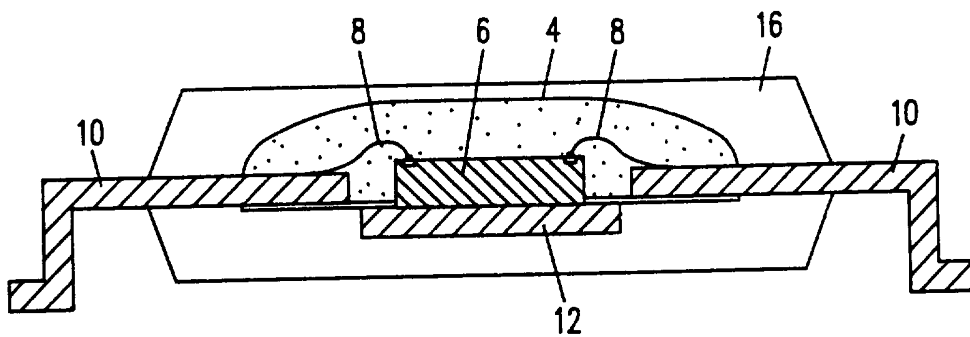
16. A packaged integrated circuit as recited in claim 12 wherein the wiring trace includes bonding pads of adjacent dies or circuit components, and includes electrical connections there between the aforementioned.

20 17. A packaged integrated circuit as recited in claim 12 wherein the topping material is a non-flame retardant epoxy material.

18. A packaged integrated circuit as recited in claim 12 wherein the transfer molding compound is a flame retardant material that includes at least one of bromine, antimony, and an antimony based compound.



PRIOR ART
FIG. 1a



PRIOR ART
FIG. 1b

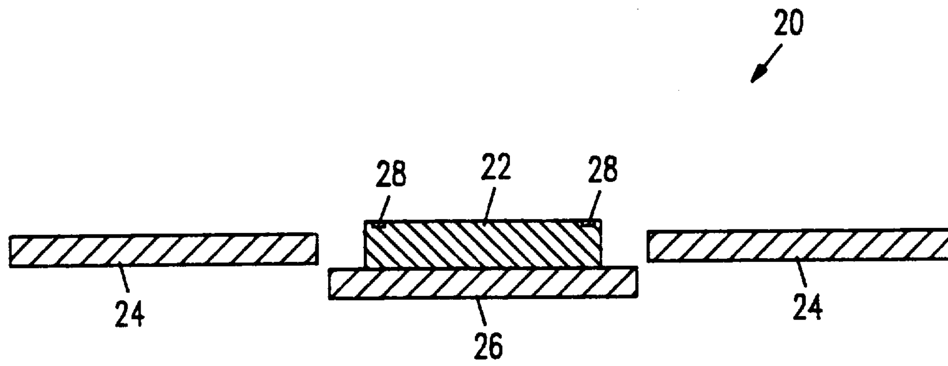


FIG. 2a

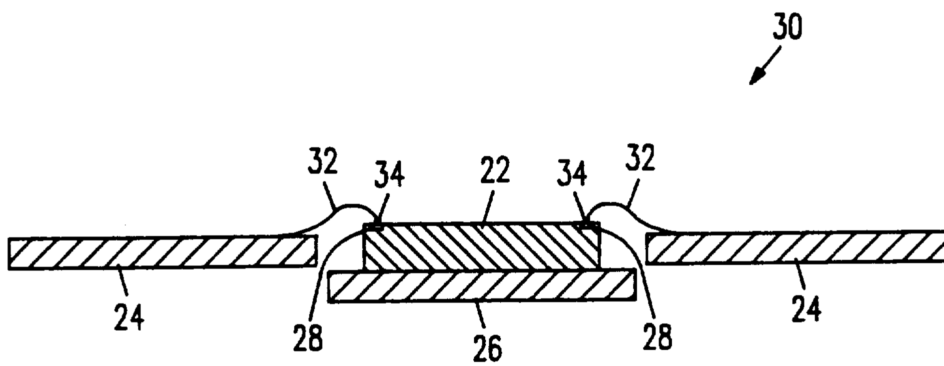


FIG. 2b

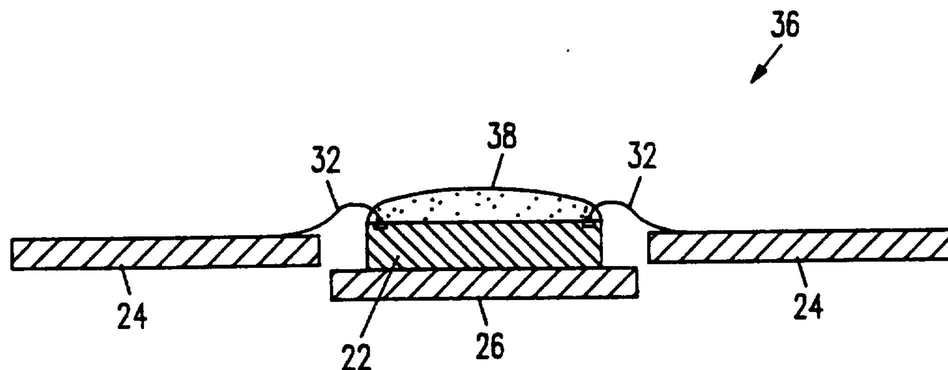


FIG. 2c

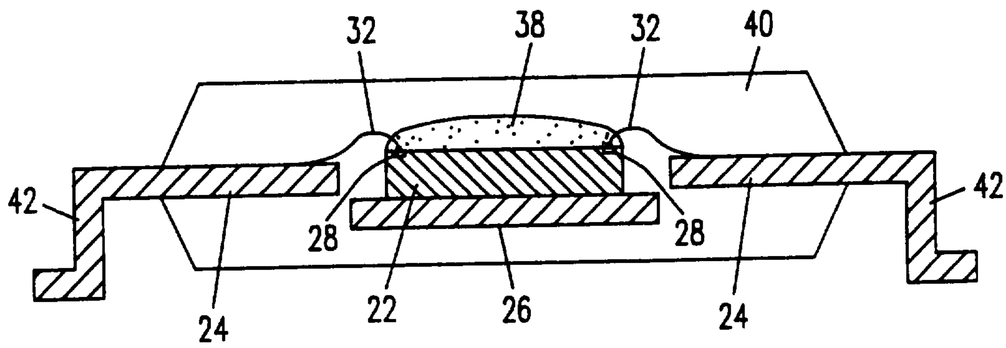


FIG. 2d

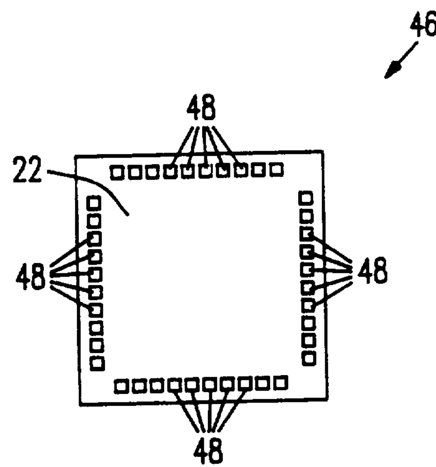


FIG. 3

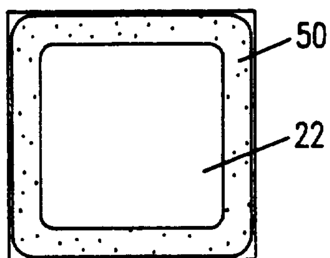


FIG. 4

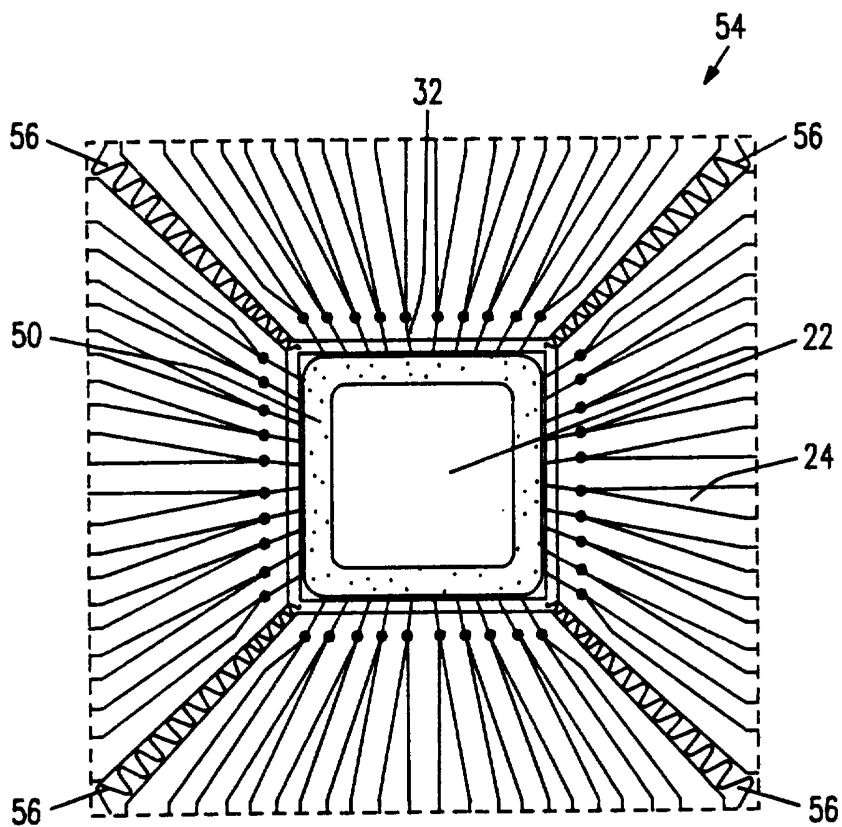


FIG. 5