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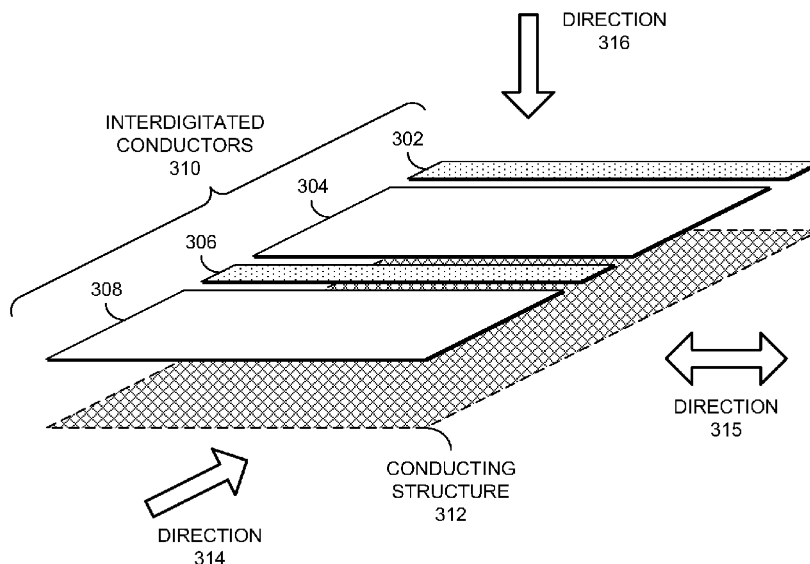

FIG. 3A

(57) Abstract: A structure for delivering power is described. In some embodiments, the structure can include conductors disposed on two or more layers. Specifically, the structure can include a first set of interdigitated conductors disposed on a first layer and oriented substantially along an expected direction of current flow. At least one conductor in the first set of interdigitated conductors may be maintained at a first voltage, and at least one conductor in the first set of interdigitated conductors may be maintained at a second voltage, wherein the second voltage is different from the first voltage. The structure may further include a conducting structure disposed on a second layer, wherein the second layer is different from the first layer, and wherein at least one conductor in the conducting structure is maintained at the first voltage.

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STRUCTURE FOR DELIVERING POWER

BACKGROUND

[0001] This disclosure generally relates to electronic circuits. A power distribution network can generally refer to circuitry and/or a structure that is used to deliver power, e.g., by delivering current between a first set of contacts and a second set of contacts. The inductance in the power distribution network is one factor to be considered in delivering reliable power with a specified target impedance. In an integrated circuit (IC) die, a contact in the first set of contacts may correspond to a terminal that is maintained at a given voltage (e.g., power supply voltage or ground), and a contact in the second set of contacts may correspond to a terminal of a circuit element. In an IC package, a contact in the first set of contacts may correspond to a power pin on the package, and a contact in the second set of contacts may correspond to a pad on the die. In a printed circuit board (PCB), a contact in the first set of contacts may correspond to a PCB contact for a power supply regulator, and a contact in the second set of contacts may correspond to a pin on an IC package.

[0002] If the total impedance of the power distribution network is high, then the power distribution network may introduce an unacceptably high amount of power noise.

[0003] FIG. 1 illustrates a structure for delivering power. Power delivery structure 102 can include conductor 104 whose left end is electrically connected to a power supply voltage and conductor 106 whose left end is electrically connected to ground. The current may flow along direction 108 (e.g., from left to right in conductor 104 and from right to left in conductor 106). The inductance (and therefore the impedance) of power delivery structure 102 may be unacceptably high, and may introduce an unacceptably high amount of power noise.

BRIEF DESCRIPTION OF THE FIGURES

[0004] FIG. 1 illustrates a structure for delivering power.

[0005] FIGs. 2A and 2B illustrate plots of the impedance of a power distribution network versus frequency in accordance with some embodiments described in this disclosure.

[0006] FIG. 3A illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0007] FIG. 3B illustrates a front view of the structure shown in FIG. 3A in accordance with some embodiments described in this disclosure.

[0008] FIG. 3C illustrates a top view of the structure shown in FIG. 3A in accordance with some embodiments described in this disclosure.

5 **[0009]** FIG. 3D illustrates how the existence of multiple current loops can decrease the overall impedance in accordance with some embodiments described in this disclosure.

[0010] FIG. 4A illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0011] FIG. 4B illustrates a structure for delivering power in accordance with some
10 embodiments described in this disclosure.

[0012] FIG. 5A illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0013] FIG. 5B illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

15 **[0014]** FIG. 6A illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0015] FIG. 6B illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0016] FIG. 7 illustrates a structure for delivering power that is part of a power
20 distribution network in an IC die in accordance with some embodiments described in this disclosure.

[0017] FIG. 8 illustrates a structure for delivering power that is part of a power distribution network in an IC package in accordance with some embodiments described in this disclosure.

25 **[0018]** FIG. 9 illustrates a structure for delivering power that is part of a power distribution network in a printed circuit board in accordance with some embodiments described in this disclosure.

DETAILED DESCRIPTION

30 **[0019]** Some embodiments presented in this disclosure feature a structure for delivering power that reduces power noise. Embodiments presented herein can generally be part of any power distribution network in which planes (or substantially planar conductors) are used for power delivery. Specifically, embodiments can be part of a power distribution network in an IC die, an IC package, or a printed circuit board.

[0020] FIGs. 2A and 2B illustrate plots of the impedance of a power distribution network versus frequency in accordance with some embodiments described in this disclosure.

[0021] In some embodiments described herein, the impedance of a power distribution network can be modeled using one or more resistances, inductances, and/or capacitances. In 5 these embodiments, as the frequency increases, the contribution of the one or more inductances to the total impedance increases, while the contribution of the one or more capacitances to the total impedance decreases.

[0022] If the total impedance of the power distribution network is high for a particular frequency range, then the power distribution network may introduce an unacceptably high 10 amount of power noise in that frequency range. For example, as shown in FIG. 2A, the impedance of the power distribution network at frequency F1 is Z1. If the value of Z1 is sufficiently high, then the power distribution network may introduce an unacceptably high amount power noise with frequencies around F1.

[0023] Some embodiments described herein decrease the impedance of the power 15 distribution network, thereby decreasing the amount of power noise introduced by the power distribution network. For example, as shown in FIG. 2B, reducing the inductance of the power distribution network decreases the overall impedance of the power distribution network. Specifically, the peak impedance value Z2 shown in FIG. 2B is lower than the peak impedance value Z1 shown in FIG. 2A.

20 **[0024]** Some embodiments described herein provide a structure for delivering power that has a low inductance, which causes the impedance of the power distribution network to be low, which, in turn, causes the amount of power noise introduced by the power distribution network to be low.

[0025] FIG. 3A illustrates a structure for delivering power in accordance with some 25 embodiments described in this disclosure.

[0026] Some embodiments can comprise conductors disposed on two or more layers. Specifically, in some embodiments, a structure for delivering power can comprise interdigitated conductors 310 disposed on a first layer, and conducting structure 312 disposed on a second layer.

30 **[0027]** As shown in FIG. 3A, interdigitated conductors 310 can include conductors 302-308. At least one conductor (e.g., conductors 302 and 306) in interdigitated conductors 310 can be maintained at voltage V1, and at least one conductor (e.g., conductors 304 and 308) in interdigitated conductors 310 can be maintained at voltage V2, wherein voltage V1 is different from voltage V2.

[0028] In general, voltages V1 and V2 can be any voltages that can be used to provide power to a circuit. Specifically, in some embodiments, voltage V1 can be ground and voltage V2 can be a power supply voltage. In other embodiments, voltage V1 can be a power supply voltage and voltage V2 can be ground.

[0029] Conducting structure 312 can include one or more conductors. In some embodiments, at least one conductor in conducting structure 312 can be maintained at voltage V1. In other embodiments, at least one conductor in conducting structure 312 can be maintained at voltage V2.

[0030] In some embodiments, the orientation of the conductors can be substantially along the expected direction of current flow. For example, in FIG. 3A, the current is expected to flow along direction 315, and therefore, interdigitated conductors 310 are substantially oriented along direction 315. In some embodiments, the shape of the conductors can be based on the pattern of current flow. For example, if the die dimension is smaller than package size, the conductors may have a tapered shape, e.g., a trapezoidal shape. The shapes and/or sizes of the conductors can be selected to ensure that the DC (direct current) resistance of the power delivery structure has a negligible impact on the operation of the circuit to which power is being delivered.

[0031] In some embodiments described herein, the inductance associated with a current loop depends on the cross-sectional area of the current loop, and the width of the current loop along a direction that is orthogonal to the plane of the current loop. If the distance between a power supply conductor and a ground conductor is large, it can cause the cross-sectional area of the current loop to be large, which, in turn, can cause the inductance of the power distribution network to be high. FIGs. 3B-3C described below explain why the inductance of the structure shown in FIG. 3A is low.

[0032] FIG. 3B illustrates a front view (i.e., a view along direction 314) of the structure shown in FIG. 3A in accordance with some embodiments described in this disclosure.

[0033] Current loop 318 is formed by a current that flows between a first set of contacts and a second set of contacts via conductor 308 and conducting structure 312. For example, the first set of contacts may be electrically connected to the left ends of conductor 308 and conducting structure 312, and the second set of contacts may be electrically connected to the right ends of conductor 308 and conducting structure 312. The inductance due to current loop 318 can depend on the cross-sectional area of current loop 318 and on the width (along direction 314) of current loop 318.

[0034] FIG. 3C illustrates a top view (i.e., a view along direction 316) of the structure shown in FIG. 3A in accordance with some embodiments described in this disclosure.

[0035] Current loop 320 is formed by a current that flows between the first set of contacts and the second set of contacts via conductors 308 and 306. Current loop 320 also contributes an inductance to the power distribution network.

[0036] The inductances contributed by current loops 318 and 320 are coupled in parallel. Therefore, the effective inductance of these two loops is less than the individual inductances of either of the two loops. This effective inductance can be less than the inductance of a corresponding structure that does not have interdigitated conductors, e.g., a structure similar to the one shown in FIG. 1. In some embodiments, the structure illustrated in FIG. 3A can be more effective in reducing the overall inductance of the power distribution network when the distance between the two layers (e.g., the distance between interdigitated conductors 310 and conducting structure 312) is large and/or the distance between adjacent conductors in the set of interdigitated conductors (e.g., interdigitated conductors 310) is small.

[0037] Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present disclosure. Some variations and modifications of the embodiment illustrated in FIG. 3A are described below.

[0038] FIG. 4A illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0039] The structure shown in FIG. 4A comprises conductors disposed on two or more layers. Specifically, the structure comprises interdigitated conductors 410 disposed on a first layer, and a monolithic conductor 412 disposed on a second layer.

[0040] In some embodiments, interdigitated conductors 410 can include conductors 402-408. At least one conductor (e.g., conductors 402 and 406) in interdigitated conductors 410 can be maintained at voltage V1, and at least one conductor (e.g., conductors 404 and 408) in interdigitated conductors 410 can be maintained at voltage V2, wherein voltage V1 is different from voltage V2. In general, voltages V1 and V2 can be any voltages that can be used to provide power to a circuit. Specifically, in some embodiments, voltage V1 can be ground and voltage V2 can be a power supply voltage. In other embodiments, voltage V1 can be a power supply voltage and voltage V2 can be ground.

[0041] In some embodiments, conductor 412 can be maintained at the same voltage as conductors 402 and 406, i.e., voltage V1. In some embodiments, conductor 412 can be maintained at voltage V2.

[0042] In some embodiments (as shown in FIG. 4A), conductors 402 and 406 can have smaller widths than conductors 404 and 408. In some embodiments, conductors 402 and 406 can have the same widths as conductors 404 and 408.

[0043] The inductance of the structure shown in FIG. 4A can be less than the inductance of a structure in which conductors 402 and 406 have the same widths as conductors 404 and 408. The inductance of a structure in which conductors 402 and 406 have the same widths as conductors 404 and 408 can be less than the inductance of a structure that does not include interdigitated conductors (e.g., a structure similar to the one shown in FIG. 1).

[0044] FIG. 4B illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0045] The structure shown in FIG. 4B is a variation of the structure shown in FIG. 4A. Both of these structures comprise conductors disposed on two or more layers. However, unlike FIG. 4A, interdigitated conductors 430 (which include conductors 422-428) are disposed on a lower layer, and monolithic conductor 432 is disposed on an upper layer.

[0046] FIG. 5A illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0047] The structure shown in FIG. 5A comprises conductors disposed on two or more layers. Specifically, the structure comprises interdigitated conductors 510 disposed on a first layer, and interdigitated conductors 530 disposed on a second layer.

[0048] Interdigitated conductors 510 can include conductors 502-508, and interdigitated conductors 530 can include conductors 522-528. At least one conductor (e.g., conductors 502 and 506) in interdigitated conductors 510 can be maintained at voltage V1, and at least one conductor (e.g., conductors 504 and 508) in interdigitated conductors 510 can be maintained at voltage V2. Further, at least one conductor (e.g., conductors 524 and 528) in interdigitated conductors 530 can be maintained at voltage V1, and at least one conductor (e.g., conductors 522 and 526) in interdigitated conductors 510 can be maintained at voltage V2.

[0049] Voltages V1 and V2 are different from one another, and can generally be any set of voltages that can be used to provide power to a circuit. Specifically, in some embodiments, voltage V1 can be ground and voltage V2 can be a power supply voltage. In other embodiments, voltage V1 can be a power supply voltage and voltage V2 can be ground.

[0050] In FIG. 5A, the voltage of a conductor in a layer (e.g., conductor 506 in the upper layer) is different from the voltages of adjacent conductors in the same layer (e.g., conductors 504 and 508 in the upper layer), and is also different from the voltage of the corresponding conductor in the other layer (e.g., conductor 526 in the lower layer).

[0051] In FIG. 5A, conductors 502-508 and 522-528 are shown as having substantially the same widths. However, in other embodiments, the conductors may have different widths.

[0052] FIG. 5B illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0053] The structure shown in FIG. 5B is a variation of the structure shown in FIG. 5A. Both of these structures comprise interdigitated conductors disposed on two or more layers. Specifically, interdigitated conductors 550 (which include conductors 542-548) are disposed on an upper layer, and interdigitated conductors 560 (which include conductors 552-558) are disposed on a lower layer. Furthermore, as in FIG. 5A, the voltage of a conductor in a layer (e.g., conductor 546) is different from the voltages of adjacent conductors in the same layer (e.g., conductors 544 and 548). However, unlike FIG. 5A, the voltage of a conductor in a layer (e.g., conductor 546 in the upper layer) is the same as the voltage of the corresponding conductor in the other layer (e.g., conductor 556 in the lower layer). Although the conductors in FIG. 5B are shown as having substantially the same widths, the conductors can have different widths in other embodiments.

[0054] FIG. 6A illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

[0055] The structure shown in FIG. 6A comprises conductors disposed on three or more layers. Specifically, the structure comprises interdigitated conductors 610 (which include conductors 602-608) disposed on a first layer, monolithic conductor 612 disposed on a second layer, and interdigitated conductors 630 (which include conductors 622-628) disposed on a third layer.

[0056] At least one conductor (e.g., conductors 602 and 606) in interdigitated conductors 610 can be maintained at voltage V1, and at least one conductor (e.g., conductors 604 and 608) in interdigitated conductors 610 can be maintained at voltage V2. Similarly, at least one conductor (e.g., conductors 622 and 626) in interdigitated conductors 630 can be maintained at voltage V1, and at least one conductor (e.g., conductors 624 and 628) in interdigitated conductors 630 can be maintained at voltage V2. In some embodiments, conductor 612 can be maintained at voltage V1, and in other embodiments, conductor 612 can be maintained at voltage V2.

[0057] Voltages V1 and V2 are different from one another, and can generally be any set of voltages that can be used to provide power to a circuit. Specifically, in some embodiments, voltage V1 can be ground and voltage V2 can be a power supply voltage. In other embodiments, voltage V1 can be a power supply voltage and voltage V2 can be ground.

[0058] In FIG. 6A, conductors 602, 606, 622, and 626 are shown as having smaller widths than conductors 604, 608, 624, and 628. In other embodiments, the conductors may have

the same widths. The inductance of the structure shown in FIG. 6A may be less than the inductance of a structure in which conductors have the same widths.

[0059] FIG. 6B illustrates a structure for delivering power in accordance with some embodiments described in this disclosure.

5 **[0060]** The structure shown in FIG. 6B is a variation of the structure shown in FIG. 6A. Both of these structures comprise conductors disposed on three or more layers. Specifically, the structure shown in FIG. 6B comprises monolithic conductor 640 disposed on a first layer, a set of interdigitated conductors that include conductors 642-648 disposed on a second layer, and monolithic conductor 650 disposed on a third layer.

10 **[0061]** At least one conductor (e.g., conductors 642 and 646) in the set of interdigitated conductors can be maintained at voltage V1, and at least one conductor (e.g., conductors 644 and 648) in the set of interdigitated conductors can be maintained at voltage V2. Monolithic conductors 640 and 650 can be maintained at voltage V1 or V2.

[0062] FIG. 7 illustrates a structure for delivering power that is part of a power
15 distribution network in an IC die in accordance with some embodiments described in this disclosure.

[0063] IC die 700 can include a power distribution network that supplies power to various circuit elements in the IC die. The power distribution network can include conductors disposed on two or more metal layers, including a set of interdigitated conductors 702-708
20 disposed on one of the metal layers. The conductors can be oriented substantially along an expected direction of current flow, and may or may not have the same dimensions and/or shapes. Adjacent conductors in the set of interdigitated conductors 702-708 can have different voltages. For example, conductors 702 and 706 may be maintained at voltage V1 and conductors 704 and 708 may be maintained at voltage V2. Voltages V1 and V2 can generally be any pair of voltages
25 that are capable of being used to deliver power to a circuit. The power distribution network may also include other conducting structures (not shown) that are disposed on other metal layers of the IC die.

[0064] FIG. 8 illustrates a structure for delivering power that is part of a power distribution network in an IC package in accordance with some embodiments described in this
30 disclosure.

[0065] IC package 800 can include a power distribution network that supplies power to die 802. The power distribution network can include conductors disposed on two or more layers, including a set of interdigitated conductors 804-818 disposed on a first layer. Conductors 804-810 are trapezoidal, and are oriented substantially along the expected direction of current flow.
35 Conductors 812-818 are rectangular and are oriented substantially along the expected direction of

current flow. Conductors 812-818 do not extend to an edge of IC package 800, and have different lengths. Adjacent conductors in the set of interdigitated conductors 804-818 can have different voltages. For example, conductors 804 and 808 may be maintained at voltage V1 and conductors 806 and 810 may be maintained at voltage V2. Similarly, conductors 814 and 818
5 may be maintained at voltage V3 (which may or may not be the same as voltage V1) and conductors 812 and 816 may be maintained at voltage V4 (which may or may not be the same as voltage V2). The power distribution network may also include other conducting structures (not shown) that are disposed on other layers.

[0066] FIG. 9 illustrates a structure for delivering power that is part of a power
10 distribution network in a printed circuit board in accordance with some embodiments described in this disclosure.

[0067] Printed circuit board 900 can include a power distribution network that supplies power from set of contacts 904 to IC package 902. The power distribution network can include conductors disposed on two or more layers, including a set of interdigitated conductors 906-912
15 disposed on a first layer. As shown in FIG. 9, conductors 906-912 can be rectangular in shape, and can be oriented substantially along the expected direction of current flow, namely, between set of contacts 904 and IC package 902. Further, adjacent conductors in the set of interdigitated conductors 906-912 can have different voltages. For example, conductors 906 and 910 may be maintained at voltage V1 and conductors 908 and 912 may be maintained at voltage V2. The
20 power distribution network may also include other conducting structures (not shown) that are disposed on other layers.

[0068] In some embodiments, IC die 700, and IC packages 800 and 902 can include memory devices. Examples of memory devices include, but are not limited to, static random access memory devices, dynamic random access memory (DRAM) devices such as synchronous
25 double data rate (DDR) DRAM, and non-volatile memory devices such as Flash memory devices.

[0069] Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present
30 disclosure. Thus, the scope of the present disclosure is not limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

What Is Claimed Is:

1. A structure for delivering power, comprising:

a first set of interdigitated conductors disposed on a first layer and oriented substantially along an expected direction of current flow, wherein at least one conductor in the first set of interdigitated conductors is maintained at a first voltage, and wherein at least one conductor in the first set of interdigitated conductors is maintained at a second voltage, wherein the second voltage is different from the first voltage; and

a conducting structure disposed on a second layer, wherein the second layer is different from the first layer, and wherein at least one conductor in the conducting structure is maintained at the first voltage.

2. The structure of claim 1, wherein the first voltage is ground and the second voltage is a power supply voltage.

3. The structure of claim 1, wherein the first voltage is a power supply voltage and the second voltage is ground.

4. The structure of claim 1, wherein adjacent conductors in the first set of interdigitated conductors have different voltages.

5. The structure of claim 1, wherein at least one conductor in the first set of interdigitated conductors has a trapezoidal shape.

6. The structure of claim 1, wherein the conducting structure includes only one conductor.

7. The structure of claim 1, wherein the conducting structure includes a second set of interdigitated conductors that are oriented substantially along the expected direction of current flow, wherein at least one conductor in the second set of interdigitated conductors is maintained at the first voltage, and wherein at least one conductor in the second set of interdigitated conductors is maintained at the second voltage.

8. The structure of claim 7, wherein a conductor in the first set of interdigitated conductors is maintained at a different voltage than a corresponding conductor in the second set of interdigitated conductors.

5 9. The structure of claim 7, wherein a conductor in the first set of interdigitated conductors is maintained at the same voltage as a corresponding conductor in the second set of interdigitated conductors.

10. The structure of claim 1, wherein the structure is part of a power distribution
10 network in an integrated circuit die.

11. The structure of claim 1, wherein the structure is part of a power distribution network in an integrated circuit package.

15 12. The structure of claim 1, wherein the structure is part of a power distribution network in a printed circuit board.

13. An integrated circuit (IC) package, comprising:
a set of pins;
20 a die; and
a structure, comprising:
a first set of interdigitated conductors disposed on a first layer and oriented substantially along a direction of current flow between the set of pins and the die, wherein at least one conductor in the first set of interdigitated conductors is maintained at a first
25 voltage, and wherein at least one conductor in the first set of interdigitated conductors is maintained at a second voltage, wherein the second voltage is different from the first voltage; and
a conducting structure disposed on a second layer, wherein the second layer is different from the first layer, and wherein at least one conductor in the conducting
30 structure is maintained at the first voltage.

14. The IC package of claim 13, wherein the first voltage is ground and the second voltage is a power supply voltage.

15. The IC package of claim 13, wherein the first voltage is a power supply voltage and the second voltage is ground.

16. The IC package of claim 13, wherein the conducting structure includes only one conductor.

17. The IC package of claim 13, wherein the conducting structure includes a second set of interdigitated conductors that are oriented substantially along the direction of current flow between the set of pins and the die, wherein at least one conductor in the second set of interdigitated conductors is maintained at the first voltage, and wherein at least one conductor in the second set of interdigitated conductors is maintained at the second voltage.

18. A printed circuit board, comprising:

a set of contacts;

an integrated circuit (IC) package; and

a structure, comprising:

a first set of interdigitated conductors disposed on a first layer and oriented substantially along a direction of current flow between the set of contacts and the IC package, wherein at least one conductor in the first set of interdigitated conductors is maintained at a first voltage, and wherein at least one conductor in the first set of interdigitated conductors is maintained at a second voltage, wherein the second voltage is different from the first voltage; and

a conducting structure disposed on a second layer, wherein the second layer is different from the first layer, and wherein at least one conductor in the conducting structure is maintained at the first voltage.

19. The printed circuit board of claim 18, wherein the first voltage is ground and the second voltage is a power supply voltage.

20. The printed circuit board of claim 18, wherein the first voltage is a power supply voltage and the second voltage is ground.

21. The printed circuit board of claim 18, wherein the conducting structure includes only one conductor.

22. The printed circuit board of claim 18, wherein the conducting structure includes a second set of interdigitated conductors that are oriented substantially along the direction of current flow between the set of contacts and the IC package, wherein at least one conductor in the second set of interdigitated conductors is maintained at the first voltage, and wherein at least one
5 conductor in the second set of interdigitated conductors is maintained at the second voltage.

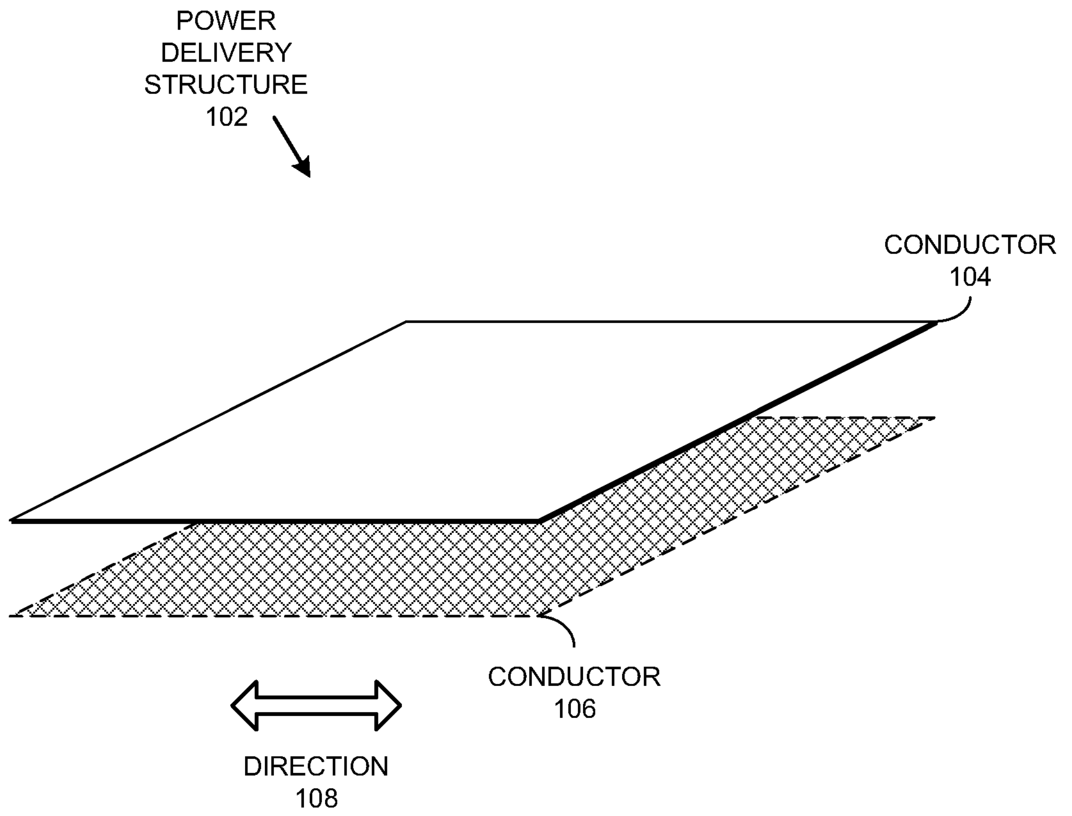

FIG. 1
(PRIOR ART)

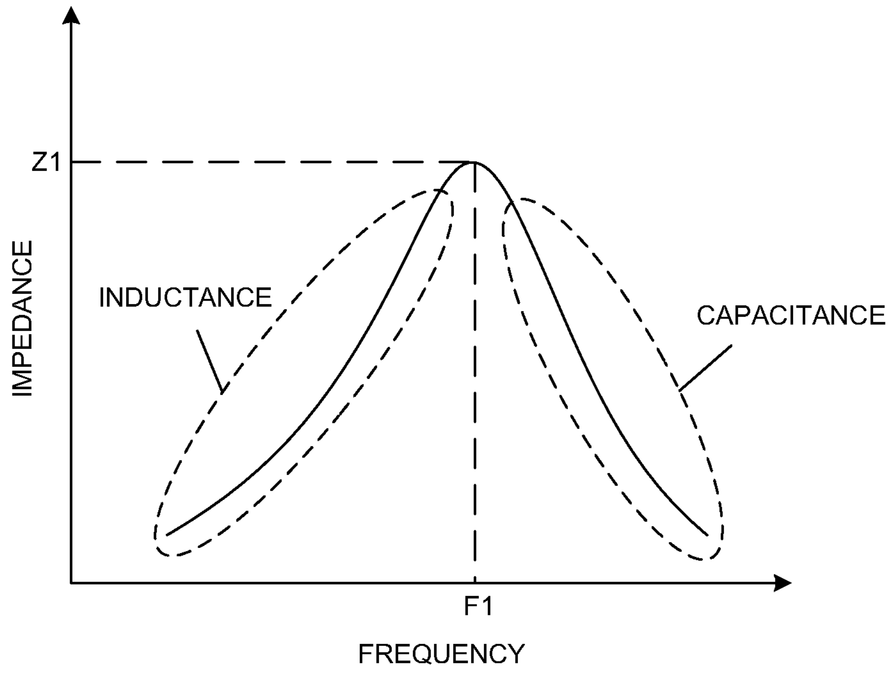

FIG. 2A

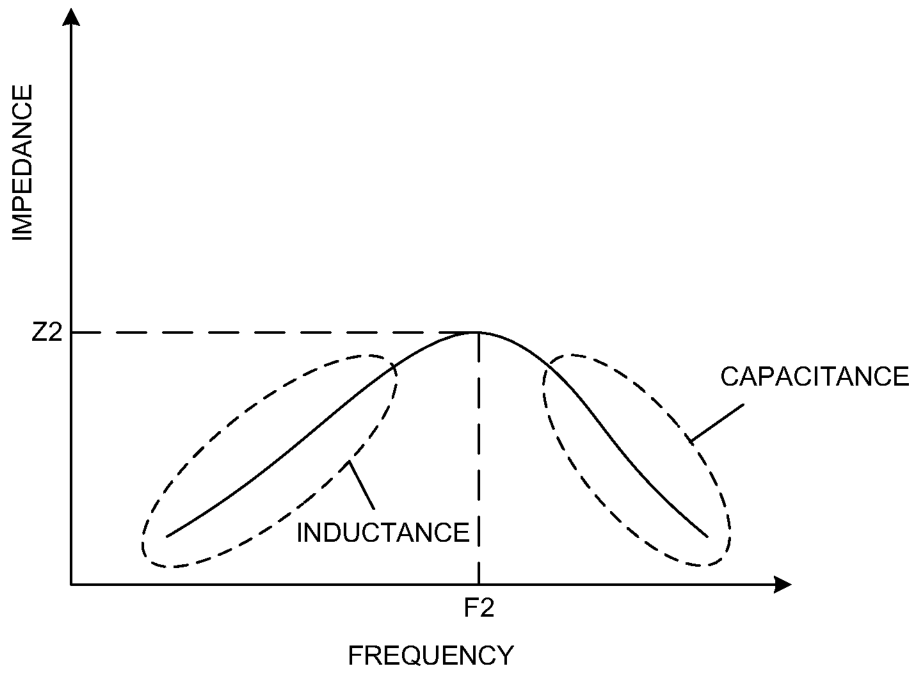

FIG. 2B

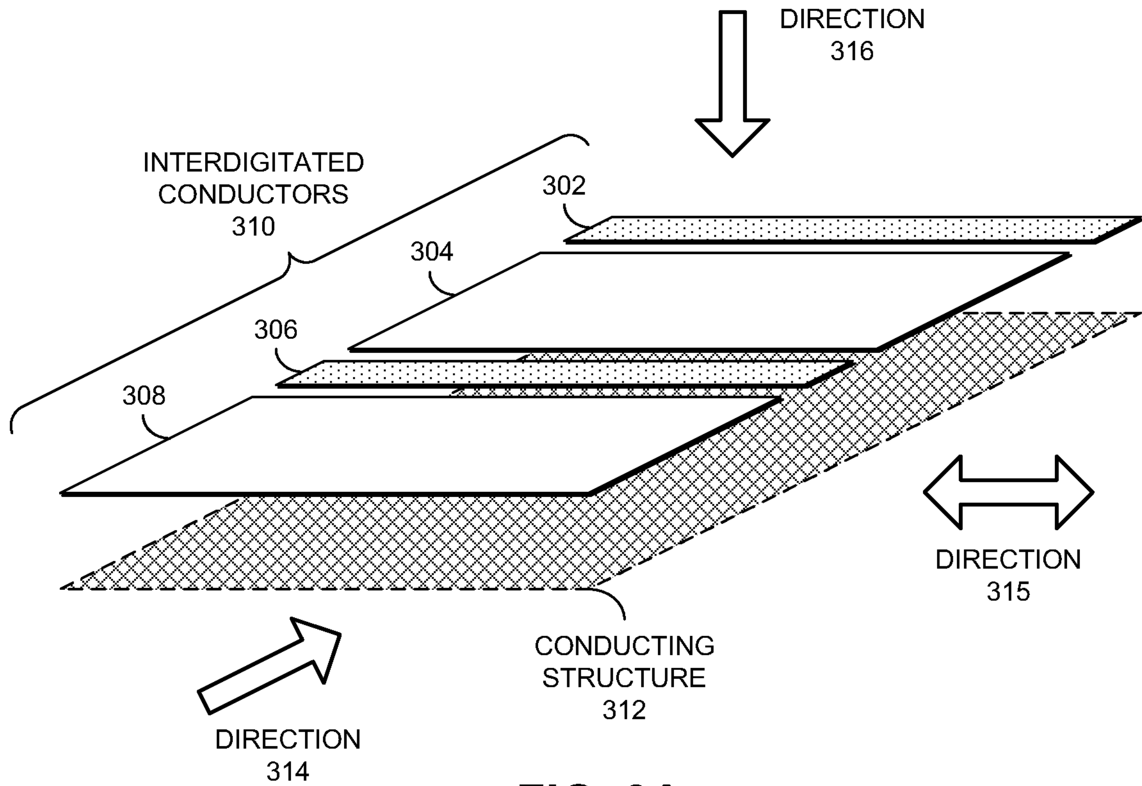

FIG. 3A

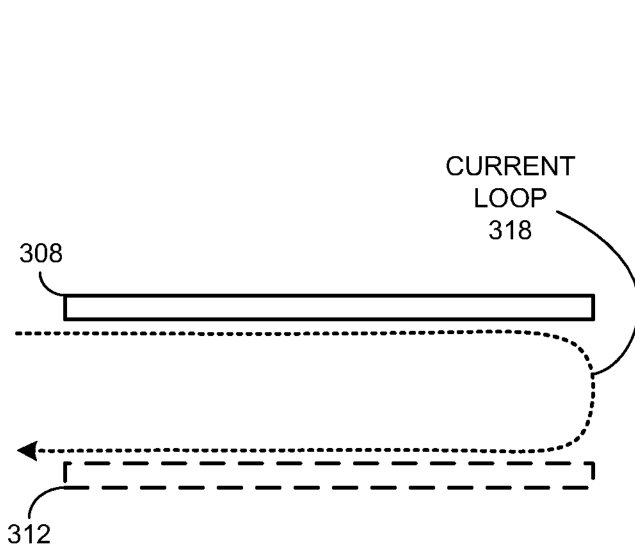

FIG. 3B

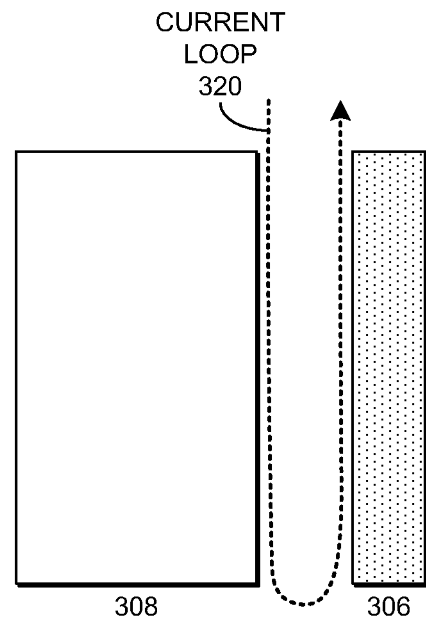

FIG. 3C

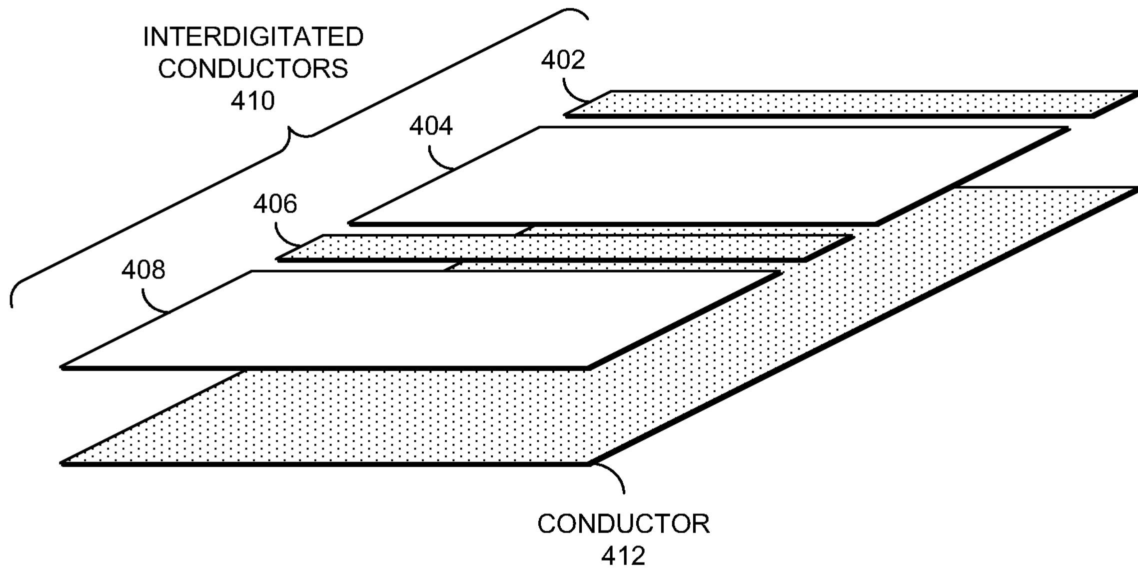

FIG. 4A

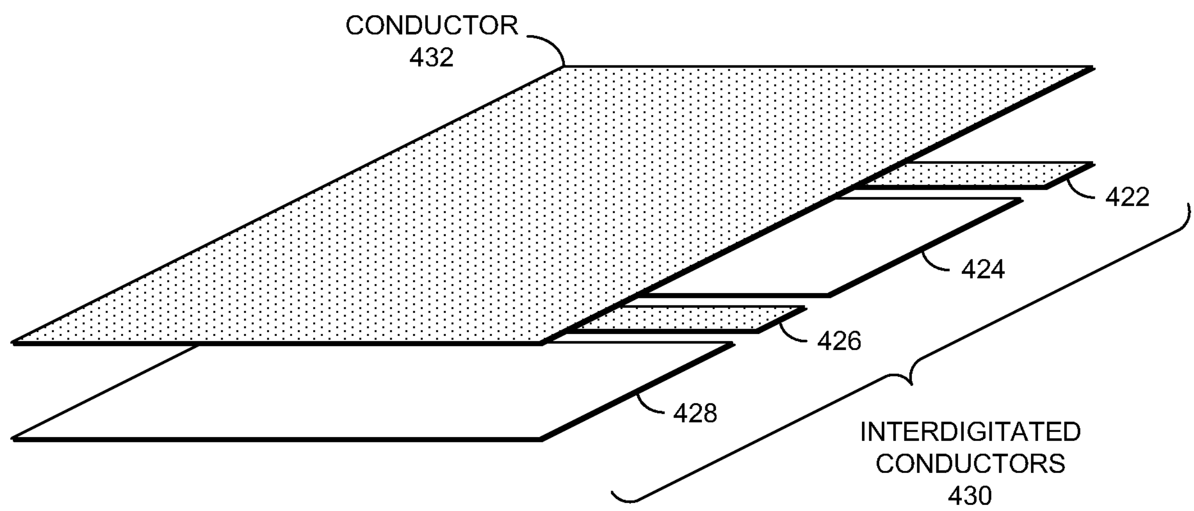

FIG. 4B

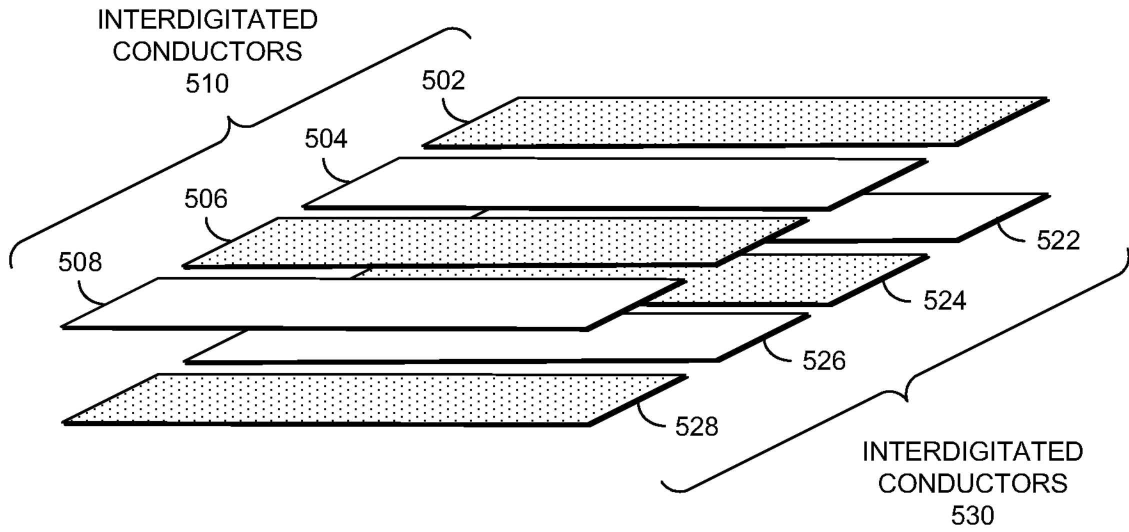

FIG. 5A

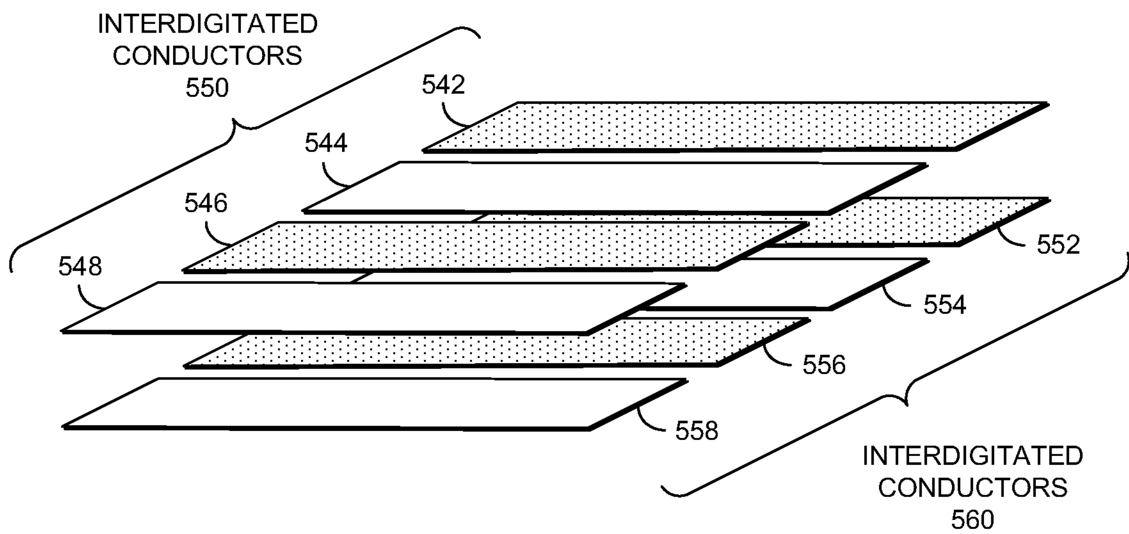

FIG. 5B

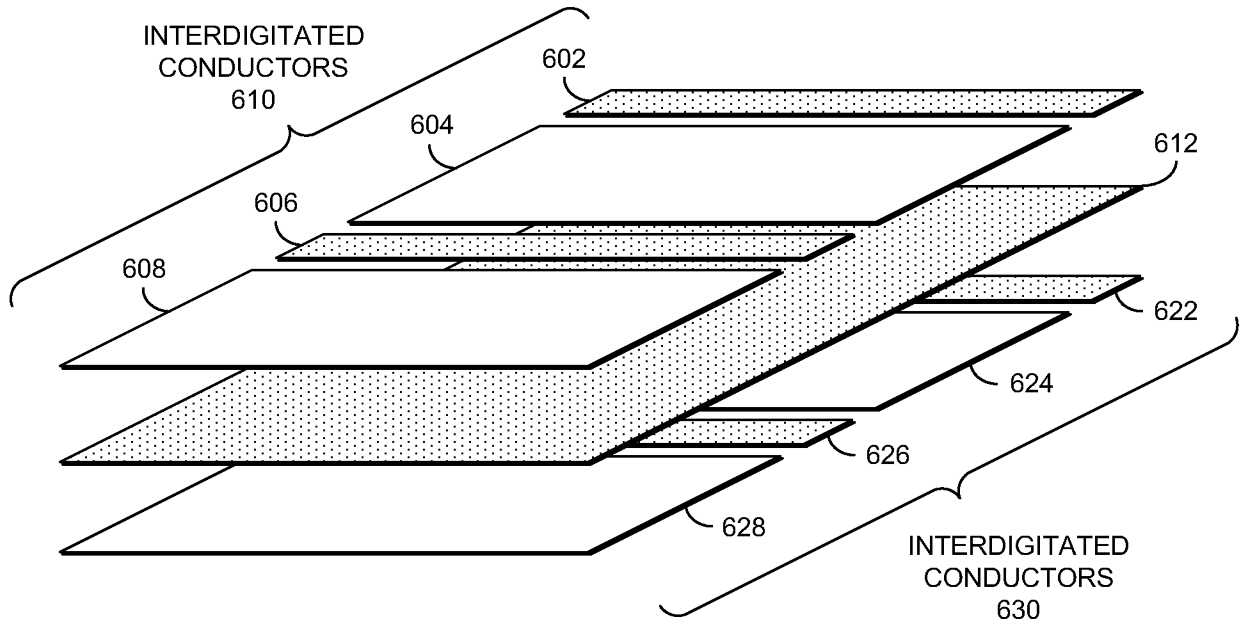

FIG. 6A

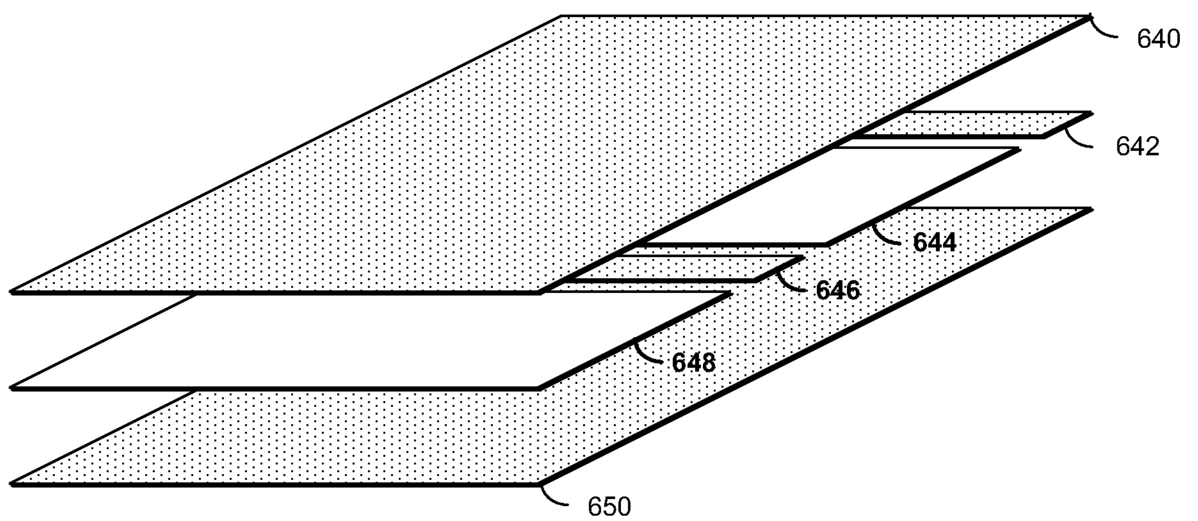

FIG. 6B

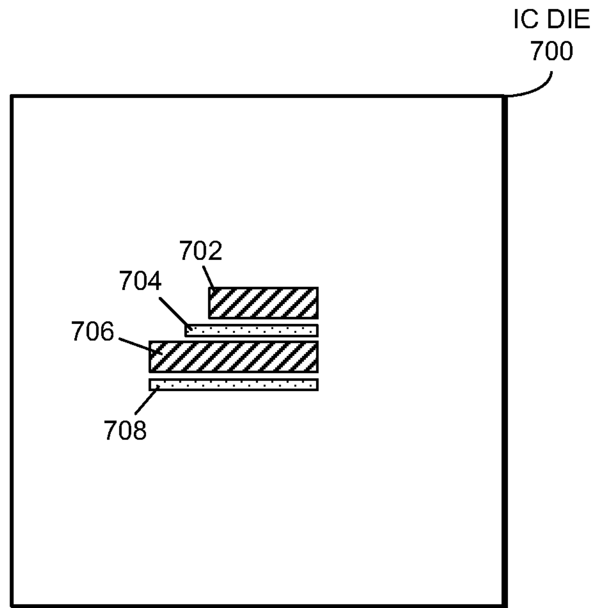

FIG. 7

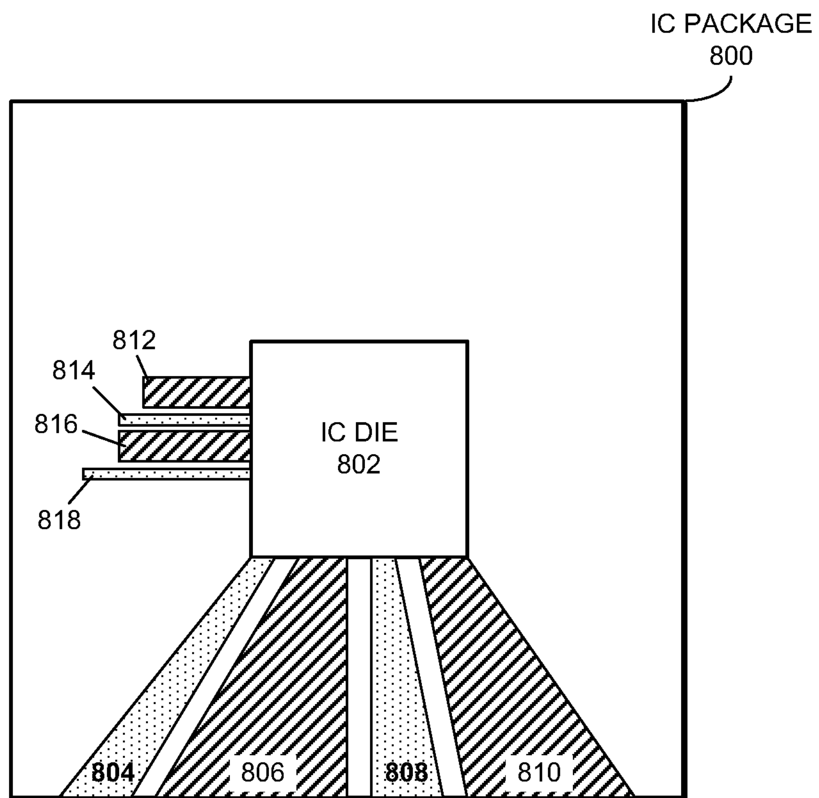

FIG. 8

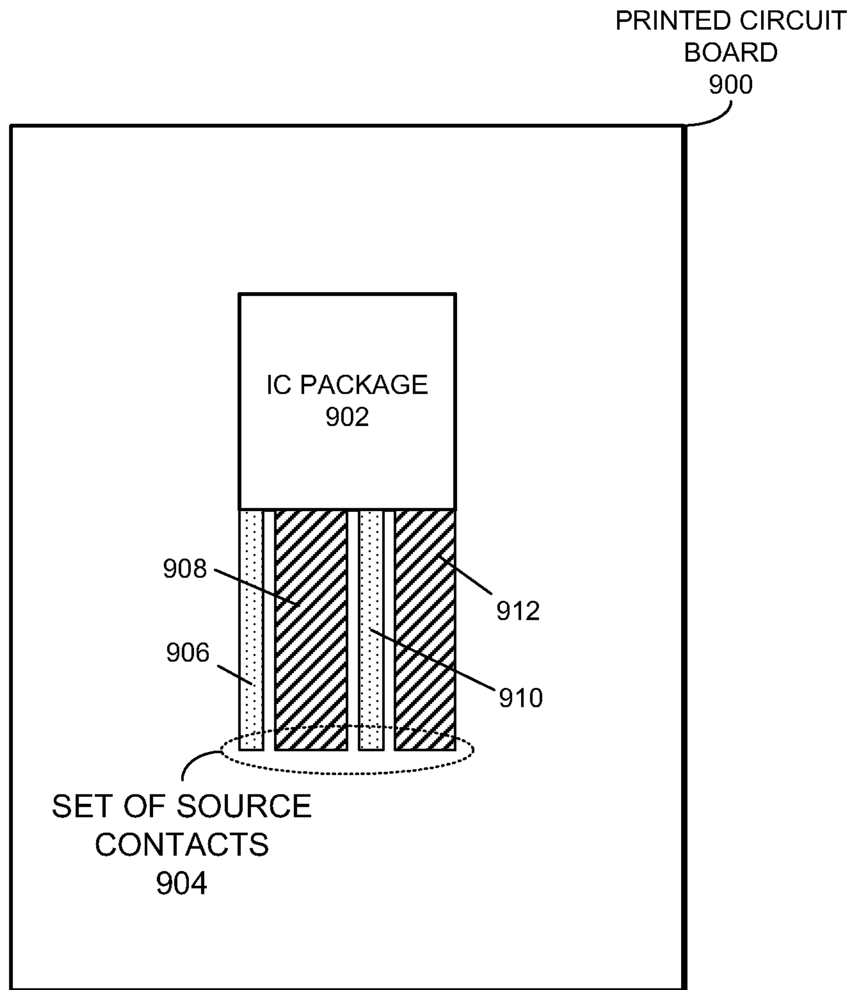

FIG. 9

INTERNATIONAL SEARCH REPORT	International application No. **PCT/US2012/050730**

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/18(2006.01)i, G06F 1/26(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F1/18, G06F1/26, G06F1/00, G06F17/50, G06F1/32

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: integrated circuit, die, IC, pcb, voltage, power, distribution, conductor and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 7,120,886 B2 (DELEULE, ARNAUD) 7 October 2008 See column 3, lines 3-6 and 15-43; claims 1-12; and figures 1-2.	1-12 13-22
A	US 7,127,688 B2 (LING, FENG et al.) 24 October 2006 See column 3, lines 36-67; claims 1-3; and figure 1.	1-22
A	US 2010-0250973 A1 (BREEN, III JOHN J. et al.) 30 September 2010 See paragraphs [0042]-[0045]; claims 1-7; and figures 2-3.	1-22
A	US 2010-0223485 A1 (ZOU, HUA) 2 September 2010 See paragraphs [0015]-[0018]; claims 1-3; and figure 3.	1-22
A	US 6,522,034 B1 (NAKAYAMA, MASASHI) 13 February 2003 See column 2, lines 29-55; column 5, lines 15-63; claims 1 and 3-5; and figures 5-7.	1-22

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents:
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"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
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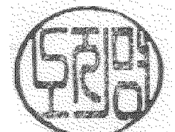
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 JANUARY 2013 (31.01.2013)	**01 FEBRUARY 2013 (01.02.2013)**

Name and mailing address of the ISA/KR	Authorized officer
	NHO, Ji Myong 
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-8528

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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