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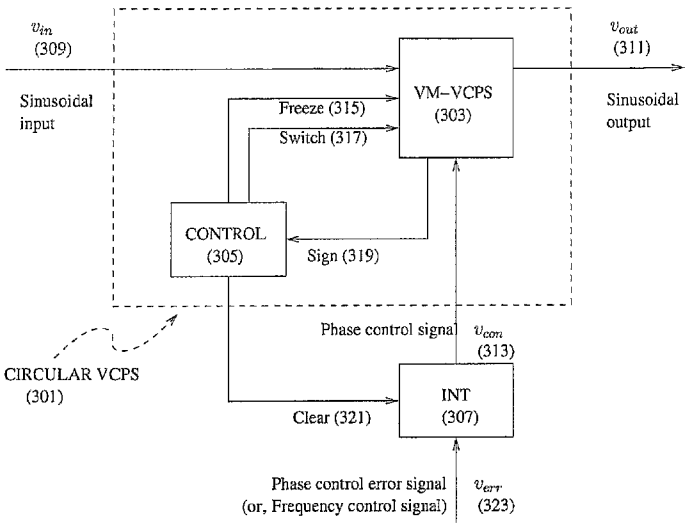
(54) **Title:** A CIRCULAR VOLTAGE-CONTROLLED PHASE SHIFTER



(57) **Abstract:** A circular voltage-controlled phase shifter (VCPS) configured to have actually unlimited phase shift range is invented. This is made possible by configuring the system to operate in a circular way differently from the conventional finite VCPS which operates in a linear way, so, whose phase output saturates as the phase control input exceeds some value. The preferred circular VCPS is composed of a vector modulationbased VCPS, a reset block, a control block. In particular, the invented VCPS shows an excellent linear phase shifting characteristic with respect to the control signal due to the vector modulation by a modulation signal with a pseudo-sinusoidal transfer curve as a function of the control signal. The modulation signal generator exploits the currentvoltage (IV) curve of a MOS differential amplifier pair. Thanks to this, the invented circular VCPS is appropriate for implementation in analogue CMOS circuit.

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Description

A CIRCULAR VOLTAGE-CONTROLLED PHASE SHIFTER

Technical Field

[1] This invention relates to a phase control mechanism, and more specifically to a voltage-controlled phase shifter, a voltage-controlled frequency shifter and their application to phaselocked loopbased systems employed in a communication transceiver so as to substantially extend the control signal range and the phase shifting range.

Background Art

[2] The voltage-controlled phase shifter (VCPS) is a phase shifter which shifts the phase of input RF (or, IF) signal by an amount in proportion to a control voltage input. It finds application in many electronic devices like phaselocked loop (PLL), delaylocked loop (DLL) and other phase controlling systems. In particular, there were several attempts to apply a VCPS to multiple antenna receivers or beamformer. Among them, [Ref 1] tried to produce an enhanced signal quality by adjusting the phases of signals received at the multiple antennas and combining them.

[3]

[4] [Ref 1] F. Ellinger and et. Al., "Ultracompact reflectivetype phase shifter mmic at cband with 360 degrees phasecontrol range for smart antenna combining," IEEE JSSC, pp.481486, Apr. 2002.

[5]

[6] A problem is that the variable range of the output phase is limited to some value (for example, 180 degrees) under normal CMOS process, and their common interest was to extend the limit using additional circuitry. In this invention, we call the VCPS with a finite phase range a finite VCPS in short. Another problem still remains even if a full phase shift range (360 degrees) is achieved. When a phase control system (e.g., PLL) operates in an autonomous way, the control voltage may exceed a value corresponding to the maximum phase shift (360 degrees) during operation. Without any other means, the control system is highly likely to be stuck at some boundary point. Because of the problem, the above beamformers with the finite VCPS are provided with necessary phase control information, which is confined within 360 degrees range, from a separate baseband signal processor. Obviously, this makes the system quite complex. In this case, it can be a solution to have a means to reset the controlled phase to zero phase shift with a phase domain change being made in some way when the controlled phase reaches the boundary point. By doing so, instead of being stuck at the boundary point, the control mechanism can operate in an autonomous way. In other words, the VCPS should operate in a circular way, as is described in this invention, in order that the

phase control system can work in a standalone way.

[7]

[8] In general, the VCPS is a device which takes in a RF sinusoidal signal and outputs its phaseshifted version whose phase is shifted by an amount commanded by a control voltage. Here, the input sinusoid includes both a continuous wave from a local oscillator with a fixed frequency and a narrow band RF (or IF) signal. Mathematically saying, the input sinusoid and the phaseshifted output sinusoid can be expressed as

$$v_{in}(t) = A(t) \cdot \sin\{2\pi f_c t + \theta(t)\}$$

and

$$v_{out}(t) = A(t) \cdot \sin\{2\pi f_c t + \theta(t) + \phi(v_{con})\}$$

, respectively. Here, A(t) and θ(t) mean the amplitude and phase of the input sinusoid which may be modulated according to a certain modulation format. Also, f_c and $\varphi(v_{con})$ mean the center frequency of the reference sinusoid and the phase shift as a function of the control voltage v_{con}, respectively. We will explain the principle of the circular VCPS referring to Fig. 1.

[9]

[10] Basically, the finite VCPS, which has been often used in conventional phase control systems, has a transfer curve (101) with a finite input control voltage range

$$v_{con} \in [-v_0, v_0]$$

and a finite output phase shift range

$$\phi(v_{con}) \in [-\phi_0, \phi_0]$$

as depicted in Fig. 1 (A). Therefore, the finite VCPS operates in a linear way in the control range, but saturates at a certain value beyond the range. This can cause a serious problem when the finite VCPS is put in a control loop and operated in an autonomous way. The control voltage of the finite VCPS may happen to exceed the fixed range during operation, then the control loop will end up being stuck there. On the contrary, the invented circular VCPS operates in a circular way in order to overcome the problem of the finite VCPs.

[11]

[12] To solve the problem, first, we generate L replicas of the input sinusoid whose i th replica is phaseshifted by $(i-1)\cdot\varphi_0$ where i=1,…,L and $\varphi_0=360^o/L$. Then, we configure them so that the transfer curve of the system will operate along the curves (103), (105), (107) with the direction indicated in Fig. 1 (B) as v_{con} varies. Note that the curves (103), (105), (107) correspond to the 2nd, 1st, L th phaseshifted version (i.e., phase domain), respectively. The curve (107) is the L th phaseshifted version because the L th phaseshifted version has phase shifting by $(L-1)\cdot\varphi_0=-\varphi_0$ using $L\varphi_0=360^o$. Assuming

an initial operating point at (b), $\varphi(v_{con})$ will move along the 1st phase domain ((a)(b)(c)) in (103) as long as v_{con} lies in $[-v_0, v_0]$. However, when v_{con} reaches v_0, the phase domain switches to the 2nd phase domain and $\varphi(v_{con})$ will move along the 2nd phase domain ((d)(e)(f)) in (103) starting from (e). That is, v_{con} resets to zero while φ keeps the same value. On the other hand, when v_{con} reaches $-v_0$, the phase domain switches to the L th phase domain and $\varphi(v_{con})$ will move along the L th phase domain ((g)(h)(i)) in (107) starting from (h). That is, v_{con} resets to zero while φ keeps the same value. The phase shift range can be extended infinitely according to the above method. Unwrapping the v_{con} range in xaxis each time the reset of v_{con} happens, the desired VCPS characteristics with infinite input phase control voltage range and infinite output phase shift range are obtained as depicted in Fig. 28 (C). Because the L phase domains cover 360° and repeats the same 360° phase shifting in a circular way each time v_{con} crosses multiple of $L \cdot v_0$, the VCPS is called a circular VCPS. Note that this curve has a hysterisis characteristic. That is, starting from (g), it will follow the path connecting (g)(h)(i)(b)(c)(e)(f) as v_{con} increases. However, starting from (f), it will follow a different path (f)(e)(d)(b)(a)(h)(g) as v_{con} decreases. The reason why the hysterisis characteristic is introduced is to avoid a phase domain bouncing at the phase domain switching point.

[13]

[14] A prior art similar to the invented circular VCPS is found in [Ref 2]:

[15]

[16] [Ref 2]: T. H. Lee and K. S. Donnelly and T.C. Ho, "Voltage controlled phase shifter with unlimited range", U.S. Patent 5,554,945, 1996.

Disclosure of Invention

Technical Problem

[17] The [Ref 2] also exploits the circular operation to achieve unlimited output phase range. However, because it is basically designed for phase shifting of digital signals whereas the invented VCPS is for phase shifting of analogue signals, direct comparison between the two is not appropriate. Also, the implementation details of the two are quite different. For example, the phase shifting mechanism of [Ref 2] is not so linear with respect to the control signal whereas that of the current invention shows an excellent linear phase shifting characteristics exploiting a pseudosinusoidal characteristic of the MOS transistor. In addition, the [Ref 2] did not consider hysterisis in the phase domain change whereas the current invention introduced the hysterisis mechanism in the phase domain change so as to avoid the phase domain bouncing problem. Therefore, the invented circular VCPS shows superior performance to that of [Ref 2] even if the two are directly compared.

Technical Solution

[18] According to an aspect of an exemplary embodiment of the present invention, there is provided a voltage-controlled phase shifter (VCPS) with an input sinusoid, an output sinusoid and a phase control signal input, the voltage controlled phase shifter comprising : a vector modulation-based VCPS configured to generate a continuously phaseshifted version of an input sinusoid in accordance to a phase control signal; a control block configured to receive necessary information signals including a Sign signal and to generate necessary control signals including a Switch signal, a Clear signal and a Freeze signal; and a reset block configured to pass said phase control signal to said vector modulationbased VCPS in normal operation and to reset its output to zero in accordance to said clear signal from said control block.

[19] According to another aspect of an exemplary embodiment of the present invention, there is provided a voltage-controlled frequency shifter (VCFS) with an input sinusoid, an output sinusoid and a frequency control signal input, the voltage controlled frequency shifter comprising: the VCPS wherein said reset block in said VCPS is replaced by said integrator outside said VCPS; a integrator is configured to store phase information and to dump its output to zero when a clear signal is activated from said control block as well as to integrate said frequency control signal.

[20] The voltage-controlled phase shifter (VCPS) may further comprise: a IQ splitter configured to split the phase of said input sinusoid into a quadrature sinusoid pair of said input sinusoid; a modulation signal generator configured to generate a pseudo-sinusoidal modulation signal pair in an analogue circuit as a function of said phase control signal input; and a vector modulator configured to modulate said a quadrature sinusoid pair of said input sinusoid by said a pseudo-sinusoidal modulation signal pair in order to generate a phaseshifted version of said input sinusoid.

[21] The voltage controlled phase shifter (VCPS) may further comprise: a pseudo-sinusoidal waveform generation means configured to generate the first intermediate pseudo-sinusoidal modulation signal pair as a function of said phase control signal input with a finite range; a switching means configured to switch said first intermediate pseudo-sinusoidal modulation signal pair to generate the second pseudo-sinusoidal modulation signal pair so that said second pseudo-sinusoidal modulation signal pair suits the required phase domain; a clutching means configured to pass said second pseudo-sinusoidal modulation signal pair in normal operation and to provide a temporary modulation signal pair during the phase domain change period in order to achieve a seamless phase shifting; and a threshold detection means configured to detect a threshold point at which phase domain change must take place, and to generate a logic level to said control block.

[22] The clutching means may be realized as a sample and hold block configured to pass said modulation signal pair while operating within a phase domain, and to sample and hold said modulation signal pair in a phase domain change period according to a Freeze signal activated from said control block , in order to achieve smooth phase domain changeover.

[23] The threshold detection means may be realized as a zero crossing detector configured to detect a zero crossing point of either of said modulation signal pair and to generate a Sign signal, and apply it to said control block .

[24] The control block may comprise a finite state machine configured to receive phase domain change information like a Sign signal from said threshold detection means, and to change its state in an appropriate way, and to generate necessary control signals like a Switch signal, a Clear signal, and a Freeze signal, and to apply them to said switching means, to said reset block, and said clutching means, respectively.

[25] According to another aspect of an exemplary embodiment of the present invention, there is provided a modulation signal generator configured to generate a pseudo-sinusoidal waveform pair as a function of a phase control control signal in such a way that: first, the first intermediate pseudo-sinusoidal modulation signal waveforms are generated as a function of said phase control signal within a finite range between an lower and upper boundary points; second, as soon as said phase control signal crosses over either said lower or uppper boundary point, said first intermediate pseudo-sinusoidal modulation signal waveforms are switched to the second intermediate pseudo-sinusoidal modulation signal waveforms, and said phase control signal is reset to zero (phase domain change) so that the second intermediate pseudo-sinusoidal modulation signal waveforms are continuously connected to the previous second intermediate pseudo-sinusoidal modulation signal waveforms as the phase control signal varies; third, said second intermediate pseudo-sinusoidal modulation signal waveforms are passed to the final pseudo-sinusoidal waveform pair when said phase control signal is within said lower and upper boundary points, and sampled and holded while said first intermediate pseudo-sinusoidal modulation signal waveforms are in the process of switching.

[26] A modulation signal generator may be configured to have a fintie number of phase domains which overlap with neighbouring phase domains, and said phase domain change is configured so that the phase shifting has a hysterisis characteristic as a function of said phase control signal.

[27] According to another aspect of an exemplary embodiment of the present invention, there is provided a modulation signal generator comprising: a pseudo-sinusoidal waveform generator configured to generate the first intermediate pseudo-sinusoidal modulation signal pair as a function of said phase control signal input within a finite

range; a switch box configured to switch said first intermediate pseudo-sinusoidal modulation signal pair to generate the second pseudo-sinusoidal modulation signal pair so that said second pseudo-sinusoidal modulation signal pair suits the required phase domain, according to a Switch signal activated from a control block; a sample and hold block configured to pass said second pseudo-sinusoidal modulation signal pair while operating within a phase domain, and to sample and hold said second pseudo-sinusoidal modulation signal pair in a phase domain change period, and to generate a final pseudo-sinusoidal modulation signal pair, according to a Freeze signal activated from a control block; a zero crossing detector configured to detect a zero crossing point of either of said first pseudo-sinusoidal modulation signal pair and to generate a logic signal Sign, and apply it to a control block; and a control block comprising a finite state machine configured to receive phase domain change information like a Sign signal from said zero crossing detector and to change its state in an appropriate way, and to generate necessary control signals like a Switch signal, a Clear signal, and a Freeze signal, and to apply them to said switch box, to an outer reset block, and said sample and hold block, respectively.

[28] The modulation signal generator may be configured without said switch box provided that said second intermediate pseudo-sinusoidal modulation signal pair is identical to said first intermediate pseudo-sinusoidal modulation signal pair.

[29] The pseudo-sinusoidal waveform generator may comprises inphase modulation signal generator and quadraturephase modulation signal generator is configured to generate a pseudo-cosine and pseudo-sine modulation signal pair as a function of said phase control signal input for a finite input range.

[30] The pseudo-sine waveform (odd function) may be synthesized by superimposing multiple copies of a basic waveform, where said basic waveform takes the form of pseudo-sine curve in a finite input range, and said copy may be a shifted version in x-axis and/or reversed version in y-axis and/or x-axis of said basic waveform.

[31] The pseudo-cosine waveform (even function) may be synthesized by superimposing multiple copies of a basic waveform and some constant value, where said basic waveform takes the form of quasisine curve in a finite input range, and said copy may be a shifted version in x-axis and/or reversed version in y-axis and/or x-axis of said basic waveform.

[32] The basic waveform may be obtained from the I-V curve (output current vs. input voltage transfer curve) of a transistor pair (e.g., MOS or BJT or any similar devices) in order to achieve an approximation to the true sine waveform, and said copy is obtained by shifting input voltage level and/or reversing input voltage ports and/or output current branches of said transistor or transistor pair.

[33] The basic waveform may be obtained from the I-V curve (output current vs. input

voltage transfer curve) of a plural number of said transistor pairs in parallel in order to achieve a better approximation to the true sine waveform.

[34] The basic waveform may be obtained from the I-V curve (output current vs. input voltage transfer curve) of a plural number of said transistor pairs in parallel in order to achieve an approximation to any required waveform.

[35] The shifting input voltage level of said transistor or transistor pair may be achieved by an appropriate adjustment of W/L (width to length ratio) and a bias current of said MOS according to a way exploiting the dependency of the gate-source voltage of the MOS on the inverse-root of W/L and the dependency on the root of the bias current as described in the body or any other similar way for other devices.

[36] The modulation signal generator may further comprise: a pseudo-sinusoidal waveform generation means configured to generate the first intermediate pseudo-sinusoidal modulation signal pair for a finite input range which spans two periods of the sine waveform as a function of said phase control signal input; a clutching means configured to pass said first pseudo-sinusoidal modulation signal pair in normal operation and to provide a temporary modulation signal pair during the phase domain change period in order to achieve a seamless phase shifting; and a threshold detection means configured to detect a threshold point at which phase domain change must take place, and to generate a logic level to said control block.

[37] The pseudo-sinusoidal waveform generation means may be configured to generate; A pseudo-sinusoidal waveform pair for 720 degrees range according to a phase control signal input; and said control block is configured to make phase domain change only when said control signal input reaches either limit values whose phase shifts correspond to 360 degrees and -360 degrees, respectively.

Advantageous Effects

[38] In this invention, we can see that the unlimited phase shifting is achieved in a circular way (except during the phase domain change period), and the phase shifting is almost linear in the normal intervals. The maximum phase deviation from the linear slope due to the nonideality of the pseudosinusoids is measured to be 3.5 degrees. At the same time, the maximum amplitude deviation ratio from the constant envelope is measured to be 2.2 percent. These values are regarded as small enough to demonstrate effectiveness of the invented circular VCPS.

Brief Description of the Drawings

[39] These and other aspects of the present invention will become more apparent and more readily appreciated from the following description of exemplary embodiments thereof, with reference to the accompanying drawings, in which:

[40] Figure 1 is (A) transfer curve of a finite VCPS, (B) transfer curve example of the

circular VCPS, (C) Unwrapped transfer curve of the circular VCPS according to the current invention.

[41] Figure 2 is a block diagram of the invented circular VCPS.

[42] Figure 3 is a block diagram of the invented circular VCFS.

[43] Figure 4 is an embodiment example of the invented vector modulationbased VCPS (VMVCPS).

[44] Figure 5 is transfer curves of (A) pseudocosine waveform ($v_{mod\text{-}I\text{-}1}$), (B) pseudosine waveform ($v_{mod\text{-}Q\text{-}1}$) and (C) output phase shift characteristic $\varphi(v_{con})$ as a function of v_{con}.

[45] Figure 6 is required modulation signal pairs ($v_{mod\text{-}I\text{-}2}$, $v_{mod\text{-}Q\text{-}1}$) for the respective phase domains D1 D4 (ex: L = 4).

[46] Figure 7 is a state transition diagram of the control box.

[47] Figure 8 is transfer curves of (A) $v_{mod\text{-}I\text{-}1}$, (B) $v_{mod\text{-}Q\text{-}1}$ and generation of common control signals (C) SignI, (D) SignQ, (E) Clear, (F) Freeze to and from the control box as a function of v_{con}.

[48] Figure 9 is (A) a basic differential amplifier pair and (B) its IV curve.

[49] Figure 10 is (A) a double differential amplifier pair and (B) its IV curve.

[50] Figure 11 is (A) an extended differential amplifier pair with input voltage offset and (B) its IV curve.

[51] Figure 12 is (A) transfer curve of pseudocosine waveform ($v_{mod\text{-}I\text{-}1}$) as a function of v_{con} and (B)(D) necessary IV curves for its synthesis.

[52] Figure 13 is (A) transfer curve of pseudosine waveform ($v_{mod\text{-}Q\text{-}1}$) as a function of v_{con} and (B)(D) necessary IV curves for its synthesis.

[53] Figure 14 is an embodiment of pseudocosine waveform generator ($v_{mod\text{-}I\text{-}1}$).

[54] Figure 15 is an embodiment of pseudosine waveform generator ($v_{mod\text{-}Q\text{-}1}$).

[55] Figure 16 is an example of sample and hold block.

[56] Figure 17 is an example of IQ splitter.

[57] Figure 18 is an example of vector modulator.

[58] Figure 19 is the second embodiment example of the invented vector modulationbased VCPS (VMVCPS).

[59] Figure 20 is transfer curves of (A) pseudocosine ($v_{mod\text{-}I\text{-}1}$), (B) pseudosine ($v_{mod\text{-}Q\text{-}1}$) and output phase shift characteristic $\varphi(v_{con})$ as a function of v_{con} for the second embod iment.

[60] Figure 21 is (A) transfer curve of $v_{mod\text{-}I\text{-}1}$, (B) transfer curve of $v_{mod\text{-}Q\text{-}1}$ and generation of control signals (C) SignI, (D) SignQ, (E) Clear, (F) Freeze to and from the control box for the second embodiment example.

[61] Figure 22 is a state transition diagram of the control box for the second embodiment.

[62] Figure 23 is (A) transfer curve of $v_{mod\text{-}i\text{-}1}$ as a function of v_{con}, and (B)(H) necessary IV

curves for its synthesis.

[63] Figure 24 is (A) transfer curve of $v_{mod-Q-1}$ as a function of V_{con}, and (B)(F) necessary IV curves for its synthesis.

[64] Figure 25 is an embodiment of $v_{mod-I-1}$ generator for the second embodiment example.

[65] Figure 26 is an embodiment of $v_{mod-Q-1}$ generator for the second embodiment example.

[66] Figure 27 is (A) generated pseudocosine (v_{mod-I}) and pseudosine (v_{mod-Q}) waveforms, (B) phase shifting characteristic, (C) amplitude variation characteristic.

Best Mode for Carrying Out the Invention

[67] Structure:

[68] The block diagram of the invented circular voltage-controlled phase shifter (VCPS) is shown in Fig. 2. The circular VCPS (201) is composed of a vector modulationbased VCPS (denoted VMVCPS) (203) and a control block (denoted CONTROL) (205) and a reset block (denoted RESET) (207). It has a RF input sinusoid v_{in} (209), a RF output sinusoid v_{out} (211) and a phase control signal v_{con} (213). It has also internal control signals like Clear (221), Sign (219), Freeze (215) and Switch (217). Assuming v_{con} is inside boundary points, v_{con} is forwarded to VMVCPS as it is and shifts the phase of v_{in} and produces its phaseshifted version v_{out}. When v_{con} goes beyond either boundary point, the control block detects the event through Sign signal from VMVCPS, and sends Clear signal to the reset block. Then, the remainder (223) after subtracting the boundary value from v_{con} is applied to the VMVCPS, and carries out the same operation as above. Other control signals like Freeze and Switch are used to control VMVCPS.

[69] The block diagram of the invented circular voltage-controlled frequency shifter (VCFS) is shown in Fig. 3. The VCFS is obtained by substituting the reset block with an integrator with a reset functionality. Therefore, it is composed of a vector modulationbased VCPS (denoted VMVCPS) (303) and a control block (denoted CONTROL) (305) and an integrator block (denoted INT) (307). It has a RF input sinusoid v_{in} (309), a RF output sinusoid v_{out} (311) and a phase control error signal v_{err} (323) (or frequency control signal). The output of the integrator becomes the phase control signal v_{con} (313). It has also internal control signals like Clear (321), Sign (319), Freeze (315) and Switch (317). Its operation is almost the same as that of the VCPS except that its control input is the phase control error signal, instead of phase control signal. The phase control error signal becomes the phase control signal after the integrator. Due to the integration operation, the VCFS shifts the center frequency of the input sinusoid as much as commanded by the frequency control signal (so, the name VCFS). Because many closed loop phase control systems generate the phase control error signal and employ an integrator in front of the VCPS, the above combined structure VCFS (VCPS

(301) and INT (307)) is very useful. Especially, this structure has advantage that it can conserve the phase information explicitly in the integrator (a kind of memory) and can reuse it for some purpose. For example, in a beamforming system under timedivision duplexing (TDD) system, the phase information obtained from the receive beamforming can be reused for the transmit beamforming by storing it in the integrator. In such reasons, we will describe the invented circular VCPS assuming existence of the integrator although the integrator is not necessary component of the circular VCPS itself.

[70] The vector modulationbased VCPS (VMVCPS) (203) (303) plays a central role in the circular VCPS. The block diagram of an embodiment example of the VMVCPS is shown in Fig. 4. The VMVCPS comprises a modulation signal generator (denoted MODULATION SIG GEN) (405), a IQ splitter (denoted IQ SPLITTER) (401), a vector modulator (denoted VECTOR MODULATOR) (403).

[71] The modulation signal generator (405) is again composed of a pseudocosine waveform generator (denoted PSEUDOCOS GEN) (409), a pseudosine waveform generator (denoted PSEUDOSIN GEN) (411), a control signal switch box (denoted SWITCH BOX) (415), a sample and hold (denoted S/H) (417) and a zero crossing detector (denoted ZCD) (413). The combination of the pseudocosine waveform generator and the pseudosine waveform generator is called the pseudosinusoidal waveform generator (denoted PSEUDOSINUSOID GEN) (407).

[72] The IQ splitter (401) splits the RF input sinusoidal signal (denoted v_{in}) (419) into a quadrature pair (denoted v_{in-I} (421) and v_{in-Q} (423)) of v_{in}. The modulation signal generator produces a quadrature pair of modulation signals (denoted v_{mod-I} (437) and v_{mod-Q} (439)) as a function of v_{con} (427) and auxiliary logic signals from the control block. The pseudocosine waveform generator and the pseudosine waveform generator generate the first intermediate quadrature pair (denoted $v_{mod-I-1}$ (429) and $v_{mod-Q-1}$ (431)). The zero crossing detector detects the zero crossing time of $v_{mod-I-1}$ and $v_{mod-Q-1}$ in order to generate corresponding Sign signals (denoted SignI (441) and SignQ (443)), respectively, and sends them to the control box in order to notify the current state. The switch box switches $v_{mod-I-1}$ and $v_{mod-Q-1}$ into the second intermediate quadrature pair (denoted $v_{mod-I-2}$ (433) and $v_{mod-Q-2}$ (435)) under control of the Switch signals (denoted Switch1 (445) and Switch2 (447)) from the control box. The sample and hold generates the final quadrature pair (denoted v_{mod-I} (437) and v_{mod-Q} (439)), which is the sample and holded version of $v_{mod-I-2}$ and $v_{mod-Q-2}$, under control of the Freeze signal (denoted Freeze) (449) from the control box. The vector modulator performs a vector modulation taking in the inputs such as the quadrature pair of RF input signals (denoted v_{in-I} and v_{in-Q}) from the IQ splitter block and the quadrature pair of modulation signals (denoted v_{mod-I} and v_{mod-Q}) from the sample and hold block,

generating the desired phaseshifted version v_{out} (425) of the RF input sinusoidal wave v_{in} as a function of v_{con}.

[73]

[74] Operation:

[75] Operation of the VMVCPS in Fig. 4 is based on a vector modulation. Let the RF input sinusoidal signal as

[76]
$$v_{in}(t) = A(t) \cdot \sin\{2\pi f_c t + \theta(t)\}$$

(1)

[77] where A(t), f_c and θ(t) are the amplitude, center frequency and phase modulation, if any, of the signal. Then, the ouput sinusoidal signal v_{out} should be a phaseshifted version of v_{in} as commanded by the control signal v_{con}. That is,

[78]
$$v_{out}(t) = A(t) \cdot \sin\{2\pi f_c t + \theta(t) + \phi(v_{con})\}$$

(2)

[79] where $\varphi(v_{con})$ is the desired phase shift as a function of v_{con}. We put A(t)=1 for convenience. To implement v_{out}(t) as expressed in (2), we analyze (2) using a wellknown trigonometric equality as

[80]
$$v_{out}(t) = \sin\{2\pi f_c t + \theta(t)\} \cdot \cos\{\phi(v_{con})\} + \cos\{2\pi f_c t + \theta(t)\} \cdot \sin\{\phi(v_{con})\}$$

. (3)

[81] From (3), we can see that v_{out}(t) can be obtained following the next steps: First, generate a quadrature pair of the RF input signal as

$$v_{in-I}(t) = \cos\{2\pi f_c t + \theta(t)\}$$

and

$$v_{in-Q}(t) = \sin\{2\pi f_c t + \theta(t)\}$$

. Second, generate a quadrature pair of the modulation signal as a function of v_{con} as

$$v_{\mathrm{mod}-I}(v_{con}) = \cos\{\phi(v_{con})\}$$

and

$$v_{\mathrm{mod}-Q}(v_{con}) = \sin\{\phi(v_{con})\}$$

. Finally, vectormodulate the two quadrature pairs to generate the output signal as

[82]

[83]
$$v_{out}(t) = v_{in-Q}(t) \cdot v_{\mathrm{mod}-I}(v_{con}) + v_{in-I}(t) \cdot v_{\mathrm{mod}-Q}(v_{con})$$

.

[84]

[85] In this invention, for notational convenience, cosine and sine components of any quadrature pair are taken as inphase and quadraturephase components, respectively.

Accordingly, their notations have suffix I and Q, repectively.

[86] For the most desired performance, we assume a linear phase shifting characteristic of $\varphi(v_{con})$. That is,

$$\varphi(v_{con}) = \frac{\varphi_0}{v_0} v_{con}$$

so that $\varphi(v_0)=\varphi_0$, $\varphi(0)=0$ and $\varphi(-v_0)=-\varphi_0$. Accordingly, the above modulation signal pair can be written as

[87]

[88]

$$v_{\text{mod-}I}(v_{con}) = \cos(\frac{\varphi_0}{v_0} v_{con})$$

, (4)

[89]

$$v_{\text{mod-}Q}(v_{con}) = \sin(\frac{\varphi_0}{v_0} v_{con})$$

. (5)

[90]

[91] In other words, if we generate the modulation signal pair as a function of v_{con} as given by (4) and (5) and apply them to the modulation ports of the vector modulator, the output RF signal will be phaseshifted as much as

$$\frac{\varphi_0}{v_0} v_{con}$$

for some positive φ_0 and v_0 according to

[92]

$$v_{out}(t) = \sin\{2\pi f_c t + \theta(t) + \frac{\varphi_0}{v_0} v_{con}\}$$

. (6)

[93]

[94] The above description is the principle of the VMVCPS. The major problem is how to generate the modulation signal pair in (4) and (5) in an analogue circuit. This could be a trivial job if a lookup table is available. However, without employing a lookup table requiring an ADC/DAC pair and a digital circuit, it is not a trivial job to generate the sinusoidal waveform in an analogue circuit as a function of the control signal whose range should extend indefinitely. The method employed in this invention is to generate a pseudosinusoidal waveform for a finite range first (i.e., $-v_0 \le v_{con} \le v_0$), which approximate the true sinusoidal waveform for the region, and manipulate the waveform in such a way that it can cover the unlimited range of v_{con}.

[95]

[96] Modulation signal generator:

[97] An example of the pseudosinusoidal waveforms (denoted $v_{mod\text{-}I\text{-}1}$ (501) and $v_{mod\text{-}Q\text{-}1}$ (503)) are shown in Fig. 5 (A) and (B). They resembles the true cosine and sine waveforms in a finite range of the phase control signal (i.e., $-v_0 \le v_{con} \le v_0$). As a result, when these waveforms are directly applied to the modulation signal ports (denoted $v_{mod\text{-}I}$ (437) and $v_{mod\text{-}Q}$ (439)) of the vector modulator in Fig. 4, it will shift the phase of v_{in} from $-\varphi_0$ to φ_0 as v_{con} varies from $-v_0$ to v_0 according to (6) as shown in the curve (505) in Fig. 5 (C). However, the pseudosinusoidal waveforms in this state cannot be extended indefinitely in a sinusoidal fashion due to the hardware limitation of the analogue circuit. In fact, they are saturated at a certain value (so does $\varphi(v_{con})$) if v_{con} goes beyond the boundary point.

[98] As a solution for that, we switch the pseudosinusoidal waveforms as the control signal crosses over the boundary values such as v_0 and $-v_0$ so that the phase shifting characteristic curve can show a circular operation with a proper phase domain change. This phase domain change is realized by using the switch box under control of the switching signals from the control box. The switch box switches the first intermediate quadrature pair (denoted $v_{mod\text{-}I\text{-}1}$ and $v_{mod\text{-}Q\text{-}1}$) to the second intermediate quadrature pair (denoted $v_{mod\text{-}I\text{-}2}$ and $v_{mod\text{-}Q\text{-}2}$) under control of the logic signals Switch (denoted Switch1 and Switch2) from the control box in order to extend the pseudosinusoidal waveform indefinitely. The generation of the modulation signal using the switching mechanism is one of the novelties of the current invention.

[99] As a typical example, we divide the whole phase range into four (i.e., L=4) overlapping phase domains: D1 (-90° to 90°), D2 (0° to 180°), D3 (90° to 270°), D4 (-180° to 0°) with $\varphi_0 = 90^\circ$. They overlap with the neighbouring phase domains in order to have a hysterisis characteristic. An appropriate switching mechanism is shown in Fig. 6. The Fig. 6 (A), (B), (C), (D) describes the required modulation signals (denoted $v_{mod\text{-}I\text{-}2}$ (solid curve) and $v_{mod\text{-}Q\text{-}2}$ (dashed curve)) for the phase domains D1, D2, D3, D4, respectively.

[100] To help understanding, let us initialize the operation at $v_{con}=0$ (indicated (a') in Fig. 6 (A)). In D1, $v_{mod\text{-}I\text{-}2}$ is set to

$$\cos\left(\frac{\varphi_0}{v_0} v_{con}\right)$$

(601) and $v_{mod\text{-}Q\text{-}2}$ is set to

$$\sin\left(\frac{\varphi_0}{v_0} v_{con}\right)$$

(603). As v_{con} increases to reach v_0 (indicated (b)), the phase domain should be changed from D1 to D2 with $v_{mod\text{-}I\text{-}2}$ set to

$-\sin(\frac{\dot{\phi}_0}{v_0}v_{con})$

(605), $v_{mod\text{-}Q\text{-}2}$ set to

$\cos(\frac{\dot{\phi}_0}{v_0}v_{con})$

(607) and v_{con} reset to zero ((b')). In D2, as v_{con} increases to reach v_0 (indicated (c)), the phase domain should be changed from D2 to D3 with $v_{mod\text{-}I\text{-}2}$ set to

$-\cos(\frac{\dot{\phi}_0}{v_0}v_{con})$

(609), $v_{mod\text{-}Q\text{-}2}$ set to

$-\sin(\frac{\dot{\phi}_0}{v_0}v_{con})$

(611) and v_{con} reset to zero ((c')). In D3, as v_{con} increases to reach v_0 (indicated (d)), the phase domain should be changed from D3 to D4 with $v_{mod\text{-}I\text{-}2}$ set to

$\sin(\frac{\dot{\phi}_0}{v_0}v_{con})$

(613), $v_{mod\text{-}Q\text{-}2}$ set to

$-\cos(\frac{\dot{\phi}_0}{v_0}v_{con})$

(615) and v_{con} reset to zero ((d')). In D4, as v_{con} increases to reach v_0 (indicated (a)), the phase domain should be changed from D4 to D1 with $v_{mod\text{-}I\text{-}2}$ set to

$\cos(\frac{\dot{\phi}_0}{v_0}v_{con})$

(601), $v_{mod\text{-}Q\text{-}2}$ set to

$\sin(\frac{\dot{\phi}_0}{v_0}v_{con})$

(603) and v_{con} reset to zero ((a')). The above operation repeats in a circular way as v_{con} keeps on increasing. Through the above way, the pseudosinusoidal waveform can be continued unlimitedly in the positive direction as v_{con} increases.

[101] In the same way, the pseudosinusoidal waveforms can be continued unlimitedly in the negative direction as v_{con} decreases. Starting from D1, $v_{mod\text{-}I\text{-}2}$ is set to

$\cos(\frac{\dot{\phi}_0}{v_0}v_{con})$

(601) and $v_{mod\text{-}Q\text{-}2}$ is set to

$\sin(\frac{\dot{\phi}_0}{v_0}v_{con})$

(603). As v_{con} decreases to reach $-v_0$ (indicated (f)), the phase domain should be changed from D1 to D4 with $v_{mod\text{-}I\text{-}2}$ set to

$$\sin(\frac{\dot{\phi}_0}{v_0} v_{con})$$

(613), $v_{mod\text{-}Q\text{-}2}$ set to

$$-\cos(\frac{\dot{\phi}_0}{v_0} v_{con})$$

(615) and v_{con} reset to zero ((d')). In D4, as v_{con} decreases to reach $-v_0$ (indicated (g)), the phase domain should be changed from D4 to D3 with $v_{mod\text{-}I\text{-}2}$ set to

$$-\cos(\frac{\dot{\phi}_0}{v_0} v_{con})$$

(609), $v_{mod\text{-}Q\text{-}2}$ set to

$$-\sin(\frac{\dot{\phi}_0}{v_0} v_{con})$$

(611) and v_{con} reset to zero ((c')). In D3, as v_{con} decreases to reach $-v_0$ (indicated (h)), the phase domain should be changed from D3 to D2 with $v_{mod\text{-}I\text{-}2}$ set to

$$-\sin(\frac{\dot{\phi}_0}{v_0} v_{con})$$

(605), $v_{mod\text{-}Q\text{-}2}$ set to

$$\cos(\frac{\dot{\phi}_0}{v_0} v_{con})$$

(607) and v_{con} reset to zero ((b')). In D2, as v_{con} decreases to reach $-v_0$ (indicated (i)), the phase domain should be changed from D2 to D1 with $v_{mod\text{-}I\text{-}2}$ set to

$$\cos(\frac{\dot{\phi}_0}{v_0} v_{con})$$

(601), $v_{mod\text{-}Q\text{-}2}$ set to

$$\sin(\frac{\dot{\phi}_0}{v_0} v_{con})$$

(603) and v_{con} reset to zero ((a')). The above operation repeats in a circular way as v_{con} keeps on decreasing.

[102] We can identify the hysterisis characteristic in the above operation, and this prevents the bouncing problem at the boundary points. For example, once the phase domain change has taken place (e.g., from D1 to D2), the phase domain will be staying in D2 in spite of small variation of v_{con}, not getting back to D1, because the VCPS starts its operation with the reset v_{con} in D2. Without this hysterisis mechanism (i.e., v_{con} not being reset to zero after phase domain change), the phase domain will be bouncing

back and force between D1 and D2 for small variation of

v_{con}

. The hysterisis mechanism is one of novelties of the current invention.

[103] One problem associated with the above phase domain change is that the phase domain change is not carried out instantly. Because of a finite time in clearing the integrator to reset v_{con} and in switching the pseudosinusoidal waveforms, the resultant phaseshifted version is venerable to switching glitches if not provided with any means.

[104] To solve the problem, we put a clutching mechanism between the switch box (415) and the vector modulator (403). The clutching mechanism disconnects the path between the two blocks temporarily while keeping the recent modulation signal values. This allows us to change the phase domain safely. During the period of the dis-connection, we can clear the integrator and switch the pseudosinusoidal waveforms without effecting on the modulation signals at the input ports of the vector modulator (denoted v_{mod-I} and v_{mod-Q}). After phase domain change, the path is recovered. The clutching mechanism is similar to that of the car, so the name. The clutching mechanism is realized by using a sample and hold circuit (denoted S/H) (417) under control of the Freeze signal (449) from the control box. Consequently, the modulation signal generator generates an appropriate modulation signal pair (denoted v_{mod-I} (437) and v_{mod-Q} (439)) and provides them for the vector modulator. The clutching mechanism is another novelty of the current invention.

[105]

[106] Control box:

[107] In implementing the modulation signal generator, several control logics are necessary. They are generated by the control box (219), which is implemented as a digital logic circuit. This is a simple control logic and can be easily combined with analogue circuit in a mixedmode CMOS circuit. The major aim of the control box is to make a smooth change of the phase domain when

v_{con}

reaches either boundary values (v_0 or $-v_0$) so that the phase shifting can be achieved in a perfectly circular manner.

[108]

[109] When v_{con} reaches v_0 or $-v_0$, the control box resets the integrator so that v_{con} goes back to zero and switches the modulation signals so that the next phase domain transfer curve can be effective. A zero crossing detector (denoted ZCD) (413) is provided in order to detect the boundary points in terms of the zero crossing points of either $v_{mod-I-1}$ (429) or $v_{mod-Q-1}$ (431) and apply corresponding logic signals Sign (denoted SignI (441) and SignQ (443)) to the control box (see Fig. 4).

[110]

[111] The control box operates as an finite state machine whose state changes according to the input logics like SignI and SignQ from the zero crossing detector while generating appropriate control logics like Clear (221), Freeze (449) and Switch (denoted Switch1 (445) and Switch2 (447)) signals. The generated control logics are activeHigh in this invention. This means the associated operation is active when the logic is High. Here, the state is defined as the respective phase domain. As before, we explain the operation of the control box taking an example for four phase domains (i.e., L=4). Therefore, we have four states (S1, S2, S3, S4) which stands for the respective phase domains (D1, D2, D3, D4). The state transition diagram of the control box corresponding to the operation of the modulation signal generator according to the diagram in Fig. 6 is shown in Fig. 7. In the whole operations, there are two kinds of operations: one is statespecific operations, and another is common operations which happen irrepective of specific states.

[112]

[113] We explain the common operations first (see Fig. 8). There are transfer curves of $v_{mod\text{-}I\text{-}1}$ (801) and $v_{mod\text{-}Q\text{-}1}$ (803) in Fig. 8 (A) and (B) from the pseudosinusoidal waveform generator, which is the same as Fig. 5 (A) and (B) in the region of interest (i.e., $-v_0 \le v_{con} \le v_0$). Also, there are generation of SignI (805) and SignQ (807) in Fig. 8 (C) and (D) from the zero crossing detector, and generation of Clear logic signal (809) and Freeze logic signal (811) in Fig. 8 (E) and (F) from the control logic, respectively. Note that the waveform (803) of Fig. 8 (B) is different from that (503) of Fig. 5 (B) in the outer region (i.e., $v_{con} \le -v_0$, $v_{con} \ge v_0$). This is to enable a more precise waveform generation when implemented in CMOS as will be explained later.

[114] When v_{con} stays within the boundary values (i.e., $-v_0 \le v_{con} \le v_0$), The Clear and Freeze keep Low. As v_{con} reaches v_0, SignI will fall ((a) in Fig. 8 (C)) while SignQ stays High. These SignI and SignQ are applied to the control box, and the control box recogizes that it is time to make phase domain change in the positive direction. At first, the control box activates Freeze logic signal (in this diagram, Freeze goes High in (F)) so as to disconnect the path between the switch box and the vector modulator and to hold the current modulation signals sampled just before the disconnection. Then, the control box activates Clear logic signal (in this diagram, Clear goes High in (E)) so as to reset the integrator (so v_{con}) to zero.

[115] As v_{con} reaches $-v_0$, SignI will fall ((b) in Fig. 8 (C)) while SignQ stays Low. These SignI and SignQ are applied to the control box, and the control box recogizes that it is time to make phase domain change in the negative direction. At first, the control box activates Freeze logic signal (in this diagram, Freeze goes High in (F)) so as to disconnect the path between the switch box and the vector modulator and to hold the

current modulation signals sampled just before the disconnection. Then, the control box activates Clear logic signal (in this diagram, Clear goes High in (E)) so as to reset the integrator (so v_{con}) to zero.

[116] The remaining thing is for the control box to move the current phase domain over to the next phase domain by manipulating the Switch logic signals (Switch1 and Switch2). However, there are statespecific operations, and they will be explained further referring to Fig. 7.

[117] When initialized (e.g., powered on) (701), the control box is set to S1 (703) by activating Freeze and Clear to put v_{con} to zero and generating an appropriate Switch logics so that $v_{mod\text{-}i\text{-}2}$ is connected to $v_{mod\text{-}i\text{-}1}$ (= $\cos(\frac{\dot{\phi}_0}{v_0} v_{con})$) and $v_{mod\text{-}Q\text{-}2}$ is connected to $v_{mod\text{-}Q\text{-}1}$ (= $\sin(\frac{\dot{\phi}_0}{v_0} v_{con})$), respectively, as suggested in Fig. 6 (A).

[118] Explaining the operation in the positive direction first: In S1 (703) in Fig. 7, the control box changes to S2 (705) when v_{con} reaches v_0 so that SignI falls (i.e., at the negative edge) and SignQ stays High. The phase domain change from D1 to D2 is carried out by activating Freeze, and then, Clear to put v_{con} to zero and generating an appropiate Switch logics so that $v_{mod\text{-}I\text{-}2}$ is connected to $-v_{mod\text{-}Q\text{-}1}$ and $v_{mod\text{-}Q\text{-}2}$ is connected to $v_{mod\text{-}I\text{-}1}$, respectively, as suggested in Fig. 6 (B). In S2 (705) in Fig. 7, the control box changes to S3 (707) when v_{con} reaches v_0 so that SignI falls (i.e., at the negative edge) and SignQ stays High. The phase domain change from D2 to D3 is carried out by activating Freeze, and then, Clear to put v_{con} to zero and generating an appropriate Switch logics so that $v_{mod\text{-}I\text{-}2}$ is connected to $-v_{mod\text{-}I\text{-}1}$ and $v_{mod\text{-}Q\text{-}2}$ is connected to $-v_{mod\text{-}Q\text{-}1}$, respectively, as suggested in Fig. 6 (C). In S3 (707) in Fig. 7, the control box changes to S4 (709) when v_{con} reaches v_0 so that SignI falls (i.e., at the negative edge) and SignQ stays High. The phase domain change from D3 to D4 is carried out by activating Freeze, and then, Clear to put v_{con} to zero and generating an appropiate Switch logics so that $v_{mod\text{-}I\text{-}2}$ is connected to $v_{mod\text{-}Q\text{-}1}$ and $v_{mod\text{-}Q\text{-}2}$ is connected to $-v_{mod\text{-}I\text{-}1}$, respectively, as suggested in Fig. 6 (D). In S4 (709) in Fig. 7, the control box changes to S1 (703) when v_{con} reaches v_0 so that SignI falls (i.e., at the negative edge) and SignQ stays High. The phase domain change from D4 to D1 is carried out by activating Freeze, and then, Clear to put v_{con} to zero and generating an appropiate Switch logics so that $v_{mod\text{-}I\text{-}2}$ is connected to $v_{mod\text{-}I\text{-}1}$ and $v_{mod\text{-}Q\text{-}2}$ is connected to $v_{mod\text{-}Q\text{-}1}$, respectively, as suggested in Fig. 6 (A).

[119] Explaining the operation in the negative direction next: In S1 (703) in Fig. 7, the control box changes to S4 (709) when v_{con} reaches $-v_0$ so that SignI falls (i.e., at the negative edge) and SignQ stays Low. The phase domain change from D1 to D4 is carried out by activating Freeze, and then, Clear to put v_{con} to zero and generating an appropriate Switch logics so that $v_{mod-I-2}$ is connected to $v_{mod-Q-1}$ and $v_{mod-Q-2}$ is connected to $-v_{mod-I-1}$, respectively, as suggested in Fig. 6 (D). In S4 (709) in Fig. 7, the control box changes to S3 (707) when v_{con} reaches $-v_0$ so that SignI falls (i.e., at the negative edge) and SignQ stays Low. The phase domain change from D4 to D3 is carried out by activating Freeze, and then, Clear to put v_{con} to zero and generating an appropiate Switch logics so that $v_{mod-I-2}$ is connected to $-v_{mod-I-1}$ and $v_{mod-Q-2}$ is connected to $-v_{mod-Q-1}$, respectively, as suggested in Fig. 6 (C). In S3 (707) in Fig. 7, the control box changes to S2 (705) when v_{con} reaches $-v_0$ so that SignI falls (i.e., at the negative edge) and SignQ stays Low. The phase domain change from D3 to D2 is carried out by activating Freeze, and then, Clear to put v_{con} to zero and generating an appropriate Switch logics so that $v_{mod-I-2}$ is connected to $-v_{mod-Q-1}$ and $v_{mod-Q-2}$ is connected to $v_{mod-I-1}$, respectively, as suggested in Fig. 6 (B). In S2 (705) in Fig. 7, the control box changes to S1 (703) when v_{con} reaches $-v_0$ so that SignI falls (i.e., at the negative edge) and SignQ stays Low. The phase domain change from D2 to D1 is carried out by activating Freeze, and then, Clear to put v_{con} to zero and generating an appropriate Switch logics so that $v_{mod-I-2}$ is connected to $v_{mod-I-1}$ and $v_{mod-Q-2}$ is connected to $v_{mod-Q-1}$, respectively, as suggested in Fig. 6 (A). In any state, the current state is maintained without the event for state transition, in this example, the event that SignI falls.

[120] After phase domain change has been finished, the integration operation of the integrator resumes by deactivating the Clear logic, and then, deactivating the Freeze logic signal so that the path between the switch box and the vector modulator is recovered, that is, v_{mod-I} is connected to $v_{mod-I-2}$ and v_{mod-Q} is connected to $v_{mod-Q-2}$. Here, the time intervals of activation of Clear and Freeze logic signals should be appropriately chosen. In other words, they should be small enough not to harm continuous phase shifting as well as large enough to make sure safe phase domain change.

[121]

[122] Pseudosinusoidal waveform generator:

[123]

[124] One of the novelties of the invented method is provision of a means for generating the modulation signal pair (i.e., $v_{mod-I-1}$ (429) and $v_{mod-Q-1}$ (431)) which resembles the cosine and sine waveforms for a finite control signal range so that associated modulation signal switching and the vector modulation results in unlimited phase shifting capability. It is called the pseudosinusoidal waveform generator (denoted

PSEUDOSINUSOID GEN) (407) in this invention, and comprises the pseudocosine waveform generator (denoted PSEUDOCOS GEN) (409) and the pseudosine waveform generator (denoted PSEUDOSIN GEN) (411) as shown in Fig. 4. The waveform generator is implemented with CMOS circuit to exploit its area, power efficiency and high performance. By superimposing several waveform components, which are derived from a basic currentvoltage (IV) curve of the MOS differential amplifier pair, desired pseudosinusoidal waveforms can be synthesized for a desired control signal range.

[125]

[126] We consider a MOS differential amplifier pair using NMOS shown in Fig. 9 (A). This is called the basic differential amplifier pair in the invention. It is composed of two MOS's M1 (901), M2 (903) and a current source I_{SS} (905). The sources of M1 and M2 are tied together, and connected to the I_{SS}. Given the gate voltage V_{G1} (907), V_{G2} (909) and the drain current I_{D1} (911), I_{D2} (913) of M1 and M2, respectively, its transfer curve between the differential current output $\Delta I(v_{con})=I_{D1}-I_{D2}$ and the differential voltage input $v_{con}=V_{G1}-V_{G2}$ is given by

[127]

$$\Delta I(v_{con}) = \begin{cases} \frac{1}{2} K_n \left(\frac{W}{L}\right)_1 v_{con} \sqrt{\frac{4I_{SS}}{K_n \left(\frac{W}{L}\right)_1} - v_{con}^2}, & -V_Q \le v_{con} \le V_Q, \\ I_{SS}, & v_{con} \ge V_Q, \\ -I_{SS}, & v_{con} \le -V_Q \end{cases}$$

(7)

[128]

[129] where

$$V_Q = \sqrt{\frac{2I_{SS}}{K_n \left(\frac{W}{L}\right)_1}}$$

is the saturation voltage for the differential amplifier pair, and I_{SS} is the source bias current, K_n is the NMOS constant, and

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$

is the widthtolength ratio (or, aspect ratio) of M1 and M2. This is called the basic IV curve in this invention, and the basic IV curve (915) is plotted in Fig. 9 (B). Even though the embodiment is achieved using NMOS, an embodiment using PMOS is

equally possible under the same principle.

[130]

[131] If we look at the waveform (915), we can see that it resembles a portion of the true sine curve (i.e., 90 to 90 degrees interval) for $-V_Q \le v_{con} \le V_Q$. However, its mathematical form given in (7) is obviously different from the true sine curve. We may employ other devices for better approximation or may derive a better approximation to the true sine curve by manipulating the basic IV curve. One method to achieve a better approximation is shown in Fig. 10 (A). This method employs a plural number of the basic differential amplifier pair in parallel, and adjusts V_Q and I_{SS} values for each basic differential amplifier pair in order to synthesize a better approximation of the true sine waveform. In Fig. 10 (A), two basic differential amplifier pairs are employed for a typical example. Therefore, it is called the double differential amplifier pair in the invention. The first pair comprises M11 (1001), M21 (1003) and I_{SS1} (1009), and the second pair comprises M12 (1005), M22 (1007) and I_{SS2} (1011) with a constraint $I_{SS1}+I_{SS2}=I_{SS}$. Also, the gates of the corresponding MOS's (e.g., M11 and M12, M21 and M22) are tied together, and connected to the differential inputs V_{G1} and V_{G2}, and the drains of the corresponding MOS's (e.g., M11 and M12, M21 and M22) are tied together, and connected to the differential outputs I_{D1} and I_{D2}, respectively. In Fig. 10 (B), the IV curve for $\Delta I(v_{con})=I_{D1}-I_{D2}$ as a function of $v_{con}=V_{G1}-V_{G2}$ is plotted. As a result of optimization of the V_Q and I_{SS} values, the IV curve of the double differential amplifier pair (solid) (1013) is more close to the true sine waveform than that of the basic differential amplifier pair (dashed) (1015).

[132]

[133] Note that the above IV curves are symmetrical with respect to the origin. Besides the symmetrical IV curve, we need some offset versions to synthesize the desired pseudosinusoidal waveforms. The IV curve with input voltage offset can be implemented by adding some voltage shifting means on both input ports to the differential amplifier pair. The differential amplifier pair with the input voltage shifting means is called the extended differential amplifier pair in the invention. An example of the extended differential amplifier pair is shown in Fig. 11 (A). It is composed of a differential amplifier pair (basic in Fig. 9 (A) or double in Fig. 10 (A) or other substitute) (denoted DIFF AMP PAIR) (1101) and additional MOS's M3 (1103), M4 (1105) and current sources I_{SS3} (1107), I_{SS4} (1109). In this embodiment, the M3 and M4 are chosen as PMOS, which is the opposite type to the M1 and M2 in the differential amplifier pair considering a headroom problem related to the lower power supply voltage. Even though the embodiment is achieved using PMOS, an embodiment using NMOS is equally possible under the same principle.

[134]

[135] The combination of M3 and I_{SS3} (also, M4 and I_{SS4}) constitutes a source follower. The gatesource voltage drop V_{GS3} (1111) and V_{GS4} (1113) of M3 and M4 can be fixed to have some different values, respectively. Denoting the offset voltage $V_{OFF}=|V_{GS4}|-|V_{GS3}|$, the IV curve of the extended differential amplifier pair has a waveform which is offset in xaxis by V_{OFF} from the symmetrical IV curve of the original differential amplifier pair. This curve (1115) is plotted in Fig. 11 (B).

[136]

[137] The offset voltage can be adjusted by varying

$$\left(\frac{W}{L}\right)_3$$

and

$$\left(\frac{W}{L}\right)_4$$

of the two additional MOS's. Using the basic equation of MOS

$$|V_{GS3}|=V_{TH}+\sqrt{\frac{2I_{SS3}}{K_p\left(\frac{W}{L}\right)_3}}$$

and

$$|V_{GS4}|=V_{TH}+\sqrt{\frac{2I_{SS4}}{K_p\left(\frac{W}{L}\right)_4}}$$

, and assuming $I_{SS3}=I_{SS4}$, the offset voltage is expressed as

[138]

[139]

$$V_{OFF}=\sqrt{\frac{2I_{SS3}}{K_p}}\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_4}}-\frac{1}{\sqrt{\left(\frac{W}{L}\right)_3}}\right)$$

. (8)

[140]

[141] Here, V_{TH} and K_P are the threshold voltage and the PMOS constant, respectively. To obtain a voltage offset of a positive integer multiple of a reference voltage

$$V_P=\sqrt{\frac{2I_{SS3}}{K_p\left(\frac{W}{L}\right)_3}}$$

, let

[142]

[143] $$\left(\frac{W}{L}\right)_4 = \frac{1}{(N+1)^2}\left(\frac{W}{L}\right)_3$$

(9)

[144]

[145] for some N=1,2,3,…. Then, inserting (9) to (8), we get

[146]

[147] $V_{OFF} = NV_P$. (10)

[148]

[149] In summary, we can obtain a postive voltage offset version $\triangle I(V_{con}-NV_P)$, N=1,2,3,…, of the basic IV curve $\triangle I(V_{con})$ by implementing a CMOS circuit like Fig. 11 (A) with

$$\left(\frac{W}{L}\right)_4 = \frac{1}{(N+1)^2}\left(\frac{W}{L}\right)_3$$

with

$$V_P = \sqrt{\frac{2I_{ss3}}{K_p\left(\frac{W}{L}\right)_3}}$$

. Normally, V_P is fixed to have the same value as V_Q in (7). A negative voltage offset version $\triangle I(v_{con}+NV_P)$ can be obtained from $\triangle I(v_{con}-NV_P)$ by reversing $\triangle I(v_{con}-NV_P)$ with respect to yaxis to obtain $\triangle I(-v_{con}-NV_P)$, then reversing $\triangle I(-v_{con}-NV_P)$ with respect to xaxis to obtain $-\triangle I(-v_{con}-NV_P)$. Because $\triangle I(v_{con})$ is symmetrical with respect to the origin (i.e., $-\triangle I(-v_{con})=\triangle I(v_{con})$), we can see that the result of the two reversions is equal to $\triangle I(v_{con}+NV_P)$, which is the desired one. The reversions with respect to yaxis and xaxis can be easily achieved by just reversing the differential input voltage ports (V_{G3} and V_{G4}) and the differential ouput current branches (I_{D1} and I_{D2}) of the extended differential amplifier pair block, respectively.

[150]

[151] Now, we describe an embodiment of the functional blocks of the invented pseudo sinusoidal waveform generator using the CMOS circuit technology described above. The pseudo sinusoidal waveform generator generates $v_{mod-I-1}$ (501) and $v_{mod-Q-1}$ (503) as a function of the phase control signal v_{con} as indicated in Fig. 5 (A) and (B), respectively. The $v_{mod-I-1}$ and $v_{mod-Q-1}$ resemble the true cosine and sine waveforms in $-v_0 \le v_{con} \le v_0$, respectively. In order to implement the desired waveforms using circuit elements, they are redrawn in (1201) in Fig. 12 (A) and (1301) in Fig. 13 (A) with the xaxis and yaxis being scaled so that $v_0=V_P$ and $1=I_{SS}R_L$. Here, V_P and I_{SS} are defined in

the above, and R_L is a load resistance.

[152]

[153] Note that the waveform (1301) in Fig. 13 (A) is a bit different from that (503) in Fig. 5 (B). The reason why (1301) is used instead of (503) is to produce the pseudosine waveform as close to the true sine waveform as possible in the range of interest (i.e., $-v_0 \le v_{con} \le v_0$) in spite of mismatch between V_P and V_Q and irregularities of the basic IV curve of the transistor pair. Actually, the irregularities due to the secondary effect get more severe as the CMOS technology gets deeper into submicron. Of course, the same waveform such as (503) can be used for $v_{mod\text{-}Q\text{-}1}$ in (1301) if such mismatch and irregularities are negligible.

[154]

[155] The waveform for $v_{mod\text{-}I\text{-}1}$ (1201) as a function of v_{con} in Fig. 12 (A) can be synthesized by superimposing several waveforms (1203), (1205), (1207) shown in Fig. 12 (B), (C), (D). Note that the waveforms Fig. 12 (B)(D) are in the dimension of current, and the synthesized waveform Fig. 12 (A) is in the dimension of voltage. This means that the superposition is carried out by flowing the current waveforms through a common resistor R_L and measuring the voltage across the resistor. Also, differential current notations $\Delta I_a, \Delta I_b, \Delta I_c$ in the figures are used since a differential mode CMOS implementation is considered in this embodiment.

[156]

[157] The ΔI_a and ΔI_c in Fig. 12 (B) and (D) can be expressed in terms of the basic IV curve $\Delta I(v_{con})$ in (7) as $\Delta I_a = \Delta I(v_{con} + V_P)$ and $\Delta I_c = -\Delta I(v_{con} - V_P)$, respectively. The ΔI_b is realized simply by flowing a current

$-I_{SS}$

. Note that these current waveforms can be realized in CMOS circuit by using the technique discussed above. Then, the synthesized waveform for $v_{mod\text{-}i\text{-}1}$ as a function of v_{con} is obtained as the sum of the above waveforms multiplied by R_L. That is,

[158]

[159] $$v_{mod-I-1}(v_{con}) = \{\Delta I(v_{con} + V_P) - I_{SS} - \Delta I(v_{con} - V_P)\} \cdot R_L$$

. (11)

[160]

[161] In the same way, the waveform for $v_{mod\text{-}Q\text{-}1}$ (1301) as a function of v_{con} in Fig. 13 (A) can be synthesized by superimposing several waveforms (1303), (1305), (1307) shown in Fig. 13 (B), (C), (D). As mentioned above, the only waveform in Fig. 13 (C) would be enough to generate $v_{mod\text{-}Q\text{-}1}$ if the mismatch and irregularities mentioned above are negligible.

[162]

[163] The $\Delta I_a, \Delta I_b, \Delta I_c$ in Fig. 13 (B), (C), (D) can be expressed in terms of the basic IV curve $\Delta I(v_{con})$ in (7) as $\Delta I_a = -\Delta I(v_{con} + 2V_P)$, $\Delta I_b = \Delta I(v_{con})$ and $\Delta I_c = -\Delta I(v_{con} - 2V_P)$, respectively. Note that these current waveforms can be realized in CMOS circuit by using the technique discussed above. Then, the synthesized waveform for $v_{mod\text{-}Q\text{-}1}$ as a function of v_{con} is obtained as the sum of the above waveforms multiplied by R_L. That is,

[164]

[165] $$v_{mod-Q-1}(v_{con}) = \{-\Delta I(v_{con} + 2V_P) + \Delta I(v_{con}) - \Delta I(v_{con} - 2V_P)\} \cdot R_L$$

. (12)

[166]

[167] Based on the previous description, the desired pseudocosine waveform for $v_{mod\text{-}i\text{-}1}$ (1201) in Fig. 12 (A) can be generated according to the block diagram in Fig. 14. The extended differential amplifier pair blocks B1 (1401), B2 (1403) (see Fig. 11 (A) for details of each block) are arranged so that whose V_{OFF} values are adjusted to V_P, V_P, respectively. Fixing

$$\left(\frac{W}{L}\right)_3$$

of the first MOS (M3 in Fig. 11 (A)), the values of

$$\left(\frac{W}{L}\right)_4$$

of the second MOS (M4 in Fig. 11 (A)) for each extended differential amplifier pair block are chosen as

$$\frac{1}{4}\left(\frac{W}{L}\right)_3$$

,

$$\frac{1}{4}\left(\frac{W}{L}\right)_3$$

, respectively, to achieve required V_{OFF} values according to (9) and (10). Here, a constant current source I_{SS} (1405) is added to Node2 (1421) to provide the necessary waveform element $\Delta I_b = -I_{SS}$ as shown in Fig. 12 (C). The differential input voltage ports and the differential output current branches are arranged to achieve appropriate polarities in the expression of (11). The differential output current branches are connected to a common resistor pair R_L (1415) and R_L (1417) so that the proper superposition can take place. As a result, the desired pseudocosine waveform for $v_{mod\text{-}I\text{-}1}$ (1411) as a function of v_{con} (1409) is generated between Node1 (1419) and Node2 (1421).

[168]

[169] In the same way, the whole block diagram for generating $v_{mod-Q-1}$ (1301) is shown in Fig. 15. The extended differential amplifier pair blocks B1 (1501), B2 (1503), B3 (1505) (see Fig. 11 (A) for details of each block) are arranged so that whose V_{OFF} values are adjusted to $2V_P$, 0, $2V_P$ respectively. Fixing

$$\left(\frac{W}{L}\right)_3$$

of the first MOS (M3 in Fig. 11 (A)), the values of

$$\left(\frac{W}{L}\right)_4$$

of the second MOS (M4 in Fig. 11 (A)) for each extended differential amplifier pair block are chosen as

$$\frac{1}{9}\left(\frac{W}{L}\right)_3$$

,

$$\left(\frac{W}{L}\right)_3$$

,

$$\frac{1}{9}\left(\frac{W}{L}\right)_3$$

, respectively, to achieve required V_{OFF} values according to (9) and (10). The differential input voltage ports and the differential output current branches are arranged to achieve appropriate polarities in the expression of (12). The differential output current branches are connected to a common resistor pair R_L (1511) and R_L (1513) so that the proper superposition can take place. As a result, the desired pseudosine waveform for $v_{mod-Q-1}$ (1509) as a function of v_{con} (1507) is generated between Node1 (1515) and Node2 (1517).

[170]

[171] Miscellaneous blocks:

[172]

[173] The sample and hold block (417) can be implemented using MOS switches (M1 (1601), M2 (1603), M3 (1605), M4 (1607)) and capacitors (C1 (1609), C2 (1611), C3 (1613), C4 (1615)) as depicted in Fig. 16. It is provided to avoid glitches in the output signal during phase domain change. When the Freeze signal is the logic Low, the MOS switches are turned on so that the differential input signals $v_{mod-I-2}$ (433) and $v_{mod-Q-2}$ (435) are transferred to the differential output signals as v_{mod-I} (437) and v_{mod-Q} (439), respectively. On the contrary, while the Freeze signal (449) is the logic High, the MOS

switches are turned off so that the differential output signals keep the recently sampled values in the capacitors in spite of possible glitches in input signals during phase domain change.

[174]

[175] The IQ splitter (401) can be implemented using MOS (M1 (1713), M2 (1715)) and RC phase delaying components as depicted in Fig. 17. When R_1 (1703) (1705) and C_1 (1701) (1707) are tuned so that

$$2\pi f_c = \frac{1}{R_1 C_1}$$

where f_c is the center frequency of the RF input sinusoid v_{in} (419), the RC network operates as a 90 degrees phase splitter at f_c. As a result, when a differential input signal v_{in} is applied to gates of M1M2 pair, the voltage difference generated between Node1 and Node2 becomes the inphase RF input signal v_{in-I} (421), and the voltage difference generated between Node3 and Node4 becomes the quadrature RF input signal v_{in-Q} (423), respectively, with respect to v_{in}. To minimize the effect of a parasitic capacitance, we put buffers (1717) (1719) at the output stage.

[176]

[177] The vector modulator (403) can be implemented using two Gilbert cells (1801) (1803) and an external combining circuit (1809) as depicted in Fig. 18. A quadrature pair of RF input signal (v_{in-I} (421) and v_{in-Q} (423)) and a quadrature pair of the modulation signal (v_{mod-I} (437) and v_{mod-Q} (439)) are provided to the vector modulator. By the operation of each Gilbert cell, the current differences $\Delta I_{12}=I_1-I_2$ and $\Delta I_{34}=I_3-I_4$ at the output ports of Gilbert cells are expressed as $\Delta I_{12}=A_0 v_{in-Q} v_{mod-I}$ and $\Delta I_{34}=A_0 v_{in-I} v_{mod-Q}$ with some constant A_0. The two currents are combined and converted to a voltage through the load resistor (1805) (1807) to give a differential output voltage waveform v_{out} (425) as

[178]

[179] $$v_{out}(t) = v_{in-Q}(t) \cdot v_{\mathrm{mod}-I}(v_{con}) + v_{in-I}(t) \cdot v_{\mathrm{mod}-Q}(v_{con})$$

(13)

[180]

[181] As a result, $v_{out}(t)$ becomes the phaseshifted version of $v_{in}(t)$ (419) as much as commanded by v_{con} (427) as described in the previous section.

[182]

[183] Phase shifting of digital signals:

[184]

[185] Until now, the explanation of the invention was made with assumption that the input signal is an analogue signal. However, the same idea disclosed in the invention can be

applied to the phase shifting of digital signals as well. The vector modulationbased VCPS (denoted VMVCPS) for analogue input signals shown in Fig. 4 was composed of an IQ splitter, a modulation signal generator and a vector modulator. Because of the analogue signal nature, the IQ splitter was realized through RC phase delaying components as shown in Fig. 17. The digital version of the VMVCPS would be composed of an IQ splitter, a modulation signal generator and a vector modulator as well. However, although the modulation signal generator is the same as in the analogue signal case, the IQ splitter and the vector modulator should be modified reflecting the digital signal nature.

[186]

[187] For example, the splitted IQ signal pair (v_{in-I} , v_{in-Q}) can be obtained by using two divideby2 digital logic circuits which are triggered by the rising and falling edges of the input signal, respectively. At the same time, the modulation signal generator generates the modulation signal pair (v_{mod-I}, v_{mod-Q}). The (v_{in-I} , v_{in-Q}) and (v_{mod-I}, v_{mod-Q}) are vector modulated in the vector modulator in a way suitable for digital signals, and generates the desired phaseshifted version of the input signal. The details are omitted, but it should be recognized that the same idea disclosed in the invention can be applied to the phase shifting of digital signals as well.

[188]

[189] Another embodiment example:

[190]

[191] Another embodiment example of the invention is shown in Fig. 19. In the same way as the first embodiment example in Fig. 4, this second embodiment example employs a IQ splitter (1901), a vector modulator (1903) and a modulation signal generator (1905). This second embodiment example makes a difference from the first one by employing a pseudosinusoid generator (1907) with phase shift range of 720 degrees (i.e., $-\varphi_0 \le \varphi(v_{con}) \le \varphi_0$, $\varphi_0 = 360^\circ$) whereas the first one assumed a pseudosinusoid generator with phase shift range of 360 degrees or less than 360 degrees. Although the finite VCPS is not existent explicitly in the block diagram, the implicit VCPS which could be derived from the pseudosinusoid with a finite phase shifting characteristic is called the finite VCPS in this invention. In fact, the finite VCPS resulting from the pseudosinusoid of the first embodiment example was assumed to have phase shift range of 180 degrees (i.e., $-\varphi_0 \le \varphi(v_{con}) \le \varphi_0$, $\varphi_0 = 90^\circ$). The fact that the finite VCPS has phase range of 720 degrees brings about a convenience that the switch box (415) and associated Switch1 (445), Switch2 (447) signals in Fig. 4 are no longer needed. This is because we can cover the whole phase range with single phase domain D1 (-360° to 360°), and the same pseudosinusoid can be used as the next phase domain signal as it is when the phase domain change takes place.

[192]

[193] The necessary pseudosinusoids (i.e. modulation signals) according to the second embodiment example is shown in Fig. 20 (A) and (B). The modulation signals v_{mod-I} (2001) and v_{mod-Q} (2003) in Fig. 20 (A) and (B) resemble the true sine and cosine curve in the region $-v_0 \le v_{con} \le v_0$. The resultant transfer curve (2005) of the finite VCPS is shown in Fig. 20 (C). As v_{con} varies from $-v_0$ to v_0, $\varphi(v_{con})$ varies from -360° to 360°. Therefore, the finite VCPS is called 720 degrees VCPS. Note that if v_{con} is reset to 0 when v_{con} reaches either boundary values (v_0 or $-v_0$), the modulation signals can continue their sinusoidal waveforms without need of waveform switching. This makes a contract to the first embodiment example which needed waveform switching through the switch box (415) in Fig. 4.

[194]

[195] The control block (denoted CONTROL) (305) in Fig. 3 operates as a digital logic circuit to control the operation of the circular VCPS. It takes Sign (319) (i.e., SignI (1941) and SignQ (1943)) from the zero crossing detector (1913) as logic inputs, and generates Clear (321) and Freeze (315), and applies them to the integrator (307) and the VMVCPS (303), respectively. The major aim of the control block is to make a smooth switching of the phase domain when v_{con} reaches either boundary values (v_0 or $-v_0$) so that the phase shifting can be achieved in a perfectly circular manner.

[196]

[197] When v_{con} reaches v_0 or $-v_0$, let v_0, the control block resets the integrator so that v_{con} goes back to zero and the next phase domain transfer curve can be effective. For this purpose, a zero crossing detector is provided which detects the zero crossing points of either v_{mod-I} or v_{mod-Q} and applies corresponding logic states, SignI and SignQ, to the control block. The control block decides an appropriate firing instant based on the logic states.

[198]

[199] The firing instant should occur when v_{con} reaches v_0 so that v_{mod-Q} (2103) crosses a zero point from negative to positive values (so, SignQ (2107) goes from Low to High) while v_{mod-I} (2101) remains positive (so, SignI (2105) remains High) (see (e) in Fig. 21 (B)), or when v_{con} reaches $-v_0$ so that v_{mod-Q} crosses the zero point from positive to negative values while v_{mod-I} remains positive (see (a) in Fig. 21 (B)). However, the problem is that this happens not only when v_{con} reaches v_0 or $-v_0$, but also when v_{con} reaches 0 (see (c) in Fig. 21 (B)). This is inevitable as far as 720 degrees VCPS is employed. Therefore, we need a means to make sure that a proper firing can occur only when v_{con} reaches v_0 or $-v_0$.

[200]

[201] For that purpose, we divide v_{con} range into three regions: Retarding ($-v_0 \le v_{con} \le -v_0/2$

so $-360^{\circ} \le \varphi \le -180^{\circ}$), Normal ($-v_0/2 \le v_{con} \le v_0/2$ so $-180^{\circ} \le \varphi \le 180^{\circ}$) and Advancing ($v_0 \le v_{con} \le v_0$ so $180^{\circ} \le \varphi \le 360^{\circ}$) regions. Defining the two logic variables representing a particular state at certain moment, we can implement a finite state machine which takes SignI and SignQ as input, and generates Clear and Freeze as output together with an appropriate state transition. Their waveforms as a function of v_{con} are shown in Fig. 21 (C)(H). Its state transition diagram is shown in Fig. 22.

[202]

[203] On the power on (2201), the state goes to Normal. In Normal state (2203), if SignI is Low and a positive edge of SignQ takes place, where v_{con} starts to be less than $-v_0/2$ (see (b) in Fig. 21 (B)), the state changes to Retarding. If SignI is Low and a negative edge of SignQ happens, where v_{con} starts to be greater than $v_0/2$ (see (d) in Fig. 21 (B)), the state changes to Advancing. Otherwise, it keeps the previous state.

[204]

[205] In Advancing state (2205), the state changes to Normal at the positive edge of SignQ while SignI remains High where v_{con} starts to be greater than v_0 (see (e) in Fig. 21 (B)). At the same time, the finite state machine activates Freeze and Clear successively so that the phase domain switching can be achieved smoothly. Also, the state changes to Normal at the positive edge of SignQ while SignI remains Low where v_{con} starts to be less than $v_0/2$ (see (d) in Fig. 21 (B)). No output is generated from the control block in this case. Otherwise, it keeps the previous state.

[206]

[207] In Retarding state (2207), the state changes to Normal at the negative edge of SignQ while SignI remains High where v_{con} starts to be less than $-v_0$ (see (a) in Fig. 21 (B)). At the same time, the finite state machine activates Freeze and Clear successively so that the phase domain switching can be achieved smoothly. Also, the state changes to Normal at the negative edge of SignQ while SignI remains Low where v_{con} starts to be greater than $-v_0/2$ (see (b) in Fig. 21 (B)). No output is generated from the control block in this case. Otherwise, it keeps the previous state.

[208]

[209] By the way, to avoid possible glitches which may occur during phase domain switching process, a clutching means is introduced between the modulation signal generator (1905) and the vector modulator (1903) (see Fig. 19). The sample and hold (denoted S/H) (1917) plays the role of the clutch. The sample and hold samples and holds the $v_{mod\text{-}I\text{-}1}$ (1929) and $v_{mod\text{-}Q\text{-}1}$ (1931) inputs to generate the freezed $v_{mod\text{-}I}$ (1937) and $v_{mod\text{-}Q}$ (1939) outputs while the Freeze (1949) is active (i.e., High). Otherwise, $v_{mod\text{-}I\text{-}1}$ and $v_{mod\text{-}Q\text{-}1}$ are passed to the vector modulator as they are.

[210]

[211] When v_{con} reaches v_0 or $-v_0$, the phase domain switching happens. At the time, the

control block activates Clear and Freeze signals as indicated in Fig. 21 (E) and (F), respectively, and applies the Freeze signal to the sample and hold block. As a result, the v_{mod-I} and v_{mod-Q} inputs to the vector modulator, which are the values of $v_{mod-I-1}$ and $v_{mod-Q-1}$ samples just before the freezing, are prevented from being disturbed in spite of possible glitches during the activated period of Clear.

[212]

[213] In the similar way to the first embodiment example in Fig. 12 and 13, the pseudosinusoids can be generated by manipulating the basic IV curve of the differential MOS amplifier pair as shown in Fig. 23 and Fig. 24.

[214]

[215] Denoting ΔI_c in Fig. 24 (D) as a basic IV curve $\Delta I(v_{con})$, other IV curves are expressed as $\Delta I_a = \Delta I(v_{con}+4V_P)$ (see Fig. 24 (B)), $\Delta I_b = -\Delta I(v_{con}+2V_P)$ (see Fig. 24 (C)), $\Delta I_d = -\Delta I(v_{con}-2V_P)$ (see Fig. 24 (E)) and $\Delta I_e = \Delta I(v_{con}-4V_P)$ (see Fig. 24 (F)), respectively. Then, the waveform for $v_{mod-Q-1}$ in Fig. 24 (A) as a function of v_{con} can be synthesized as the sum of the above waveforms multiplied by R_L. That is,

[216]

[217]
$$v_{mod-Q-1}(v_{con}) = \{\Delta I(v_{con}+4V_P) - \Delta I(v_{con}+2V_P) + \Delta I(v_{con}) - \Delta I(v_{con}-2V_P) + \Delta I(v_{con}-4V_P)\} \cdot R_L$$

(14)

[218]

[219] In the same way, the waveform for $v_{mod-I-1}$ in Fig. 23 (A) as a function of v_{con} can be synthesized as

[220]

[221]
$$v_{mod-I-1}(v_{con}) = \{\Delta I(v_{con}+5V_P) - \Delta I(v_{con}+3V_P) + \Delta I(v_{con}+V_P) - I_{SS} - \Delta I(v_{con}-V_P) + \Delta I(v_{con}-3V_P) - \Delta I(v_{con}-5V_P)\} \cdot R_L.$$

(15)

[222]

[223] Based on the previous description, the whole block diagram for generating $v_{mod-Q-1}$ in Fig. 24 (A) is shown in Fig. 26. The extended differential amplifier pair blocks B1 (2601), B2 (2603), B3 (2605), B4 (2607), B5 (2609) (see Fig. 11 (A) for details of each block) are arranged so that whose V_{OFF} values are adjusted to $4V_P$,$2V_P$,0,$2V_P$,$4V_P$, respectively. Fixing

$$\left(\frac{W}{L}\right)_3$$

of the first (reference) MOS (M3 in Fig. 11 (A)), the values of

$\left(\frac{W}{L}\right)_4$

of the second MOS (M4 in Fig. 11 (A)) for each extended differential amplifier pair block are chosen as

$$\frac{1}{25}\left(\frac{W}{L}\right)_3,\ \frac{1}{9}\left(\frac{W}{L}\right)_3,\ \left(\frac{W}{L}\right)_3,\ \frac{1}{9}\left(\frac{W}{L}\right)_3,\ \frac{1}{25}\left(\frac{W}{L}\right)_3$$

, respectively, to achieve required V_{OFF} values according to (9) and (10). The differential input voltage ports and the differential output current branches are arranged to achieve appropriate polarities in the expression of (14). The differential output current branches are connected to a common resistor pair R_L (2611) and R_L (2613) so that the proper superposition can take place. As a result, the desired pseudosine waveform $V_{mod-Q-1}$ (2621) as a function of v_{con} (2619) is generated between Node 1 (2615) and Node 2 (2617).

[224]

[225] In the same way, the desired waveform for $V_{mod-I-1}$ in Fig. 23 (A) is generated according to the block diagram in Fig. 25. The differential amplifier blocks B1 (2501), B2 (2503), B3 (2505), B4 (2507), B5 (2509), B6 (2511) (see Fig. 11 (A) for details of each block) are arranged so that whose V_{OFF} values are adjusted to $5V_P$,$3V_P$,V_P,V_P,$3V_P$,$5V_P$, respectively. Fixing

$\left(\frac{W}{L}\right)_3$

of the first (reference) MOS (M3 in Fig. 11 (A)), the values of

$\left(\frac{W}{L}\right)_4$

of the second MOS (M4 in Fig. 11 (A)) for each differential amplifier block are chosen as

$$\frac{1}{36}\left(\frac{W}{L}\right)_3,\ \frac{1}{16}\left(\frac{W}{L}\right)_3,\ \frac{1}{4}\left(\frac{W}{L}\right)_3,\ \frac{1}{4}\left(\frac{W}{L}\right)_3,\ \frac{1}{16}\left(\frac{W}{L}\right)_3,\ \frac{1}{36}\left(\frac{W}{L}\right)_3$$

, respectively, to achieve required V_{OFF} values according to (9) and (10). Here, a constant current source I_{SS} (2513) is added to Node 2 (2523) to provide the necessary waveform element $\Delta I_d = -I_{SS}$ as shown in Fig. 23 (E). The differential input voltage ports and the differential output current branches are arranged to achieve appropriate polarities in the expression of (15). The differential output current branches are connected to a common resistor pair R_L (2517) and R_L (2519) so that the proper superposition can take place. As a result, the desired pseudocosine waveform $v_{mod-I-1}$ (2527) as a function of v_{con} (2525) is generated between Node 1 (2521) and Node 2 (2523).

[226]

[227] Simulation results:

[228]

[229] To check the phase shifting performance, we applied a RF sinusoidal signal v_{in} (309) and a constant phase control error signal v_{err} (323) with a positive value to the invented VCFS as shown in Fig. 3. This means phase control signal v_{con} (313) should be linearly increasing with respect to the time (i.e., $v_{con}(t)=K_1 \cdot t$ ($K_1>0$)) due to the operation of the integrator (307). Because the phase control signal increases linearly with respect to the time, the phase shifting should be taking place in proportion to the time elapsed as well. The simulated waveforms for v_{mod-I} (437) and v_{mod-Q} (439) (not $v_{mod-I-1}$ and $v_{mod-Q-1}$) as a function of time (μsec) are shown in Fig. 27 (A) in a solid line and a dashed line, respectively. We can see that the desired pseudosinusoidal waveforms are generated as the time elapses so as to achieve the necessary phase shifting. When either v_{mod-I} or v_{mod-Q} crosses zero, the phase domain change takes place with clearing the integrator output. This process repeats and the whole phase domains from D1 to D4 are covered. The ovals in Fig. 27 (A) indicate the phase domain change period.

[230]

[231] The phase shifting and amplitude of the output signal v_{out} (311), which are determined by

$$\tan^{-1}(v_{mod-Q}/v_{mod-I})$$

and

$$\sqrt{v_{mod-I}^2+v_{mod-Q}^2}$$

, are plotted in Fig. 27 (B) and (C), respectively. From the plot, we can see that the unlimited phase shifting is achieved in a circular way (except during the phase domain change period), and the phase shifting is almost linear in the normal intervals. The maximum phase deviation from the linear slope due to the nonideality of the pseudosinusoids is measured to be 3.5 degrees. At the same time, the maximum amplitude deviation ratio from the constant envelope is measured to be 2.2 percent. These values are regarded as small enough to demonstrate effectiveness of the invented circular VCPS.

[232] Although a few exemplary embodiments of the present general inventive concept have been shown and described, it will be appreciated by those skilled in the art that changes may be made in these exemplary embodiments without departing from the principles and spirit of the general inventive concept, the scope of which is defined in the appended claims and their equivalents.

Claims

[1] A voltage-controlled phase shifter (VCPS) with an input sinusoid, an output sinusoid and a phase control signal input, the voltage controlled phase shifter comprising :
a vector modulation-based VCPS configured to generate a continuously phaseshifted version of an input sinusoid in accordance to a phase control signal;
a control block configured to receive necessary information signals including a Sign signal and to generate necessary control signals including a Switch signal, a Clear signal and a Freeze signal; and
a reset block configured to pass said phase control signal to said vector modulationbased VCPS in normal operation and to reset its output to zero in accordance to said clear signal from said control block.

[2] A voltage-controlled frequency shifter (VCFS) with an input sinusoid, an output sinusoid and a frequency control signal input, the voltage controlled frequency shifter comprising:
a VCPS in accordance to Claim 1 wherein said reset block in said VCPS is replaced by said integrator outside said VCPS;
a integrator is configured to store phase information and to dump its output to zero when a clear signal is activated from said control block in Claim 1 as well as to integrate said frequency control signal.

[3] The voltage-controlled phase shifter (VCPS) in accordance to Claim 1 further comprising:
a IQ splitter configured to split the phase of said input sinusoid into a quadrature sinusoid pair of said input sinusoid;
a modulation signal generator configured to generate a pseudo-sinusoidal modulation signal pair in an analogue circuit as a function of said phase control signal input; and
a vector modulator configured to modulate said a quadrature sinusoid pair of said input sinusoid by said a pseudo-sinusoidal modulation signal pair in order to generate a phaseshifted version of said input sinusoid.

[4] The voltage controlled phase shifter (VCPS) in accordance to Claim 3 further comprising:
a pseudo-sinusoidal waveform generation means configured to generate the first intermediate pseudo-sinusoidal modulation signal pair as a function of said phase control signal input with a finite range;
a switching means configured to switch said first intermediate pseudo-sinusoidal modulation signal pair to generate the second pseudo-sinusoidal modulation

signal pair so that said second pseudo-sinusoidal modulation signal pair suits the required phase domain;

a clutching means configured to pass said second pseudo-sinusoidal modulation signal pair in normal operation and to provide a temporary modulation signal pair during the phase domain change period in order to achieve a seamless phase shifting; and

a threshold detection means configured to detect a threshold point at which phase domain change must take place, and to generate a logic level to said control block;

[5] The voltage controlled phase shifter (VCPS) in accordance to Claim 4, wherein the clutching means realized as a sample and hold block configured to pass said modulation signal pair while operating within a phase domain, and to sample and hold said modulation signal pair in a phase domain change period according to a Freeze signal activated from said control block in Claim 1, in order to achieve smooth phase domain changeover.

[6] The voltage controlled phase shifter (VCPS) in accordance to Claim 4, wherein the threshold detection means realized as a zero crossing detector configured to detect a zero crossing point of either of said modulation signal pair and to generate a Sign signal, and apply it to said control block in Claim 1.

[7] The voltage controlled phase shifter (VCPS) in accordance to Claim 1, wherein the control block comprising a finite state machine configured to receive phase domain change information like a Sign signal from said threshold detection means in Claim 4, and to change its state in an appropriate way, and to generate necessary control signals like a Switch signal, a Clear signal, and a Freeze signal, and to apply them to said switching means in said Claim 4, to said reset block in Claim 1, and said clutching means in Claim 4, respectively.

[8] A modulation signal generator configured to generate a pseudo-sinusoidal waveform pair as a function of a phase control control signal in such a way that:

first, the first intermediate pseudo-sinusoidal modulation signal waveforms are generated as a function of said phase control signal within a finite range between an lower and upper boundary points.

second, as soon as said phase control signal crosses over either said lower or uppper boundary point, said first intermediate pseudo-sinusoidal modulation signal waveforms are switched to the second intermediate pseudo-sinusoidal modulation signal waveforms, and said phase control signal is reset to zero (phase domain change) so that the second intermediate pseudo-sinusoidal modulation signal waveforms are continuously connected to the previous second intermediate pseudo-sinusoidal modulation signal waveforms as the phase

control signal varies.

third, said second intermediate pseudo-sinusoidal modulation signal waveforms are passed to the final pseudo-sinusoidal waveform pair when said phase control signal is within said lower and upper boundary points, and sampled and holded while said first intermediate pseudo-sinusoidal modulation signal waveforms are in the process of switching.

[9] A modulation signal generator in accordance to Claim 8 configured to have a fintie number of phase domains which overlap with neighbouring phase domains, and said phase domain change is configured so that the phase shifting has a hysterisis characteristic as a function of said phase control signal.

[10] A modulation signal generator comprising:

a pseudo-sinusoidal waveform generator configured to generate the first intermediate pseudo-sinusoidal modulation signal pair as a function of said phase control signal input within a finite range;

a switch box configured to switch said first intermediate pseudo-sinusoidal modulation signal pair to generate the second pseudo-sinusoidal modulation signal pair so that said second pseudo-sinusoidal modulation signal pair suits the required phase domain, according to a Switch signal activated from a control block;

a sample and hold block configured to pass said second pseudo-sinusoidal modulation signal pair while operating within a phase domain, and to sample and hold said second pseudo-sinusoidal modulation signal pair in a phase domain change period, and to generate a final pseudo-sinusoidal modulation signal pair, according to a Freeze signal activated from a control block;

a zero crossing detector configured to detect a zero crossing point of either of said first pseudo-sinusoidal modulation signal pair and to generate a logic signal Sign, and apply it to a control block; and

a control block comprising a finite state machine configured to receive phase domain change information like a Sign signal from said zero crossing detector and to change its state in an appropriate way, and to generate necessary control signals like a Switch signal, a Clear signal, and a Freeze signal, and to apply them to said switch box, to an outer reset block, and said sample and hold block, respectively.

[11] The modulation signal generator in accordance to Claim 10 configured without said switch box provided that said second intermediate pseudo-sinusoidal modulation signal pair is identical to said first intermediate pseudo-sinusoidal modulation signal pair.

[12] The modulation signal generator in accordance to Claim 10, wherein the pseudo-

sinusoidal waveform generator comprises inphase modulation signal generator and quadraturephase modulation signal generator is configured to generate a pseudo-cosine and pseudo-sine modulation signal pair as a function of said phase control signal input for a finite input range.

[13] The modulation signal generator in accordance to Claim 12, wherein the pseudo-sine waveform (odd function) is synthesized by superimposing multiple copies of a basic waveform, where said basic waveform takes the form of pseudo-sine curve in a finite input range, and said copy may be a shifted version in x-axis and/or reversed version in y-axis and/or x-axis of said basic waveform.

[14] The modulation signal generator in accordance to Claim 12, wherein the pseudo-cosine waveform (even function) is synthesized by superimposing multiple copies of a basic waveform and some constant value, where said basic waveform takes the form of quasisine curve in a finite input range, and said copy may be a shifted version in x-axis and/or reversed version in y-axis and/or x-axis of said basic waveform.

[15] The modulation signal generator in Claim 13 and Claim 14, wherein the basic waveform is obtained from the I-V curve (output current vs. input voltage transfer curve) of a transistor pair (e.g., MOS or BJT or any similar devices) in order to achieve an approximation to the true sine waveform, and said copy in Claim 13 and Claim 14 is obtained by shifting input voltage level and/or reversing input voltage ports and/or output current branches of said transistor or transistor pair.

[16] The modulation signal generator in Claim 13 and Claim 14, wherein the basic waveform is obtained from the I-V curve (output current vs. input voltage transfer curve) of a plural number of said transistor pairs in Claim 16 in parallel in order to achieve a better approximation to the true sine waveform.

[17] The modulation signal generator in Claim 13 and Claim 14, wherein basic waveform is obtained from the I-V curve (output current vs. input voltage transfer curve) of a plural number of said transistor pairs in Claim 15 in parallel in order to achieve an approximation to any required waveform.

[18] The modulation signal generator in Claim 15, wherein the shifting input voltage level of said transistor or transistor pair is achieved by an appropriate adjustment of W/L (width to length ratio) and a bias current of said MOS according to a way exploiting the dependency of the gate-source voltage of the MOS on the inverse-root of W/L and the dependency on the root of the bias current as described in the body or any other similar way for other devices.

[19] The modulation signal generator in accordance to Claim 3, further comprising: a pseudo-sinusoidal waveform generation means configured to generate the first

intermediate pseudo-sinusoidal modulation signal pair for a finite input range which spans two periods of the sine waveform as a function of said phase control signal input;

a clutching means configured to pass said first pseudo-sinusoidal modulation signal pair in normal operation and to provide a temporary modulation signal pair during the phase domain change period in order to achieve a seamless phase shifting; and

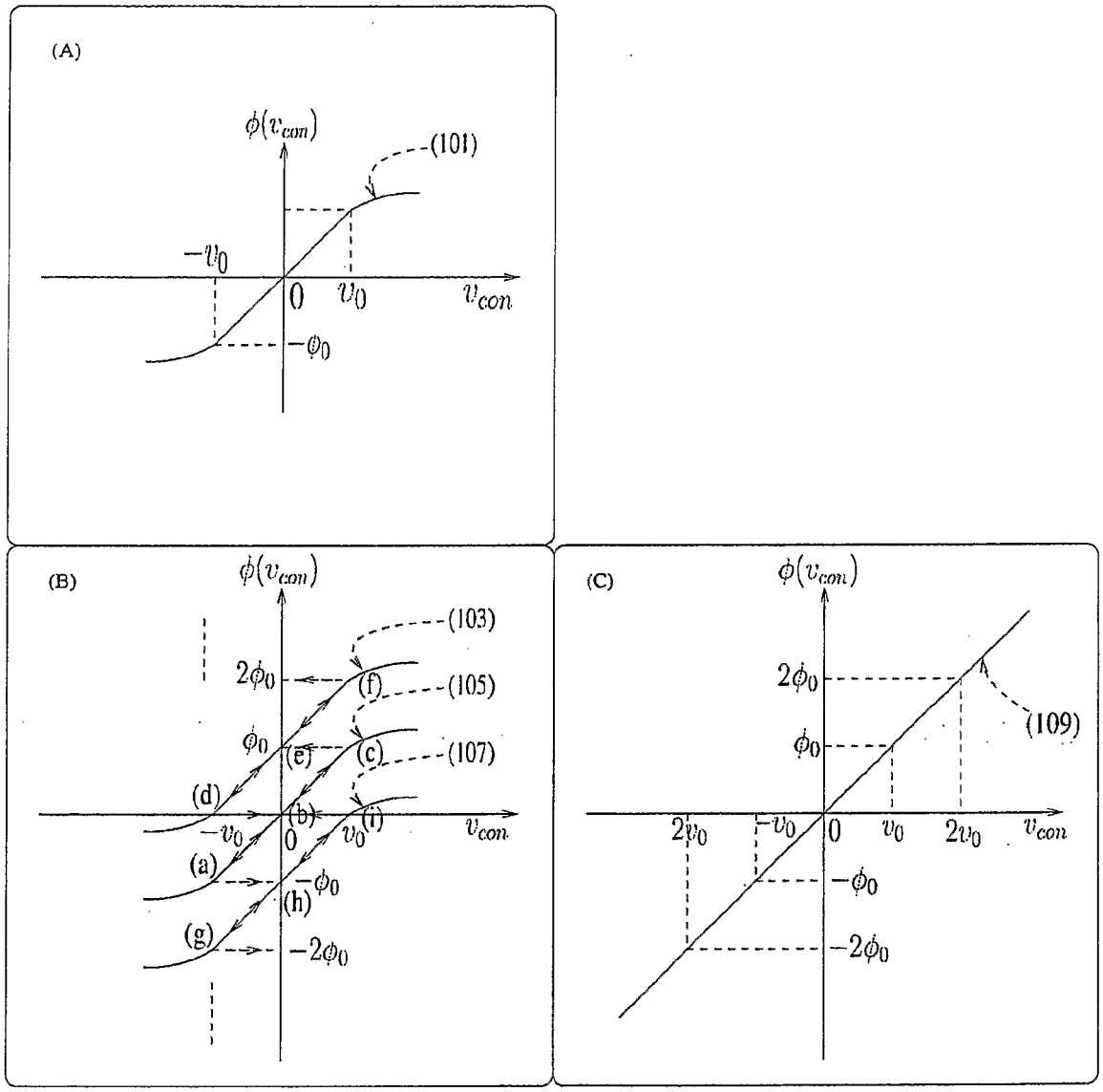
a threshold detection means configured to detect a threshold point at which phase domain change must take place, and to generate a logic level to said control block.

[20] The modulation signal generator in accordance to Claim 19, wherein the pseudo-sinusoidal waveform generation means is configured to generate;

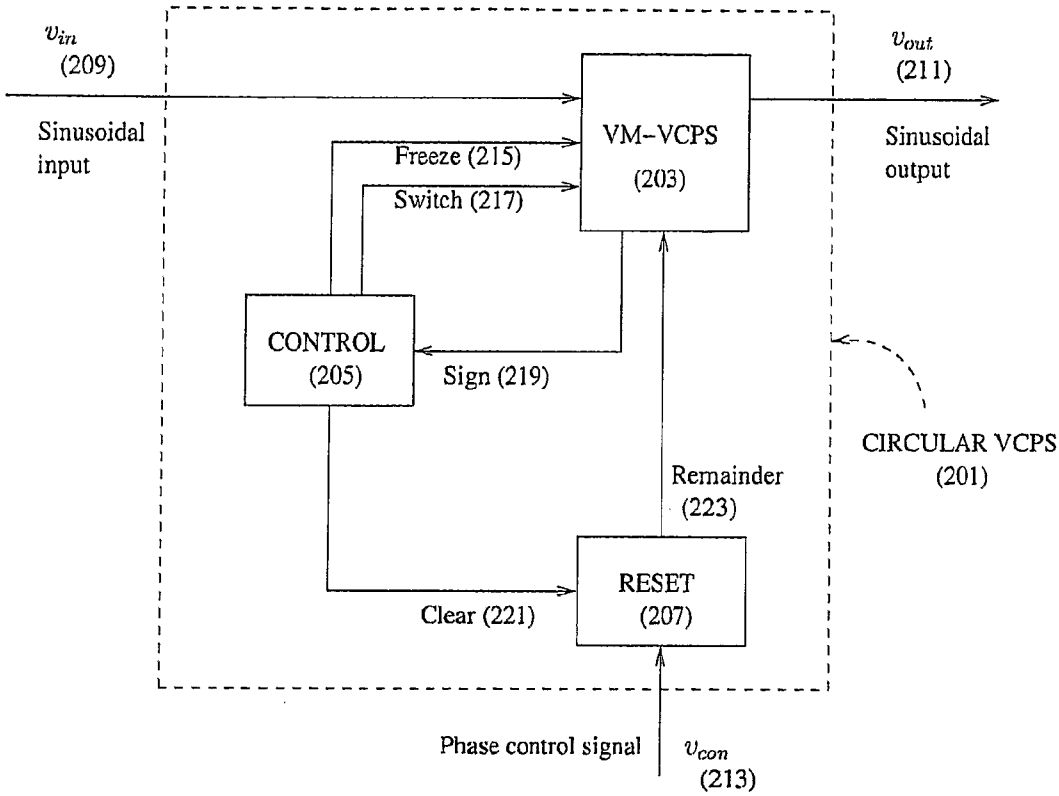
A pseudo-sinusoidal waveform pair for 720 degrees range according to a phase control signal input; and

said control block in accordance to Claim 1 is configured to make phase domain change only when said control signal input reaches either limit values whose phase shifts correspond to 360 degrees and -360 degrees, respectively.

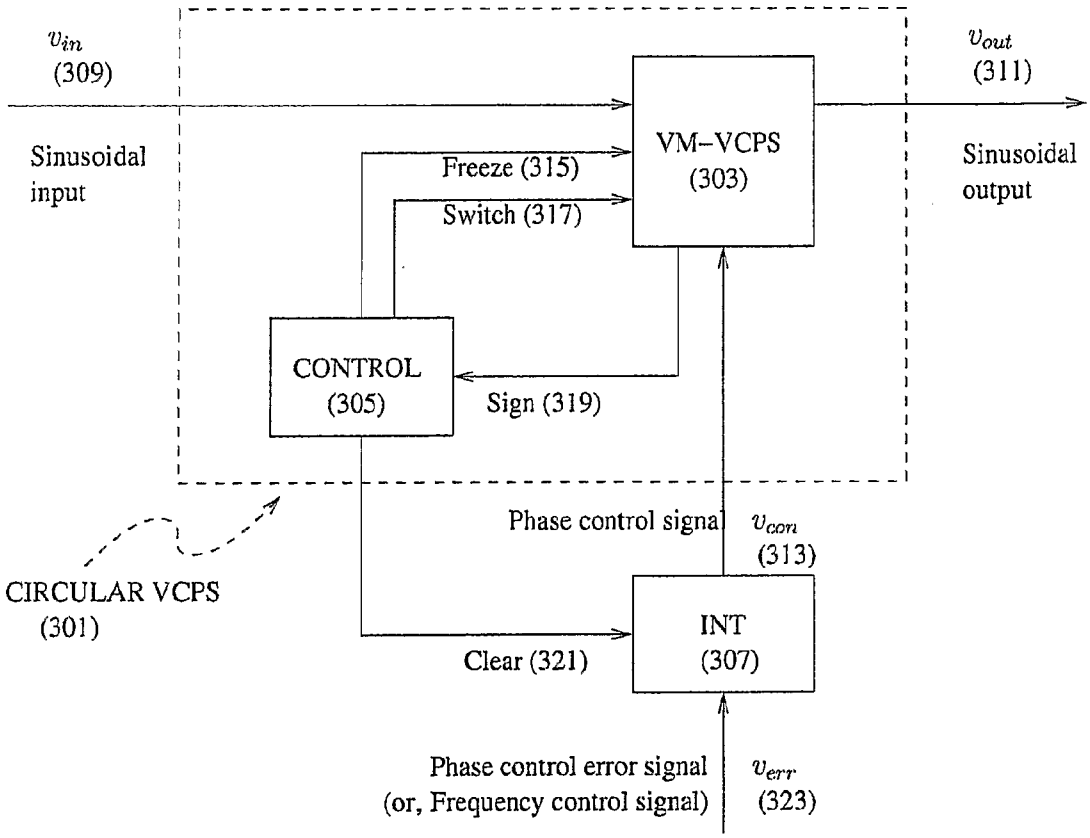
[Fig. 1]


(A)
$\phi(v_{con})$
(101)
$-v_0$
0
v_0
v_{con}
$-\phi_0$
(B)
$\phi(v_{con})$
(103)
$2\phi_0$
(f)
(105)
ϕ_0
(e)
(c)
(107)
(d)
(b)
(i)
$-v_0$
0
v_0
v_{con}
(a)
$-\phi_0$
(h)
(g)
$-2\phi_0$
(C)
$\phi(v_{con})$
$2\phi_0$
(109)
ϕ_0
$2v_0$
$-v_0$
0
v_0
$2v_0$
v_{con}
$-\phi_0$
$-2\phi_0$

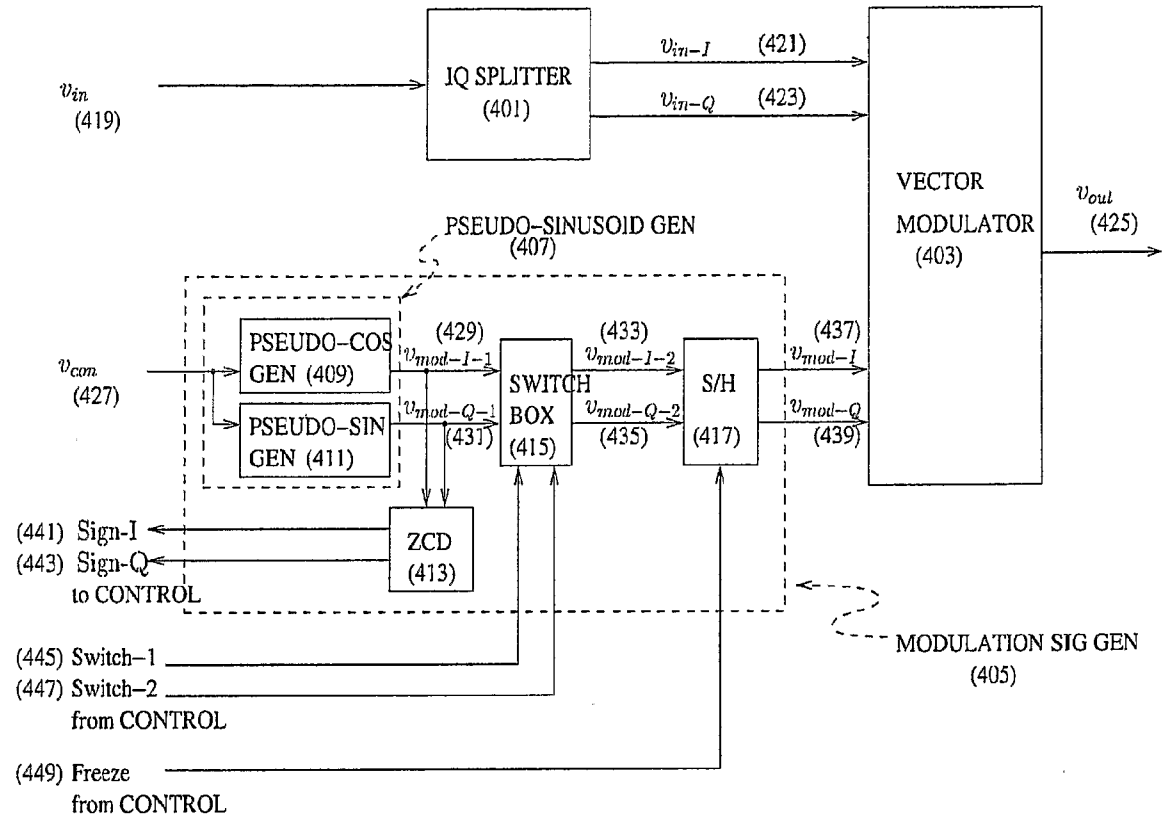
[Fig. 2]


v_{in}
(209)
Sinusoidal
input
v_{out}
(211)
Sinusoidal
output
VM-VCPS
(203)
Freeze (215)
Switch (217)
CONTROL
(205)
Sign (219)
CIRCULAR VCPS
(201)
Remainder
(223)
RESET
(207)
Clear (221)
Phase control signal
v_{con}
(213)

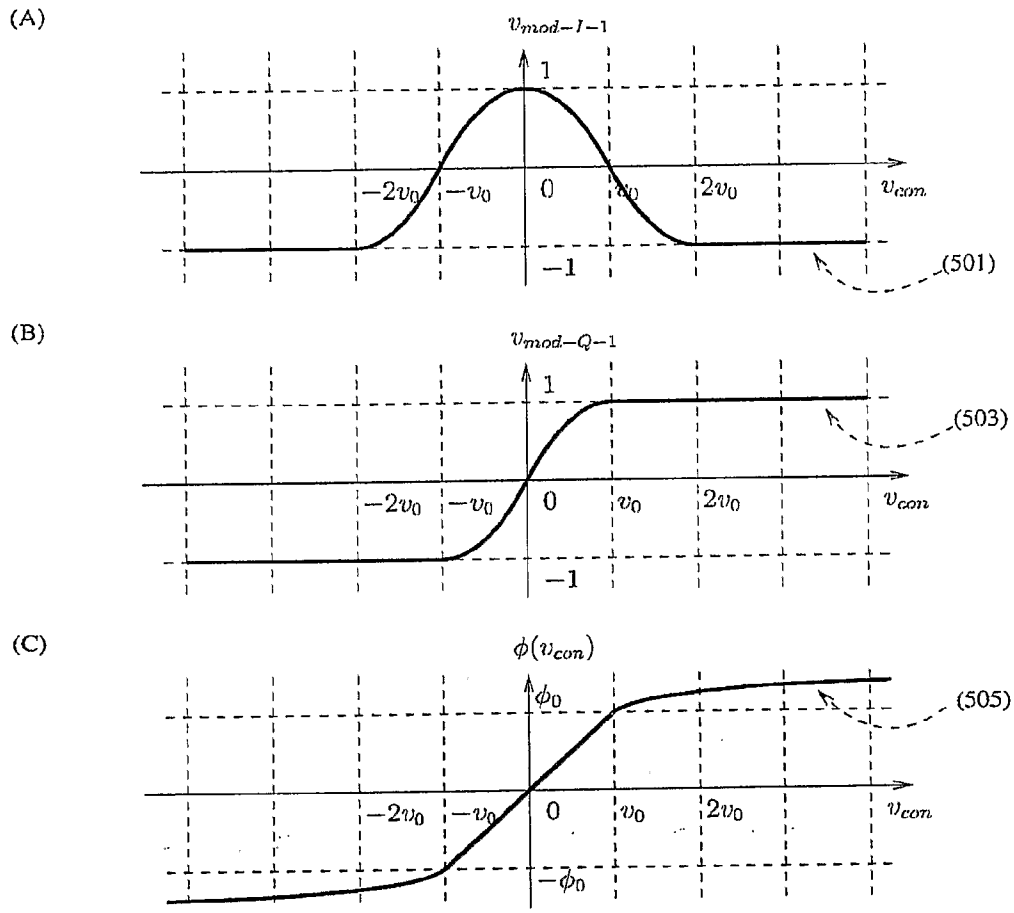
[Fig. 3]


v_{in}
(309)
Sinusoidal
input
v_{out}
(311)
Sinusoidal
output
VM-VCPS
(303)
Freeze (315)
Switch (317)
CONTROL
(305)
Sign (319)
Phase control signal
v_{con}
(313)
CIRCULAR VCPS
(301)
INT
(307)
Clear (321)
Phase control error signal
(or, Frequency control signal)
v_{err}
(323)

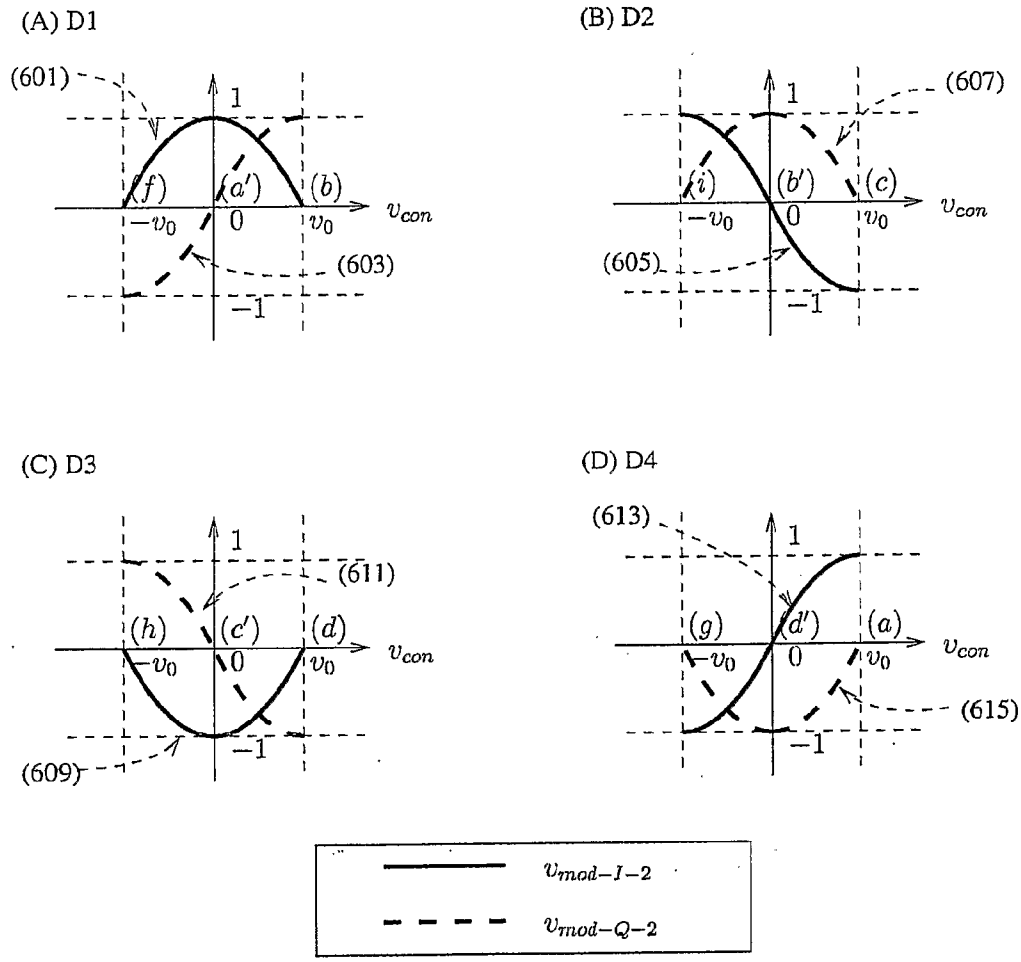
[Fig. 4]


v_{in}
(419)
IQ SPLITTER
(401)
v_{in-I} (421)
v_{in-Q} (423)
VECTOR
MODULATOR
(403)
v_{out}
(425)
PSEUDO-SINUSOID GEN
(407)
v_{com}
(427)
PSEUDO-COS
GEN (409)
PSEUDO-SIN
GEN (411)
(429)
$v_{mod-I-1}$
$v_{mod-Q-1}$
(431)
SWITCH
BOX
(415)
(433)
$v_{mod-I-2}$
$v_{mod-Q-2}$
(435)
S/H
(417)
(437)
v_{mod-I}
v_{mod-Q}
(439)
ZCD
(413)
(441) Sign-I
(443) Sign-Q
to CONTROL
MODULATION SIG GEN
(405)
(445) Switch-1
(447) Switch-2
from CONTROL
(449) Freeze
from CONTROL

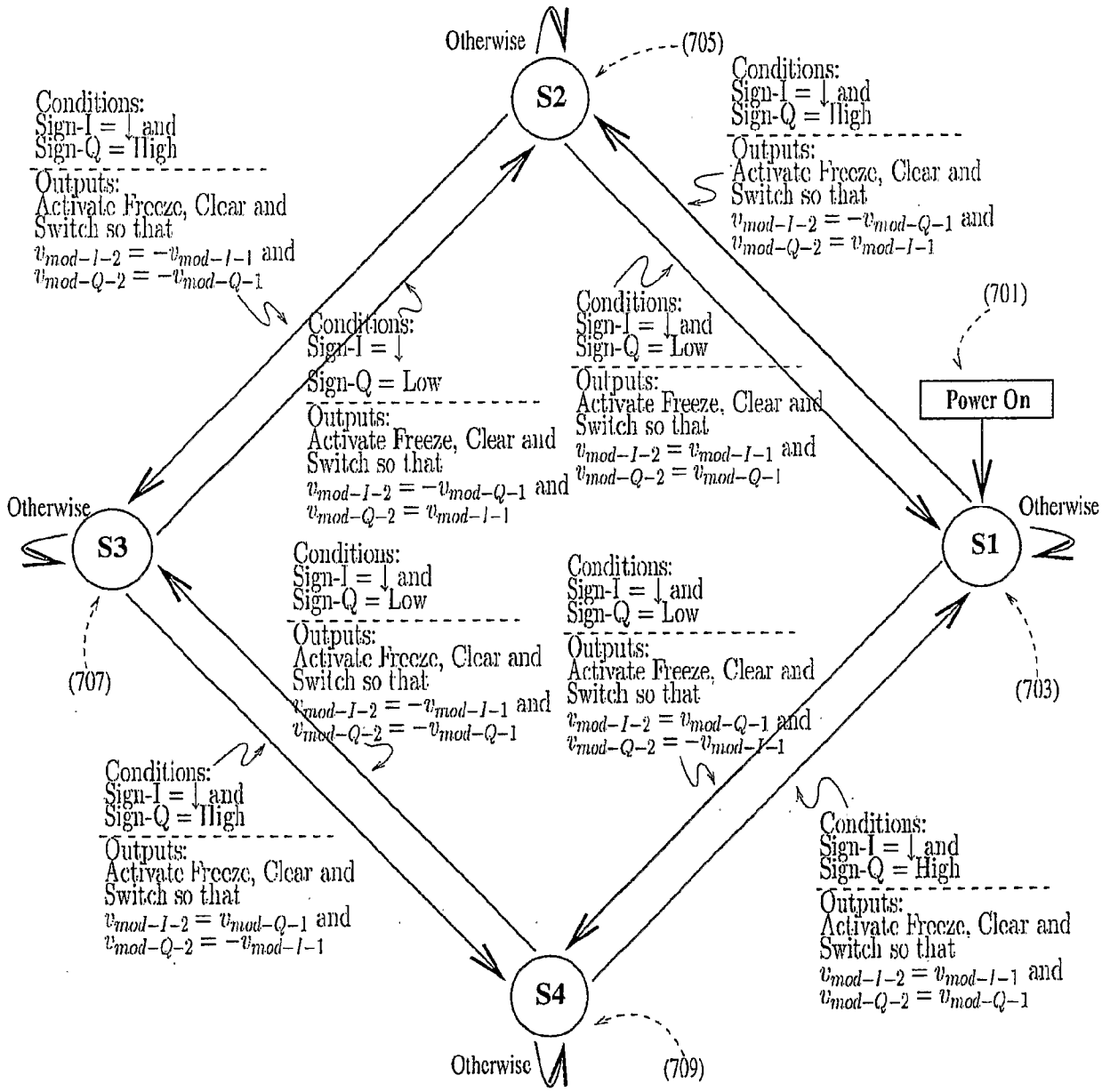
[Fig. 5]


(A)
$v_{mod-I-1}$
1
$-2v_0$
$-v_0$
0
v_0
$2v_0$
v_{con}
-1
(501)
(B)
$v_{mod-Q-1}$
1
(503)
$-2v_0$
$-v_0$
0
v_0
$2v_0$
v_{con}
-1
(C)
$\phi(v_{con})$
ϕ_0
(505)
$-2v_0$
$-v_0$
0
v_0
$2v_0$
v_{con}
$-\phi_0$

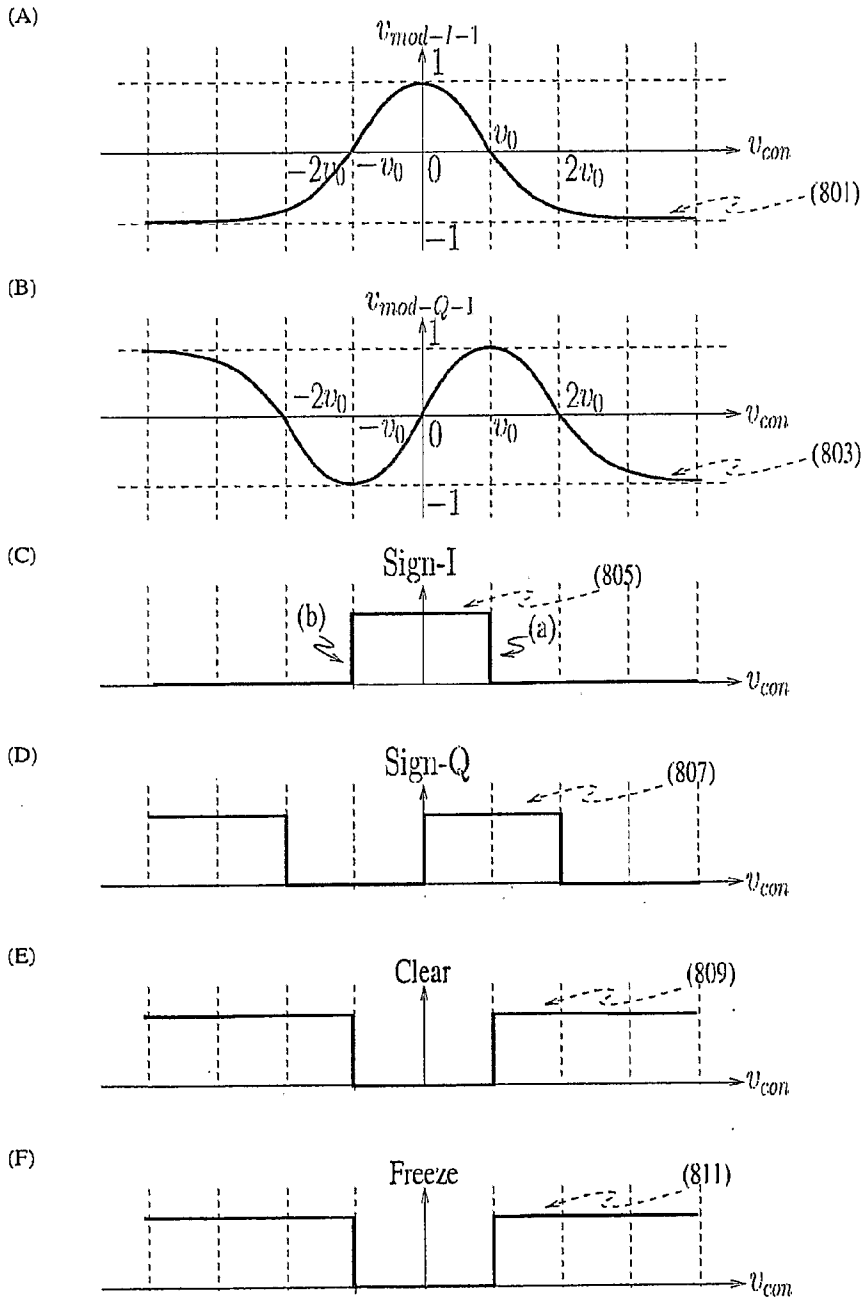
[Fig. 6]


(A) D1
(601)
1
(f)
(a')
(b)
$-v_0$
0
v_0
v_{con}
(603)
−1
(B) D2
(607)
1
(i)
(b')
(c)
$-v_0$
0
v_0
v_{con}
(605)
−1
(C) D3
1
(611)
(h)
(c')
(d)
$-v_0$
0
v_0
v_{con}
(609)
−1
(D) D4
(613)
1
(g)
(d')
(a)
$-v_0$
0
v_0
v_{con}
(615)
−1
$v_{mod-I-2}$
$v_{mod-Q-2}$

[Fig. 7]

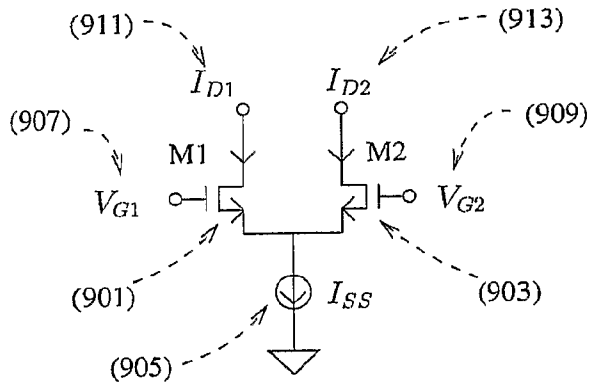

Otherwise
(705)
S2
Conditions:
Sign-I = ↓ and
Sign-Q = High
Outputs:
Activate Freeze, Clear and
Switch so that
$v_{mod-I-2} = -v_{mod-Q-1}$ and
$v_{mod-Q-2} = v_{mod-I-1}$
Conditions:
Sign-I = ↓ and
Sign-Q = High
Outputs:
Activate Freeze, Clear and
Switch so that
$v_{mod-I-2} = -v_{mod-I-1}$ and
$v_{mod-Q-2} = -v_{mod-Q-1}$
Conditions:
Sign-I = ↓
Sign-Q = Low
Outputs:
Activate Freeze, Clear and
Switch so that
$v_{mod-I-2} = -v_{mod-Q-1}$ and
$v_{mod-Q-2} = v_{mod-I-1}$
Conditions:
Sign-I = ↓ and
Sign-Q = Low
Outputs:
Activate Freeze, Clear and
Switch so that
$v_{mod-I-2} = v_{mod-I-1}$ and
$v_{mod-Q-2} = v_{mod-Q-1}$
(701)
Power On
Otherwise
S3
S1
Otherwise
(707)
(703)
Conditions:
Sign-I = ↓ and
Sign-Q = Low
Outputs:
Activate Freeze, Clear and
Switch so that
$v_{mod-I-2} = -v_{mod-I-1}$ and
$v_{mod-Q-2} = -v_{mod-Q-1}$
Conditions:
Sign-I = ↓ and
Sign-Q = Low
Outputs:
Activate Freeze, Clear and
Switch so that
$v_{mod-I-2} = v_{mod-Q-1}$ and
$v_{mod-Q-2} = -v_{mod-I-1}$
Conditions:
Sign-I = ↓ and
Sign-Q = High
Outputs:
Activate Freeze, Clear and
Switch so that
$v_{mod-I-2} = v_{mod-Q-1}$ and
$v_{mod-Q-2} = -v_{mod-I-1}$
Conditions:
Sign-I = ↓ and
Sign-Q = High
Outputs:
Activate Freeze, Clear and
Switch so that
$v_{mod-I-2} = v_{mod-I-1}$ and
$v_{mod-Q-2} = v_{mod-Q-1}$
S4
Otherwise
(709)

[Fig. 8]

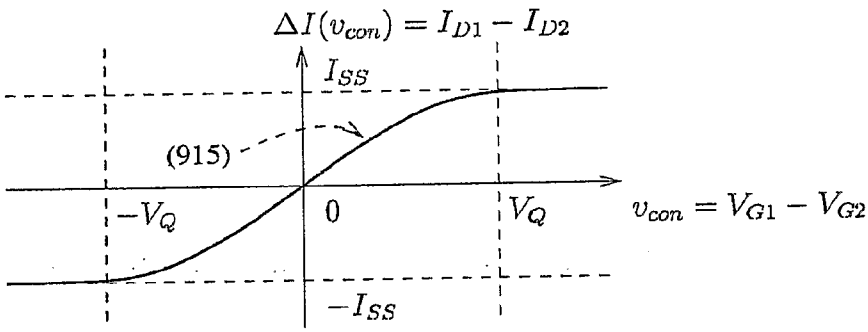

(A)
$v_{mod-I-1}$
1
v_0
v_{con}
$-2v_0$
$-v_0$
0
$2v_0$
(801)
-1
(B)
$v_{mod-Q-1}$
1
$-2v_0$
$2v_0$
v_{con}
$-v_0$
0
v_0
(803)
-1
(C)
Sign-I
(805)
(b)
(a)
v_{con}
(D)
Sign-Q
(807)
v_{con}
(E)
Clear
(809)
v_{con}
(F)
Freeze
(811)
v_{con}

[Fig. 9]

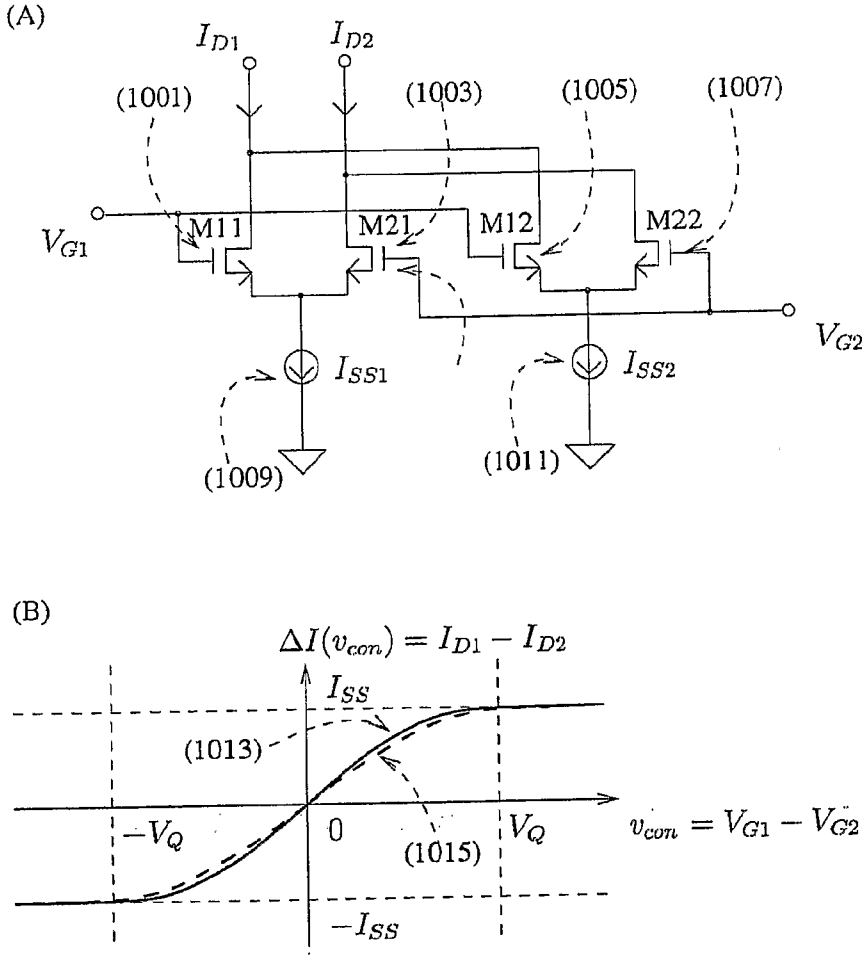
(A)


(911)
(913)
I_{D1}
I_{D2}
(907)
(909)
M1
M2
V_{G1}
V_{G2}
(901)
(903)
I_{SS}
(905)

(B)

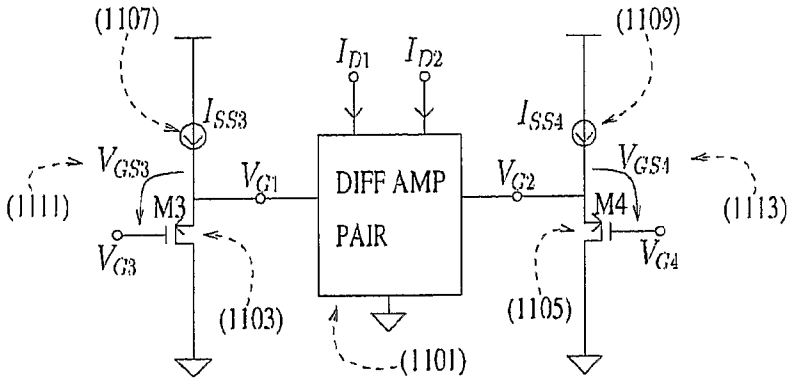

$\Delta I(v_{con}) = I_{D1} - I_{D2}$
I_{SS}
(915)
$-V_Q$
0
V_Q
$v_{con} = V_{G1} - V_{G2}$
$-I_{SS}$

[Fig. 10]

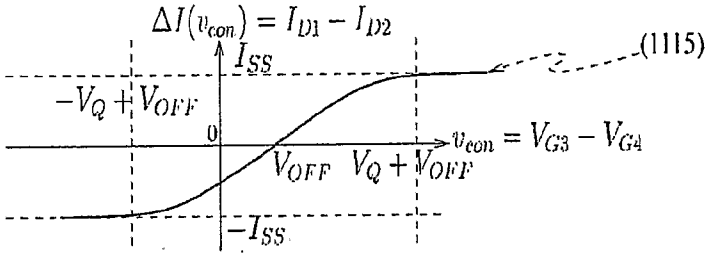

(A)
I_{D1}
I_{D2}
(1001)
(1003)
(1005)
(1007)
V_{G1}
M11
M21
M12
M22
V_{G2}
I_{SS1}
I_{SS2}
(1009)
(1011)
(B)
$\Delta I(v_{con}) = I_{D1} - I_{D2}$
I_{SS}
(1013)
$-V_Q$
0
(1015)
V_Q
$v_{con} = V_{G1} - V_{G2}$
$-I_{SS}$

[Fig. 11]

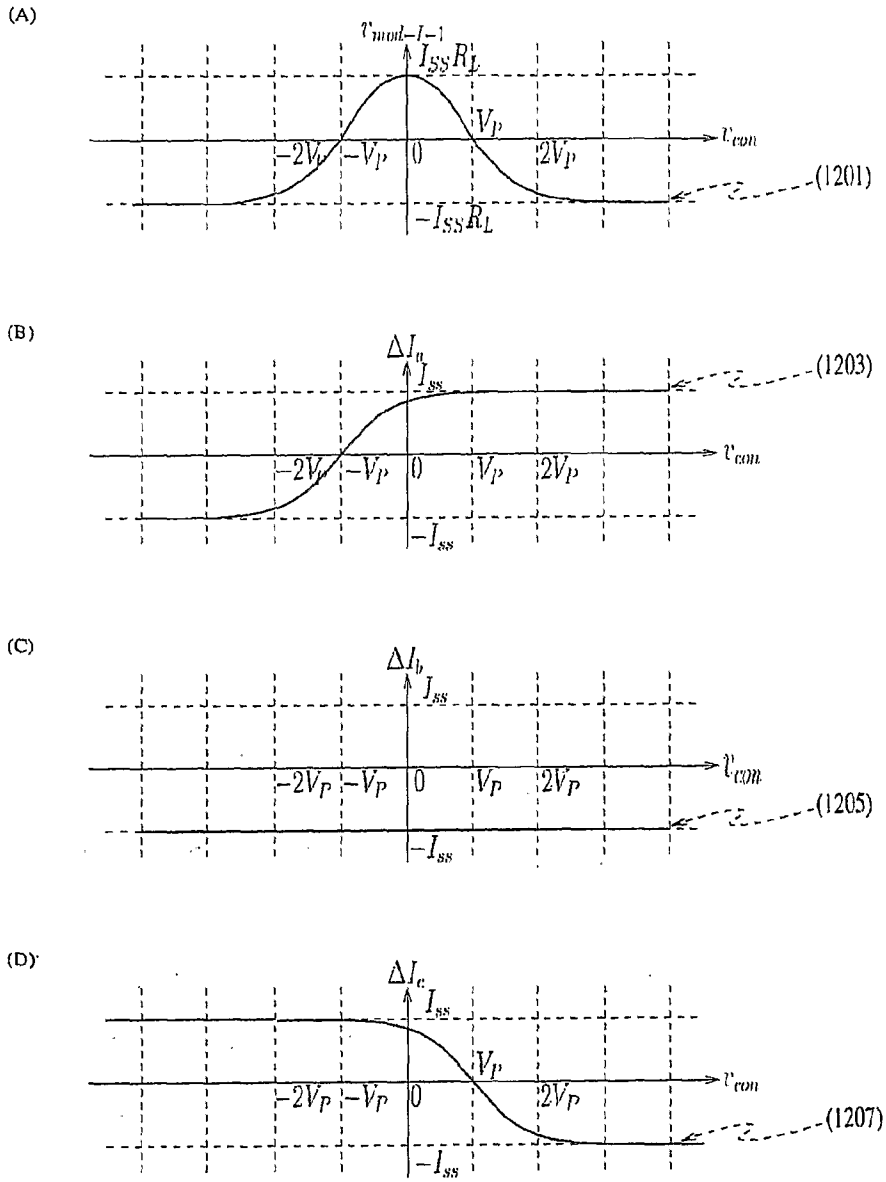
(A)


(1107)
I_{D1}
I_{D2}
(1109)
I_{SS3}
I_{SS4}
V_{GS3}
V_{G1}
DIFF AMP
PAIR
V_{G2}
V_{GS4}
(1111)
M3
M4
(1113)
V_{G3}
V_{G4}
(1103)
(1105)
(1101)

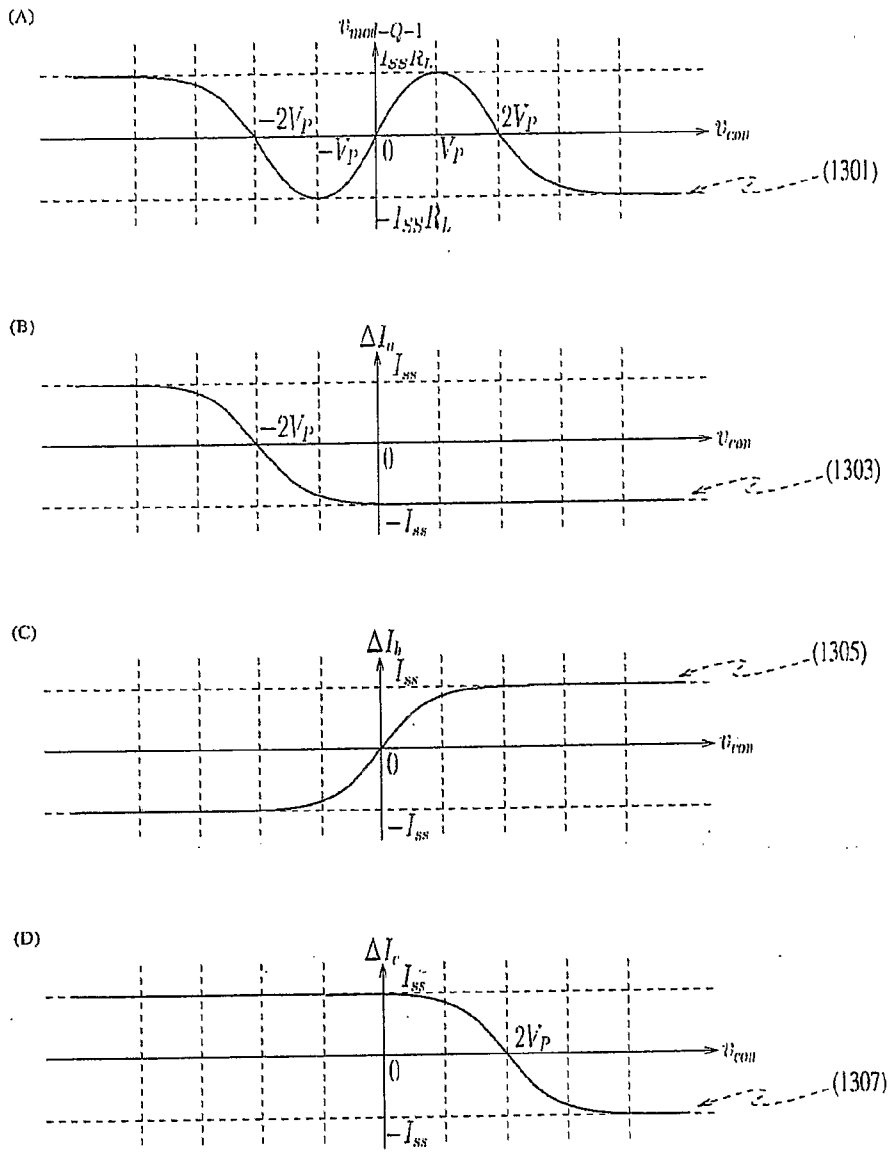
(B)


$\Delta I(v_{con}) = I_{D1} - I_{D2}$
(1115)
I_{SS}
$-V_Q + V_{OFF}$
0
$v_{con} = V_{G3} - V_{G4}$
V_{OFF}
$V_Q + V_{OFF}$
$-I_{SS}$

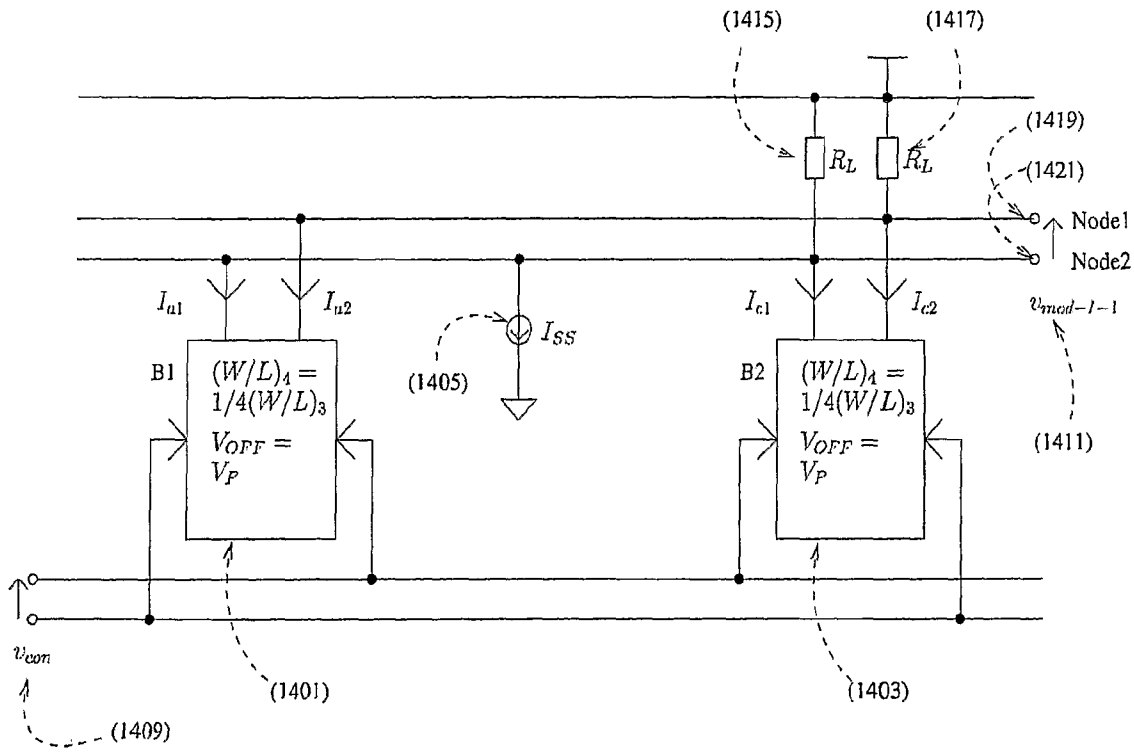
[Fig. 12]


(A)
$v_{mod-I-1}$
$I_{SS}R_L$
V_P
v_{con}
$-2V_P$
$-V_P$
0
$2V_P$
(1201)
$-I_{SS}R_L$
(B)
ΔI_a
I_{ss}
(1203)
v_{con}
$-2V_P$
$-V_P$
0
V_P
$2V_P$
$-I_{ss}$
(C)
ΔI_b
I_{ss}
v_{con}
$-2V_P$
$-V_P$
0
V_P
$2V_P$
(1205)
$-I_{ss}$
(D)
ΔI_c
I_{ss}
V_P
v_{con}
$-2V_P$
$-V_P$
0
$2V_P$
(1207)
$-I_{ss}$

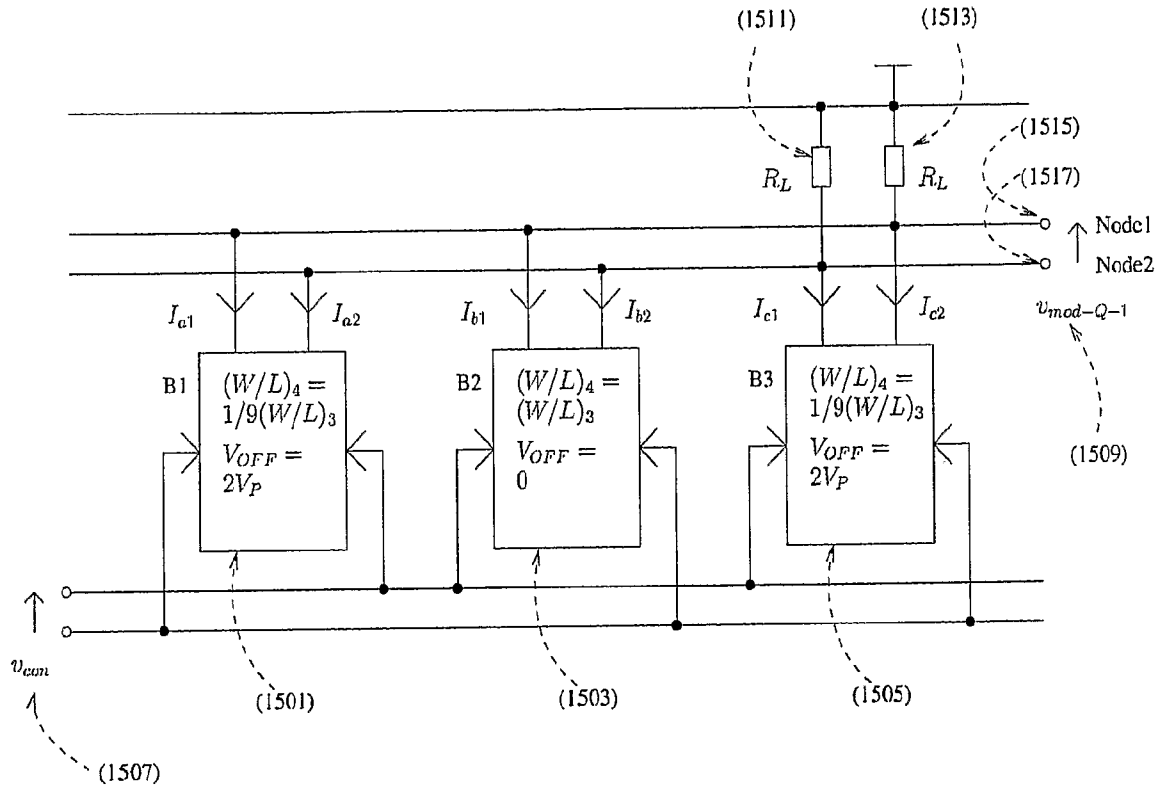
[Fig. 13]


(A)
$v_{mod-Q-1}$
$I_{SS}R_L$
$-2V_P$
$-V_P$
0
V_P
$2V_P$
v_{con}
(1301)
$-I_{SS}R_L$
(B)
ΔI_a
I_{ss}
$-2V_P$
0
v_{con}
(1303)
$-I_{ss}$
(C)
ΔI_b
I_{ss}
(1305)
0
v_{con}
$-I_{ss}$
(D)
ΔI_c
I_{ss}
$2V_P$
0
v_{con}
(1307)
$-I_{ss}$

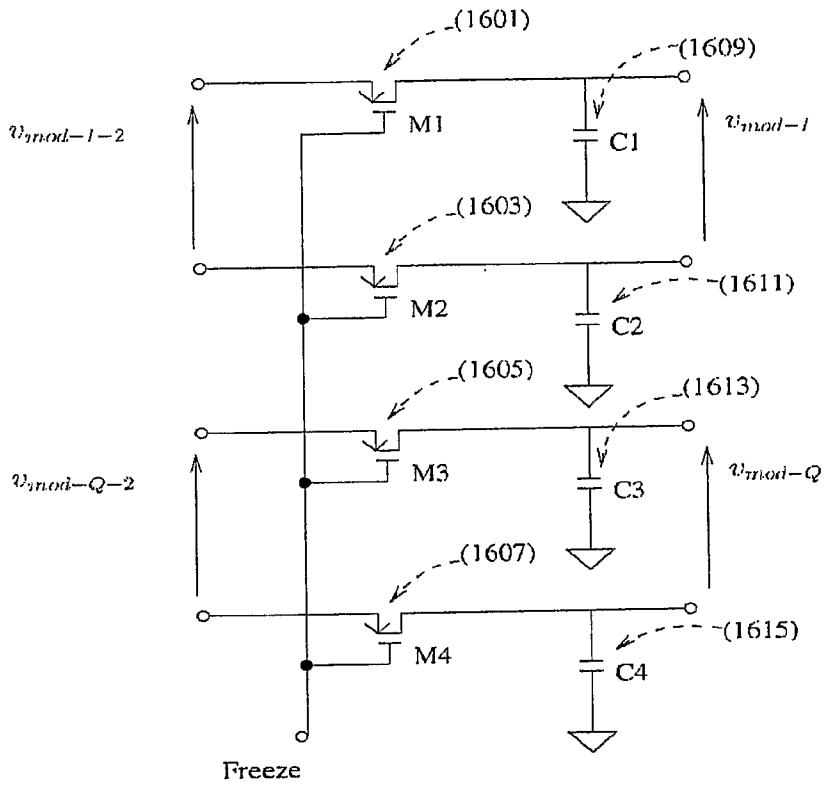
[Fig. 14]


(1415)
(1417)
(1419)
(1421)
R_L
R_L
Node1
Node2
I_{a1}
I_{a2}
I_{SS}
I_{c1}
I_{c2}
$v_{mod-1-1}$
B1
$(W/L)_1 = 1/4(W/L)_3$
$V_{OFF} = V_P$
(1405)
B2
$(W/L)_1 = 1/4(W/L)_3$
$V_{OFF} = V_P$
(1411)
v_{con}
(1401)
(1403)
(1409)

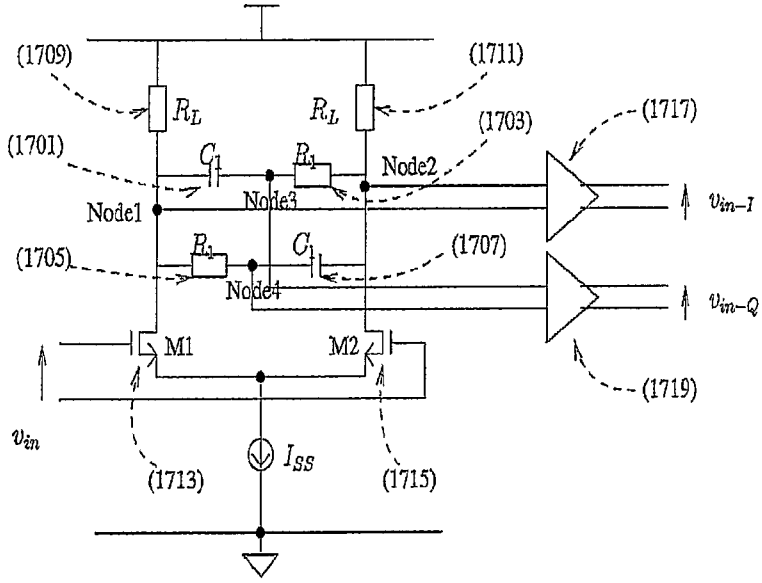
[Fig. 15]


(1511)
(1513)
(1515)
(1517)
R_L
R_L
Node1
Node2
I_{a1}
I_{a2}
I_{b1}
I_{b2}
I_{c1}
I_{c2}
$v_{mod-Q-1}$
B1
$(W/L)_4 = 1/9(W/L)_3$
$V_{OFF} = 2V_P$
B2
$(W/L)_4 = (W/L)_3$
$V_{OFF} = 0$
B3
$(W/L)_4 = 1/9(W/L)_3$
$V_{OFF} = 2V_P$
(1509)
v_{com}
(1501)
(1503)
(1505)
(1507)

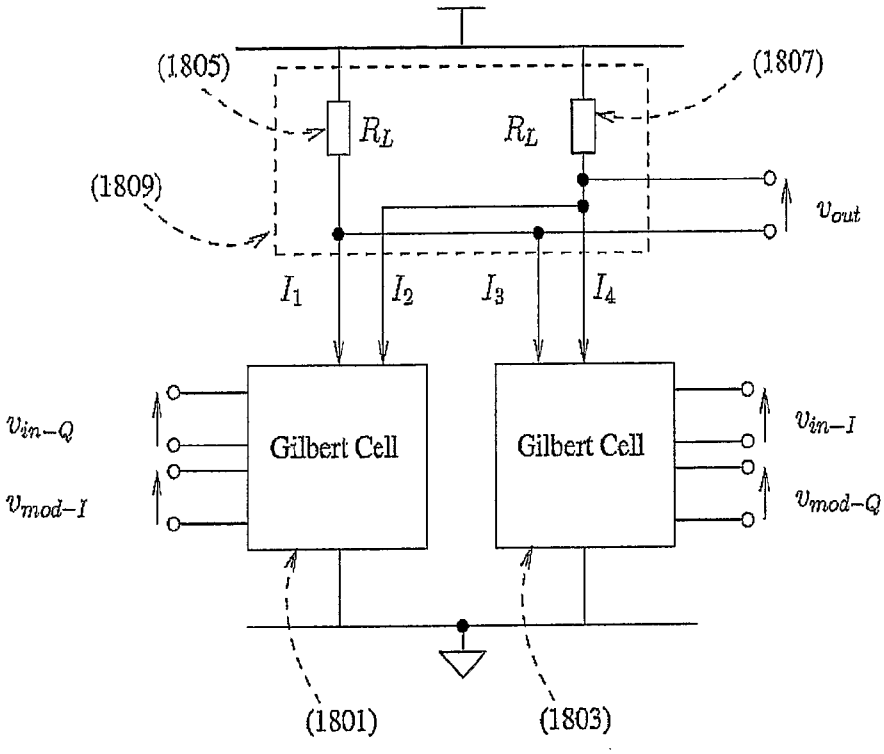
[Fig. 16]


(1601)
(1609)
$v_{mod-1-2}$
M1
C1
v_{mod-1}
(1603)
(1611)
M2
C2
(1605)
(1613)
$v_{mod-Q-2}$
M3
C3
v_{mod-Q}
(1607)
(1615)
M4
C4
Freeze

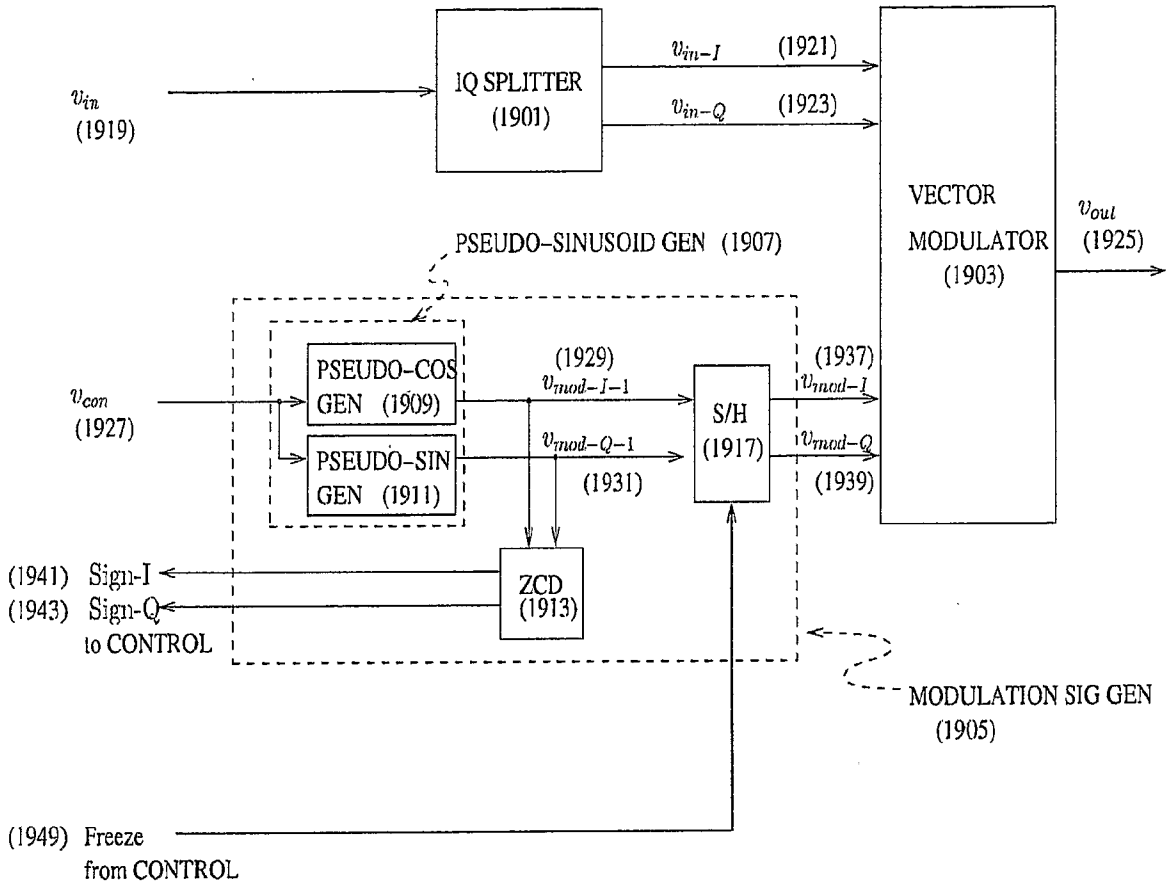
[Fig. 17]


(1709)
(1711)
R_L
R_L
(1703)
(1717)
(1701)
C_1
R_1
Node2
Node3
Node1
v_{in-I}
(1705)
R_1
C_1
(1707)
Node4
v_{in-Q}
M1
M2
(1719)
v_{in}
I_{SS}
(1713)
(1715)

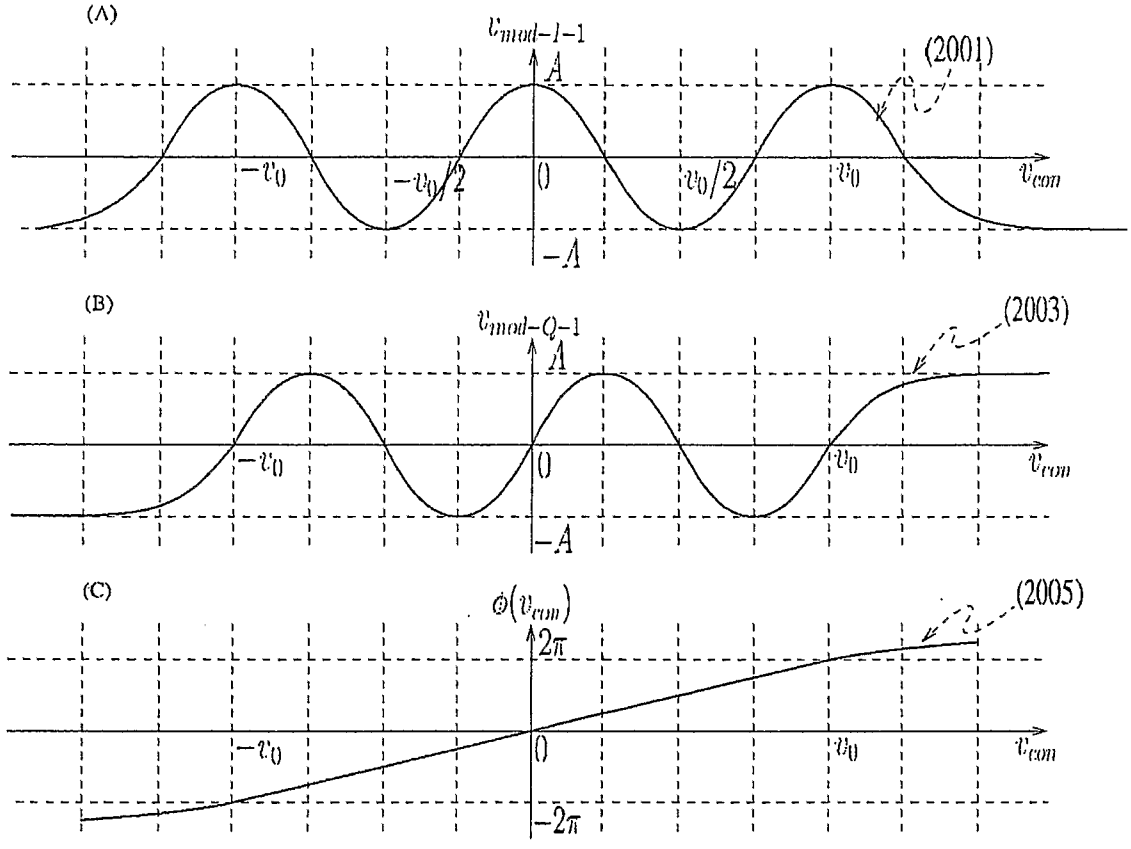
[Fig. 18]


(1805)
(1807)
R_L
R_L
(1809)
v_{out}
I_1
I_2
I_3
I_4
v_{in-Q}
v_{mod-I}
Gilbert Cell
Gilbert Cell
v_{in-I}
v_{mod-Q}
(1801)
(1803)

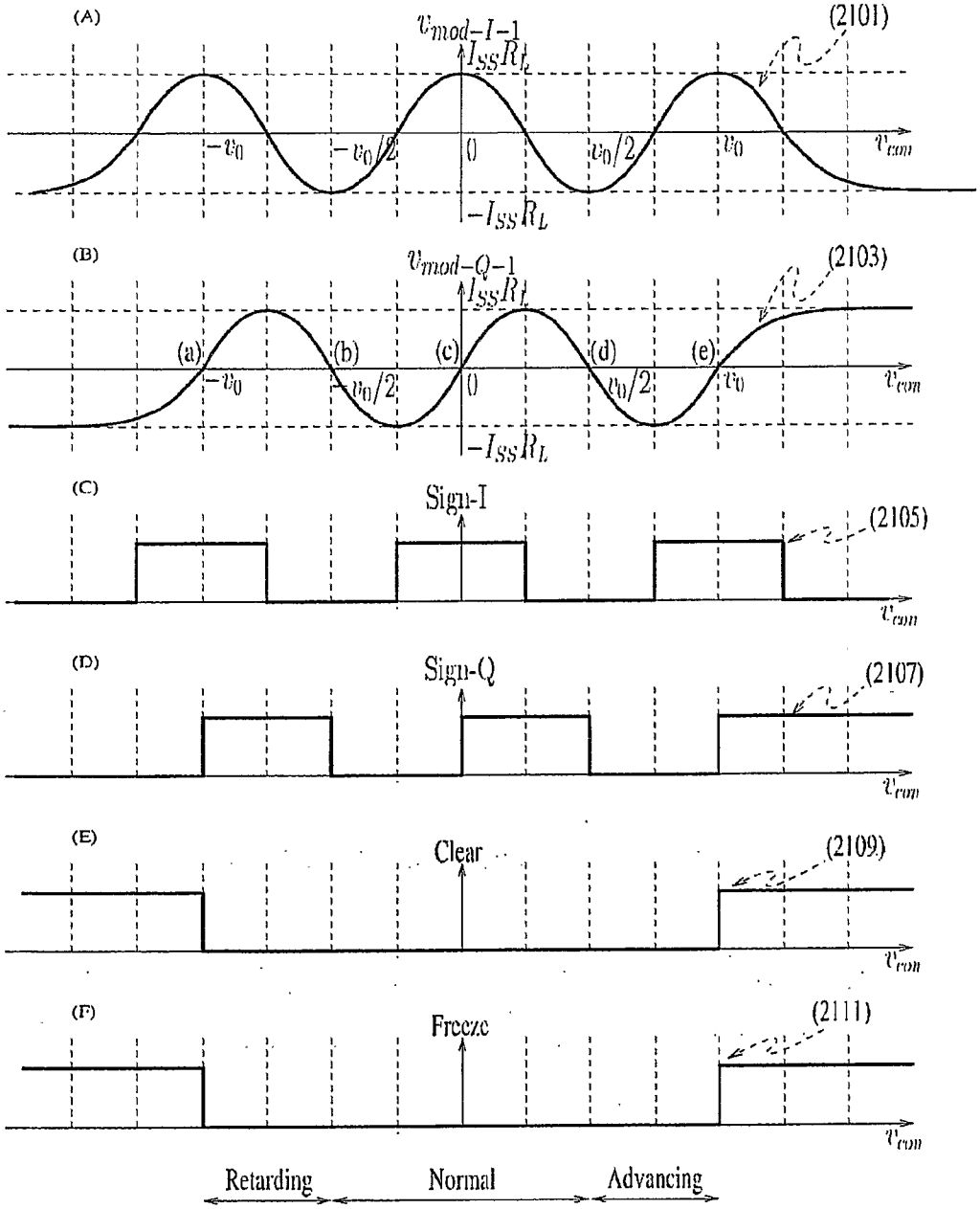
[Fig. 19]


v_{in}
(1919)
IQ SPLITTER
(1901)
v_{in-I} (1921)
v_{in-Q} (1923)
VECTOR
MODULATOR
(1903)
v_{out}
(1925)
PSEUDO-SINUSOID GEN (1907)
v_{con}
(1927)
PSEUDO-COS
GEN (1909)
PSEUDO-SIN
GEN (1911)
(1929)
$v_{mod-I-1}$
$v_{mod-Q-1}$
(1931)
S/H
(1917)
(1937)
v_{mod-I}
v_{mod-Q}
(1939)
ZCD
(1913)
(1941) Sign-I
(1943) Sign-Q
to CONTROL
MODULATION SIG GEN
(1905)
(1949) Freeze
from CONTROL

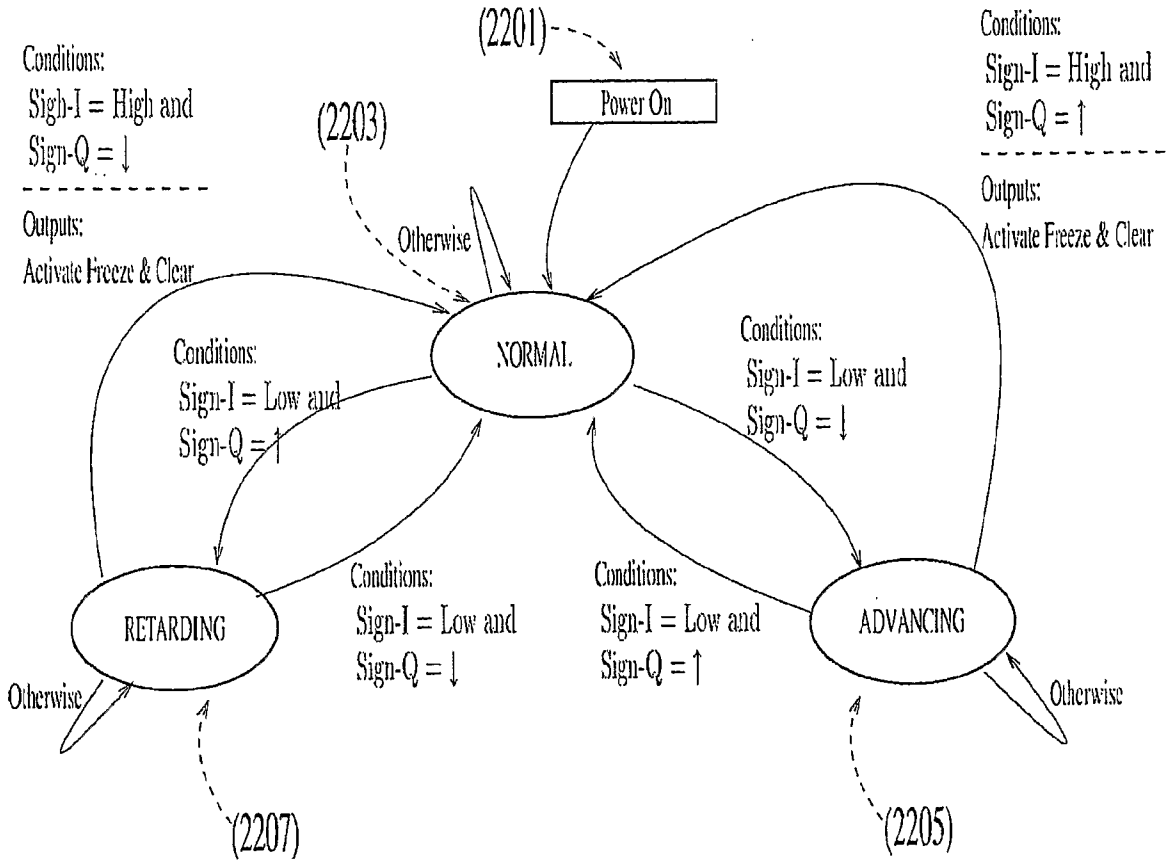
[Fig. 20]


(A)
$v_{mod-I-1}$
A
(2001)
$-v_0$
$-v_0/2$
0
$v_0/2$
v_0
v_{com}
-A
(B)
$v_{mod-Q-1}$
A
(2003)
$-v_0$
0
v_0
v_{com}
-A
(C)
$\Phi(v_{com})$
2π
(2005)
$-v_0$
0
v_0
v_{com}
-2π

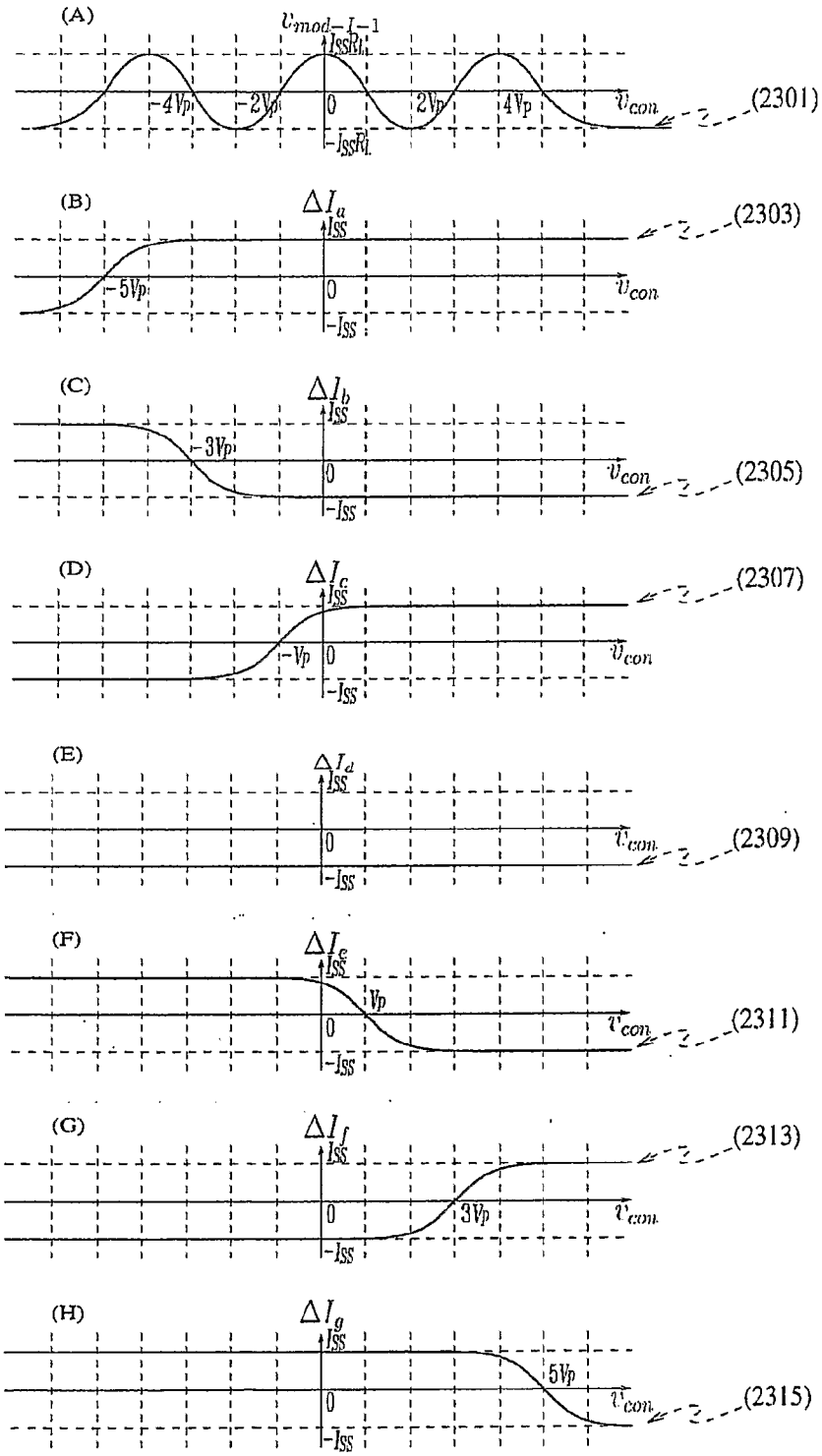
[Fig. 21]


(A)
$v_{mod-I-1}$
$I_{SS}R_L$
(2101)
$-v_0$
$-v_0/2$
0
$v_0/2$
v_0
v_{con}
$-I_{SS}R_L$
(B)
$v_{mod-Q-1}$
$I_{SS}R_L$
(2103)
(a)
(b)
(c)
(d)
(e)
$-v_0$
$v_0/2$
0
$v_0/2$
v_0
v_{con}
$-I_{SS}R_L$
(C)
Sign-I
(2105)
v_{con}
(D)
Sign-Q
(2107)
v_{con}
(E)
Clear
(2109)
v_{con}
(F)
Freeze
(2111)
v_{con}
Retarding
Normal
Advancing

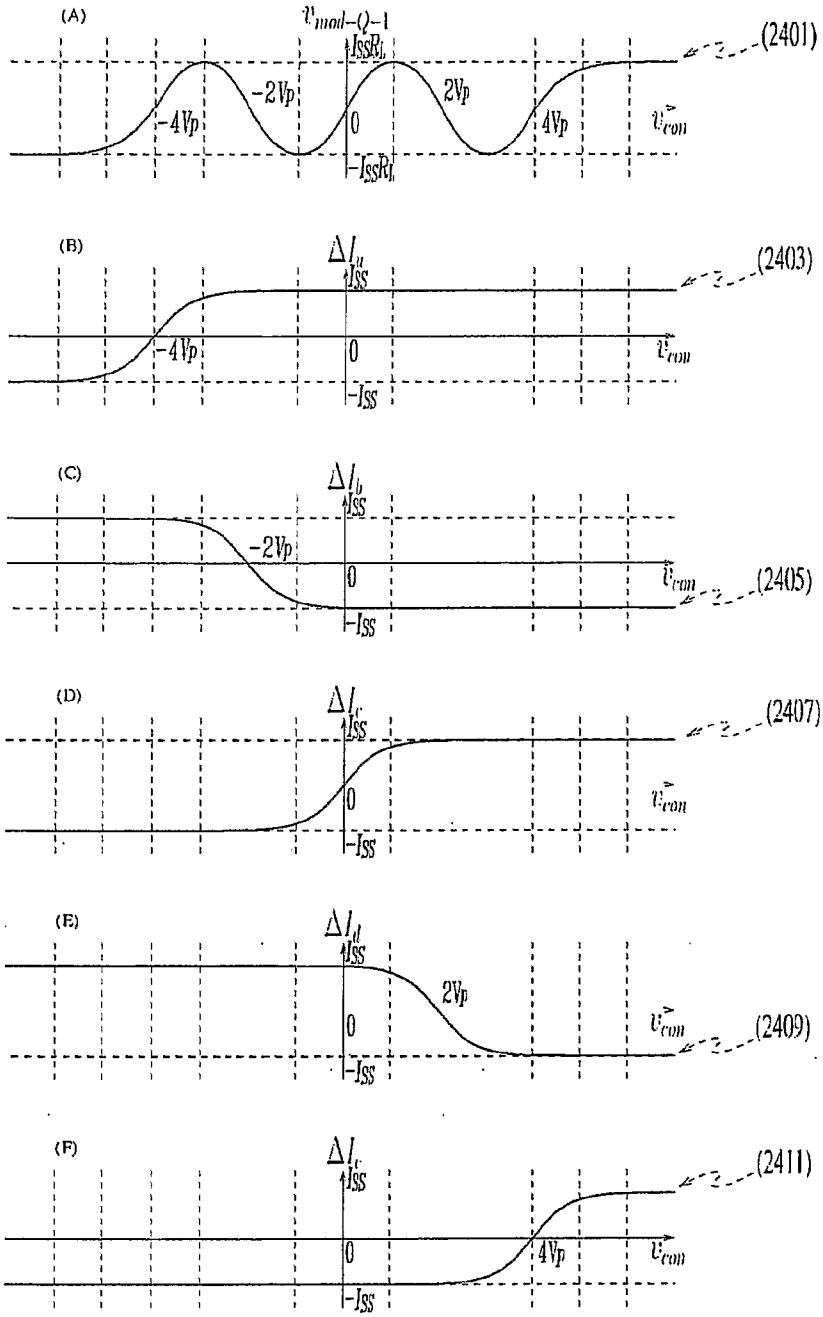
[Fig. 22]


(2201)
Power On
Conditions:
Sigh-I = High and
Sign-Q = ↓
Outputs:
Activate Freeze & Clear
(2203)
Otherwise
Conditions:
Sign-I = High and
Sign-Q = ↑
Outputs:
Activate Freeze & Clear
NORMAL
Conditions:
Sign-I = Low and
Sign-Q = ↑
Conditions:
Sign-I = Low and
Sign-Q = ↓
RETARDING
ADVANCING
Conditions:
Sign-I = Low and
Sign-Q = ↓
Conditions:
Sign-I = Low and
Sign-Q = ↑
Otherwise
Otherwise
(2207)
(2205)

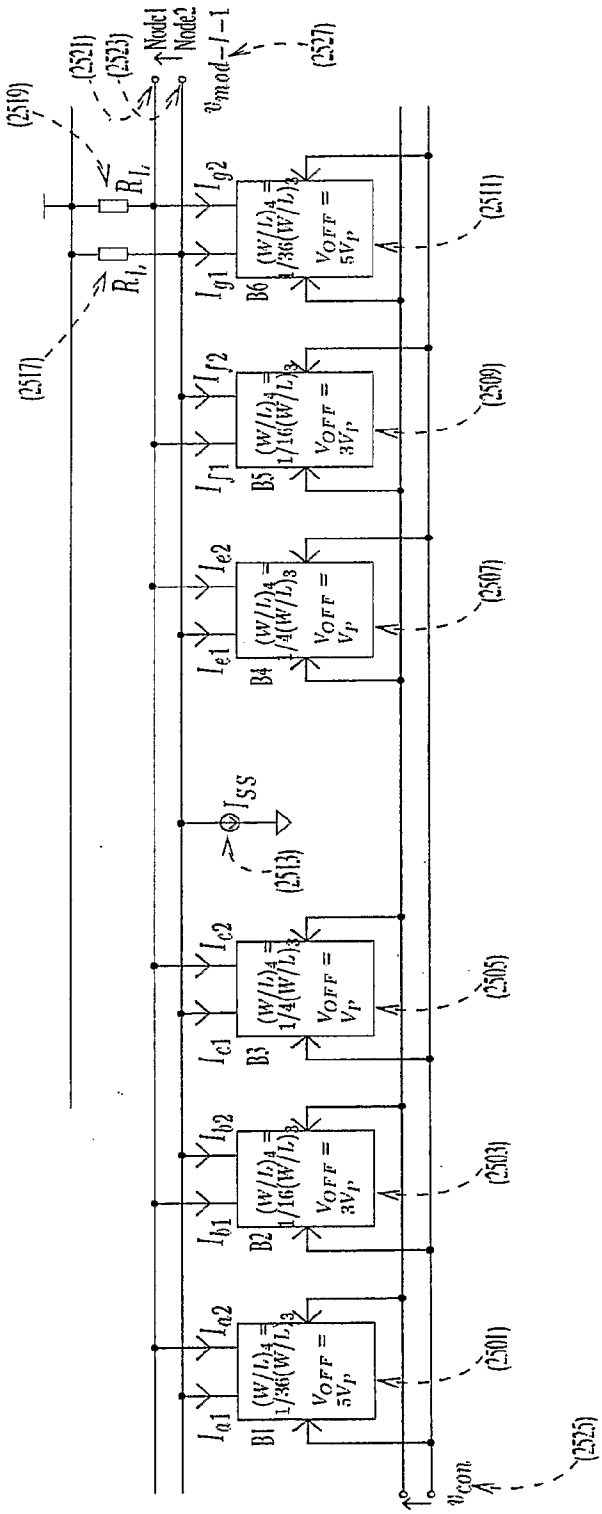
[Fig. 23]


(A)
$v_{mod-I-1}$
$I_{SS}R_L$
$-I_{SS}R_L$
$-4V_p$
$-2V_p$
0
$2V_p$
$4V_p$
v_{con}
(2301)
(B)
ΔI_a
I_{SS}
$-5V_p$
0
$-I_{SS}$
v_{con}
(2303)
(C)
ΔI_b
I_{SS}
$-3V_p$
0
$-I_{SS}$
v_{con}
(2305)
(D)
ΔI_c
I_{SS}
$-V_p$
0
$-I_{SS}$
v_{con}
(2307)
(E)
ΔI_d
I_{SS}
0
$-I_{SS}$
v_{con}
(2309)
(F)
ΔI_e
I_{SS}
V_p
0
$-I_{SS}$
v_{con}
(2311)
(G)
ΔI_f
I_{SS}
0
$3V_p$
$-I_{SS}$
v_{con}
(2313)
(H)
ΔI_g
I_{SS}
$5V_p$
0
$-I_{SS}$
v_{con}
(2315)

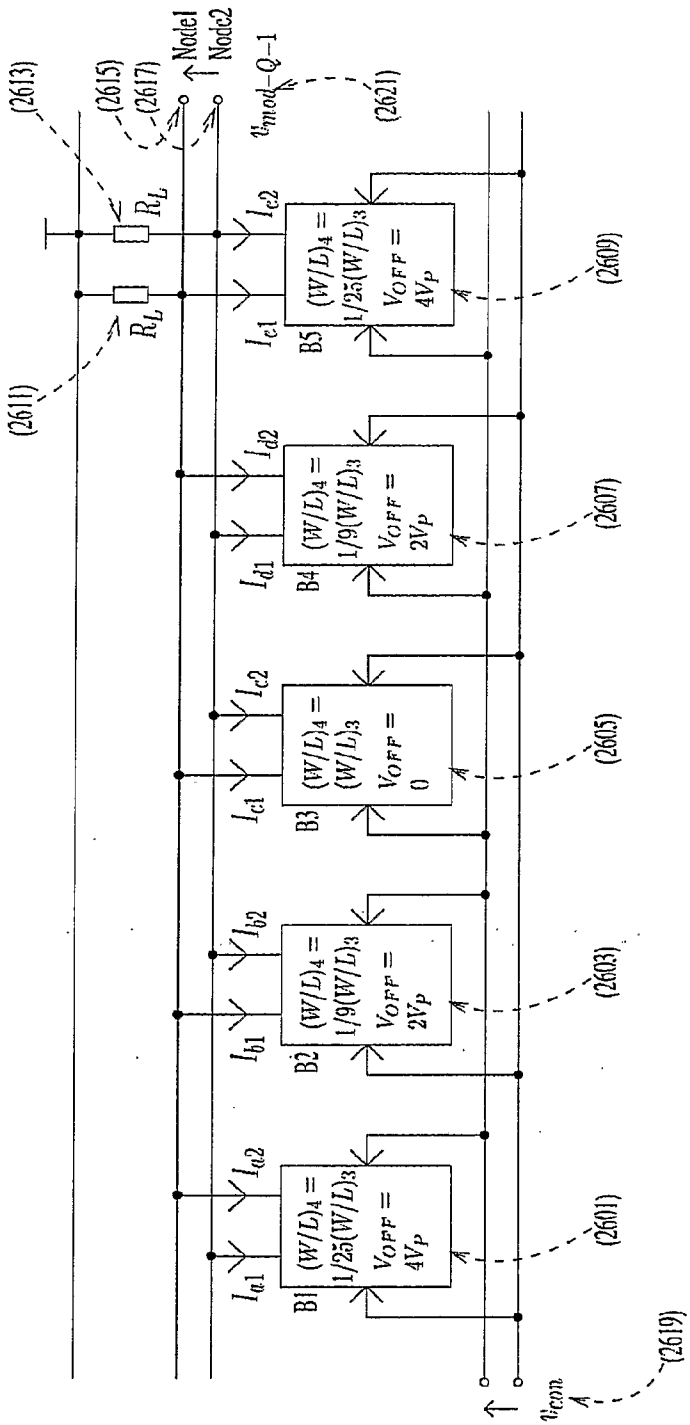
[Fig. 24]


(A)
$v_{mod-Q-1}$
$I_{SS}R_L$
-2Vp
2Vp
-4Vp
4Vp
0
$-I_{SS}R_L$
v_{con}
(2401)
(B)
ΔI_a
I_{SS}
-4Vp
0
$-I_{SS}$
v_{con}
(2403)
(C)
ΔI_b
I_{SS}
-2Vp
0
$-I_{SS}$
v_{con}
(2405)
(D)
ΔI_c
I_{SS}
0
$-I_{SS}$
v_{con}
(2407)
(E)
ΔI_d
I_{SS}
2Vp
0
$-I_{SS}$
v_{con}
(2409)
(F)
ΔI_e
I_{SS}
0
4Vp
$-I_{SS}$
v_{con}
(2411)

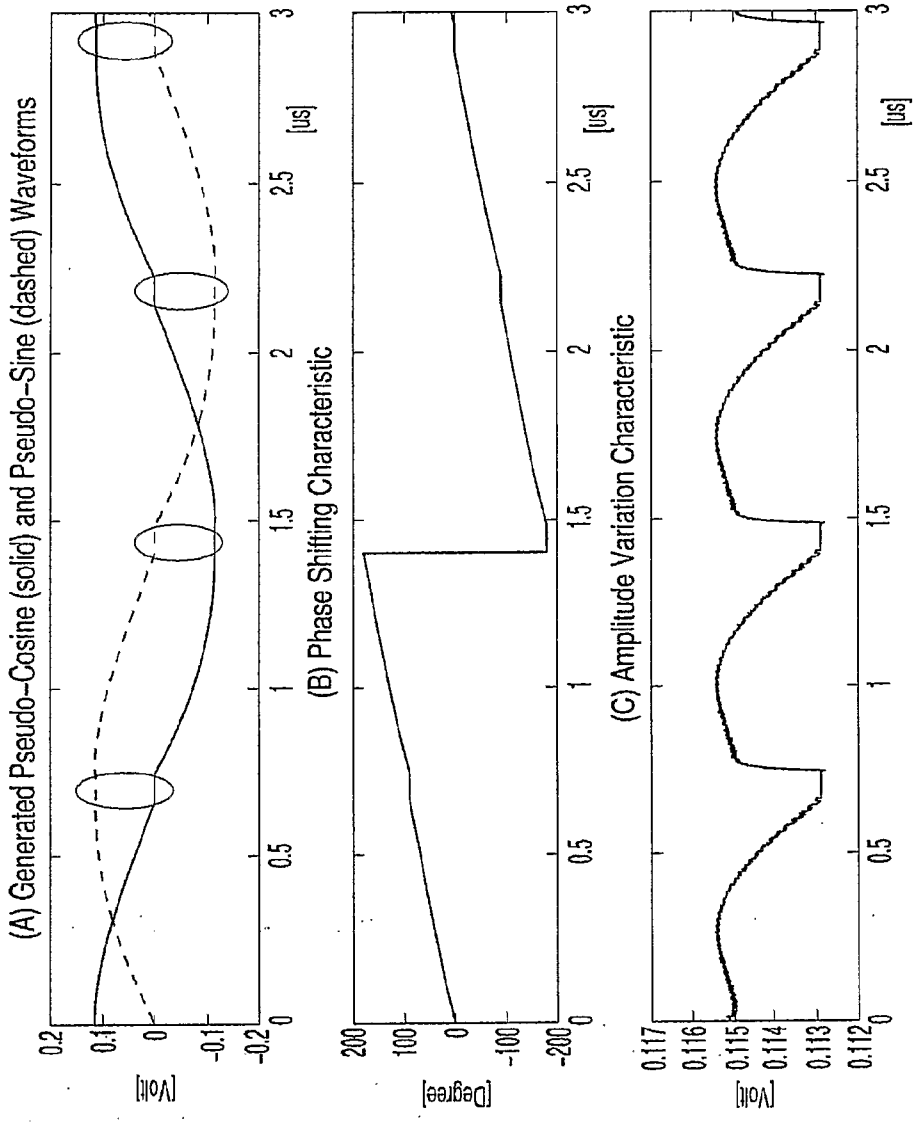
[Fig. 25]


(2519)
(2521)
(2523)
Node1
Node2
$v_{mod-1-1}$
(2527)
R_{l_1}
R_{l_2}
(2517)
I_{a1}
I_{a2}
I_{b1}
I_{b2}
I_{c1}
I_{c2}
I_{e1}
I_{e2}
I_{f1}
I_{f2}
I_{g1}
I_{g2}
I_{SS}
(2513)
B1
B2
B3
B4
B5
B6
$\frac{(W/L)_4}{1/36(W/L)_3}$
$\frac{(W/L)_4}{1/16(W/L)_3}$
$\frac{(W/L)_4}{1/4(W/L)_3}$
$V_{OFF} = 5V_T$
$V_{OFF} = 3V_T$
$V_{OFF} = V_T$
(2501)
(2503)
(2505)
(2507)
(2509)
(2511)
v_{com}
(2525)

[Fig. 26]


(2613)
(2615)
(2617)
Node1
Node2
v_{mod_Q-1}
(2621)
(2611)
R_L
R_L
I_{a1}
I_{a2}
I_{b1}
I_{b2}
I_{c1}
I_{c2}
I_{d1}
I_{d2}
I_{e1}
I_{e2}
B1 $(W/L)_4 = 1/25(W/L)_3$ $V_{OFF} = 4V_P$
B2 $(W/L)_4 = 1/9(W/L)_3$ $V_{OFF} = 2V_P$
B3 $(W/L)_4 = (W/L)_3$ $V_{OFF} = 0$
B4 $(W/L)_4 = 1/9(W/L)_3$ $V_{OFF} = 2V_P$
B5 $(W/L)_4 = 1/25(W/L)_3$ $V_{OFF} = 4V_P$
(2601)
(2603)
(2605)
(2607)
(2609)
(2619)
v_{com}

[Fig. 27]


(A) Generated Pseudo-Cosine (solid) and Pseudo-Sine (dashed) Waveforms
[Volt]
0.2
0.1
0
-0.1
-0.2
0
0.5
1
1.5
2
2.5
3
[us]
(B) Phase Shifting Characteristic
[Degree]
200
100
0
-100
-200
(C) Amplitude Variation Characteristic
[Volt]
0.117
0.116
0.115
0.114
0.113
0.112

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2007/003846

A. CLASSIFICATION OF SUBJECT MATTER

H04L 27/20(2006.01)i, H03C 3/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 8 H04L 27/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
KOREAN UTILITY MODELS AND APPLICATIONS FOR UTILITY MODELS SINCE 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS, DELPHION, ESPACENET & Keywords : phase shifter, phase control, VCPS, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6874109 B1 (RAJSKI et al.) 29.03.2005 See abstract, column 5 lines 15 - 52, figure 14	1-20
A	US 05736840 A (OTAKA et al.) 07.04.1998 See abstract, column 6 lines 20 - 55, figure 1	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 NOVEMBER 2007 (20.11.2007)	**20 NOVEMBER 2007 (20.11.2007)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	JEONG Heon Ju Telephone No. 82-42-481-8356

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2007/003846

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6874109 B1	29.03.2005	EP 1257837 A1	20.11.2002
		EP 1257837 A4	12.01.2005
		JP 3699397 B2	28.09.2005
		US 2005015688 A1	20.01.2005
		US 7263641 BB	28.08.2007
		WO 2001/38891 A1	31.05.2001
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		KR 1996-0012858 A	20.04.1996
		KR 970007614 B1	13.05.1997
		US 05650714 A	22.07.1997