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(54) **Title:** LOW COST GRAPHENE-BASED MICRODEVICES WITH MULTI-STATE RESISTIVE VALUES

(57) **Abstract:** There is provided a planar graphene oxide (GO)-based device comprising of multiple resistance state elements in response to an applied voltage and wherein the multiple resistance state elements mimic neural synapse behaviour. The device has multiple application potentials including but not limited to non-volatile electronic memory, sensors, computing for Artificial intelligence (AI) and security. Also disclosed is method of manufacturing a memristor microdevice comprising the steps of patterning metal layer and graphene oxide or reduced graphene oxide thin films on different substrates and producing reduced graphene oxide (rGO) thin film through reduction of the graphene oxide layer. Fabricating thin films of graphene oxide and reduced graphene oxide in the microdevice from an aqueous solution of graphene oxide, results in making the process simple, cost effective, and suitable for mass production of the microdevice.

LOW COST GRAPHENE-BASED MICRODEVICES WITH MULTI-STATE RESISTIVE VALUES

FIELD OF THE INVENTION

[0001] The present invention relates to the field of graphene-based microdevices, and more particularly to a planar graphene oxide (GO) - based memristor device.

BACKGROUND OF THE INVENTION

[0002] Graphene is a two-dimensional crystal of carbon atoms with unique electrical, mechanical, optical, and thermal properties that makes it ideal for enormous applications and one of the most exciting materials in the 21st century. The first method to prepare graphene sheet was reported by Andre Geim and Konstantin Novoselov in 2004. The unusual properties of graphene such as stability under ambient temperature, high electrical conductivity, flexibility, and high surface area makes it very promising candidate to substitute metal electrodes. Reduced graphene oxide (rGO) is a form of graphene which is produced by reducing graphene oxide (GO) to remove the oxygen-containing groups. Reducing graphene oxide is one of the most effective methods to manufacture graphene in sufficient quantities. The reduction of GO could be achieved by several methods based on thermal, chemical or electrical treatments. The quality of the rGO flakes to be akin to graphene depends on the techniques used in reduction. Chemical reduction of graphene oxide opens a route for mass scale production of graphene (rGO).

[0003] Recently, there has been great interest in graphene(G)-based electronics for many applications. Bio-inspired electronic devices with analog behavior have many advantages over conventional silicon-based technologies that demonstrate static digital properties. This is due to their ability to compute, process and hold information in parallel; which improves speed, storage density and power consumption of the system. Bio-inspired neuromorphic devices are of great importance in many emerging

applications; such as image and pattern recognition, machine learning and Artificial Intelligence (AI). Memristor devices are important elements in such technologies due to their non-volatility and ability to demonstrate multiple resistance levels.

SUMMARY OF THE INVENTION

[0004] Therefore it is an object of the present invention to provide a planar graphene oxide (GO)-based memristor device that exhibits conductivity change with an effective range of resistance levels.

[0005] The present invention involves a planar graphene oxide (GO) – based device, wherein the planar graphene oxide (GO) – based device comprises a memristor structure enabling the device to have an electrical behavior characterized in having multiple resistance levels in response to an applied voltage.

[0006] In another embodiment of the present invention, the electrical behavior enables the device to store data and be used as a single bit or multiple bit random access memory (RAM).

[0007] In another embodiment of the present invention, the electrical behavior enables the device to perform data processing.

[0008] In another embodiment of the present invention, the electrical behavior demonstrates a retention displayed by absence of overlap between consecutive I-V (current – voltage) sweeps.

[0009] In another embodiment of the present invention, electrical behavior of the device provides a clear distinction between the multiple resistance levels.

[0010] In another embodiment of the present invention, the device comprises a reduced graphene oxide thin film patterned on a substrate.

[0011] As another aspect of the present invention is disclosed a method of manufacturing a memristor device, comprising the steps of producing a graphene oxide layer on a substrate, patterning the graphene oxide layer, reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film; and producing a patterned metal layer on top of the reduced graphene oxide layer.

[0012] In another embodiment of the present invention, a method of manufacturing a memristor device is disclosed, comprising the steps of producing a graphene oxide layer on a substrate, reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film; and producing a patterned metal layer on top of the reduced graphene oxide layer.

[0013] In another embodiment of the present invention, a method of manufacturing a memristor device is disclosed, comprising the steps of producing a patterned metal layer on top of a substrate, producing a graphene oxide layer on top of the substrate with the metal patterned layer, patterning the graphene

oxide layer; and reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film.

[0014] In another embodiment of the present invention, the patterning the metal layer and the reduced graphene oxide thin films on different substrates is performed using a microfabrication technique.

[0015] In another embodiment of the present invention, the reduced graphene oxide thin film is produced using a liquid-phase solution of graphene oxide.

[0016] In another embodiment of the present invention, the producing a patterned graphene oxide layer on a substrate comprises coating the substrate with a photoresist layer, patterning the photoresist layer using photolithography on the substrate, developing the photoresist layer using a chemical to produce a patterned photoresist, treating the substrate with plasma to produce a treated substrate, applying a graphene oxide solution on top of the treated substrate to form a graphene oxide layer on said treated substrate, spinning and heating the treated substrate with the graphene oxide layer on said treated substrate; and removing the photoresist layer to form a patterned graphene oxide film.

[0017] In another embodiment of the present invention, the reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film on different substrates comprises reducing the graphene oxide layer on the treated substrate to produce the reduced graphene oxide film.

[0018] In another embodiment of the present invention, the substrate is a polymer substrate.

[0019] In another embodiment of the present invention, the substrate is a cyclic olefin copolymer (COC) substrate.

[0020] In another embodiment of the present invention, the plasma is O_2 plasma.

[0021] In another embodiment of the present invention, the photoresist layer coated on the polymer substrate is baked prior to the patterning the photoresist layer on the substrate.

[0022] In another embodiment of the present invention, the photoresist layer is Shipley PR1813.

[0023] In another embodiment of the present invention, the treated substrate is spun subsequent the deposition of the graphene oxide layer.

[0024] In another embodiment of the present invention, the treated substrate is baked subsequent the coating of the substrate with graphene oxide.

[0025] In another embodiment of the present invention, the treated substrate is sonicated subsequent to removing the photoresist layer on the treated substrate using acetone.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The subject matter that is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other aspects, features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which-

[0027] FIG. 1 (a) – (d) shows initial steps for manufacturing a patterned graphene oxide film and graphene film from a graphene oxide solution in accordance with the present invention.

[0028] FIG. 2 (a) - (c) shows intermediate steps for manufacturing a patterned graphene oxide film and graphene film from a graphene oxide solution in accordance with the present invention.

[0029] FIG. 3 (a) and (b) denotes the final steps for manufacturing a patterned graphene oxide film and graphene film from a graphene oxide solution in accordance with the present invention.

[0030] FIG. 4 is an SEM photograph of the word 'Graphene' made of graphene on top of a cyclic olefin copolymer (COC) substrate.

[0031] FIG. 5 is an SEM picture for Sheikh Zayed mosque and the logo of Khalifa University made of graphene thin layer on top of the cyclic olefin copolymer (COC) substrate.

[0032] FIG. 6 depicts a Planar Graphene Oxide-Based Memristor in accordance with the present invention.

[0033] FIG. 7 (a) is a graphical representation of a single positive sweep.

[0034] FIG. 7 (b) is a graphical representation of consecutive positive sweeps.

[0035] FIG. 8 (a) is a graphical representation of a single negative sweep.

[0036] FIG. 8 (b) is a graphical representation of consecutive negative sweeps.

[0037] FIG. 9 shows an example of the fabrication steps of a patterned rGO (reduced graphene oxide) thin film, in accordance with the present invention.

[0038] FIG. 10 depicts an example of using rGO as electrodes, in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0040] The aspects of a planar graphene oxide (GO)-based memristor device that exhibits conductivity change with an effective range of resistance levels according to the present invention, will be described in conjunction with Figures 1-10. In the Detailed Description, reference is made to the accompanying figures, which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

[0041] The present invention relates to a novel planar graphene oxide (GO)-based device that exhibits conductivity change with an effective range of resistance levels. The electrical behavior of the planar graphene oxide (GO)-based device demonstrates excellent retention displayed by an absence of the overlap between the consecutive I-V sweeps. This provides clear distinction between the multiple resistance states obtained by the application of each voltage sweep. The variable resistance level in the memristive junction formed at the interface between metal electrodes is directly related to the synapse plasticity change in the brain. Graphene – based microdevices (or memristor devices) exhibiting multi – state resistive values enables support of memory or storage capabilities along with information processing capabilities due to the presence of a resistive random access memory (RAM). This feature further makes the planar graphene oxide (GO)-based memristor promising for in – memory computing (IMC), machine learning and neuromorphic applications.

[0042] The memristor microdevice in accordance with the present invention is fabricated using a simple and repeatable method. In this method, metal layer and graphene oxide or reduced graphene oxide thin films are patterned on different substrates following which photolithography is successfully used to pattern solution-based graphene oxide thin films on the substrates. Reduced graphene oxide (rGO) thin film is produced through the reduction of graphene oxide layer, as this is the most effective method to sufficiently manufacture graphene in adequate quantities. Accordingly, fabricating thin films of graphene oxide (GO) and reduced graphene oxide (rGO) in the microdevice from an aqueous solution

of graphene oxide makes the process simple, cost effective, and suitable for mass production of the microdevice. The metal electrodes are patterned using photolithography through etching or liftoff processes.

[0043] In accordance with another embodiment of the present invention, a method for manufacturing a patterned graphene oxide film and graphene film from a graphene oxide solution includes the following steps. The steps included in this method as depicted in FIG. 1 (a) – (d) comprise the steps of coating a photoresist layer 104 on a substrate 102, patterning the photoresist layer 104 on the substrate 102 obtained through the previous step using photolithography. Following this, the photoresist layer on the substrate obtained through the previous step is developed using the proper chemical to produce a patterned photoresist and the substrate obtained through the previous step is treated with plasma 106. Subsequent to these initial steps, as depicted in FIG. 2 (a) – (c), intermediate steps in the manufacturing process include the graphene oxide solution 204 being dispensed on top of the substrate 202 obtained through the previous step, and the substrate 202 obtained in the previous step being spun at a proper speed and heated at a proper temperature. Further, FIG. 3 (a) and (b) denote the final steps as the photoresist on the substrate 302 obtained through the previous step being stripped off using a proper chemical to form a patterned graphene oxide film 304 and the graphene oxide layer being reduced to produce reduced graphene oxide (graphene) film 306.

[0044] The proposed device may be fabricated without patterning the GO layer by producing a rGO layer and subsequently producing a patterned metal layer on top of it.

[0045] In accordance with a preferable embodiment of the present invention, a method of manufacturing a memristor is disclosed, comprising the steps of producing a graphene oxide layer on a substrate, patterning the graphene oxide layer, reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film and producing a patterned metal layer on top of the reduced graphene oxide layer. The fabrication steps may may differ. In another embodiment, the method of manufacturing a memristor device in accordance with the present invention comprises the steps of producing a graphene oxide layer on a substrate, reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film and producing a patterned metal layer on top of the reduced graphene oxide layer. Another variation of the fabrication steps involves a method of manufacturing a memristor comprising

the steps of producing a patterned metal layer on top of a substrate, producing a graphene oxide layer on top of the substrate with the metal patterned layer, patterning the graphene oxide layer and reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film.

[0046] Considering an example in accordance with the present invention, the manufacturing of a patterned graphene film comprises the steps of coating a Shipley PR1813 photoresist layer on a cyclic olefin copolymer (COC) substrate and then baking the same at 70o C for 3 minutes. Then, the photoresist layer on the substrate obtained through the previous step is patterned using a lithography system (Dilase 650). Dilase 650 is a high resolution direct laser lithography system equipped with different laser beams. The machine is used to pattern photoresist i.e. photosensitive material. The photoresist is patterned either by a photolithography machine (Dilase 650) or through a mask and an ultra-violet (UV) exposure system. The second method requires preparing a mask, which is usually prepared by a lithography machine. However, by using the lithography system, one can pattern the photoresist using a CAD drawing. The process is similar to a printing process but at a very high resolution and using laser beams.

[0047] Then, the photoresist layer on the cyclic olefin copolymer (COC) substrate obtained through the previous step is developed using the development (MF 319) and the substrate obtained through the previous step is treated with O2 plasma for 4 minutes. MF 319 is a chemical that used to develop or etch the photoresist (Shipley PR1813 in accordance with the present invention), designed for high resolution semiconductor fabrication. The development process is performed by immersing the wafer with the photoresist layer on it into the developer (MF 319), subsequent to ultra-violet (UV) exposure. The developer MF 319 will etch or remove the photoresist in a controlled manner. The PR1813 is positive photoresist and chemical structure changes and becomes more soluble in the MF 319 photoresist developer when the photoresist is exposed to the ultra-violet (UV) light. The pattern is printed using the photolithography system (Dilase 650) which makes the photoresist material soluble into the developer in the areas intends to remove. The printed (exposed) region is washed out using the MF 319 developer by immersing the wafer into the developer.

[0048] Further, graphene oxide solution is dispensed on top of the cyclic olefin copolymer (COC) substrate obtained through the previous step, following which the substrate obtained through the

previous step is spun at 1000 rpm for 2 minutes and heated at 60o C for 10 minutes. Subsequent to this, the photoresist on the substrate obtained through the previous step is stripped off using acetone and sonicated (subjected to ultrasonic vibrations to fragment the cells, macromolecules, and membranes) for 10 minutes to remove all the photoresist from the substrate. The graphene oxide layer is reduced using hydriodic acid - a highly acidic aqueous solution of hydrogen iodide (HI) - to produce a graphene film, the patterned graphene film being shown in FIG. 4.

[0049] Considering another example in accordance with the present invention, the manufacturing of patterned graphene film comprises the steps of coating Shipley PR1813 photoresist layer on a cyclic olefin copolymer (COC) substrate and then baking the same at 50oC for 5 minutes. Then, the photoresist layer on the substrate obtained through the previous step is patterned using a lithography system (Dilase 650). Further, the photoresist layer on the cyclic olefin copolymer (COC) substrate obtained through the previous step is developed using the development (MF 319) and the substrate obtained through the previous step is treated with O2 plasma for 3 minutes. Following this, graphene oxide solution is dispensed on top of the cyclic olefin copolymer (COC) substrate obtained through the previous step and the substrate obtained through the previous step is spun at 1000 rpm for 2 minutes and heated at 60o C for 5 minutes.

[0050] The photoresist layer coated on the cyclic olefin copolymer (COC) substrate is baked prior to patterning the photoresist layer on the cyclic olefin copolymer (COC). This is very well known process in photolithography. The substrate is baked "soft bake" and "hard bake". The first is prior exposure to UV and the second is after the exposure. Then, the photoresist on the substrate obtained through the previous step is stripped off using acetone and sonicated for 2 minutes to remove all the photoresist from the substrate. The graphene oxide layer is then reduced using hydriodic acid - a highly acidic aqueous solution of hydrogen iodide (HI), to produce graphene film, the patterned graphene film being shown in FIG. 5.

[0051] The order of the steps in the fabrication process could be changed. Photoresist layer could be easily changed and other substrates also work. Baking may be performed at different temperatures and durations.

[0052] FIG. 6 depicts the device or wafer illustration of the planar graphene oxide-based memristor in accordance with the present invention.

[0053] In an embodiment of the present invention, electrical behavior of the planar graphene oxide (GO) – based memristor device demonstrates excellent retention displayed by the absence of the overlap between the consecutive I-V (current - voltage) sweeps.

[0054] In another embodiment of the present invention, electrical behavior of the planar graphene oxide (GO) – based memristor device provides clear distinction between the multiple resistance states obtained by application of each voltage sweep.

[0055] Accordingly, FIG. 7 (a) is a graphical representation of a single positive sweep, FIG. 7 (b) is a graphical representation of consecutive positive sweeps, FIG. 8 (a) is a graphical representation of a single negative sweep and FIG. 8 (b) is a graphical representation of consecutive negative sweeps.

[0056] The GO-based memristor device presented in this patent is the first to demonstrate multiple resistance states that mimic the neural synapse behavior. The device unique characteristics of having multiple resistance state element in response to applied voltage makes it a good candidate for various application in electronics industry. Several examples of such applications include - multi bit non-volatile Resistive memory for Programmable Read-only-memory (ROM) - similar to Flash with but with limited writability and in - memory computing. There is great interest for resistive random access memory (RRAM) in machine learning and artificial intelligence (AI) wherein inherent parallelism and small device sizes will provide high throughputs with low power. An application of the developed rGO film is to use it as conductive film.

[0057] The type of resistive memory achieved through the material in accordance with the present invention enables data to be stored as a resistance state and to be combined with other signals represented by a voltage, in order to carry on any function. Other applications include sensing applications especially when compound with other materials which transfer environment variables into voltages, following which the voltages are translated into resistances and variable or tunable resistors - which are needed for many Analog and RF circuits to implement high speed and reliable circuits.

[0058] In another embodiment of the present invention, a schematic describing the fabrication process of patterned rGO thin film is shown in FIG. 9. Initially, a substrate is cleaned by sonicating it in an

isopropanol bath for ten minutes (step 1). The substrate is then dried with compressed nitrogen and baked on top of a hotplate at 70 °C for ten minutes. Next, a thin photoresist layer is deposited on top of the substrate using a spin coater (Step 2). The photoresist layer is then patterned using a photolithography system and developed using a suitable developer (steps 3 and 4). Following the development of the photoresist layer, the substrate is washed with deionized water, backed at 70 °C, and then treated with oxygen plasma for three minutes to increase surface wettability (step 5). Immediately after the treatment with plasma, GO aqueous solution is dispersed on top of the patterned photoresist layer using a pipette then uniformly spread on the substrate using a spin coater (steps 6 and 7). Next, the substrate is baked for ten minutes at 70 °C to evaporate the water and improve the adhesion of the GO flakes to the substrate (step 8). The following step involves immersing the substrate in an acetone bath to remove the photoresist layer (step 9). The substrate is then washed with deionized water, dried with compressed nitrogen, and baked at 70 °C for ten minutes. At this stage the GO thin film has been patterned on top of the substrate (step 10). The last step of this fabrication process is to reduce the GO thin film to rGO by immersing the substrate in hydroiodic acid for three hours to get a patterned rGO film (steps 11 and 12).

[0059] The main goal of this work is to fabricate patterned, flexible, conductive films of rGO and use them for lab-on-chip applications. The ability to use the liftoff approach to pattern GO from a solution form makes the fabrication method simple, repeatable, and low cost. It also allows for the use of conventional photolithography methods, thus enabling mass production and eliminating the need to use toxic chemicals. Using polymer substrates brings about the advantage of being flexible, disposable, and transparent. Cyclic olefin copolymer (COC) material is increasingly used as a substrate for microfluidic devices. This work investigates the use of COC substrates/films plus the liftoff method assisted by plasma treatment and ultrasonic vibration to fabricate graphene-based electrodes for lab-on-chip applications. Different patterns of rGO films were fabricated on COC substrates. The GO film was initially patterned on the substrate then chemically reduced to rGO.

[0060] Several rGO films were fabricated using the fabrication process shown in FIG. 9. PR1813 photoresist (MicroChem) was deposited on the COC substrate (Sirris.be) using a spin coater (WS650Hzb-23NPP UD-3 from Laurell Technologies Corporation). The photoresist layer was backed

at 70°C for five minutes then patterned using a photolithography system (Dilase 650 from Kloe). The photoresist layer was exposed to UV light as recommended by the supplier. The substrate was then cleaned, baked, and treated with oxygen plasma (PDC-002 from Harrick Plasma) for three minutes before a thin film of GO (4 mg/ml dispersion in water from Sigma Aldrich) was deposited using a spin coater. The plasma treatment of the patterned substrate increases its wettability, thus improving the bond force between the GO flakes and the COC substrate. The substrate was then backed at 70 °C for 10 minutes using a hotplate in order to improve the adhesion of the GO flakes to the substrate and to remove any remaining water. Next, liftoff was performed by soaking the substrate in acetone and sonicating it briefly using a sonicator (Thomas Scientific) to dissolve the photoresist layer. The wafer was then rinsed with ethanol and dried using compressed nitrogen. Finally, the patterned GO film was chemically reduced to rGO by immersing the substrate in hydroiodic acid (Sigma Aldrich) for three hours.

[0061] FIG. 10 shows the aggregation of cells due to pDEP (a phenomenon called positive DEP) at 5 Vpp at 1 MHz. The three electrodes shown in FIG. 10 are made from rGO and connected in sequence to AC function generator terminals ("r" and "O" to one terminal, while "G" to the other terminal). The dense accumulation of red blood cells is shown between the three electrodes where the electric field gradient is high. The cells are clearly visible on top of the electrodes.

[0062] Electrical characteristics of a memristor device display a change in resistance of the device in response to voltage level the new value persists (non-volatile). This is referred to as resistive Random Access memory (RRAM). There is a lot of interest in the research and industry in developing computing platforms based on this type of technology to complement CMOS technology or as a stand-alone. The ability to support memory and perform computations on the same device is promising, which makes it attractive for artificial intelligence (AI) and big data applications - the reason being that there is no need to move data from memory to execution or a processing unit. A memristor is a type of resistive Random Access memory (RRAM) consisting of a thin oxide film which stores information with zero leakage current, has high endurance, relatively fast write time and small cell size. The two-terminal device has displays both storage and information processing capabilities, which make it a potential building block for in-memory computing (IMC).

[0063] Many changes, modifications, variations and other uses and applications of the subject invention will become apparent to those skilled in the art after considering this specification and the accompanying drawings, which disclose the preferred embodiments thereof. All such changes, modifications, variations and other uses and applications, which do not depart from the spirit and scope of the invention, are deemed to be covered by the invention, which is to be limited only by the claims which follow.

CLAIMS

1. A planar graphene oxide (GO) – based device, wherein the planar graphene oxide (GO) – based device comprises a memristor structure enabling the device to have an electrical behaviour characterized in having multiple resistance levels in response to an applied voltage.

2. The planar graphene oxide (GO) – based device according to claim 1, wherein the electrical behaviour enables the device to store data and be used as a single bit or multiple bit random access memory (RAM).

3. The planar graphene oxide (GO) – based device according to any one of claims 1 to 2, wherein the electrical behaviour enables the device to perform data processing.

4. The planar graphene oxide (GO) – based device according to any one of claims 1 to 3, wherein the electrical behaviour demonstrates a retention displayed by absence of overlap between consecutive I-V (current – voltage) sweeps.

5. The planar graphene oxide (GO) – based device according to any one of claims 1 to 4, wherein the electrical behaviour of the device provides a clear distinction between the multiple resistance levels.

6. The planar graphene oxide (GO) – based device according to any one of claims 1 to 5, wherein the device comprises a reduced graphene oxide thin film patterned on a substrate.

7. A method of manufacturing a memristor device according to any one of claims 1 to 6, comprising the steps of:

– producing a graphene oxide layer on a substrate;

– patterning the graphene oxide layer;

– reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film; and

– producing a patterned metal layer on top of the reduced graphene oxide layer.

8. A method of manufacturing a memristor device according to any one of claims 1 to 6, comprising the steps of:

- producing a graphene oxide layer on a substrate;
- reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film; and
- producing a patterned metal layer on top of the reduced graphene oxide layer.

9. A method of manufacturing a memristor device according to any one of claims 1 to 6, comprising the steps of:

- producing a patterned metal layer on top of a substrate;
- producing a graphene oxide layer on top of the substrate with the metal patterned layer;
- patterning the graphene oxide layer; and
- reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film.

10. The method of manufacturing a memristor device according to any one of claims 1 to 9, wherein the patterning the metal layer and the reduced graphene oxide thin films on different substrates is performed using a microfabrication technique.

11. The method of manufacturing a memristor device according to any one of claims 1 to 10, wherein the reduced graphene oxide thin film is produced using a liquid-phase solution of graphene oxide.

12. The method of manufacturing a memristor device according to any one of claims 1 to 11, wherein:

- the producing a patterned graphene oxide layer on a substrate comprises:
  - coating the substrate with a photoresist layer;
  - patterning the photoresist layer using photolithography on the substrate;

- developing the photoresist layer using a chemical to produce a patterned photoresist;
- treating the substrate with plasma to produce a treated substrate;
- applying a graphene oxide solution on top of the treated substrate to form a graphene oxide layer on said treated substrate;
- spinning and heating the treated substrate with the graphene oxide layer on said treated substrate; and
- removing the photoresist layer to form a patterned graphene oxide film; and

– the reducing the graphene oxide layer to produce a reduced graphene oxide (rGO) thin film on different substrates comprises reducing the graphene oxide layer on the treated substrate to produce the reduced graphene oxide film.

13. The method of manufacturing a memristor device according to any one of claims 1 to 12, wherein the substrate is a polymer substrate.

14. The method of manufacturing a memristor device according to any one of claims 1 to 13, wherein the substrate is a cyclic olefin copolymer (COC) substrate.

15. The method of manufacturing a memristor device according to any one of claims 1 to 14, wherein the plasma is O_2 plasma.

16. The method of manufacturing a memristor device according to claim 1 to 15, wherein the photoresist layer coated on the polymer substrate is baked prior to the patterning the photoresist layer on the substrate.

17. The method according to claim 1 to 16, wherein the photoresist layer is Shipley PR1813.

18. The method according to any one of claims 1 to 17, wherein the treated substrate is spun subsequent the deposition of the graphene oxide layer.

19. The method according to any one of claims 1 to 18, wherein the treated substrate is baked subsequent the coating of the substrate with graphene oxide.

20. The method according to any one of claims 1 to 19, wherein the treated substrate is sonicated subsequent to removing the photoresist layer on the treated substrate using acetone.

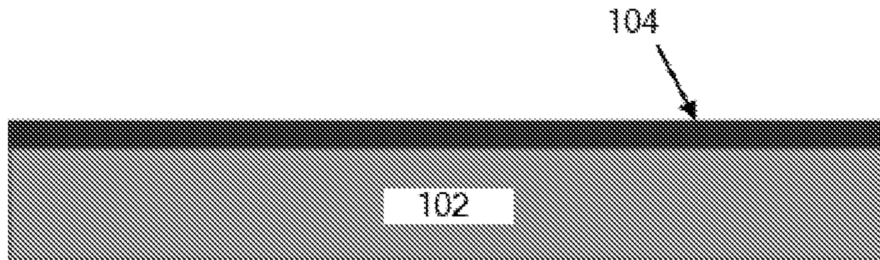

FIGURE 1 (a)

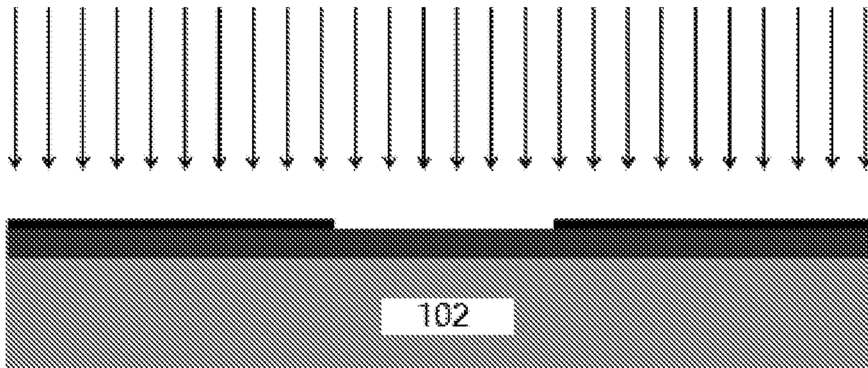

FIGURE 1 (b)

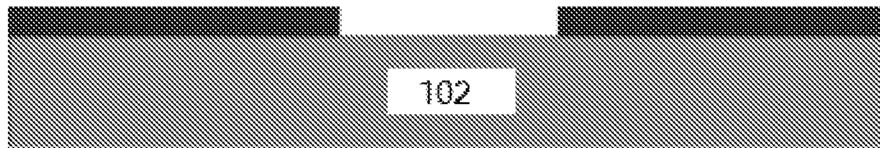

FIGURE 1 (c)

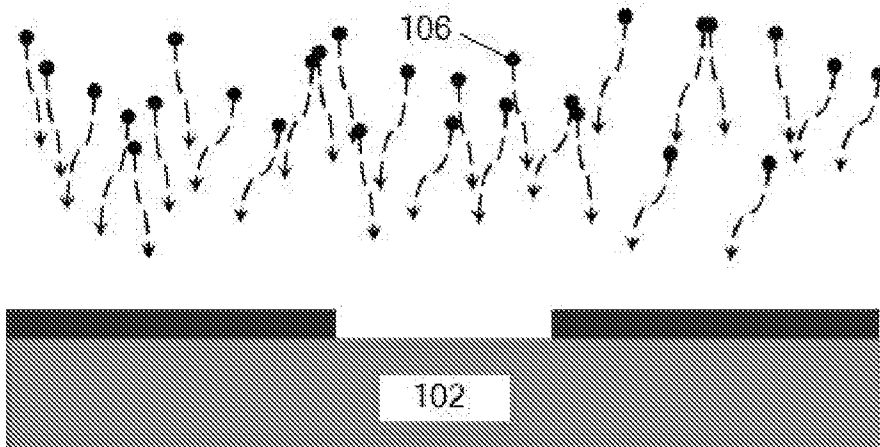

FIGURE 1 (d)

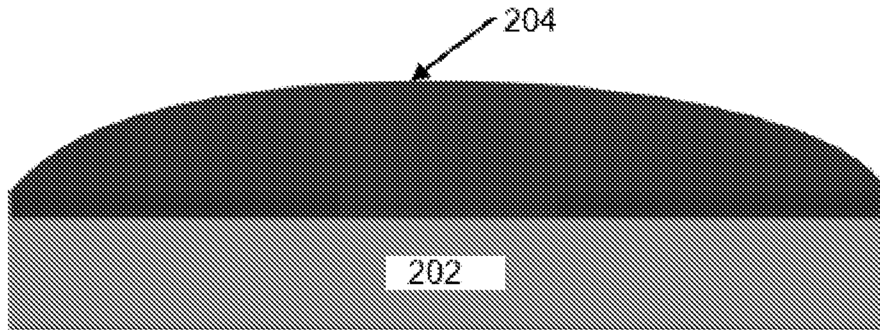

FIGURE 2 (a)

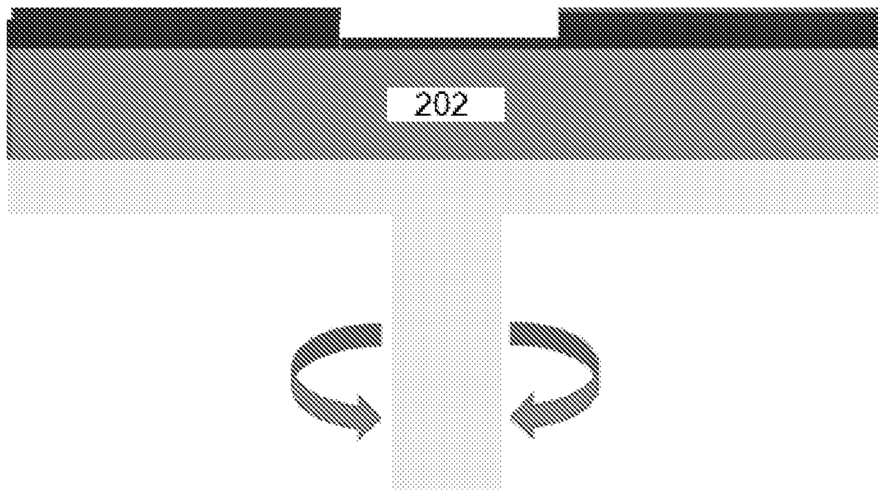

FIGURE 2 (b)

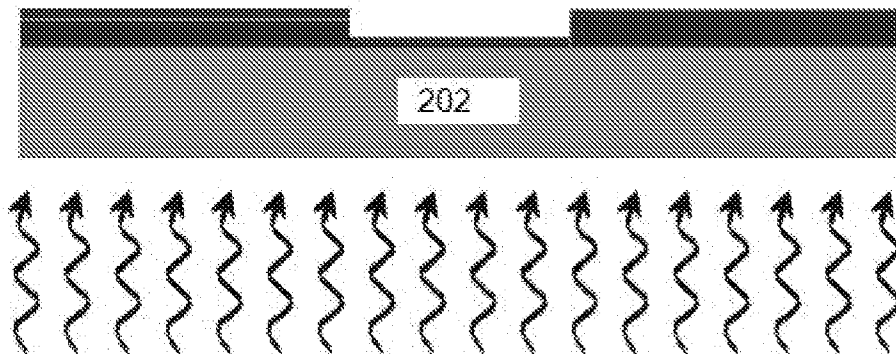

FIGURE 2 (c)

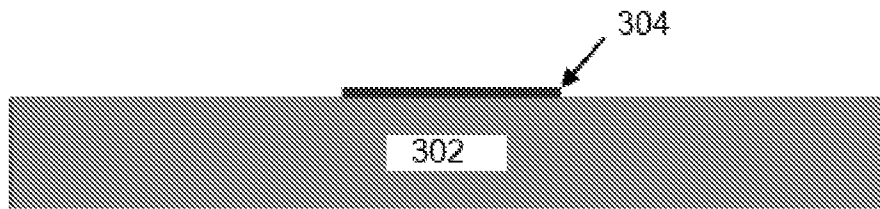

FIGURE 3 (a)

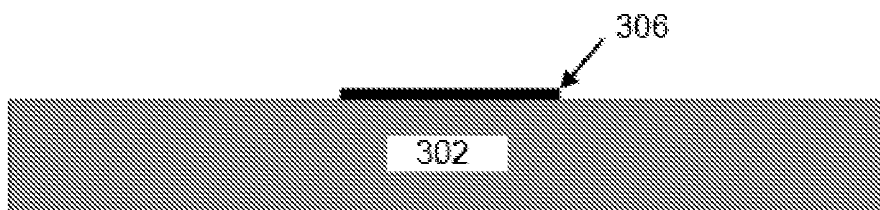

FIGURE 3 (b)

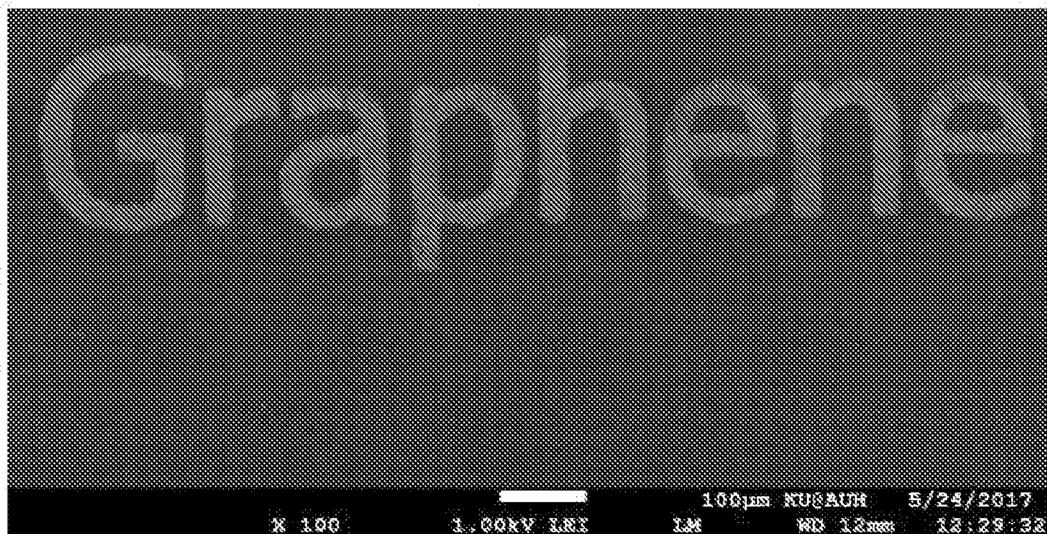

FIGURE 4

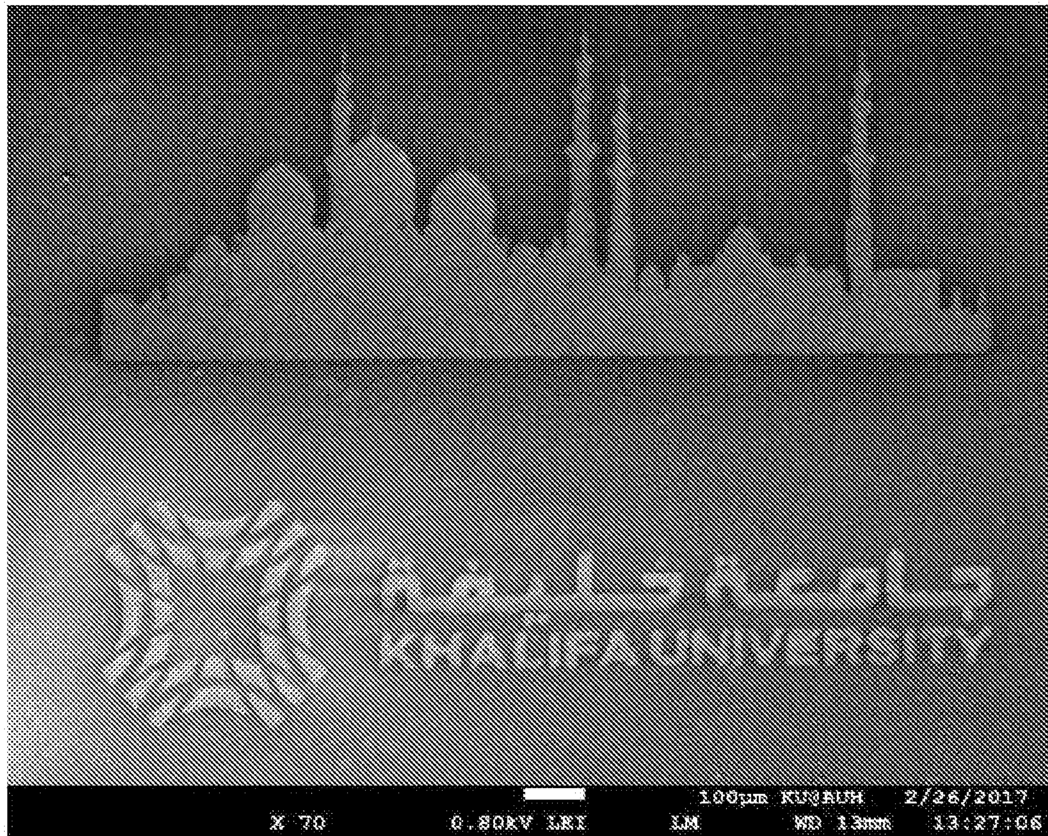

FIGURE 5

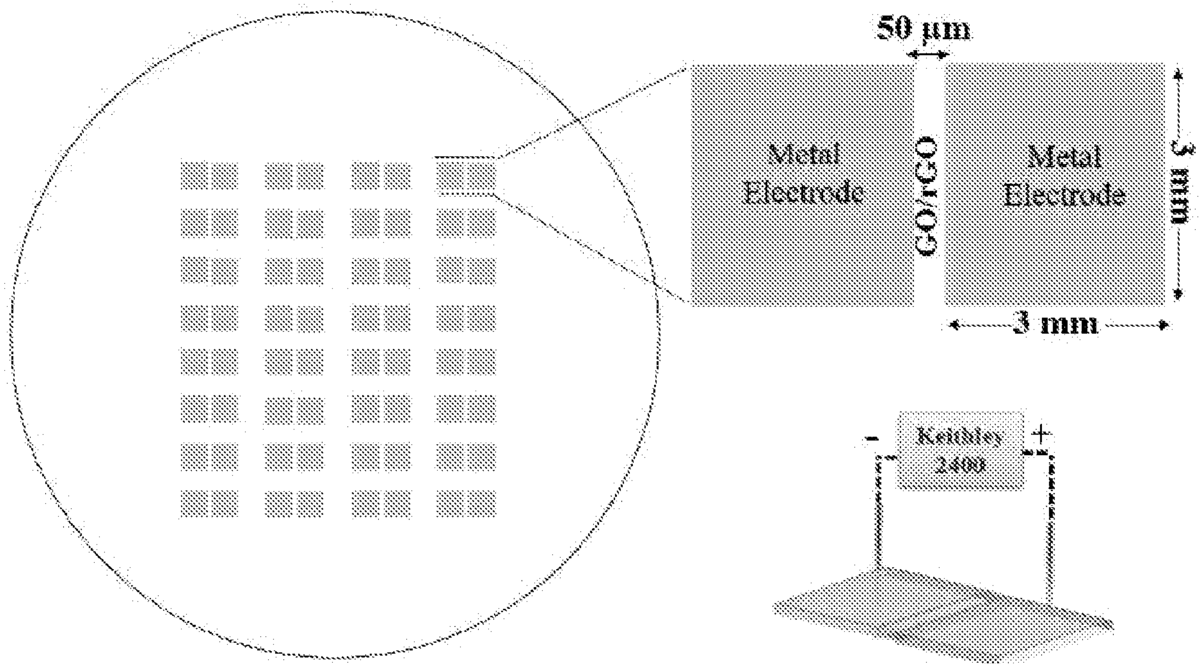

FIGURE 6

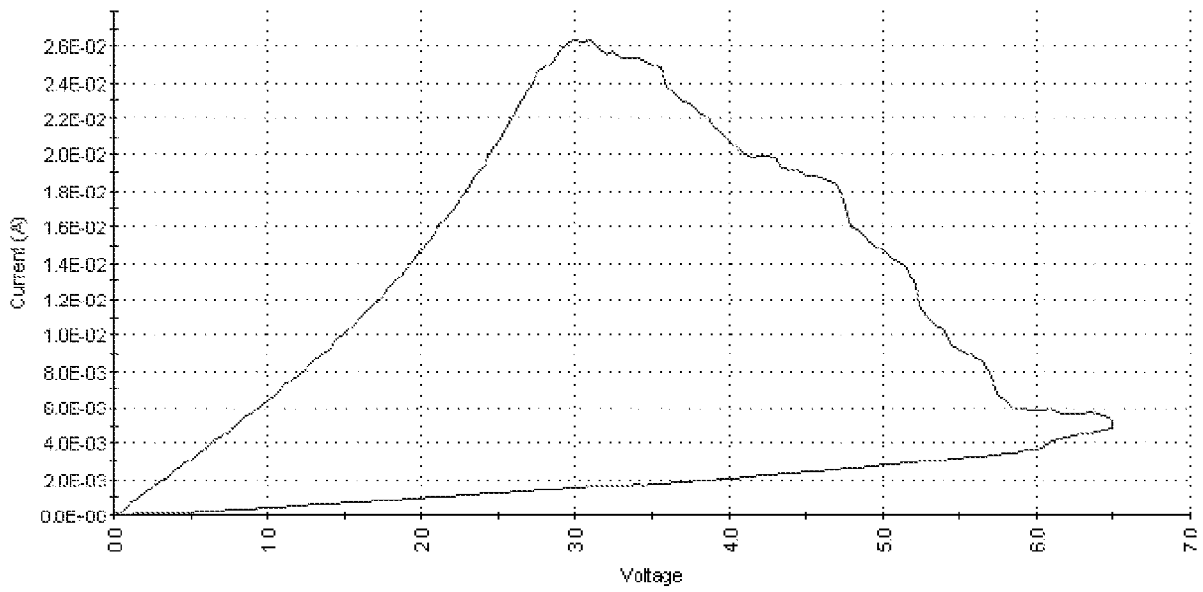

FIGURE 7 (a)

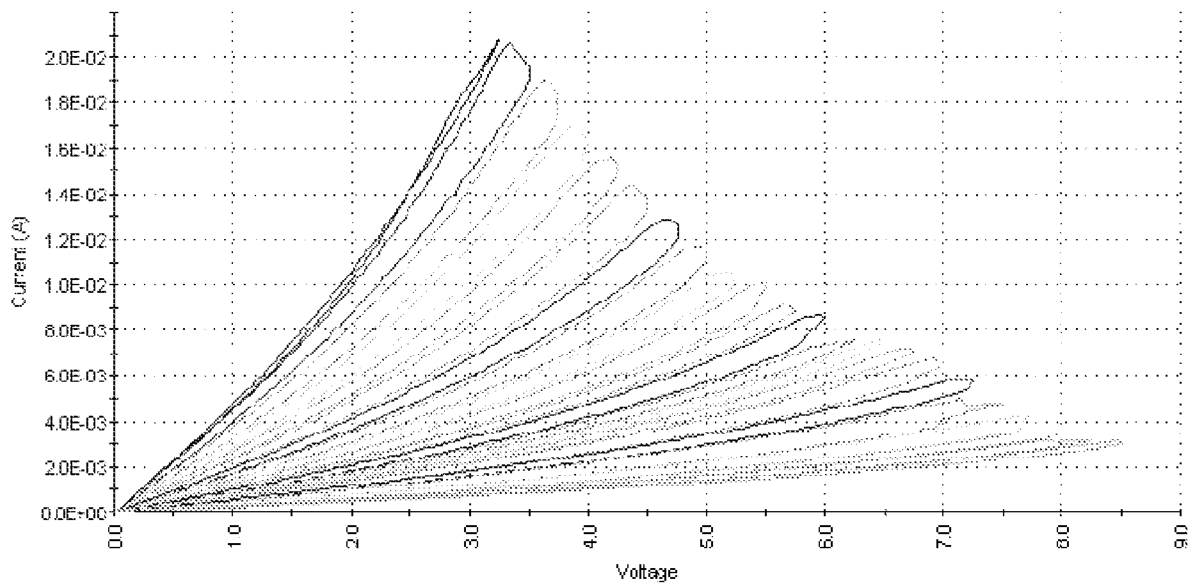

FIGURE 7 (b)

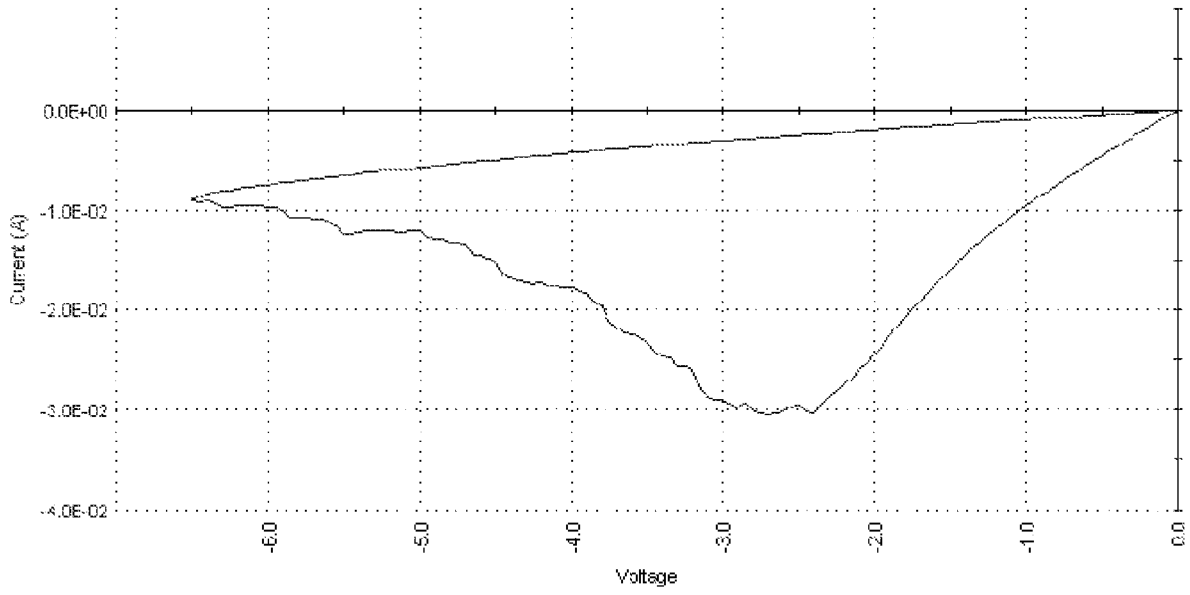

FIGURE 8 (a)

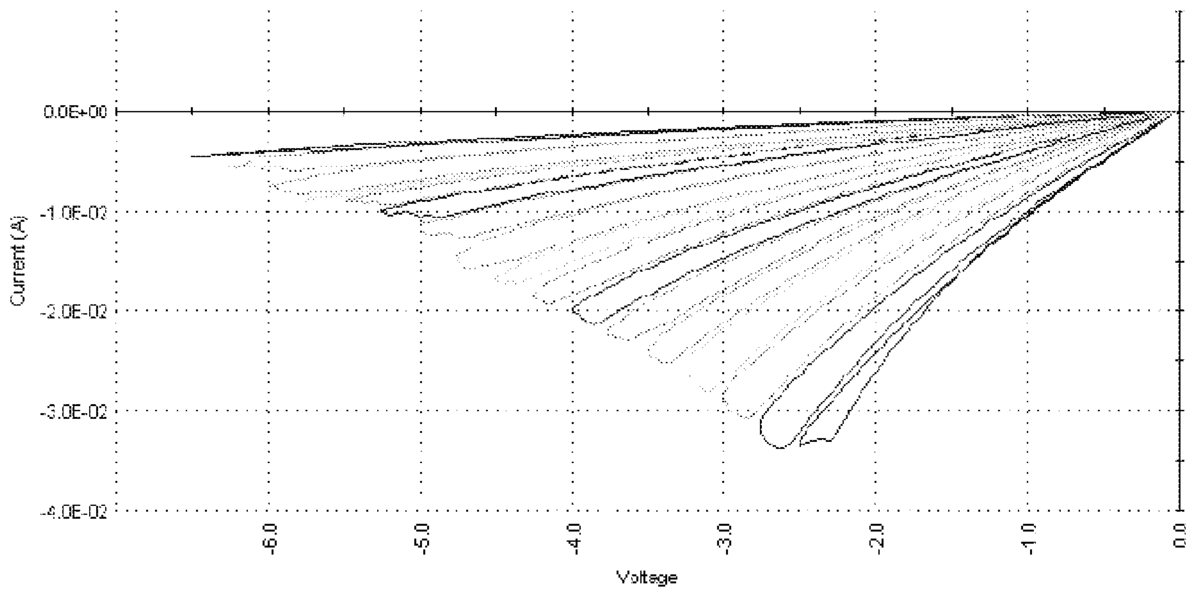

FIGURE 8 (b)

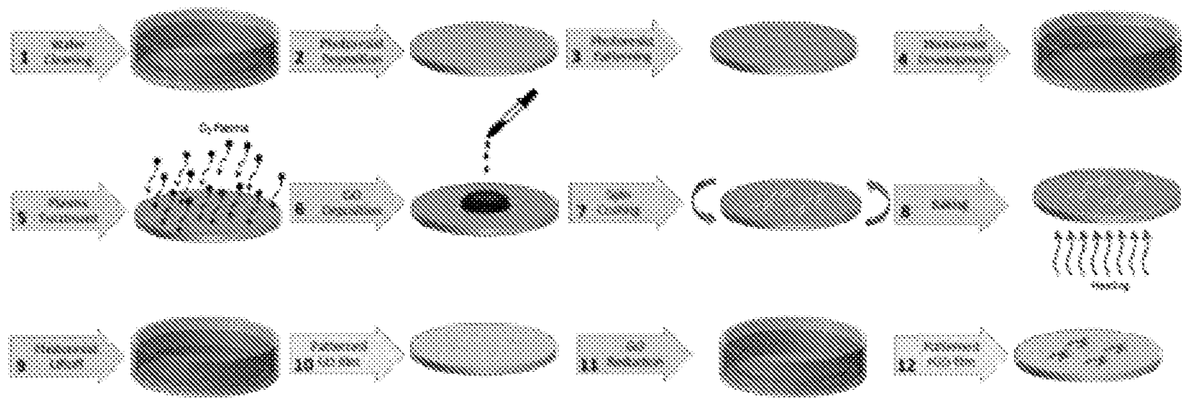

FIGURE 9

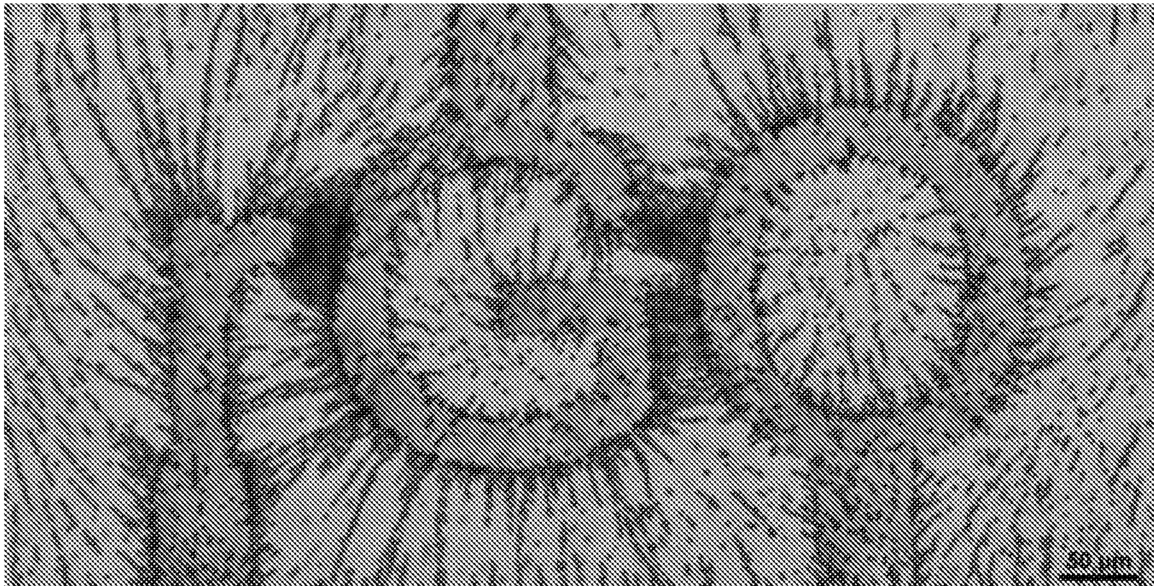

FIGURE 10