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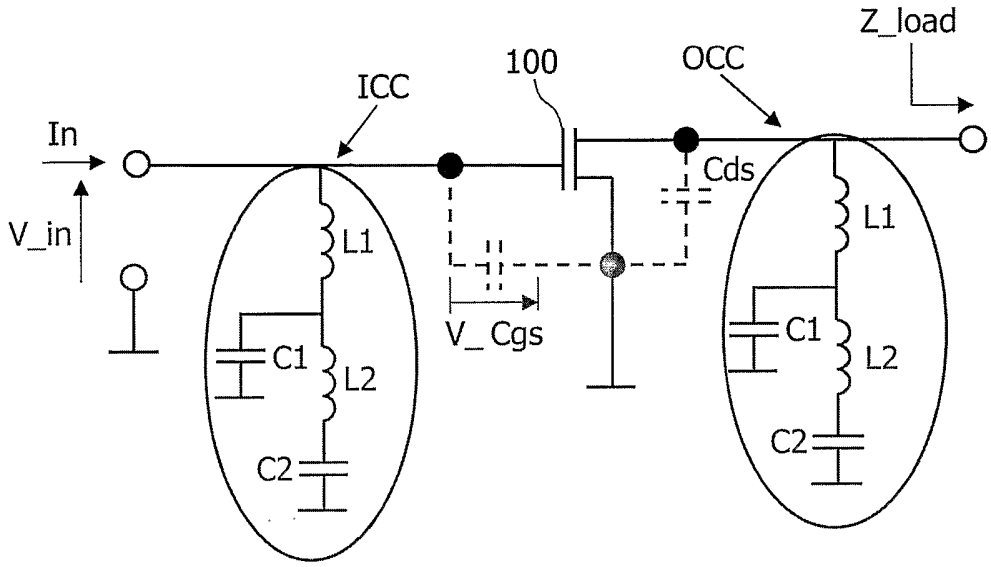
(54) Title: INTEGRATED F-CLASS AMPLIFIER WITH OUTPUT PARASITIC CAPACITANCE COMPENSATION



(57) Abstract: The present invention relates to an integrated F-class amplifier arrangement with a semiconductor power device (100) for receiving a first signal (In) and for amplifying the first signal (In) to generate a first amplified signal. Said F-class amplifier stage (100) comprises an output compensation circuit (OCC) for compensating a parasitic output capacitance of the at least first amplifier stage at fundamental frequency and at least one odd or even multiple thereof.

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Integrated F-class amplifier with output parasitic capacitance compensation

The present invention relates to an integrated F-class amplifier arrangement and a method of compensating of input and output parasitic capacitance of a semiconductor power devices at higher harmonic frequencies in such a F-class amplifier arrangement.

In order to achieve an ideal class-F wave form, the output voltage or current waveform should only contain higher odd-order or even order harmonics while the current waveform should only contain higher even-order or odd harmonics at proper phase arrangement.

In F. Raab "Class E, Class C and Class F Power Amplifiers based upon finite number of harmonics", IEEE MTT, v 49, N8, 2001 as well as in F. Raab "Class F Power Amplifiers with maximally flat waveform" IEEE MTT v. 45, N11, 1997, p. 2007, an improvement of the power amplifier efficiency for F-class technique amplifiers is shown. Within the F-class operation input/output voltage and current shaping is required for high efficiency performances. A major problem in the F-class performance of power devices is the parasitic output capacitance as it causes major difficulties in the design of the output circuitry at RF circuits. The parasitic capacitance at the drain or the collector of a transistor prevents the required high impedance seen by the transistor output at higher even or odd harmonics of the fundamental signal. This is in particular important for the so-called voltage peaking at even or odd harmonics. Currently the best F-class efficiency can be realized for devices with a frequency $f_0 <<$f_max as the parasitic capacitance C_{out} has relatively small negative effect on device performance in F-class and therefore negligible. Accordingly, a sufficient number and sufficient power of harmonics can be used. In addition, the output current wave of the device can be improved by respective input signal shaping which requires a specific input impedance response at the fundamental signal and its harmonic signals.

It is therefore an object of the invention to provide an improved F-class amplifier arrangement with a compensated output parasitic capacitance at higher harmonic frequencies.

This object is achieved by an integrated F-class amplifier arrangement as claimed in claim 1, an output compensation circuit as claimed in claim 11 and by a method of

compensating an output parasitic capacitance of such a F-class amplifier arrangement as claimed in claim 13.

Therefore, an integrated F-class amplifier arrangement is provided with a semiconductor power device and an output compensation circuit for compensating a parasitic output capacitance of the power device at fundamental frequency and at least one odd or even multiple thereof.

Accordingly, this measure serves to suppress the power of higher harmonics of the fundamental frequency at the output of the F-class amplifier arrangement. The power of undesired harmonics can be suppressed in two different ways: by providing very high or very low impedance to the output of the power transistor at frequency of specific harmonic. In this way the one component of output power of the harmonics is being eliminated, i.e. the voltage or the current, depending on the impedance presented to the device output- drain or collector. The suggested F-class output circuit is providing a high impedance for all odd harmonics and a very low impedance for all even harmonics or the way around. It is possible due to compensation of parasitic Cout of power device at several required harmonic (even or odd), where high impedance is required. Due to the properties of this circuit, it also at the same time provides a very low impedance or short circuit for all other harmonics.

The inductors of the output compensation circuit may be at least partly made of bond wires. Again, this provides the advantage of reduced power loss, especially at higher harmonics of the fundamental up to 15GHz.

The invention also relates to an output compensation circuit for compensating the parasitic output capacitance of a semiconductor power device in an F-class amplifier stage. The output compensating circuit comprises a series inductances and parallel capacitances or equivalents thereof.

The invention furthermore relates to a method for amplifying an input signal in a F-class amplifier arrangement. The parasitic output capacitance of the first amplifying stage is compensated at fundamental frequency and at least one odd multiple thereof.

The invention is based on the idea to provide a compensation circuit connected to the input/gate/base and/or output/drain/collector of RF power transistor (in a F-class amplifier) having parasitic input and/or output capacitance. The compensation circuits provide the parallel resonance with these parasitic capacitances at fundamental fo and parallel resonance or "short circuit" at its odd harmonics 3fo, 5fo etc and the "short circuit" or parallel resonance at even harmonics 2fo, 4fo etc. At required frequency of higher harmonics the compensation circuit helps to achieve a required output voltage or current wave shape by

proper phase of every each specific harmonic. The compensation circuit may consist of series inductances and parallel capacitances or equivalent made of distributed transmission lines. Alternatively, the compensation circuit comprises equivalents of the inductance and parallel capacitances made of distributed transmission lines.

If RF power devices are used in F-class amplifiers the parasitic output capacitance should be neutralized for those harmonics where the voltage peaking is required, i.e. which may be odd or even harmonics, depending to the which type of F-class amplification is required. The F-class operation is provided by peaking the odd or even harmonics of the voltage signal and the even or odd harmonics of the current signal by a compact and effective circuit when applied to the input and/or output of the power device. Accordingly, the shape of the output current signal of the device corresponds to a half sine-wave and the shape of the output voltage signal corresponds to a sine-wave with a flattened top as well as bottom sides. In the ideal case, i.e. at $f_0 << f\_max$, the shape of the output voltage wave signal approaches to a rectangular shape.

For better power efficiency of F-class amplification a compensation circuitry at the input side of the power device should be able to provide a reduced rise and fall time of the output current. For MOS, FET and LDMOST devices such a compensation circuit must provide a rectangular-like shape of the voltage across the input capacitance C_{gs} with emphasized voltage of all odd harmonics. If in such a case the input voltage signal is substantially of rectangular voltage shape, then the output current pulse may result in a minimal rise and fall time. Accordingly, the conditions for F-class amplification are provided. A similar input compensation circuit as described for the output capacitance will result in high input impedance at odd harmonics and peaking of the odd harmonics and rectangular voltage across input of the device. Thus, a higher efficiency performance can be delivered .

The compensation circuit may be connected to input/gate/base and/or output/drain/collector of RF power device.

The present invention will now be described based on a preferred embodiment with reference to the accompanying drawings, in which:

Fig. 1 shows a circuit diagram of an amplifier arrangement according to a preferred embodiment;

Fig. 2 shows a harmonic current distribution in the circuit diagram of an amplifier arrangement according to Fig. 1;

Fig. 3 shows a circuit diagram of an amplifying arrangement according to a second embodiment;

Fig. 4 shows a frequency characteristics of the real and imaginary part of the impedance of an output compensation circuit with an output parasitic capacitance as seen by power device;

Fig. 5 shows a circuit diagram of the output part of the amplifying arrangement according to a third embodiment;

Fig. 6 shows a frequency characteristics of the impedance of the output compensation circuit of Fig. 5;

Figs. 7A and 7B show a circuit diagram of the amplifying arrangement of Fig. 5, and an implementation example of the circuit diagram of Fig. 7A;

Fig. 8 shows a graph of the output power and power added efficiency versus input power;

Fig. 9 shows a graph of the one tone output power and IMD power levels vs input power of the F-class amplifier versus AB-class amplifier;

Fig. 10A shows another embodiment of an output network for an integrated F-class type amplifier with an F-class circuit; and

Fig. 10B shows an implementation of the circuit of Fig. 10A.

The preferred embodiment will now be described in connection with an MMIC (Monolithic Microwave Integrated Circuit) Technology, which may be used in a transceiver design of a wireless system or any other radio frequency (RF) system. The application of MMIC technology has enabled miniaturization of microwave and millimeter-wave systems, combined with increasing performance.

In mobile RF transceivers of emerging wireless systems such as WCDMA, CDMA2000 or Wireless Local Area Network (WLAN) systems according to the IEEE 802.11 (a)/(g) standard, power amplifiers are used in transmitter stages, where the modulated RF signal is amplified before being supplied to the antenna for wireless transmission. These power amplifiers are the most power consuming part of these RF transceivers. Using the F-class type amplifier arrangement in Doherty type amplifier can provide a higher power efficiency of transmitter.

In the power amplifier arrangement according to the preferred embodiment a F-class amplifier structure is used, where circuit size is reduced for integration by using lumped elements to replace distributed circuit like power splitters and transmission lines. Furthermore, inductive coupling is used to increase inductance values and output parasitic capacitances are used as a part of lumped element analog transmission lines. Moreover, to avoid power losses in lumped elements and provide stable characteristic impedance in a wide frequency band including 2fo...nfo harmonics of fundamental signal, bond wires are suggested to be used as inductances. Bondwires provide very high parasitic parallel resonance frequency, e.g. above 15 GHz , as lumped inductance suitable for building a wideband lumped element equivalent of an RF transmission line.

The F-class amplifier may comprise a power device in bipolar technology, MOS (Metal Oxide Semiconductor) technology, LDMOST (Lateral Defused Metal Oxide Semiconductor Transistor) technology, FET (Field Effect Transistor) technology, or HBT (Heterojunction Bipolar Transistor) technology. The LDMOST technology provides high gain and good linearity compared to the other semiconductor technologies. However, complex modulation schemes, like WCDMA, make further device improvements for linearity still very desirable. For example, HBT MMIC power devices may be used, where the heterojunction increases breakdown voltage and minimizes leakage current between junctions.

Fig. 1 shows a circuit diagram of an amplifier arrangement according to a preferred embodiment. Here, the amplifier arrangement comprises an input compensation circuit ICC, an F-class amplifier 100 and an output compensation circuit OCC. The F-class amplifier 100 comprises a parasitic output capacitance Cds. The input signal In is received by the input compensation circuit ICC and the output compensation circuit OCC is connected to the output of the amplifier 100. The input compensation circuit ICC as well as the output compensation circuit OCC each comprise a first inductor L1, a second inductor L2 and a second capacitor C2 in series connection with a first capacitor C1 connected in parallel to the junction point of the first and second inductor L1, L2 and the ground or reference potential. The input compensation circuit as well as the output compensation circuit both serve as compensation for the parasitic output capacitor Cds. It should be noted that the angle between Vds and Id depends on a combination of the Z_{load} and the resonance frequency of the Internal Shunt Inductance (INSHIN) circuit.

In Fig. 2 a circuit diagram of an F-class amplifier arrangement according to Fig. 1 is shown. The circuit diagram of Fig. 2 substantially corresponds to the circuit diagram

of Fig. 1. By the respective selection of the first and second inductance L1, L2 as well as the first and second capacitor C1, C2 the frequencies, for which the parasitic capacitance Cgs, Cds are compensated by the parallel resonance circuit in the input compensation circuit ICC and in the output compensation circuit OCC are defined. In the output compensation circuit OCC the current I_{f0} will travel mostly through the parasitic capacitance Cds, the first and second inductance L1, L2 and the second capacitor C2. The current I_{f0+2f0} will mainly pass through the parasitic capacitance Cds, the first inductance L1 and the first capacitor C1. Therefore, this current will be defined mainly by these three elements.

Fig. 3 shows a circuit diagram of an amplifying arrangement according to a second embodiment. The circuit diagram of the third embodiment substantially corresponds to the circuit diagram of the preferred embodiment according to Fig. 1 and Fig. 2. However, the circuit diagram according to the third embodiment is shown for the case when $f_0 << f_{max}$ of the RF power device. Accordingly, more higher order harmonics may be used for better shaping of the output voltage and current waves. Therefore, the output compensation circuit OCC now comprises a first, second and third inductance L1, L2, L3 and a third capacitor C3 in series connection, while the first capacitor C1 is connected in parallel between the junction point of the first and second inductor L1, L2 and ground or reference potential. The second capacitor C2 is arranged in parallel between the junction point of the second and third inductor L2, L3 and ground or reference potential. The current I_{f0} will flow through the parasitic capacitance Cds, the first, second and third inductor L1, L2, L3 and the third capacitor C3. The current with the 2fo harmonics will flow through the parasitic capacitance Cds, the first and second inductor and the second capacitor C2. The current for the 4f0 harmonics will flow through the capacitance Cds, the first inductor L1 and the first capacitor C1. In case of very high operation frequency in the microwave and millimeter wave band, when the L1 and L2 required values may become very low and less available as a bondwires, than they can be made as a short microstripline cuts, providing a good quality factor and reproducibility in mass production.

Fig. 4 shows the frequency characteristic of the real (upper positive curve) and imaginary (lower positive and negative curve) part of the impedance Z1 presented by the output compensation circuit OCC to the transistor output according to the second embodiment of Fig. 8. It can be seen from Fig. 4 that the effect of the parasitic output capacitance Cds is neutralized or compensated at the odd harmonics fo, 3fo, 5fo. However, the "short" circuit characteristics are maintained at even harmonics (2fo, 4fo and 6fo). An adaptation to the load impedance Z1 (e.g. 50 Ohm) is provided selectively at the fundamental

frequency fo and the odd-fold of the fundamental frequency 3fo, 5fo. At these frequency points, the imaginary part of the impedance is zero. Furthermore, at the even-fold fundamental frequency 2fo, 4fo and 6fo both real part and imaginary part of the impedance are substantially zero, which corresponds to a short circuit, so that the even-fold fundamental frequency harmonics power is blocked by the compensation circuit OCC. This arrangement provides a rejection of even-fold 2fo, 4fo harmonics power at the output of F-lass amplifier which are the root cause of inter-modulation distortions. Also a compensation of output capacitance of RF power devices at 3fo, 5fo together with $\lambda/4$ line or lumped element analog, attached between device output and load provide a high impedance around 3fo, 5fo and voltage wave shape at transistor collector or drain.

Fig. 5 shows a circuit diagram of the output part of the amplifying arrangement according to a third embodiment. This circuit diagram is based on the output part of the circuit diagram of Fig. 3. It also comprises three inductance in series L11, L12, L19 to a third capacitor C11, while a first capacitor C6 is connected in parallel between the junction point of the first and second inductor L12, L19 and ground or reference potential and the second capacitor C7 is connected in parallel between the junction point of the second and third inductor L12, L19 and ground or reference potential. The circuit diagram also comprises an emphasizing circuit EC and a load Ld connected in parallel to the output compensation circuit OCC. The emphasizing circuit EC comprises two inductors L15, L16 and two capacitors C4, C5. The two inductors L15, L16 are connected in parallel with a capacitor C5 coupled between respective first ends of the two inductors L15, L16. The second ends of the inductors L15, L16 form a junction point. The capacitor C4 is connected between this junction point and ground or reference potential. This emphasizing circuit EC serves to emphasize the higher odd harmonics of fo.

Fig. 6 shows a frequency characteristic of the real and imaginary part of the impedance Z1 of the output compensation circuit OCC with an additional $\lambda/4$ line between the output compensation circuit OCC and the load.

Fig. 7A shows a circuit diagram of the amplifying arrangement of Fig. 5. Fig. 7B shows an implementation example of the circuit diagram of Fig. 7A. On the right hand side of this figure, the circuit diagram of the output compensation circuit and the emphasizing circuit EC is shown in Figs. 7A and in Fig. 7B the implementation of the lumped elements is shown. On the left hand side of the figure, i.e. the input side, the input compensation circuit ICC is shown as circuit diagram in Fig. 7A and as implementation in Fig. 7B. The amplifier 100 is embodied as a MOSFET amplifier. The output compensation circuit OCC and the

emphasizing circuit EC are designed as a lumped element matching circuit for the output of F-class amplifier. The input compensation circuit ICC forms as input LC pre-match circuit.

Fig. 8 shows a graph of the output power and power added efficiency versus input power for F-class and AB-class amplifiers.

Fig. 9 shows a graph of the output power and IMD power level of F-class versus AB-class amplifier.

Fig. 10A shows another embodiment of an output network for an integrated F-class type amplifier with an F-class circuit. Fig. 10B shows a circuit implementation of the output network of Fig. 10A for microwave or millimeter wave frequency band amplifiers.

In Fig. 10B the input In of the is connected to the active die area AA of the power device in Fig. 10A. The inductors L2 to L5 are implemented as bond wires. The substrate Sub may be Si, GaAs etc. The main difference regarding the implementation of Fig. 10B compared to the implementation of Fig. 7A and 7B is the first inductor L1. In Fig. 7B this inductor L1 is implemented as a bond wire while in Fig. 10B the inductor is embedded in the substrate. This solution provides the best repeatability and precision of the small inductance value to achieve. In addition, L4, L5 and C4 form the emphasizing circuit. A similar design can be used for input parasitic capacitance compensation, because its value is usually higher and requires even smaller value of compensation inductance required.

Accordingly, a lumped element compensation circuit comprising a series inductance and parallel capacitance connected to the input/gate and/or output/drain collector of a RF power transistor with parasitic input capacitance and parasitic output capacitance is provided. A parallel resonance of these parasitic capacitances at the fundamental frequency fo and its odd harmonics 3fo, 5fo and the RF "short circuit" at even harmonics 2fo, 4fo is provided.

The output circuitry with the compensation circuit comprises distributed or lumped elements analog of the transmission line, wherein the output circuitry is connected between the output of the transistor and the transistor load.

As mentioned above a major problem in realizing the F-class performance of power device for the case of "flat voltage" at transistor output is a development of special circuitry for compensation of the output, drain or collector parasitic capacitance at odd or even harmonics depending on required F-class operation mode. It is required for correct phase of odd harmonics voltage to achieve a flatten output voltage wave. Also in this case a "short circuit" at even harmonics is required to provide a half sine-wave shape of output current. The best F-class efficiency can be realized when device is used at frequency fo <<

f_max, which allows for high levels of current harmonics in the output signal. The device can be improved by shaping the input signal, where the required current and/or voltage harmonics amplitudes and phases are properly arranged.

A simple, compact and effective circuitry, i.e. the above compensation circuit, can be applied to the input and output of power device providing the F-class operation by peaking the even or odd voltage harmonics and odd or even current harmonics or the way around if required. As a result the device's output current shape approaches the half sine-wave or rectangular shape and the output voltage has a shape approaching a rectangular shape with flatten top and bottom sides or half-sine wave shape, which in ideal case at fo<< f_max becomes of rectangular shape. Input circuitry should provide a conditions for decreasing of "Rise" and "Fall" time of output current. In case of the LDMOST devices the compensation circuit for input capacitance must maximize the input impedance and RF voltage at fo and all odd harmonics, providing required harmonic's phase, anti-phase or 180 degree between fundamental and 3rd harmonic, for example. Due to the fact that LDMOST devices usually are operating at frequencies which are close to the f_max like 8 GHz, only a few first harmonics 2fo, 3fo, 4fo can be used for F-class operation. So, better efficiency in F-class operation can be achieved, if in this case the input signal is of "rectangular" voltage shape. Than output current pulse will have minimal possible "rise" and "fall" time, providing better conditions for F-class mode amplifications. With similar compensation circuit for output parasitic capacitance, the transistor output will see the load with high impedance at odd or even, if required harmonics of fundamental, which will peak the output voltage or current at odd or even harmonics, delivering a higher efficiency.

It is further noted that the present invention is not limited to the above preferred embodiments and can be varied within the scope of the attached claims. In particular, the described drawing figures are only schematic and are not limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. Where the term 'comprising' is used in the present description and claims, it does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun, e.g. 'a' or 'an', 'the', this includes a plural of that noun unless something else is specifically stated. The terms first, second, third and the like in the description and in the claims are used for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is to be understood that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein. Moreover, although preferred embodiments, specific

constructions and configurations have been discussed herein, various changes or modifications in form and detail may be made without departing from the scope of the attached claims.

CLAIMS:

1. An integrated F-class amplifier arrangement, comprising:

- a semiconductor power device (100) for receiving a first signal (In) and for amplifying the first signal (In) to generate a first amplified signal; and

- an output compensation circuit (OCC) for compensating a parasitic output capacitance (Cds) of the power device (100) at fundamental frequency and at least one odd or even multiple thereof.

2. An amplifier arrangement according to claim 1, further comprising:

- an input compensation circuit (ICC) for compensating a parasitic input capacitance of the power device (100).

3. An amplifier arrangement according to claim 1 or 2, wherein said input and/or output compensation circuit (ICC, OCC) is adapted to provide a high or low impedance at a frequency of at least one odd multiple of said fundamental frequency and a low or high impedance at a frequency of at least one even multiple of said fundamental frequency, respectively.

4. An amplifier arrangement according to claim 3, wherein the input and/or output compensation circuit (ICC, OCC) comprise a series inductances and parallel capacitances or equivalents thereof.

5. An amplifier arrangement according to claim 4, wherein said input and/or said output compensation circuit (ICC, OCC) comprise at least two inductors (L1, L2) and two capacitors (C1, C2) or their equivalents.

6. An amplifier arrangement according to claim 5, wherein said inductors of said input and/or output compensation circuit (ICC, OCC) are made at least partly of bond wires.

7. An amplifier arrangement according to claim 1, wherein said semiconductor power device (100) comprise at least one of bipolar elements, metal oxide semiconductors, LDMOST elements, field effect transistors, and HBT elements.

8. An amplifier arrangement according to claim 1, wherein said semiconductor power device (100) is adapted for RF, microwave or millimeter wave frequencies.

9. An amplifier arrangement according to claim 5, wherein said input and/or output compensation circuit (ICC, OCC) comprise at least two inductors (L1, L2) and a first capacitor (C2) connected in series with a second capacitor (C1) coupled in parallel.

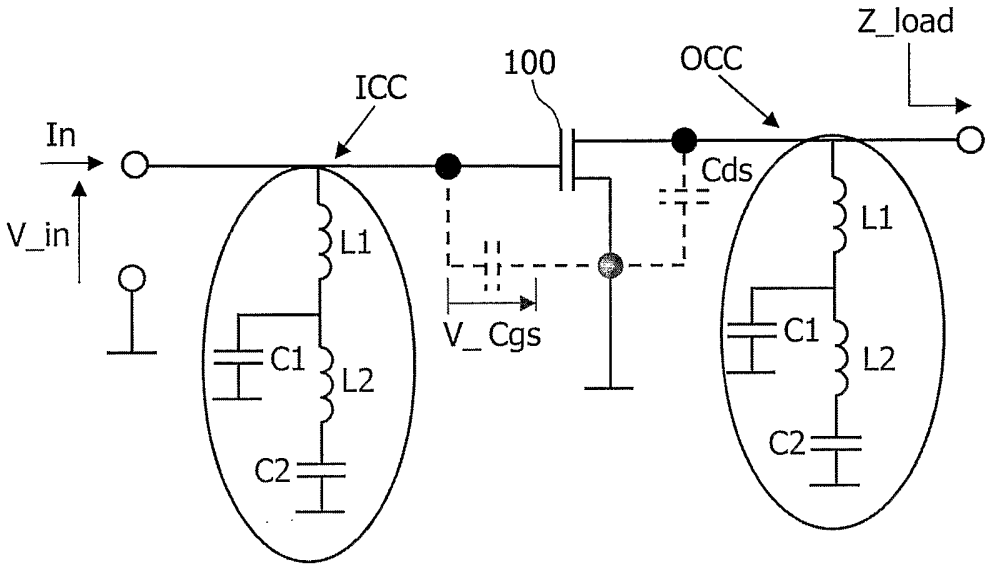
10. An amplifier arrangement according to claim 1, further comprising an emphasizing circuit (EC) coupled in parallel to the output compensation circuit (OCC) for emphasizing higher odd or even harmonics of the fundamental frequency.

11. Output compensation circuit for compensating the parasitic output capacitance of a semiconductor power device in a F-class amplifier stage, comprising a series inductances and parallel capacitances or equivalents thereof.

12. Output compensation circuit according to claim 11, comprising at least a first and second inductance (L1, L2) and a first capacitance (C1) connected in series, and at least a second capacitance (C2) coupled in parallel.

13. Method for amplifying an input signal in a F-class amplifying arrangement, comprising the steps of:

- amplifying a first signal in a F-class amplifier to generate at least a first amplified signal, and
- compensating a parasitic output capacitance of the F-class amplifying stage at fundamental frequency and at least one odd or even multiple thereof.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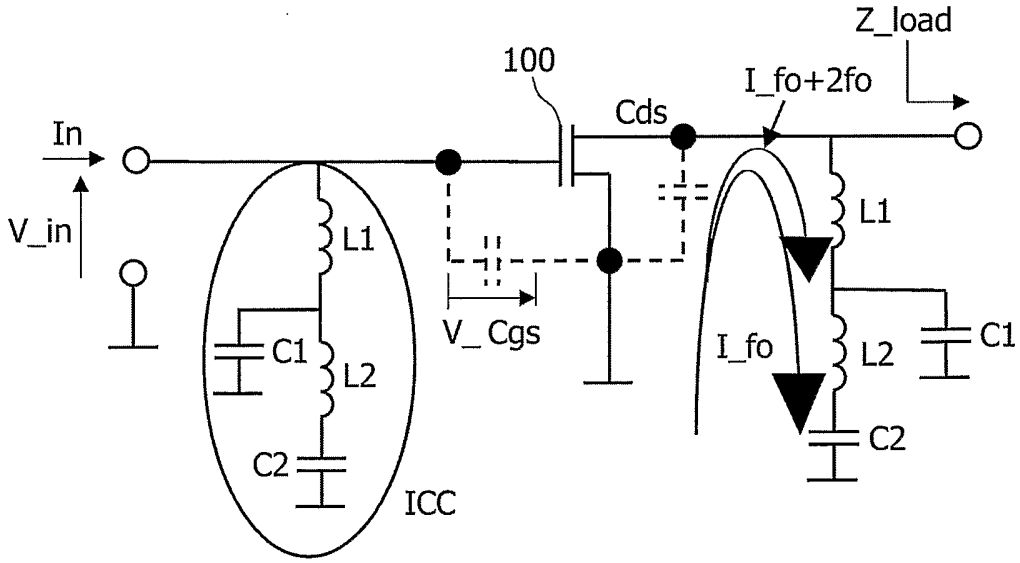
100
OCC
ICC
In
Cds
V_in
L1
C1
L2
V_ Cgs
C2
L1
C1
L2
C2

FIG.1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100
I_fo+2fo
Cds
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V_in
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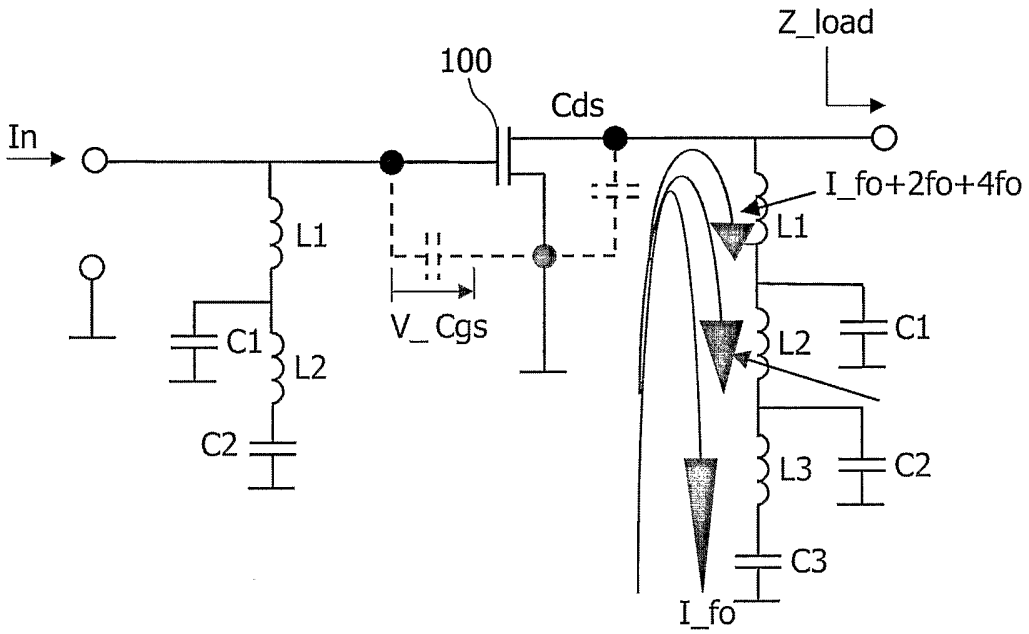
C1
L2
V_ Cgs
I_fo
L1
L2
C1
C2
C2
ICC

FIG.2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Cds
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C1
L2
C2
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I_fo+2fo+4fo
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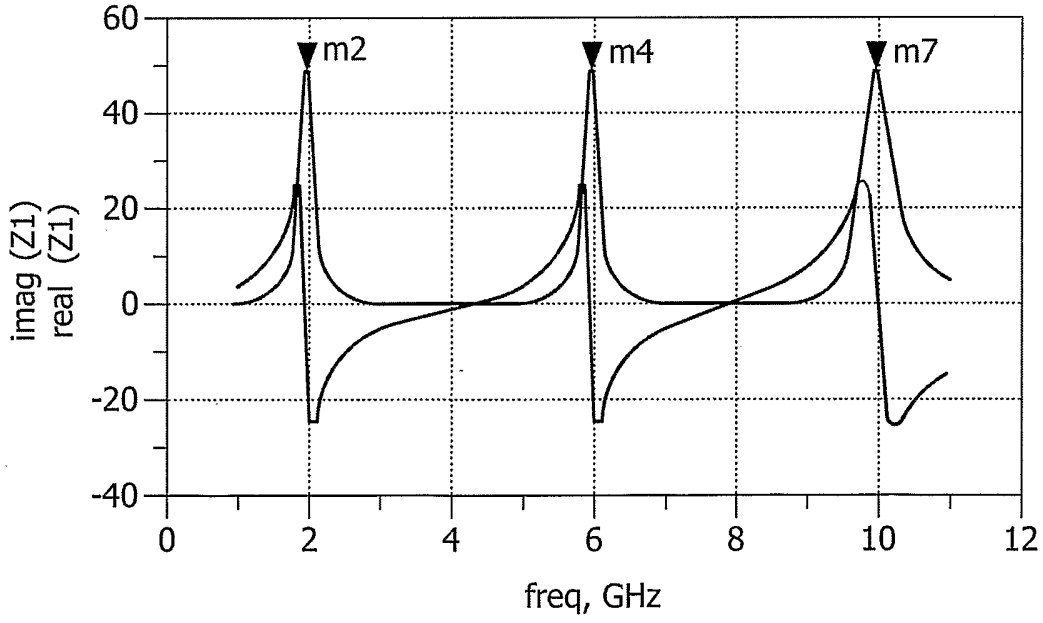
I_fo

FIG.3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20
0
-20
-40
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real (Z1)
m2
m4
m7
0
2
4
6
8
10
12
freq, GHz

FIG.4

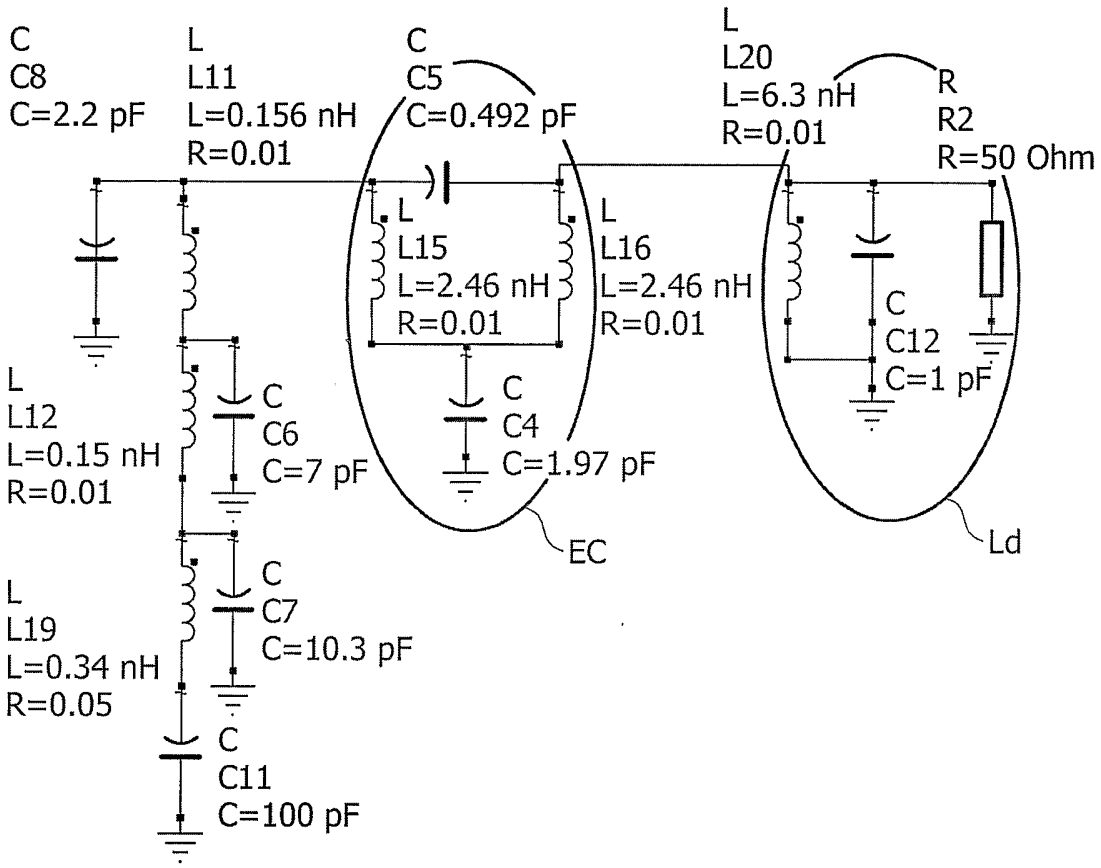
C
C8
C=2.2 pF
L
L11
L=0.156 nH
R=0.01
C
C5
C=0.492 pF
L
L20
L=6.3 nH
R=0.01
R
R2
R=50 Ohm
L
L15
L=2.46 nH
R=0.01
L
L16
L=2.46 nH
R=0.01
C
C12
C=1 pF
L
L12
L=0.15 nH
R=0.01
C
C6
C=7 pF
C
C4
C=1.97 pF
EC
Ld
L
L19
L=0.34 nH
R=0.05
C
C7
C=10.3 pF
C
C11
C=100 pF

FIG.5

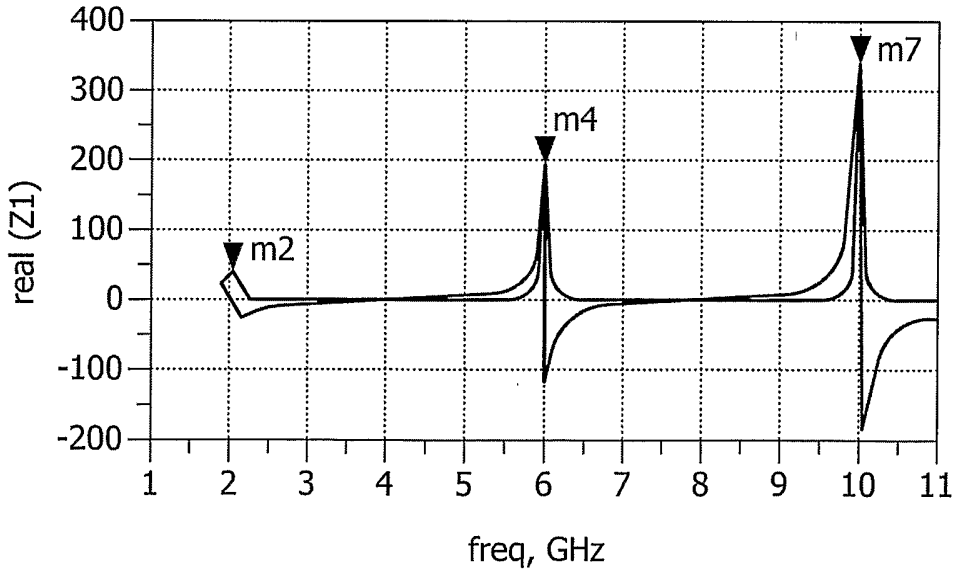
400
300
200
100
0
-100
-200
real (Z1)
m2
m4
m7
1
2
3
4
5
6
7
8
9
10
11
freq, GHz

FIG.6

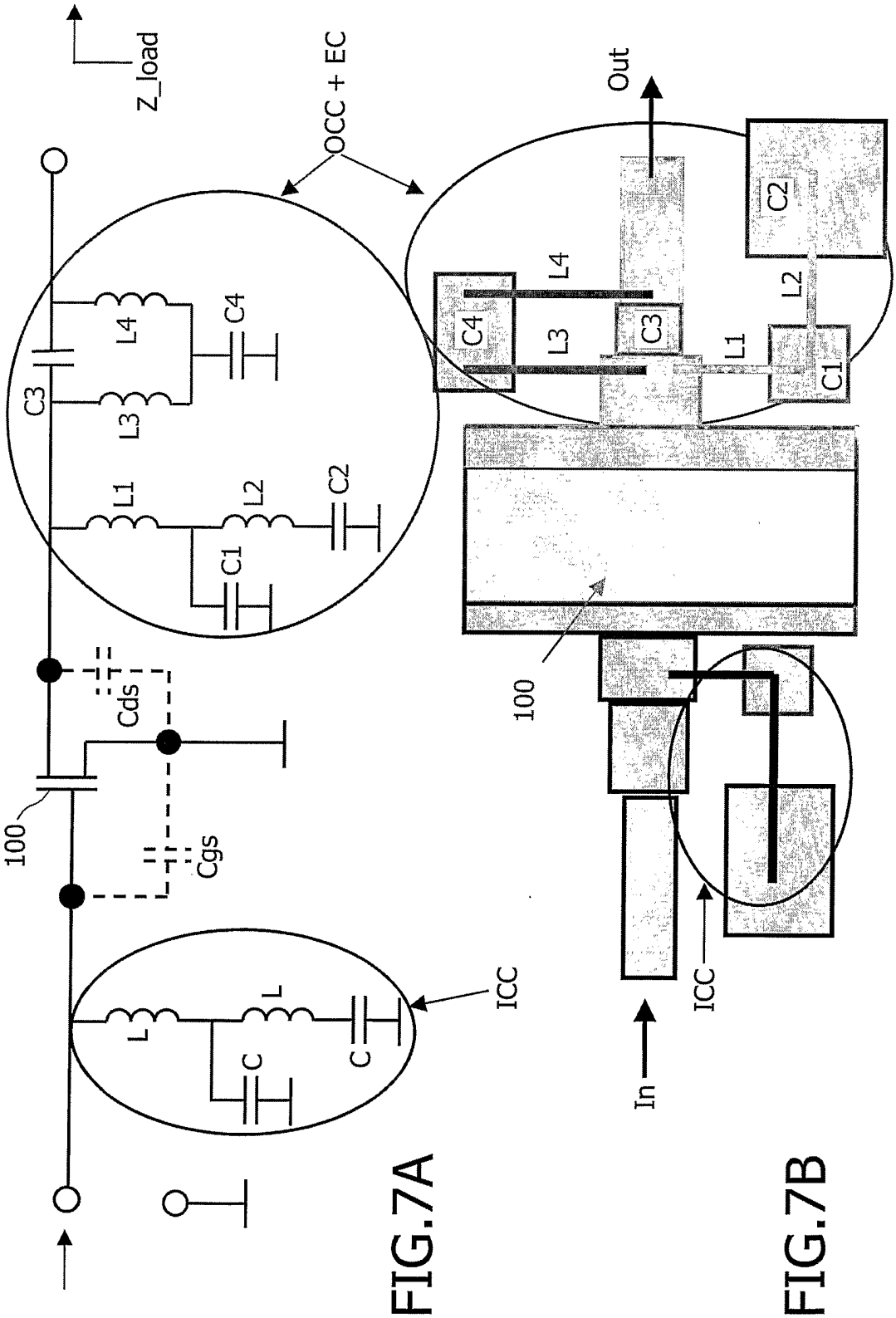
Z_load
OCC + EC
C3
L4
C4
L3
L1
L2
C2
C1
Cds
Cgs
100
L
C
ICC

FIG.7A

Out
C4
L4
L3
C3
L1
L2
C2
C1
100
In
ICC

FIG.7B

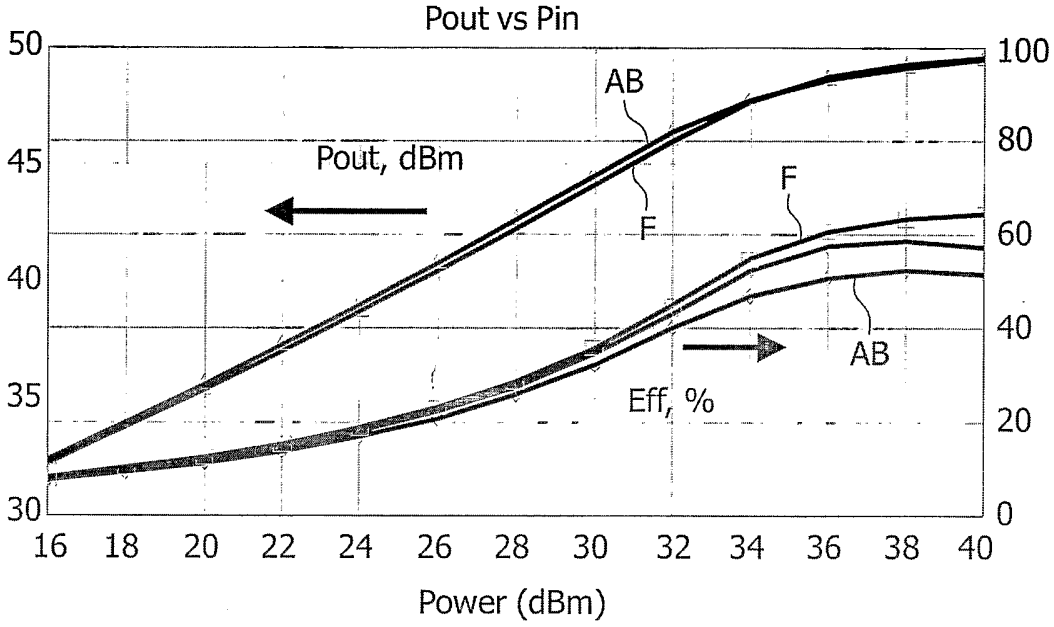
Pout vs Pin
50
45
40
35
30
100
80
60
40
20
0
AB
F
Pout, dBm
F
AB
Eff, %
16 18 20 22 24 26 28 30 32 34 36 38 40
Power (dBm)

FIG.8

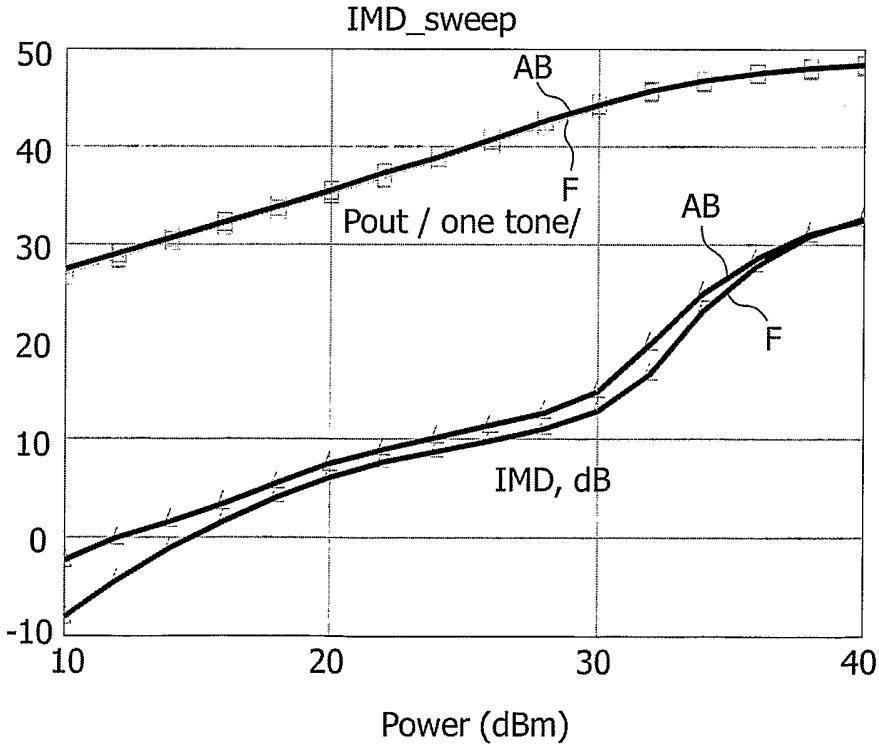
IMD_sweep
50
40
30
20
10
0
-10
AB
F
Pout / one tone/
AB
F
IMD, dB
10 20 30 40
Power (dBm)

FIG.9

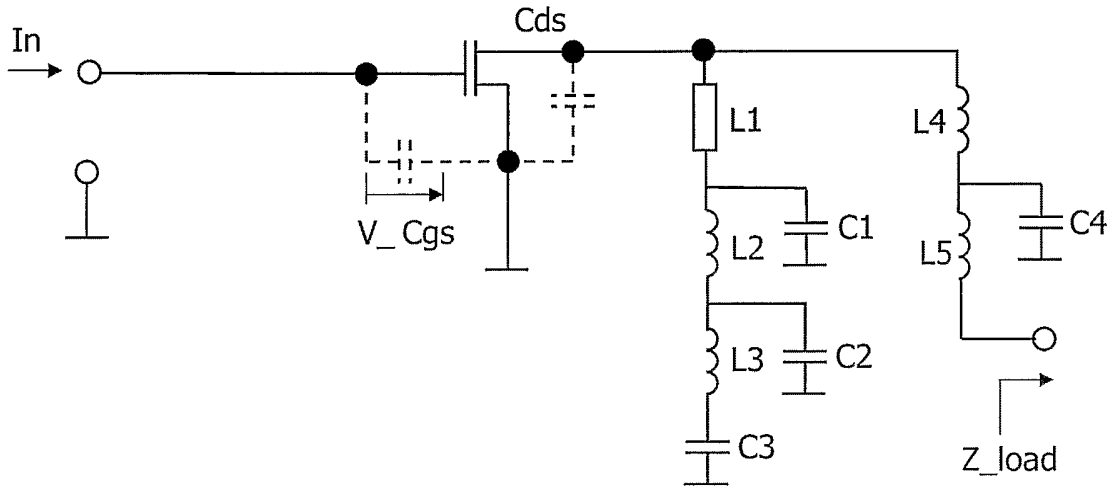

FIG.10A

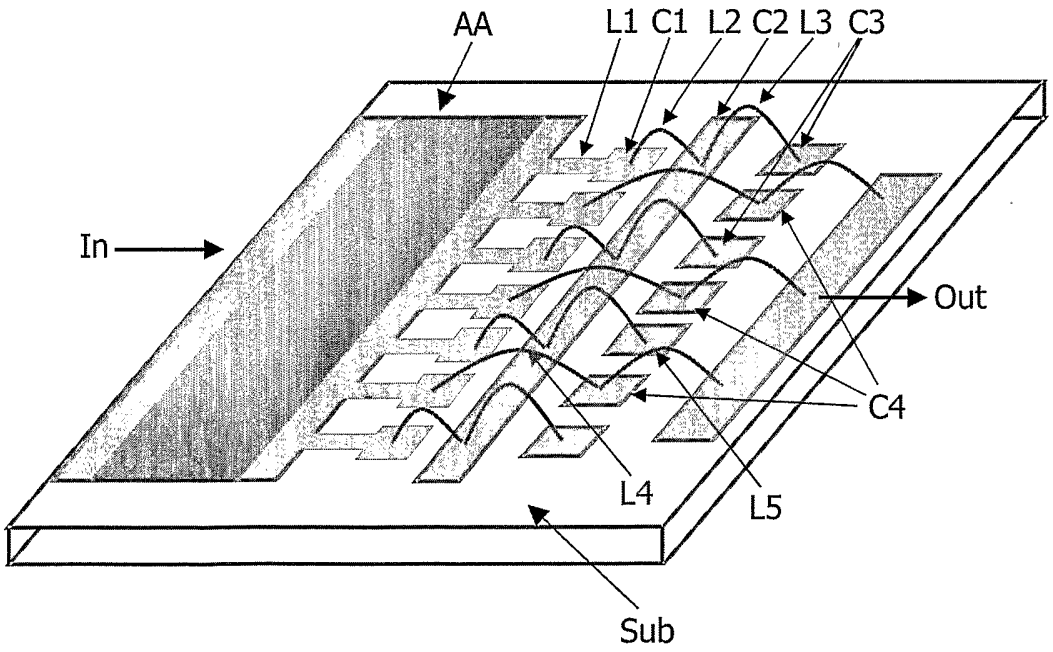

FIG.10B

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2005/052484

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F1/14 H03F1/08 H03F3/191 H03F3/217

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 300 895 A (JONES ET AL) 5 April 1994 (1994-04-05) column 1, line 55 - column 2, line 9 column 3, line 61 - column 7, line 19; figures 3b,4b,5	1-13
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-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 November 2005	16/11/2005

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	DIETSCHE S ET AL: "DESIGN OF HIGH POWER-ADDED EFFICIENCY FET AMPLIFIERS OPERATING WITHVERY LOW DRAIN BIAS VOLTAGES FOR USE IN MOBILE TELEPHONES AT 1.7GHZ" PROCEEDINGS OF THE 23RD. EUROPEAN MICROWAVE CONFERENCE. MADRID, SEPT. 6 - 9, 1993, PROCEEDINGS OF THE EUROPEAN MICROWAVE CONFERENCE, TUNBRIDGE WELLS, REED EXHIBITION COMPANY, GB, 6 September 1993 (1993-09-06), pages 252-254, XP000629924 ISBN: 0-946821-23-2 the whole document	1-8, 10-13
X	WO 03/065569 A (KONINKLIJKE PHILIPS ELECTRONICS N.V; BLEDNOV, IGOR, I; VENNEMA, ALLE,) 7 August 2003 (2003-08-07) page 4, lines 27-29 page 6, line 7 - page 10, line 9; figures 2-10	1-9, 11-13
X	WO 02/47256 A (ERICSSON INC; DENT, PAUL, W) 13 June 2002 (2002-06-13) page 5, line 9 - line 24; figures 2-9	1-13
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/IB2005/052484

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