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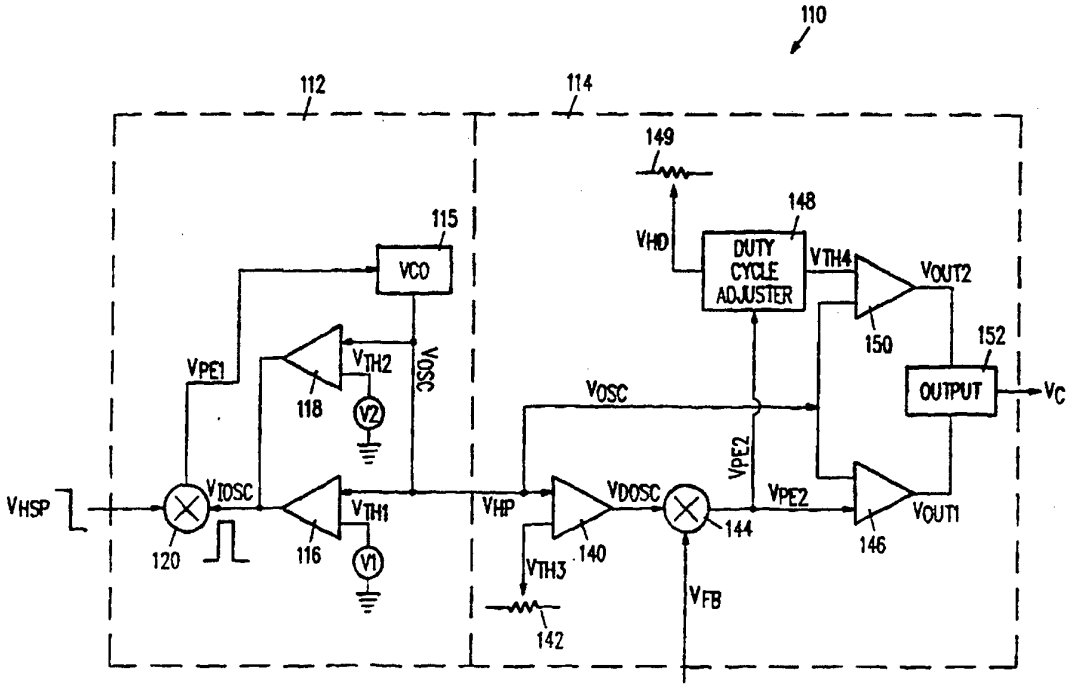

(57) Abstract

A phase-lock-loop circuit fixes the phase relationship between an input sync signal and a controlled signal by utilizing a first loop to fix the phase relationship between an oscillator output signal generated by the first loop and the input sync signal, and a second loop to fix the phase relationship between the controlled signal and the oscillator output signal.

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A REDUCED PHASE-JITTER HORIZONTAL SWEEP CONTROL PHASE-LOCK-LOOP AND METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to phase-lock-loops (PLL) and, in particular, to a reduced jitter PLL in a horizontal sweep control circuit which is suitable for implementation as a monolithic integrated circuit.

2. Background of the Related Art

A horizontal sweep control circuit is a circuit that controls the horizontal sweep of an electron beam as it moves across each line of the display screen of a cathode ray tube (CRT). A picture is formed on the display screen when the electron beam excites phosphor on the screen. The intensity of the electron beam, and therefore the picture, is controlled by a video signal.

As is well known, the National Television Systems Committee (NTSC) standard defines the frequency of the video signal along with various control signals which are incorporated within the video signal. Recently, however, new standards are emerging which define video signals with frequencies which are from two to eight times greater than the frequency of a standard television video signal. Additionally, these new standards often incorporate differing control signals. As a result, there is a need for a horizontal sweep control circuit that can operate within these new standards.

The conventional horizontal sweep control circuit typically includes a deflection yoke that controls the horizontal movement of the electron beam. The deflection yoke controls the horizontal movement of the beam by generating a magnetic field which steers the beam. As is well known, both a positive and a negative magnetic field are formed when the yoke conducts a positive and a negative yoke current, respectively.

A resonance circuit sinks and sources the positive yoke current and the negative yoke current, respectively, from the deflection yoke. The resonance circuit typically includes a transistor that sinks the positive yoke current in response to a control signal, a capacitor that stores the energy released from the deflection yoke when the transistor stops sinking the positive yoke current, and a damper diode that provides a path for the negative yoke current.

In operation, the control signal turns on the transistor which then sinks the positive yoke current from the deflection yoke. In addition to forming the positive magnetic field, the positive yoke current causes a positive current energy to be stored in the yoke.

At the end of each horizontal sweep, the control signal turns off the transistor which then stops sinking the positive yoke current. When the positive yoke current stops, the positive current energy stored in the yoke is released as an inductive yoke current which charges up the capacitor.

When the positive current energy is depleted and the inductive current ends, the capacitor begins sourcing the negative yoke current back into the yoke. The negative yoke current reverses the polarity of the magnetic field, thereby forming the negative magnetic field. The diode limits the low voltage of the capacitor as the capacitor sources the negative yoke current, thereby stopping the oscillation between the yoke and the capacitor after the first half cycle.

During the transition from the end of the positive yoke current to the beginning of the negative yoke current, the rapid change in yoke current causes the generation of a half sine-waveform flyback pulse. Since the flyback pulse coincides with the end of the positive yoke current, a phase-lock-loop is utilized to set a phase relationship between the flyback pulse and a horizontal sync pulse signal which, as is well known, defines the end of each line of the horizontal sweep. By controlling the phase relationship

between the horizontal sync pulse signal and the flyback signal, the end of each line of the horizontal sweep can be adjusted relative to the horizontal sync pulse signal.

FIG. 1 shows a block diagram of a conventional horizontal sweep control PLL 10. As shown in FIG. 1, PLL 10 includes a horizontal sync re-generator 12 that generates a square-wave intermediate sync pulse signal VISP in response to a horizontal sync pulse signal VHSP. Horizontal sync re-generator 12 generates the intermediate sync pulse signal VISP, in part, by charging and discharging a capacitor within horizontal sync re-generator 12.

A phase detector 14 compares the intermediate sync pulse signal VISP to an intermediate flyback signal VIFB and then generates an error signal VERR which indicates the phase difference between the intermediate sync pulse signal VISP and the intermediate flyback signal VIFB. Phase detector 14 generates the error signal VERR by charging a capacitor within phase detector 14 in response to the leading edge of the intermediate sync pulse signal VISP, by discharging the capacitor when the leading edge of the intermediate flyback signal exceeds a threshold voltage, and by stopping the charging or discharging of the capacitor in response to the trailing edge of the intermediate sync pulse signal VISP.

FIG. 2 shows a timing diagram of the operation of phase detector 14 which illustrates the horizontal sync pulse signal VHSP, the intermediate sync pulse signal VISP, the intermediate flyback signal VIBF, and the error signal VERR. As shown in FIG. 2, the leading edge 15 and the falling edge 17 of the intermediate sync pulse signal VISP is formed by the horizontal sync re-generator 12 to be substantially coincident with the leading edge 19 and the falling edge 21 of the horizontal sync pulse signal VHSP. The error signal VERR begins charging in response to the leading edge 15 of the intermediate sync pulse signal VISP, begins discharging in response to the leading edge 23 of the intermediate flyback signal VIBF, and stops discharging in response to the falling edge 17 of the intermediate sync pulse signal VISP. When the flyback signal (not shown) is locked onto the horizontal sync pulse signal VHSP, the ending voltage of the error signal VERR is equivalent to the starting voltage.

As further shown in FIG. 2, the horizontal sync pulse signal VHSP includes an interlaced pulse VILP which is utilized for interlaced scanning. When interlaced scanning is not being performed, proper operation of the horizontal sweep control circuit requires that the interlaced pulse VILP be ignored. Thus, as shown in FIG. 2, horizontal sync re-generator 12 must generate an intermediate sync pulse signal which ignores the interlaced pulse VILP.

Referring again to FIG. 1, the intermediate flyback signal VIFB represents the original half sine-waveform flyback signal VOFB generated by the resonance circuit (not shown) which has been modified by a delay one shot 16 and a ramp former 18. Delay one shot 16, which generates a square-wave flyback signal VSFB in response to the original flyback signal VOFB, provides a technique for phase delaying the original flyback signal VOFB with respect to the horizontal sync pulse signal VHSP.

As shown in FIG. 1, the amount of phase delay can be varied by adjusting a potentiometer 20. By phase delaying the flyback signal VOFB, the horizontal position of an image on the CRT screen can be adjusted. Delay one shot 16 generates the square-wave flyback signal VSFB, in part, by charging and discharging a capacitor within delay one shot 16.

Ramp former 18 then generates the intermediate flyback signal VIFB by converting the square-wave flyback signal VSFB into a ramp waveform. Ramp former 18 also generates the intermediate flyback signal VIFB, in part, by charging and discharging a capacitor within ramp former 18. As stated above, phase detector 14 then compares the intermediate flyback signal VIFB with the intermediate sync pulse signal VISP to generate the error voltage VERR.

A summing circuit 22 combines a set voltage VSET and the error voltage VERR to produce a summed voltage VSUM which sets a voltage controlled oscillator (VCO) 24 to generate a triangle-wave oscillator output signal VOSC at a frequency which is substantially equivalent to the frequency of the

horizontal sync pulse signal VHSP. VCO 24 also generates the oscillator output signal VOSC, in part, by charging and discharging a capacitor within VCO 24.

The set voltage VSET is generated by a frequency-to-voltage converter 26 which senses the frequency of the horizontal sync pulse signal VHSP. In operation, the set voltage VSET is generated to be proportional to the frequency of the horizontal sync pulse signal VHSP and is the primary contributor to the summed voltage VSUM which, as stated above, sets VCO 24 to generate the oscillator output signal VOSC at a frequency which is substantially equivalent to the frequency of the horizontal sync pulse signal VHSP.

Since the set voltage VSET is the primary factor in setting the frequency of the oscillator signal VOSC, by changing the set voltage VSET the frequency of the oscillator signal VOSC can be changed to track the frequency of a number of different horizontal sync pulse signals VHSP, each of which correspond to a different display type, over a wide frequency range. Thus, PLL 10 can automatically lock onto or acquire a number of different horizontal sync pulse signals without the need to manually readjust the PLL each time the frequency of the horizontal sync pulse signal changes.

As further shown in FIG. 1, the control signal VC represents the oscillator output signal VOSC which has been modified by a duty cycle comparator 28 and an output driver 30. Duty cycle comparator 28, which generates a square-wave intermediate oscillator signal VSSC in response to the ramp-waveform oscillator output signal VOSC, provides a technique for varying the duty cycle of the control signal VC.

As shown in FIG. 1, the duty cycle can be varied by adjusting a potentiometer 32. By varying the duty cycle of the control signal VC, both the image distortion and the efficiency of the horizontal sweep control circuit can be optimized. Output driver 30 then generates the control signal VC by driving the intermediate oscillator signal VSSC out to the base of the transistor of the resonance circuit (not shown).

As stated above, horizontal sync re-generator 12, delay one shot 16, ramp former 18, and VCO 24 each operate, in part, by charging and discharging internal capacitances with respect to some defined voltage. Typically switching comparators are utilized to determine when the voltages on the respective internal capacitances have reached the desired voltage level. As is well known, switching comparators generate noise in the process of comparing one voltage to another.

As a result, the principal disadvantage of PLL 10 is that during each horizontal sync pulse period the many switching comparators associated with PLL 10 introduce a substantial phase jitter. Since modern CRTs are using shorter horizontal scan lines, the phase jitter produced by PLL 10 limits the maximum frequency of operation for a set performance standard. Thus, there is a need for a horizontal sweep control PLL that reduces the phase jitter, thereby increasing the total amount of each horizontal scan line that can be utilized for video information.

SUMMARY OF THE INVENTION

The present invention provides a reduced jitter horizontal sweep control phase-lock-loop (PLL) that utilizes the leading edge of the horizontal sync pulse signal to control when the capacitor associated with the phase detector begins discharging, as opposed to utilizing the leading edge of the intermediate flyback signal, thereby eliminating the horizontal sync re-generator and its associated jitter producing comparator. In addition, the PLL utilizes a single ramp forming circuit to control the phase relationship between an externally-generated first input signal, such as a horizontal sync pulse signal, and an externally-generated second input signal, such as a flyback signal, thereby eliminating the ramp former and its associated jitter producing comparator.

A reduced jitter PLL in accordance with the present invention includes a first detector, such as a phase detector, that generates a first phase error signal which is indicative of a phase relationship between the first input signal and an oscillator output signal. A controlled oscillator, such as a voltage controlled

oscillator, generates the oscillator output signal which has a phase that varies with the first phase error signal. A second detector, such as a phase detector, generates a second phase error signal which is indicative of a phase relationship between the oscillator output signal and the second input signal. A phase shifter generates a control signal in response to the oscillator output signal and the second phase error signal so that the phase of the control signal varies with the second phase error signal.

In operation, the first phase error signal causes the frequency of the oscillator output signal to change until the oscillator output signal locks onto the first input signal. The second phase error signal causes the phase of the control signal to change until the phase of the second input signal locks onto the phase of the oscillator output signal. Since the oscillator output signal is locked onto the first input signal, and since the second input signal is locked onto the oscillator output signal, the PLL controls the phase relationship between the first input signal and the second input signal.

The first detector includes means for generating the first phase error signal by charging a capacitor within the first detector in response to the leading edge of the oscillator output signal, discharging the capacitor in response to the leading edge of the first input signal, and stopping the discharge of the capacitor in response to the trailing edge of the oscillator output signal.

The phase shifter includes a first comparator, a duty cycle adjuster, a second comparator, and an output driver. The first comparator generates a first output signal that transitions from a high to a low when the oscillator output signal passes a first threshold voltage set by the second phase error signal. The duty cycle adjuster sets a second threshold voltage by combining an externally-generated horizontal duty cycle control signal and the second phase error signal. The second comparator generates a second output signal that transitions from a low to a high when the oscillator output signal passes the second threshold voltage. The output driver combines the rising edge of the second output signal with the falling edge of the first output signal to form the control signal. Thus, the control signal has a pulse width which is a function of the horizontal duty cycle control signal.

The phase shifter can also include a first adjuster, such as a potentiometer, that sets the voltage of the horizontal duty cycle control signal. The first adjuster provides a way of manually adjusting the duty cycle of the control signal.

The second detector includes a third comparator that sources a delayed oscillator signal to the second detector in response to the oscillator signal by providing a variable delay. The third comparator generates the delayed oscillator signal when the oscillator output signal passes a third threshold voltage which is set by an externally-generated horizontal position control signal. The second detector can also include a second adjuster, such as a potentiometer, that sets the voltage of the horizontal position control signal.

The first detector includes a fourth comparator that generates a rising edge when the oscillator output signal passes a fourth threshold voltage, and a fifth comparator that generates a falling edge when the oscillator output signal passes a fifth threshold voltage. The value of the fourth and fifth threshold voltages can be set, for example, by a fixed reference voltage or a variable reference voltage.

In accordance with the method, a first phase error signal is generated which is indicative of a phase relationship between the first input signal and an oscillator output signal. The oscillator output signal is generated to have a phase which varies with the first phase error signal. A second phase error signal is generated which is indicative of a phase relationship between the oscillator output signal and the second input signal. A control signal is generated from the oscillator output signal so that the control signal has a phase which varies with the second phase error signal.

In an alternative embodiment, the PLL further includes a frequency-to-voltage convertor that produces a set signal which is indicative of a frequency of the first input signal, and a summer that combines the set signal with the first phase error signal to produce a summed signal that drives the

controlled oscillator. The frequency-to-voltage converter and the summer provide a way for covering first input signals over a wide frequency range.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description and accompanying drawings which set forth an illustrative embodiment in which the principles of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a conventional horizontal sweep control phase-lock-loop.

FIG. 2 is a timing diagram illustrating the operation of phase detector 14.

FIG. 3 is a block diagram illustrating a reduced-jitter horizontal sweep control phase-lock-loop (PLL) circuit 110 in accordance with the present invention.

FIG. 4 is a timing diagram illustrating the operation of the input phase-lock-loop 112.

FIG. 5 is a timing diagram illustrating the operation of the phase delay loop 114.

FIG. 6 is a block diagram illustrating an alternative PLL 210.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 3 shows a block diagram of a reduced-jitter horizontal sweep control phase-lock-loop (PLL) circuit 110 in accordance with the present invention. As described above, a horizontal sweep control PLL is commonly utilized to fix a phase relationship between a flyback signal and a horizontal sync pulse signal. As described in greater detail below, PLL circuit 110 fixes the phase relationship between a flyback signal V_{FB} and a horizontal sync pulse signal V_{HSP} by utilizing an input phase-lock-loop 112 to lock an oscillator output signal V_{OSC} onto the horizontal sync pulse signal V_{HSP}, and a phase delay loop 114 to fix the phase relationship between the flyback signal V_{FB} and the oscillator output signal V_{OSC}, thereby fixing the phase relationship between the flyback signal V_{FB} and the horizontal sync pulse signal V_{HSP}.

As shown in FIG. 3, the input phase-lock-loop 112 of PLL circuit 110 includes a voltage controlled oscillator (VCO) 115 that generates the oscillator output signal V_{OSC} as a ramp waveform in response to a first phase error signal V_{PE1}. A comparator 116 generates a rising edge when the oscillator output signal V_{OSC} passes a first threshold voltage V_{TH1} which is set by a fixed voltage source V1.

Similarly, a comparator 118 generates a falling edge when the oscillator output signal V_{OSC} passes a second threshold voltage V_{TH2} which is set by a fixed voltage source V2. As further shown in FIG. 3, the output of comparator 116 and the output of comparator 118 are connected together to form an intermediate oscillator signal V_{IOSC} from the rising edge generated by comparator 116 and the falling edge generated by comparator 118.

Alternately, a variable voltage source can be utilized in place of either fixed voltage source V1 or V2. Further, when a variable voltage source is utilized in place of fixed voltage source V2, the variable voltage source can be connected to the first threshold voltage V_{TH1}.

By utilizing a variable voltage source in place of fixed voltage source V1, the location of the rising edge of the intermediate oscillator signal V_{IOSC} on the ramp waveform of the oscillator output signal V_{OSC} can be adjusted. By utilizing a variable voltage source which is connected to the first threshold voltage V_{TH1} in place of fixed voltage source V2, the duty cycle of pulse width of the intermediate oscillator signal V_{IOSC} can also be adjusted.

A phase detector 120 generates the first phase error signal V_{PE1} in response to the phase difference between the intermediate oscillator signal V_{IOSC} and a horizontal sync pulse signal V_{HSP}. Phase detector 120 generates the first phase error signal V_{PE1} by charging a capacitor within phase detector 120 in response to the leading edge of the intermediate oscillator signal V_{IOSC}, by discharging the capacitor in response to the leading edge of the horizontal sync pulse signal V_{HSP}, and by stopping the discharging of the capacitor in response to the trailing edge of the intermediate oscillator signal V_{IOSC}.

In operation, the first phase error signal V_{PE1} causes the phase of the oscillator output signal V_{OSC} to change which, in turn, changes the phase of the intermediate oscillator signal V_{IOSC} generated by comparators 116 and 118. The net result is that the phase of the oscillator output signal V_{OSC} is adjusted so as to reduce any phase difference between the intermediate oscillator output signal V_{IOSC} and the horizontal sync pulse signal V_{HSP}. Thus, the input phase-lock-loop 112 fixes the phase relationship between the oscillator output signal V_{OSC} and the horizontal sync pulse signal V_{HSP}.

FIG. 4 shows a timing diagram of the operation of the input phase-lock-loop 112 which illustrates the relationship between the oscillator output signal V_{OSC}, the intermediate oscillator signal V_{IOSC}, and the horizontal sync pulse signal V_{HSP}. As shown in FIG. 4, the rising edge 130 of the intermediate oscillator signal V_{IOSC} is formed when the oscillator output signal V_{OSC} exceeds the first threshold voltage V_{TH1}.

Similarly, the falling edge 132 of the intermediate oscillator signal V_{IOSC} is formed when the oscillator output signal V_{OSC} exceeds the second threshold voltage V_{TH2}. The value of the first and second threshold voltages V_{TH1} and V_{TH2} can be changed if a different pulse width is required. In addition, both comparators 116 and 118 can be can be configured to operate on the falling edge as well as the rising edge of the oscillator output signal V_{OSC}.

As also shown in FIG. 4, the falling edge 134 of the horizontal sync pulse signal V_{HSP} corresponds with a center point 136 of the intermediate oscillator signal V_{IOSC} when the intermediate oscillator signal V_{IOSC} is locked to the horizontal sync pulse signal V_{HSP}.

As further shown in FIG. 4, the horizontal sync pulse signal V_{HSP} includes an interlaced horizontal sync pulse V_{SPI}. Since the interlaced horizontal sync pulse V_{SPI} does not correspond with any of the pulses of the intermediate oscillator signal V_{IOSC}, the interlaced horizontal sync pulse signals V_{SPI} are ignored by PLL 110.

Referring again to FIG. 3, the phase delay loop 114 of PLL circuit 110 includes a comparator 140 that generates a square-wave delayed oscillator signal V_{DOSC} when the oscillator output signal V_{OSC} passes a third threshold voltage V_{TH3}. In operation, each time the oscillator output signal V_{OSC} exceeds the third threshold voltage V_{TH3}, comparator 140 generates a rising edge.

Thus, by increasing or decreasing the voltage of the third threshold voltage V_{TH3}, the phase of the leading edge of the delayed oscillator signal V_{DOSC} can be phase-delayed or phase-advanced, respectively, thereby providing a fixed relationship between the oscillator output signal V_{OSC} and the horizontal sync pulse signal V_{HSP}. As shown in FIG. 3, a potentiometer 142 can be utilized to generate the third threshold voltage V_{TH3}.

A phase detector 144 generates a second phase error signal V_{PE2} in response to a phase difference between the delayed oscillator signal V_{DOSC} and the flyback signal V_{FB}. Phase detector 144 generates the second phase error signal V_{PE2} by charging a capacitor within phase detector 144 in response to the initial rising point of the flyback signal V_{FB}, by discharging the capacitor in response to the leading edge of the delayed oscillator signal V_{DOSC}, and by stopping the discharging of the capacitor in response to the final falling point of the flyback signal V_{FB}.

A comparator 146 generates an output signal V_{OUT1} that transitions from a high voltage to a low voltage each time the oscillator output signal V_{OSC} passes the voltage of the second phase error signal V_{PE2}. As is well known, by increasing or decreasing the voltage of the second phase error signal V_{PE2}, a phase-delayed or phase-advanced falling edge, respectively, can be generated due to the longer time required to exceed an increased voltage and, conversely, the shorter time required to exceed a decreased voltage.

As further shown in FIG. 3, a duty cycle adjuster 148 generates a fourth threshold voltage V_{TH4} by combining the voltages of the second phase error signal V_{PE2} and an externally-generated horizontal duty cycle control signal V_{HD}. In the preferred embodiment, duty cycle adjuster 148 forms the fourth threshold voltage V_{TH4} by subtracting the voltage of the externally-generated horizontal duty cycle control signal V_{HD}

from the voltage of the second phase error signal V_{PE2}. As shown in FIG. 3, a potentiometer 149 can be utilized to generate the horizontal duty cycle control signal V_{HD}.

A comparator 150 generates an output signal V_{OUT2} that transitions from a low voltage to a high voltage when the oscillator output signal V_{OSC} passes the fourth threshold voltage V_{TH4}. Since the fourth threshold voltage V_{TH4} is a function of the second phase error signal V_{PE2}, increases or decreases in the second phase error signal V_{PE2} will cause the rising edge of output signal V_{OUT2} to track the phase-delay or phase-advance, respectively, of the falling edge of output signal V_{OUT1}. Further, since the fourth threshold voltage V_{TH4} is also a function of the externally-generated horizontal duty cycle control signal V_{HD}, increases or decreases in the horizontal duty cycle control signal V_{HD} will also cause the rising edge to be phase-delayed or phase-advanced, respectively.

An output driver 152 combines the rising edge of output signal V_{OUT2} and the falling edge of output signal V_{OUT1} by utilizing well known circuitry to form a control signal V_C. As described above, a resonant circuit utilizes the control signal V_C to turn on and off a transistor to sink a positive yoke current which, in turn, creates a positive magnetic field. As also described above, the flyback signal V_{FB} is generated when the transistor turns off and stops conducting the positive yoke current.

In operation, the second phase error signal V_{PE2} causes the phase of the falling edge of the control signal V_C to change which, in turn, causes the phase of the rising edge of flyback signal V_{FB} to change so as to reduce any phase difference between the flyback signal V_{FB} and the delayed oscillator signal V_{DOSC}. Thus, the phase delay loop 114 fixes the phase relationship between the flyback signal V_{FB} and the oscillator output signal V_{OSC}.

FIG. 5 shows a timing diagram of the operation of the phase delay loop 114 which illustrates the relationship between the oscillator output signal V_{OSC}, the delayed oscillator signal V_{DOSC}, the control signal V_C, and the flyback signal V_{FB}.

As shown in FIG. 5, the rising edge 160 of the delayed oscillator signal V_{DOSC} is formed when the oscillator output signal V_{OSC} exceeds the third threshold voltage V_{TH3}. Similarly, the falling edge 162 of the delayed oscillator signal V_{DOSC} is formed when the oscillator output signal V_{OSC} falls below the third threshold voltage V_{TH3}. As further shown in FIG. 5, the rising edge 160 of the delayed oscillator signal V_{DOSC} corresponds with a center point 164 of the flyback signal V_{FB} when the delayed oscillator signal V_{DOSC} is locked to the flyback signal V_{FB}.

As additionally shown in FIG. 5, the rising edge 166 of the control signal V_C is formed when the oscillator output signal V_{OSC} falls below the fourth threshold voltage V_{TH4}. Similarly, the falling edge 168 of the control signal V_C is formed when the oscillator output signal V_{OSC} exceeds the voltage of the second phase error signal V_{PE2}. A capacitor (not shown) is connected to the node which connects detector 144, comparator 146, and adjuster 148 to hold the voltage of the second phase error signal V_{PE2}. In addition, both comparators 146 and 150 can be can be configured to operate on the falling edge as well as the rising edge of the oscillator output signal V_{OSC}.

Further, the falling edge 168 of the control signal falls a time T prior to the initial rising point of 170 the flyback signal V_{FB}. As described above, a transistor in the resonance circuit turns on and off to sink the positive yoke current. When turned on, the transistor is saturated. Since the transistor is saturated, the time T represents the time required before the transistor actually stops conducting the positive yoke current.

Since the falling edge 168 of the control signal V_C plus the time T controls the rising point 170 of flyback signal V_{FB}, by controlling the falling edge 168 the phase position of the rising point 170 of flyback signal V_{FB} can be controlled, thereby setting phase relationship between the flyback signal V_{FB} and the horizontal sync pulse signal V_{HSP}.

FIG. 6 shows a block diagram of an alternative PLL 210. As shown in FIG. 6, PLL 210 is equivalent to PLL 110 except for the inclusion of a frequency-to-voltage converter 212 and a summer

214. Frequency-to-voltage converter 212 and summer 214 allow PLL 210 to operate on horizontal sync pulse signals over a wide range of operating frequencies.

As shown in FIG. 6, frequency-to-voltage converter 212 has it input connected to the horizontal sync pulse signal V_{HSP}. Summer 214 has one input connected to the output of frequency-to-voltage converter 212, its remaining input connected to phase detector 120, and its output connected to VCO 115.

In operation, frequency-to-voltage converter 212 senses the frequency of the horizontal sync pulse signal V_{HSP}, which may typically vary over a range of two to one, depending upon the operating frequency of the CRT display, and generates a reference DC voltage V_{REF} in response. The reference DC voltage V_{REF} has a magnitude which is a function of the frequency of the horizontal sync pulse signal V_{HSP}.

Summer 214 generates a summed voltage V_{SUM} by summing the reference DC voltage V_{REF} and the first phase error signal V_{PE1}. The summed voltage V_{SUM} is fed to the input of VCO 115. VCO 115 and frequency-to-voltage converter 212 are implemented such that VCO 115 will assume a nominal operating frequency approximately equal to the frequency of the horizontal sync pulse signal V_{HSP}. Since the frequency of the oscillator output signal V_{OSC} is close to the frequency of the horizontal sync pulse signal V_{HSP}, PLL 210 is able to acquire or lock on to the horizontal sync pulse signal V_{HSP}.

Thus, frequency-to-voltage converter 212 and summer 214 allow PLL 210 to operate on horizontal sync pulse signals over a wide range of operating frequencies. Therefore, many different CRT display types, such as multisync and the like can be used by incorporating PLL 210 without the need to manually readjust PLL 210 when the display type is changed.

In the preferred embodiment of the present invention, the components of PLL 110 and 210 are implemented in a common monolithic integrated circuit.

It should be understood that various alternatives to the structures described herein may be employed in practicing the present invention. It is intended that the following claims define the scope of the invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. A phase-lock-loop (PLL) circuit for controlling a phase relationship between a first input signal and a second input signal derived from a control signal produced by the PLL circuit, the PLL circuit comprising:

a first detector that generates a first phase error signal indicative of a phase relationship between the first input signal and an oscillator output signal;

a controlled oscillator that generates the oscillator output signal having a phase which varies with the first phase error signal;

a second detector that generates a second phase error signal indicative of a phase relationship between the oscillator output signal and the second input signal; and

a phase shifter that produces the control signal from said oscillator output signal, the control signal having a phase which varies with the second phase error signal.

2. The circuit of claim 1 wherein the first detector includes means for generating the first phase error signal by charging a capacitor within the first detector in response to a leading edge of the oscillator output signal, discharging the capacitor in response to a leading edge of the first input signal, and stopping the discharge of the capacitor in response to a trailing edge of the oscillator output signal.

3. The circuit of claim 1 wherein the oscillator output signal is a ramp signal.

4. The circuit of claim 3 wherein said phase shifter includes a first comparator that generates a first output signal that transitions from a high to a low when said oscillator output signal passes a first threshold voltage set by the voltage of said second phase error signal.

5. The circuit of claim 4 wherein said phase shifter further includes a duty cycle adjuster that forms a second threshold voltage by combining the voltage of said second phase error signal with a first adjustable voltage.

6. The circuit of claim 5 wherein said phase shifter further includes a second comparator that generates a second output signal that transitions from a low to a high when said oscillator output signal passes the second threshold voltage.

7. The circuit of claim 6 wherein said control signal is in the form of an output pulse having a width which is a function of the first adjustable voltage.

8. The circuit of claim 7 wherein the control signal has a leading edge determined by said low to high transition of the second output signal and a trailing edge determined by said high to low transition of said first output signal.

9. The circuit of claim 8 wherein the phase shifter further includes a first adjuster connected to the duty cycle adjuster that sets and adjusts the magnitude of the first adjustable voltage in response to external control.

10. The circuit of claim 9 wherein the first adjuster includes a potentiometer whereby the duty cycle of the control signal can be manually altered by adjusting the magnitude of the first adjustable voltage.

11. The circuit of claim 3 wherein said second detector includes a phase delay that delays said oscillator output signal to introduce a delay between the first input signal and the second input signal.

12. The circuit of claim 11 wherein said phase delay includes a third comparator that generates a delayed oscillator signal when the oscillator output signal passes a third threshold voltage.

13. The circuit of claim 12 wherein the second detector further includes a second adjuster connected to the third comparator that sets and adjusts the magnitude of the third threshold voltage in response to external control.

14. The circuit of claim 13 wherein the second adjuster includes a potentiometer whereby the phase delay of the oscillator output signal can be manually altered by adjusting the magnitude of the third threshold voltage.

15. The circuit of claim 1 wherein said first detector further includes a pulse former that forms a square-waveform intermediate oscillator signal in response to the oscillator output signal.

16. The circuit of claim 15 and further including an output terminal for coupling the control signal to a cathode ray tube driver circuit and further including an input terminal for receiving the second input signal output from the driver circuit, whereby the PLL circuit functions to compensate for any indeterminate phase shift introduced by the driver circuit.

17. The circuit of claim 16 wherein the first detector comprises a phase detector.

18. The circuit of claim 17 wherein the second detector comprises a phase detector.

19. A method for controlling a phase relationship between a first input signal to a phase-lock-loop circuit and a second input signal derived from a control signal produced by the phase-lock-loop circuit, the method comprising the steps of:

generating a first phase error signal indicative of a phase relationship between the first input signal and an oscillator output signal;

generating the oscillator output signal having a phase which varies with the first phase error signal;

generating a second phase error signal indicative of a phase relationship between the oscillator output signal and the second input signal; and

producing the control signal from said oscillator output signal, the control signal having a phase which varies with the second phase error signal.

20. A phase-lock-loop (PLL) circuit for controlling a phase relationship between a first input signal to the phase-lock-loop circuit and a second input signal derived from a control signal produced by the PLL circuit, the PLL circuit comprising:

a frequency-to-voltage converter that produces a frequency signal indicative of a frequency of the first input signal;

a first detector that generates a first phase error signal indicative of a phase relationship between the first input signal and an oscillator output signal;

a summer that generates a summed signal by combining the frequency signal and the first phase error signal;

a controlled oscillator that generates the oscillator output signal having a phase which varies with the summed signal;

a second detector that generates a second phase error signal indicative of a phase relationship between the oscillator output signal and the second input signal; and

a first phase shifter that produces the control signal from said oscillator output signal, the control signal having a phase which varies with the second phase error signal.

21. A phase-lock-loop (PLL) circuit for controlling a phase relationship between a first input signal and a second input signal derived from a control signal produced by the PLL circuit, the PLL circuit comprising:

a first detector that generates a first phase error signal indicative of a phase relationship between the first input signal and an oscillator output signal; and

a controlled oscillator that generates the oscillator output signal having a phase which varies with the first phase error signal,

wherein the first detector generates the first phase error signal by charging a capacitor within the first detector in response to a leading edge of the oscillator output signal, discharging the capacitor in response to a leading edge of the first input signal, and stopping the discharge of the capacitor in response to a trailing edge of the oscillator output signal.

22. The circuit of claim 21 and further comprising:

a second detector that generates a second phase error signal indicative of a phase relationship between the oscillator output signal and the second input signal; and

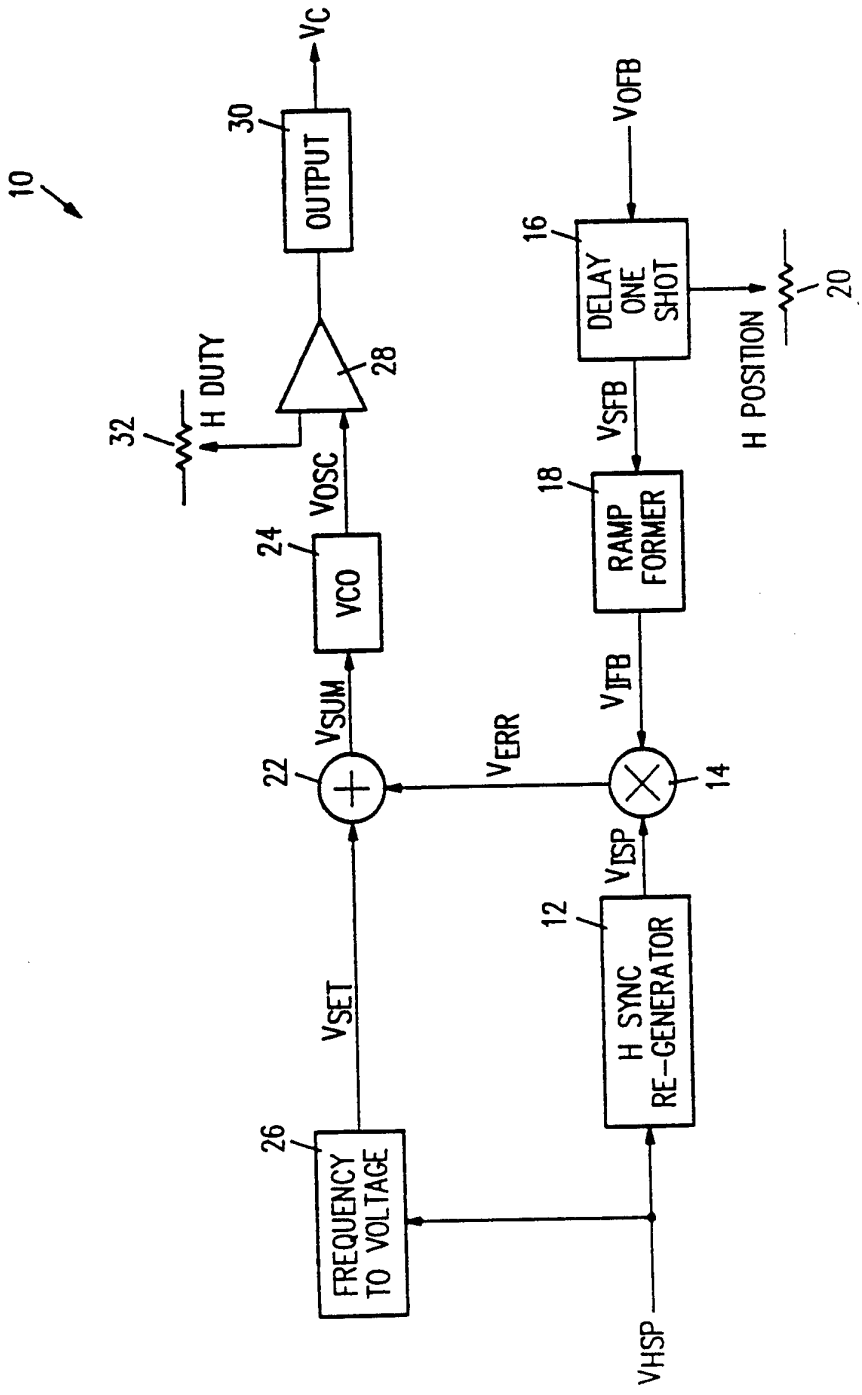
a phase shifter that produces the control signal from said oscillator output signal, the control signal having a phase which varies with the second phase error signal.

23. The circuit of claim 15 wherein the pulse former includes a first comparator that generates the rising edge of the intermediate oscillator signal when the oscillator output signal exceeds a first threshold voltage, and a second comparator that generates the falling edge of the intermediate oscillator signal when the oscillator output signal exceeds a second threshold voltage.

24. The circuit of claim 23 wherein the first threshold voltage is set by a first fixed voltage source.

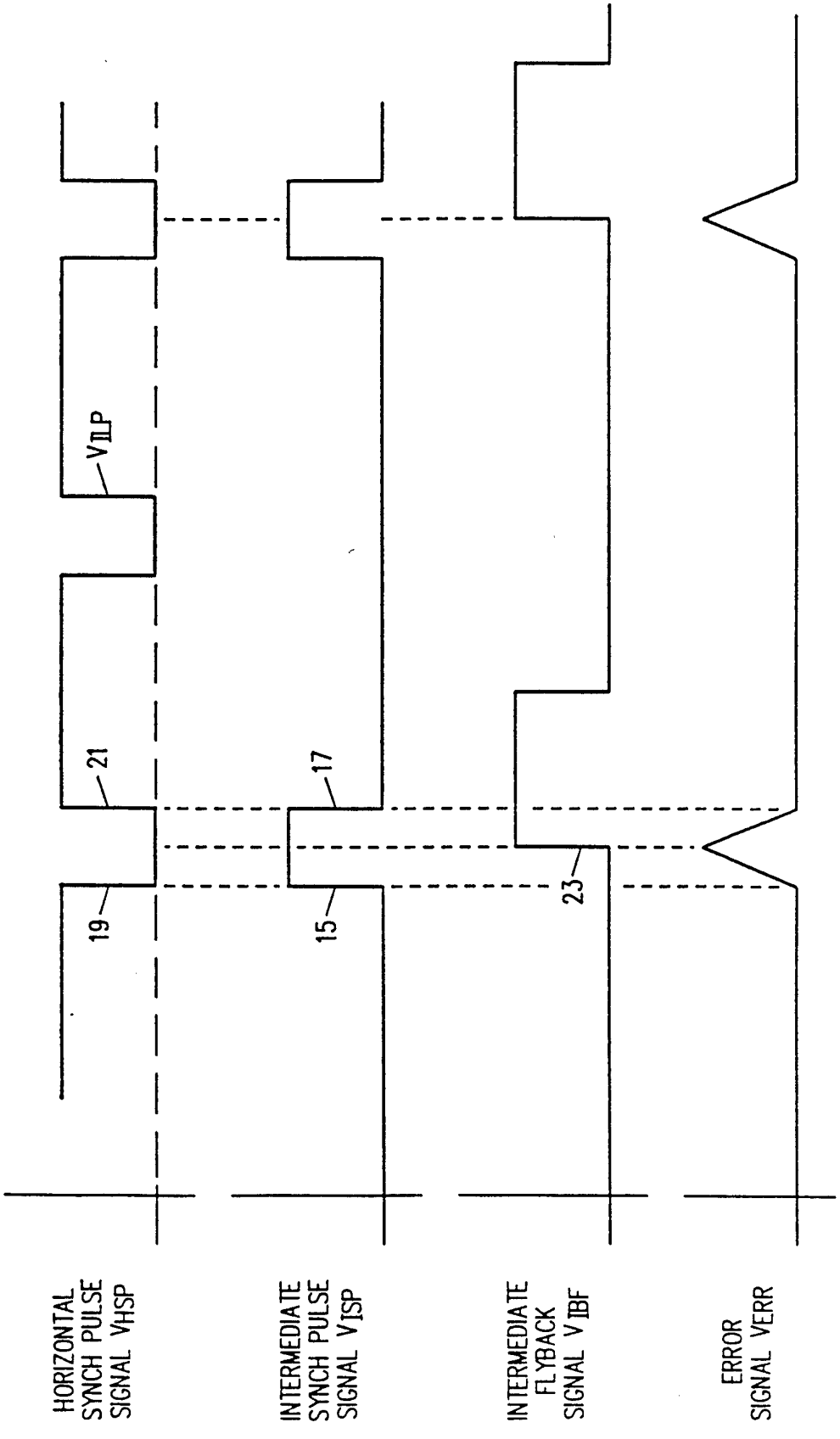
25. The circuit of claim 23 wherein the first threshold voltage is set by a first variable voltage source.

26. The circuit of claim 23 wherein the second threshold voltage is set by a second fixed voltage source.



PRIOR ART

FIG. 1



PRIOR ART
FIG. 2

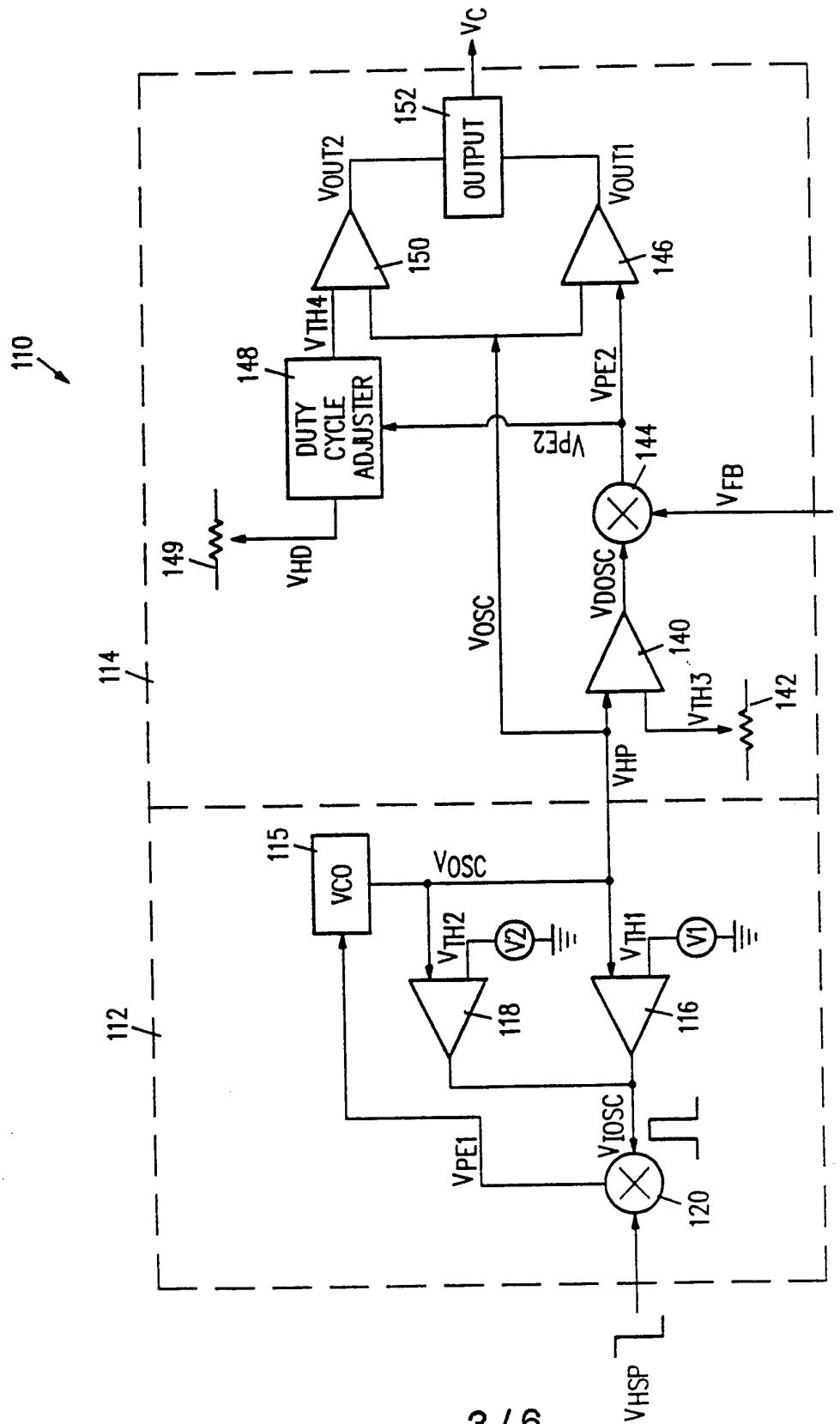

110
114
112
115
VCO
VOSC
VTH2
V2
VTH1
V1
118
116
VIOSC
VPE1
120
VHSP
VHP
VTH3
142
140
VDOSC
VFB
144
VPE2
VPE2
148
DUTY CYCLE ADJUSTER
VTH4
149
VHD
150
146
VOUT2
VOUT1
152
OUTPUT
VC

FIG. 3

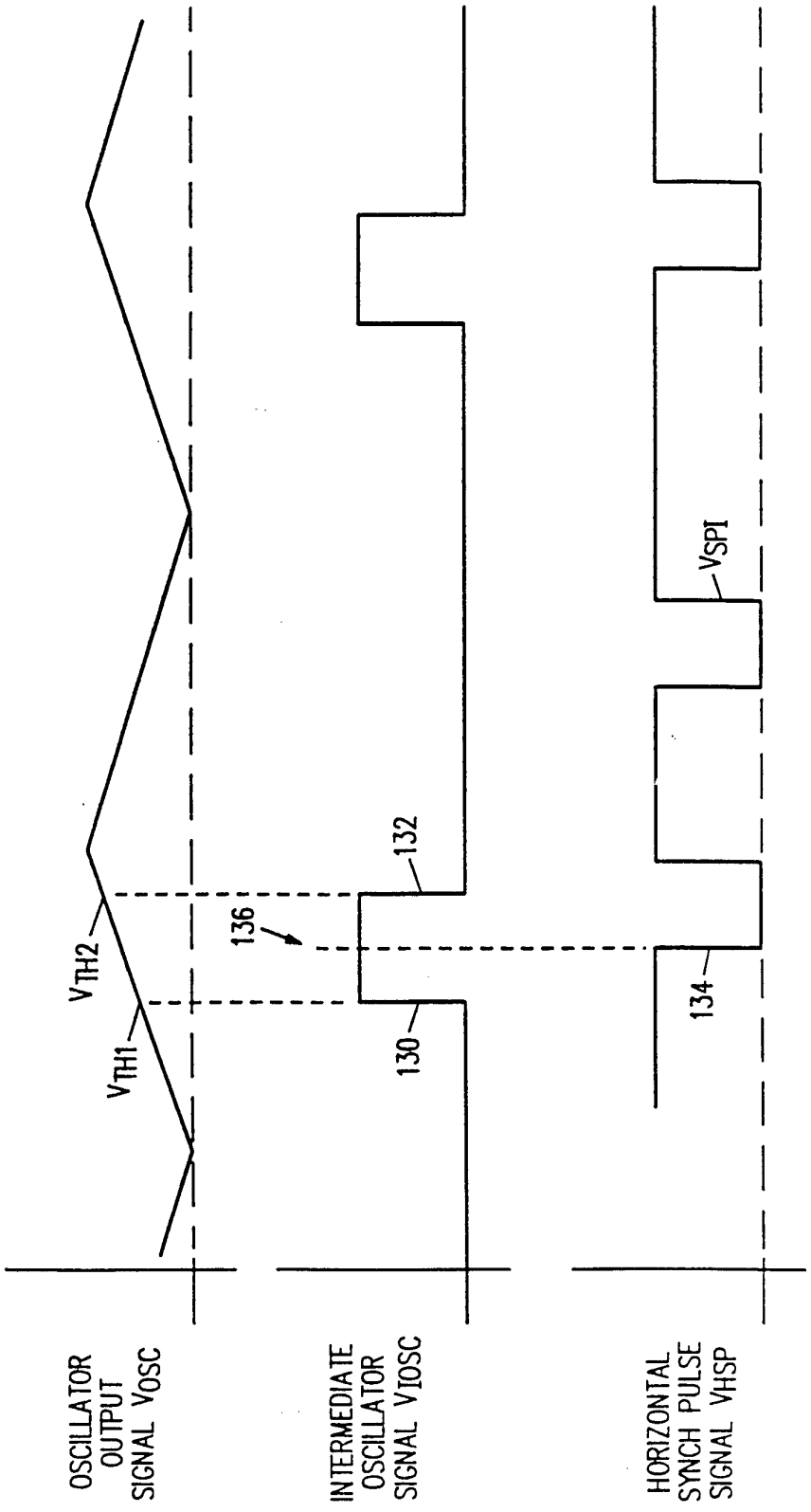

OSCILLATOR OUTPUT SIGNAL VOSC
INTERMEDIATE OSCILLATOR SIGNAL VIOSC
HORIZONTAL SYNCH PULSE SIGNAL VHSP
VTH2
VTH1
136
132
130
134
VSPI

FIG. 4

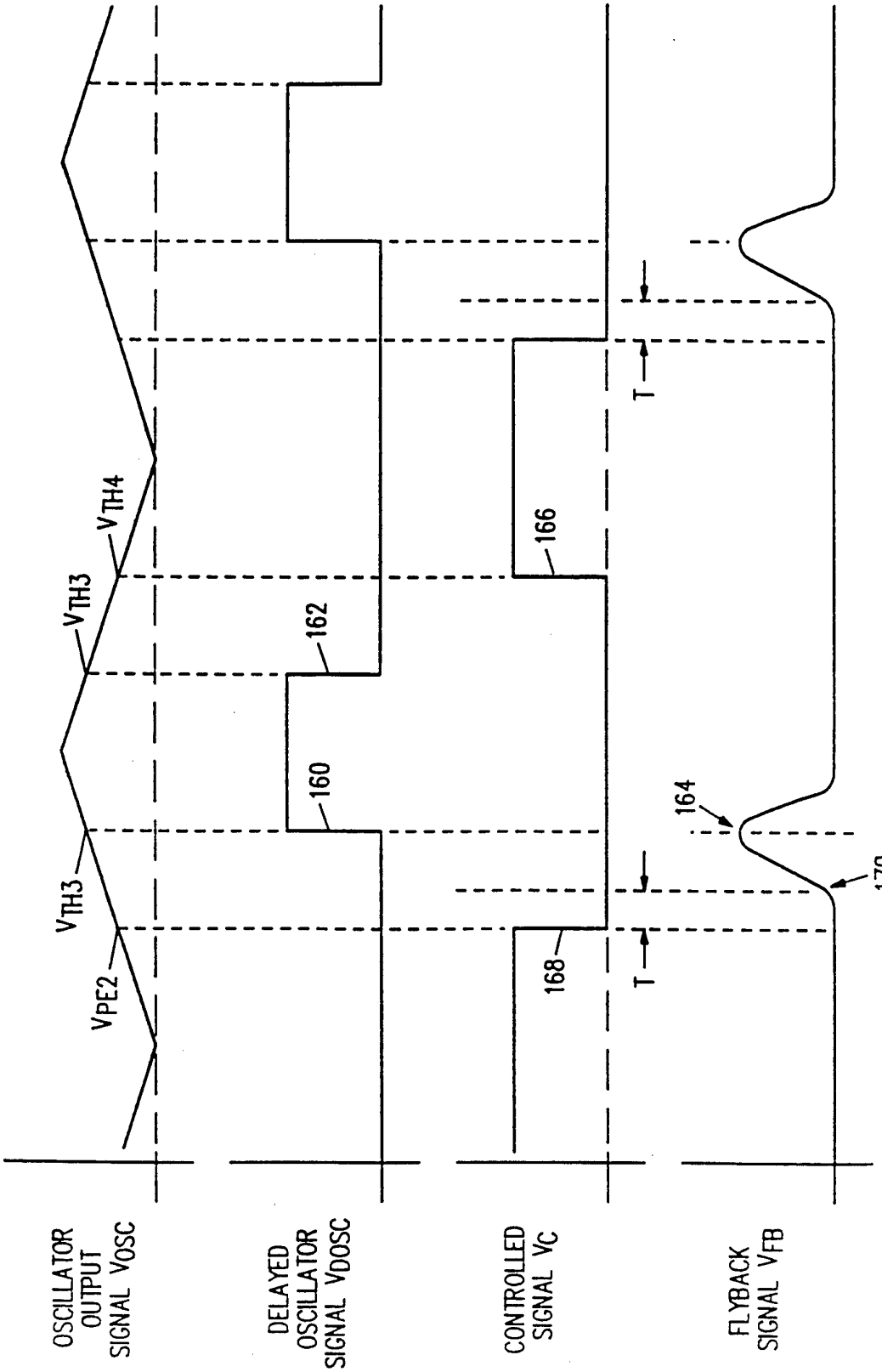

OSCILLATOR OUTPUT SIGNAL VOSC
DELAYED OSCILLATOR SIGNAL VDOSC
CONTROLLED SIGNAL VC
FLYBACK SIGNAL VFB
VTH4
VTH3
VTH3
VPE2
160
162
166
168
164
170
T
T

FIG. 5

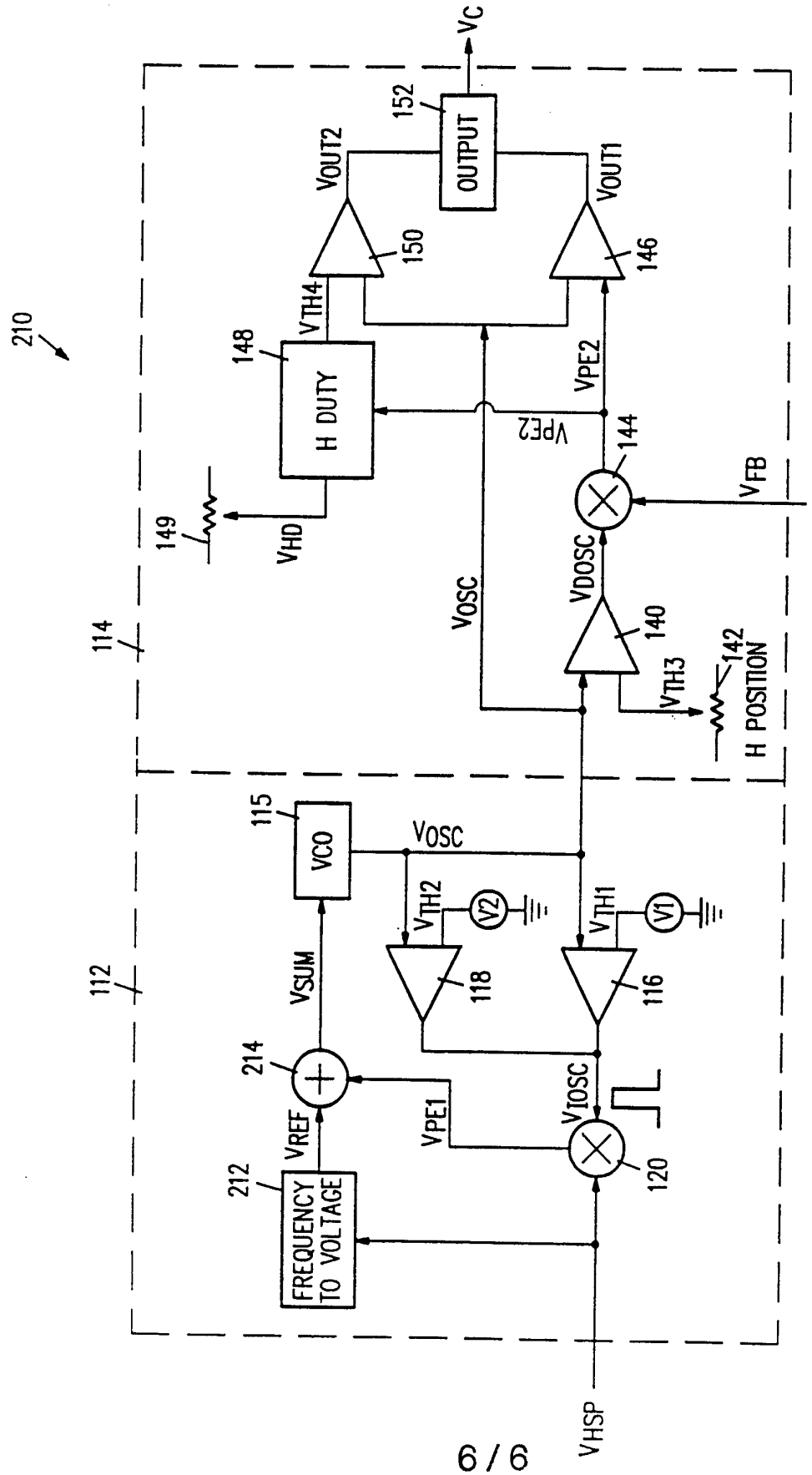

210
VC
152
OUTPUT
VOUT2
VOUT1
150
146
VTH4
148
H DUTY
VPE2
144
VFB
149
VHD
VOSC
VDOSC
114
140
VTH3
142
H POSITION
115
VCO
VOSC
VTH2
V2
VTH1
V1
112
VSUM
118
116
214
VIOSC
VPE1
VREF
120
212
FREQUENCY TO VOLTAGE
VHSP

FIG. 6

INTERNATIONAL SEARCH REPORT

Intc. .onal Application No
PCT/US 94/06093

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H03L7/081 H04N5/12 H04N3/27

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H03L H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US,A,4 634 939 (DIETZ) 6 January 1987 see column 3, line 62 - column 4, line 4; figure 1 ---	1,19,20 15,16 16-18
X A	DE,A,25 25 927 (BLAUPUNKT-WERKE GMBH) 16 December 1976 see page 4, line 22 - page 5, line 21; figure 1 ---	1,19 16-18
P,X P,Y	US,A,5 247 229 (NGO ET AL.) 21 September 1993 see column 7, line 16 - line 50; figure 2 ---	1,15-19 20
Y	US,A,4 317 133 (FERNSLER ET AL.) 23 February 1982 see column 4, line 25 - column 28; figure 1 --- -/--	15,16

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 September 1994	23. 09. 94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+ 31-70) 340-3016	Peeters, M

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INTERNATIONAL SEARCH REPORT

Inte .onal Application No
PCT/US 94/06093

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	IEEE TRANSACTIONS ON CONSUMER ELECTRONICS, vol.36, no.3, August 1990, NEW YORK US pages 458 - 466 PERKINS,TSUI AND CHEUNG: 'Multimode high definition and personal computer monitor chip set' see left column, line 17 - line 24; figure 6 ---	20
A	EP,A,0 195 500 (ADVANCED MICRO DEVICES) 24 September 1986 see figure 3 ---	2
A	ELECTRONIQUE APPLICATIONS, no.32, October 1983, PARIS FR pages 41 - 49 J. REBERGA: 'Balayage horizontal et vertical en circuit intégré (pour téléviseurs ou moniteurs vidéo)' see figure 4 -----	3

INTERNATIONAL SEARCH REPORT

information on patent family members

Inte .onal Application No
PCT/US 94/06093

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DE-A-2525927	16-12-76	NONE		
US-A-5247229	21-09-93	NONE		
US-A-4317133	23-02-82	CA-A-	1168354	29-05-84
		EP-A,B	0049965	21-04-82
		JP-C-	1622015	09-10-91
		JP-A-	57087680	01-06-82
		JP-B-	61023708	06-06-86
EP-A-0195500	24-09-86	US-A-	4668918	26-05-87
		DE-A-	3688621	05-08-93
		DE-T-	3688621	20-01-94
		JP-A-	61182319	15-08-86