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[54] FREQUENCY COMPENSATING CIRCUIT FOR VOLTAGE REGULATORS

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[52] **U.S. Cl.** **321/5,** 321/6, 321/19, 323/20

[51] **Int. Cl.**.....**H05b 37/02**

[58] **Field of Search**.....321/5, 5 A, 6, 7, 9, 9 A, 18, 321/19, 61; 323/20, 34, 102, 106, 110, 119; 322/24; 307/105

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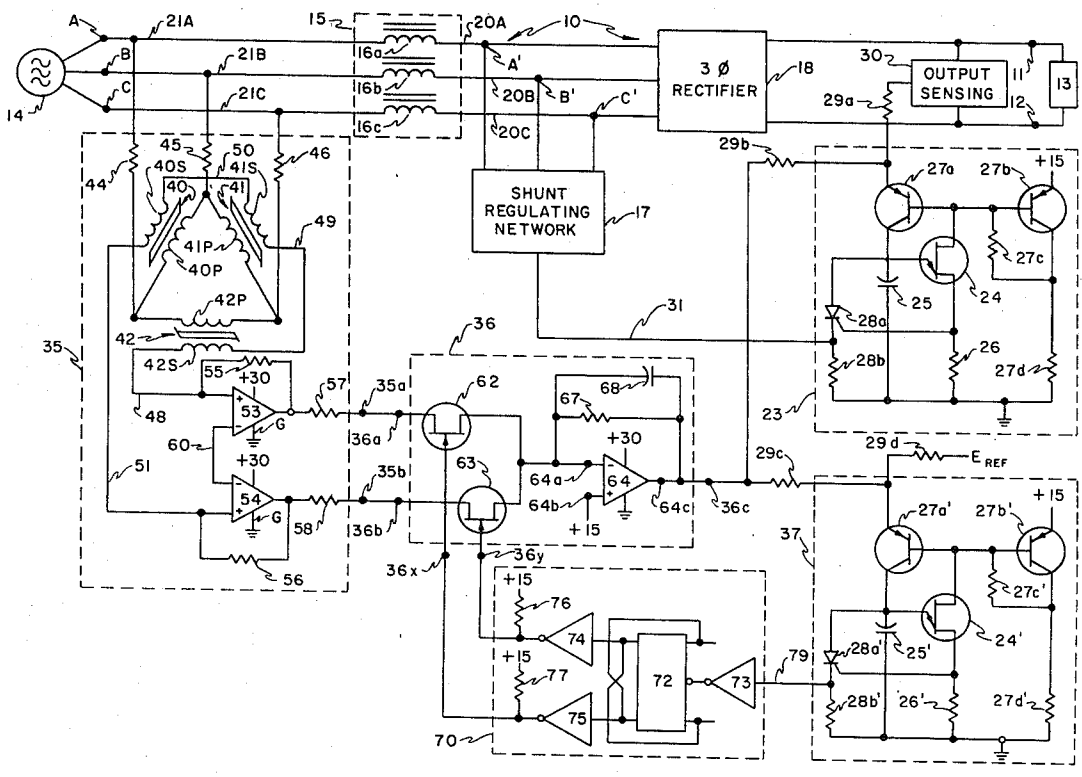
Attorney—John Howard Smith

[57] **ABSTRACT**

A control circuit for eliminating the effect of changes in the frequency of an a-c input voltage on a regulated output voltage in voltage regulator circuits utilizing variable frequency regulating waves. A phase-lock loop controls the frequency of a first, reference oscillator in accordance with the frequency of the a-c input voltage to provide a frequency error signal proportional to the difference between the actual frequency of the input voltage and the nominal frequency of that voltage. The frequency error signal is applied to a second, control oscillator which is not part of the phase-lock loop. This allows the control oscillator to follow input voltage frequency variations without being locked in phase to the input voltage and thus allows the control oscillator to be controlled in accordance with the magnitude as well as the frequency of the a-c input voltage.

12 Claims, 5 Drawing Figures



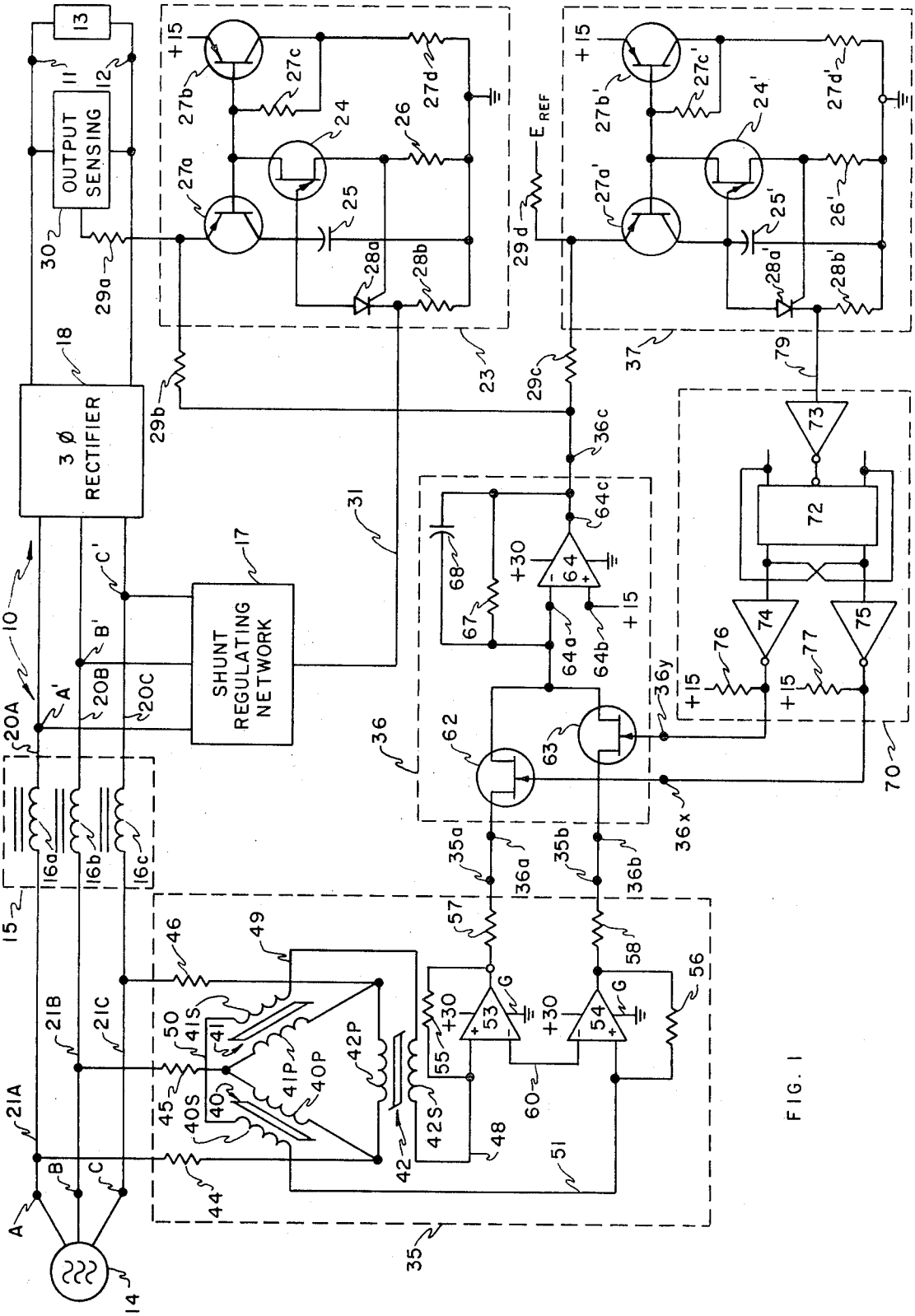

13
OUTPUT SENSING
11
12
30
29a
18
3 Ø RECTIFIER
29b
+15
27a
27b
27c
27d
24
25
26
28a
28b
23
E_{REF}
29d
27a'
27b'
27c'
27d'
24'
25'
26'
28a'
28b'
37
79
29c
36c
31
17
SHUNT REGULATING NETWORK
10
A'
B'
C'
20A
20B
20C
16a
16b
16c
15
21A
21B
21C
A
B
C
14
64c
64
+30
68
67
64a
64b
+15
36
62
63
36y
36x
72
73
74
75
76
77
70
35a
35b
36a
36b
57
58
56
53
54
55
G
60
46
49
50
41S
41
40
45
40S
41P
40P
42P
42S
42
48
51
44
35

FIG. 1

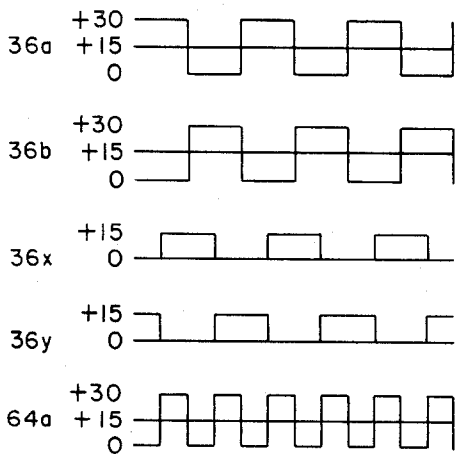


FIG. 2A

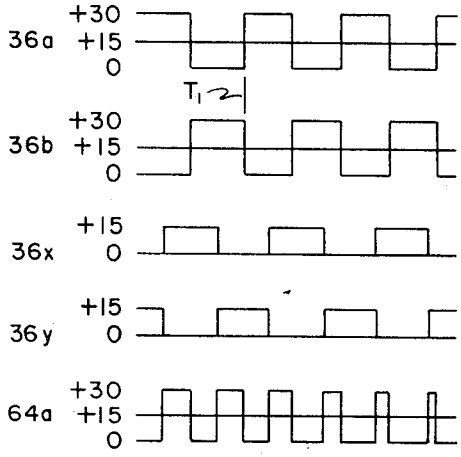


FIG. 2B

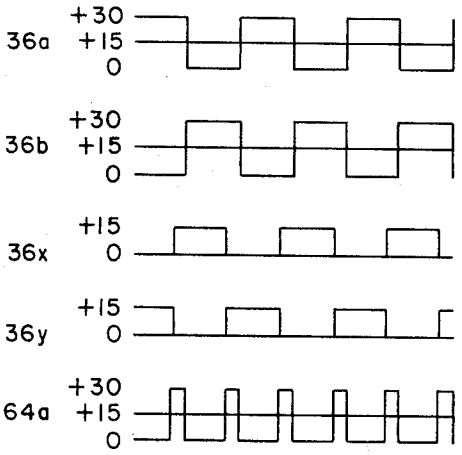


FIG. 2C

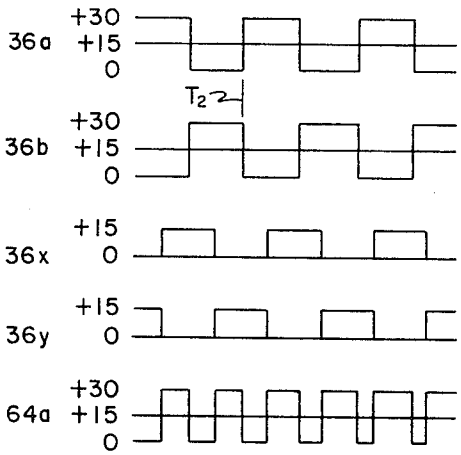


FIG. 2D

FREQUENCY COMPENSATING CIRCUIT FOR VOLTAGE REGULATORS

BACKGROUND OF THE INVENTION

The present invention relates to frequency compensating circuits and is directed more particularly to frequency compensating circuitry for voltage regulator circuits utilizing variable frequency regulating waves.

In providing a regulated a-c or d-c output voltage from an unregulated a-c input voltage, circuits utilizing series-connected inductors together with shunt-connected wave generating circuits have long been known and used. Early forms of such regulator circuits were known as ferroresonant regulators and utilized wave generating circuits including capacitors and saturable core magnetic units.

The common characteristic of such voltage regulator circuits is that each includes wave generating circuitry which generates a regulating wave that can be shifted in phase, with respect to the a-c input voltage, to control the voltage across and current through the load. In order to produce this characteristic, the regulating wave generating circuit must have a quiescent frequency that is equal to the nominal a-c input frequency when the output voltage is at its quiescent or regulated value. The wave generating circuit must also be adapted to vary the frequency of the regulating waves to change the input voltage-regulating wave phase angle, as required, to counteract variations in the output voltage from its quiescent or regulated value. The latter frequency variations continue only so long as is necessary to establish an input voltage-regulating wave phase angle at which the circuitry establishes the regulated output voltage. Thereafter, the frequency of the regulating waves must once again be equal to the nominal frequency of the a-c input voltage.

The problem with regulating circuits of the above type was the conflict between the requirement that the regulating wave had to be at its quiescent frequency when the output voltage was at its regulated value and the requirement that the quiescent frequency of the regulating wave had to be equal to the nominal frequency of the input voltage. This conflict arose when the input frequency was not constant since the quiescent frequency of the regulating waves could not, prior to the present invention, be fixed by the regulated output voltage and yet vary with the frequency of the a-c input voltage. As a result, regulating circuits of the above type were used only where the frequency of the a-c input voltage could be maintained within narrow frequency limits.

In accordance with the present invention, there is provided frequency compensating circuitry whereby the frequency of the a-c input voltage of voltage regulator circuits may be varied over wide limits without substantial affect upon the voltage to be regulated.

SUMMARY OF THE INVENTION

It is an object of the invention to provide control circuitry for eliminating narrow input frequency tolerances in regulating circuits utilizing variable frequency regulating waves.

Another object of the invention is to provide regulator control circuitry which is subject to control both in accordance with the magnitude of a regulated output voltage and in accordance with the frequency of an unregulated a-c input voltage, thus eliminating the effect of input frequency changes on output voltage.

It is another object of the invention to provide regulator control circuitry for generating a control signal having a frequency which varies directly with output voltage with respect to a variable or floating reference, the latter reference being varied, as required, to counteract the effect of changes in the frequency of the input voltage on the regulated output voltage.

Yet another object of the invention is to provide a control circuit which senses the frequency of an a-c input voltage and varies the operating frequency of a control oscillator, as required, to make that operating frequency follow variations in the frequency of the input voltage.

Still another object of the invention is to provide a control circuit for generating a frequency error signal which synchronizes a reference oscillator to an a-c input voltage, and for supplying a second, substantially equal frequency error signal to a control oscillator.

Another object of the invention is to provide a phase-lock loop for generating a control signal which causes the frequency of a reference oscillator to follow variations in the frequency of an a-c input voltage, and to utilize that control signal to vary the frequency of a control oscillator which is not a part of the phase-lock loop.

It is yet another object of the invention to provide a phase-detector for determining the difference between the frequency of a reference oscillator and the frequency of an a-c input voltage, the phase-detector being arranged to generate a frequency error signal equal to the signal required to bring the reference oscillator into synchronism with the a-c input voltage.

A further object of the invention is to provide a control circuit of the above character including a control oscillator which is substantially similar to the reference oscillator and including means for applying the above frequency error signal to the control oscillator to cause the frequency of the latter of follow variations in the frequency of the a-c input voltage.

Another object of the invention is to provide a control oscillator of the above character having a frequency which can be varied in accordance with the voltage which is to be regulated.

Other objects and advantages of the invention will become apparent from the following description and accompanying drawings.

DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of one exemplary circuit embodying the invention, and

FIGS. **2***a*, **2***b*, **2***c* and **2***d* are timing diagrams showing the voltages which appear in the circuit of FIG. **1** under various operation conditions.

DESCRIPTION OF THE INVENTION

Referring to FIG. **1** there is shown circuitry **10** for producing a regulated voltage at the terminals **11** and **12** of a d-c load **13** from the unregulated a-c voltages which a polyphase source **14** establishes at terminals A, B and C. Regulating circuit **10** includes a series regulating network **15** for supporting the difference between the unregulated a-c input voltage at terminals A, B and C, and the regulated output voltage at terminals **11** and

12. Regulating network 15 may include inductance means 16A, 16B and 16C which may be wound on a single magnetic core. Regulating circuit 10 also includes a shunt regulating network 17 for controlling the voltage across and current through series regulating network 15, as required, to establish the desired output voltage at the required output current. Finally, regulating circuit 10 includes rectifying means 18 for converting the regulated a-c voltage at terminals A', B' and C' to a regulated d-c voltage at terminals 11 and 12.

Shunt regulating network 17 controls the regulating activity of inductors 16A, 16B and 16C by establishing a set of regulating voltage waves on terminals A', B' and C'. These regulating waves are applied to first respective ends of inductors 16A, 16B and 16C through conductors 20A, 20B and 20C. Since the polyphase input voltages of source 14 are applied to second respective ends of inductors 16A, 16B and 16C through conductors 21A, 21B and 21C, respectively, the voltage across and current through the regulating inductors is dependent upon the phase angle between the a-c input voltages generated by source 14 and the regulating voltage waves established by shunt regulating network 17. Consequently, controlling the phase angle between the regulating voltage waves at A', B' and C' and the a-c input voltages A, B and C controls the voltage between terminals 11 and 12. One shunt regulating network which is suitable for use in regulator 10 is described, in detail, in my copending U.S. Pat. application Ser. No. 254,697, entitled "Regulator Circuit Having A Multi-Stepped Regulating Wave."

To the end that the phase relationship between the a-c input voltages on terminals A, B and C, and the regulating voltage waves generated by shunt regulating network 17 may be controlled in accordance with the d-c voltage between terminals 11 and 12, there is provided a control oscillator 23 including a unijunction oscillator network comprising unijunction transistor 24, a timing capacitor 25 and a resistor 26 and including a differential drive network comprising PNP transistors 27*a* and 27*b* and resistors 27*c* and 27*d*. The unijunction oscillator network operates in the conventional manner to provide frequency control pulses to regulating network 17, through a conductor 31, at a rate determined by the rate of flow of charging current into timing capacitor 25. The differential drive network, in turn, controls the rate of flow of charging current into capacitor 25, in accordance with externally generated voltage error and frequency error signals, which signals are applied to control oscillator 23 through resistors 29*a* and 29*b*, respectively.

The advantage of utilizing the differential drive network shown in FIG. 1 is that it allows error signals having quiescent values of +15 volts to be applied to the emitter of transistor 27*a* and at the same time allows the available +15 volt bias source to be used to bias the base of transistor 27*a*. This is because transistor 27*b* causes the base of transistor 27*a* to be at a potential of +15 volts minus the base-emitter voltage drop of transistor 27*b*, thus cancelling the effect of the base-emitter voltage drop of transistor 27*a* on signals having a quiescent value of +15 volts.

The term quiescent as used herein with respect to a given network or signal indicates that that network or signal is in the condition which exists when the voltages or currents that control that network or signal are at their nominal or ideal values. The term equilibrium as used herein with respect to a given network or signal has reference to a condition in which the environmental circuitry produces no voltages or currents which tend to alter the then existing condition of that network or signal. Thus, quiescence is a condition which might be regarded as ideal while equilibrium is a balanced condition attained by operation of the invention in compensating for aberrations in the power supply from the quiescent state.

Control oscillator 23 may also include a pulse shaping network including a thyristor 28*a* and a resistor 28*b*. Because the gate-cathode circuit of thyristor 28*a* is connected across unijunction oscillator resistor 26 and because the anode-cathode circuit of thyristor 28*a* is connected across timing capacitor 25, it will be seen that as transistor 24 conducts through resistor 26, thyristor 28*a* is turned on to speed up the discharge of capacitor 25. This speeded up discharge assures that regulating network 17 is provided with frequency control pulses of desirably short rise times.

When the voltage between terminals 11 and 12 is at its regulated value, output sensing circuit 30 produces a current through the path including resistor 29*a*, the base-emitter path of transistor 27*a* and resistors 27*c* and 27*d*, which is sufficient to cause transistor 27*a* to drive oscillator 23 at a frequency proportional to the nominal frequency of the voltage of source 14. Under these conditions, shunt regulating network 17 generates regulating voltage waves having a frequency equal to the frequency of source 14. As a result, there is no tendency for the existing phase angle between the input voltage and the regulating waves to change and thus no tendency for the output voltage to change.

When, however, the voltage between terminals 11 and 12 rises above its regulated value, output sensing circuit 30 increases the voltage error current through the base-emitter of transistor 27*a* and thereby increases the frequency of the pulses generated by capacitor 25 and unijunction transistor 24. This, in turn, increases the frequency of the control pulses applied to shunt regulating network 17 and thereby increases the frequency of the regulating voltage waves at terminals A', B' and C'. This reduces the phase angle between the a-c input voltage and the regulating waves to drive the output voltage back toward its regulated value. Thereafter, as the output voltage becomes equal to its regulated value, the frequency of the regulating waves becomes equal to the input frequency, causing the phase angle between the a-c input voltage and the regulating waves to attain a new equilibrium value appropriate to the circuit conditions which initially caused the output voltage to increase from its regulated value.

When, on the other hand, the output voltage decreases from its regulated value, output sensing circuit 30 decreases the voltage error current through transistor 27 and thereby decreases the operative frequency of oscillator 23 to decrease the frequency of the regulating waves generated by shunt regulating network 17. This will increase the phase angle between the input voltage and the regulating waves to drive the output voltage back toward its regulated value. Thereafter, as the output voltage becomes equal to its regulated

value, the frequency of the regulating waves becomes equal to the input frequency, causing the phase angle between the input voltage and the regulating waves to attain a new equilibrium value appropriate to the circuit conditions which initially caused the output voltage to decrease from its regulated value.

In view of the foregoing, it will be seen that the frequency of control oscillator **23** varies from its quiescent value only for the time required to change the input voltage-regulating wave phase angle to the extent required to re-establish the output voltage. This quiescent frequency is, of course, fixed by the nominal frequency of the input voltage.

A serious problem with the above described regulating circuitry is that as the frequency of source **14** varies from its nominal value, oscillator **23** causes the output voltage to assume a new and undesired value, the magnitude of which is dependent upon the amount by which the frequency of the a-c input voltage differs from its nominal value. Thus, regulating circuit **10** together with control oscillator **23** could not be used in circuits requiring accurate voltage regulation but having a variable input voltage frequency.

To the end that the above described changes in regulated output voltage may be eliminated, and in accordance with the present invention, there is provided frequency compensating circuitry including a waveshaping circuit **35** for generating, from the a-c input voltage, squarewaves having frequencies proportional to the a-c input frequency. The frequency compensating circuitry also includes a phase detector network **36** for comparing the phase displacement between the squarewaves generated by waveshaping circuit **35** and the squarewaves initiated by a reference oscillator **37** having a fixed quiescent frequency and having a response characteristic substantially similar to that of the control oscillator **23**. Finally, the frequency compensating circuit includes a feedback loop which causes phase detector **36** to generate a frequency error signal which changes the frequency of reference oscillator **37**, as required, to equalize the frequencies of the squarewaves initiated by waveshaping circuit **35** and oscillator **37**. Thus, waveshaping circuit **35**, phase detector **36** and reference oscillator **37** comprise a phase-lock loop whereby reference oscillator **37** is made to operate in synchronism with a voltage derived from the a-c input voltage.

In accordance with one feature of the present invention, the quiescent operating frequency of oscillator **37** is set by a reference voltage source E_{REF} and a resistor **29*d*** at a value equal to the nominal frequency of the squarewaves generated by waveshaping circuit **35**. This allows phase detector **36** to measure the amount by which the input frequency is different from its nominal value. In accordance with a second feature of the invention, control oscillator **23** is selected to have electrical response characteristics which are substantially similar to those of reference oscillator **37**. This is preferably accomplished by constructing oscillators **23** and **37** from substantially similar circuit elements, as is reflected by the similarity of the indicia used to identify the component parts of those oscillators. In accordance with a third feature of the invention, control oscillator **23** is connected to phase detector **36** to receive therefrom a frequency error signal which is equal to that applied to sensing oscillator **37**. This causes the frequency of control oscillator **23** to vary with the frequency of the a-c line in the same manner as reference oscillator **37**, even though control oscillator **23** is not a part of the phase-lock loop including networks **35**, **36** and **37**.

As a result of the synchronizing activity of the above described phase-lock circuitry and as a result of the connection thereof to control oscillator **23**, oscillator **23** has a variable or floating quiescent frequency which follows the frequency of the a-c input voltage. As will be described more fully presently, it is about this floating quiescent frequency that output sensing circuit **30** can temporarily vary the operating frequency of oscillator **23**, as required, to control the phase angle between the input voltage and the regulating voltage waves. Thus, the frequency error signal generated by the frequency compensating circuitry controls oscillator **23**, in accordance with the input frequency, to eliminate output voltage variations which result from variations in input frequency, and the voltage error signal generated by output sensing circuit **30** controls oscillator **23**, in accordance with the output voltage, to eliminate output voltage variations which result from changes in input voltage and output current.

The operation of the frequency compensating circuitry will now be discussed. As previously described, waveshaping circuit **35** generates squarewave voltages having a frequency determined by the frequency of the a-c input voltage. To the end that this may be accomplished, waveshaping circuit **35** includes transformers **40**, **41**, and **42** having primary windings **40P**, **41P** and **42P** which are connected in delta to the a-c line through current limiting resistors **44**, **45** and **46**. Each transformer is provided with a saturable core having a saturation characteristic such that positive saturation occurs soon after the beginning of each positive half-cycle of the voltage across the associated primary winding and negative saturation occurs soon after the beginning of each negative half-cycle of the voltage across the associated primary winding. As a result, the voltage across secondary windings **40S**, **41S** and **42S** each comprise a succession of positive and negative spikes which substantially coincide with the zero points of the a-c input voltages.

In order to derive suitable control voltage waveforms from the voltages across transformer secondary windings **40S**, **41S** and **42S**, the latter windings are connected in series by conductors **48**, **49**, **50** and **51**. This series connection causes the voltage between conductors **48** and **51** to consist of a train of positive and negative voltage spikes having a frequency three times the frequency of the voltage appearing between any pair of input terminals. This higher-than-line-frequency pulse train is desirable because it allows oscillators **23** and **37** to operate at a frequency 6 times greater than the a-c input frequency thus assuring that oscillator **23** provides a control pulse to regulating network **17** for every 1/6 cycle of the input voltage. The latter condition is, in turn, necessary to initiate the required three positive and three negative half-cycles which make up one cycle of the three phase regulating wave between terminals A′, B′ and C′.

To the end that the train of positive and negative voltage spikes appearing between conductors **48** and

51 may be converted into squarewaves suitable for application to phase detector 36, waveshaping circuit 35 includes suitable operational amplifiers 53 and 54 together with respective feedback resistors 55 and 56 and respective output resistors 57 and 58. Because feedback resistors 57 and 58 are connected to provide a positive feedback signal to the respective amplifier inputs, operational amplifiers 53 and 54 operate as two-state switching devices. Accordingly, each operational amplifier produces an output voltage of one polarity between the time that a positive pulse occurs and the time that a negative pulse occurs and produces an output voltage of the opposite polarity between the time that a negative pulse occurs and the time that a positive pulse occurs. It will be understood that because amplifiers 53 and 54 are energized by a voltage between ground G and a +30 volt supply, the terms "positive" and "negative", as applied to the output voltages of amplifiers 53 and 54, have reference to the polarity of the amplifier output voltage with respect to virtual ground which is 15 volts positive from actual ground G.

Because the negative or inverting inputs of operational amplifiers 53 and 54 are connected by a conductor 60, a positive pulse on conductor 48 drives the output of amplifier 53 in the positive direction from virtual ground and drives the output of operational amplifier 54 in the negative direction from virtual ground. Similarly, a negative pulse on conductor 48 drives the output of amplifier 53 in the negative direction and drives the output of amplifier 54 in the positive direction. Thus, amplifiers 53 and 54 generate, at waveshaper outputs 35*a* and 35*b*, complementary squarewaves having transitions which occur at the times of occurrence of the zero points of the a-c input voltages.

In order to generate, from the squarewaves at outputs 35*a* and 35*b*, a frequency error signal which has a quiescent value (+15 volts) representative of the nominal a-c input frequency and which varies from its quiescent value in accordance with variations of the a-c input frequency from its nominal value, there is provided a phase detector 36. Detector 36 includes N-channel junction field effect transistors 62 and 63, an operational amplifier 64, a resistor 67 and a capacitor 68. Transistors 62 and 63 serve to energize the inverting input 64*a* of amplifier 64 in accordance with the squarewave voltages appearing at detector inputs 36*a* and 36*b* and in accordance with the squarewave feedback voltages appearing at detector inputs 36*x* and 36*y*. More specifically, when detector input 36*x* is at virtual ground, transistor 62 energizes amplifier input 64*a* with the squarewave at detector input 36*a*, and when detector input 36*y* is at virtual ground, transistor 63 energizes amplifier input 64*a* with the squarewave at detector input 36*b*. Amplifier 64 together with resistor 67 and capacitor 68, in turn, serves as an averaging network to apply to detector output 36*c* an analog voltage having an amplitude determined by the phase angle between the squarewave voltages applied to input pairs 36*a*–36 and 36*x*–36*y* thereof.

Referring to FIG. 2*a*, there are shown the voltages which appear at inputs 36*a*, 36*b*, 36*x*, 36*y* and 64*a* when the a-c input voltage is at its nominal frequency. Assuming that the voltages at detector inputs 36*x* and 36*y* lag 90° behind the voltages at detector inputs 36*a* and 36*b*, respectively, transistor 62 will apply to amplifier input 64*a* one-half of each positive half-cycle of the voltage at input 36*a* and one-half of each negative half-cycle of that voltage. Similarly, transistor 63 applies to amplifier input 64*a* one-half of each positive half-cycle of the voltage at input 36*b* and one-half of each negative half-cycle of that voltage. This causes the voltage at amplifier input 64*a* to have positive-going and negative-going half-cycles of equal amplitude and duration and thus causes detector output 36*c* to be at its quiescent potential of +15 volts. Thus, when the a-c input voltage is at its nominal frequency, the frequency error voltage at detector output 36*c* is at its quiescent value of +15 volts with respect to ground or zero volts with respect to virtual ground.

In practice, reference oscillator 37 is forced to produce the 90° quiescent phase lag between the voltages at detector input pairs 36*a*–36*b* and 36*x*–36*y* by causing it to oscillate at its quiescent frequency when the frequency of the a-c input voltage is at its nominal value. This is because, under these conditions, only a 90° phase lag causes detector 36 to provide oscillator 37 with a frequency error signal which does not vary the frequency of oscillator 37 from its quiescent frequency. Thus, the existence of a 90° quiescent phase angle is dictated by the circuitry of detector 36 and its relationship to the nominal frequency of the a-c input voltage and the desired quiescent frequency of oscillator 37.

If, under the above conditions, the frequency of the a-c input voltage should increase from its nominal value, the voltages at junctions 36*a*, 36*b*, 36*x*, 36*y* and 64*a* will vary with time as shown in FIG. 2*b*. Referring to that Figure, it will be seen that after time T1, when the frequency of the input voltage increases from its nominal value, the negative half-cycle of the voltage at amplifier input 64*a* begins to predominate over the positive half-cycle of the voltage thereat. This, in turn, causes the frequency error signal at detector output 36*c* to rise above its quiescent potential at virtual ground. Under these conditions, the frequency of reference oscillator 37 rises above its quiescent value to increase the frequency of the feedback pulses which are applied to detector inputs 36*x* and 36*y* through a waveshaping network 70.

As a result, the frequency of the squarewaves at detector inputs 36*x* and 36*y* begin to approach the frequency of the squarewaves at detector inputs 36*a* and 36*b*. This causes the frequency error voltage at detector output 36*c* to approach a constant positive value which depends upon the deviation of the a-c input voltage frequency from its nominal value. The voltages that are present under the latter condition are depicted in FIG. 2*c* which shows a new non-quiescent equilibrium condition in which the phase lag between the waveforms at detector inputs 36*a*–36*b* and 36*x*–36*y* is greater than 90° and in which the frequency error signal at 36*c* has a constant positive value proportional to the average value of the voltage at amplifier input 64*a*.

If, on the other hand, the frequency of the a-c input voltage should decrease from its nominal value, the voltages at junctions 36*a*, 36*b*, 36*x*, 36*y* and 64*a* will vary with time as shown in FIG. 2*d*. Referring to that Figure, it will be seen that after time T_2, when the

frequency of the input voltage decreases from its nominal value, the positive half-cycle of the voltage at amplifier input **64***a* begins to predominate over the negative half-cycle of the voltage thereat. This, in turn, causes the frequency error signal at detector output **36***c* to vary below its quiescent value at virtual ground. Under these conditions, the frequency of reference oscillator **37** drops below its quiescent value to decrease the frequency of the feedback pulses which are applied to detector inputs **36***x* and **36***y* through waveshaping circuit **70**.

As a result, the squarewaves at detector inputs **36***x* and **36***y* begin to approach the frequency of the squarewaves at detector inputs **36***a* and **36***b*. This causes the frequency error voltage at detector output **36***c* to approach a constant negative value which depends on the deviation of the a-c input frequency from its nominal value. Under these conditions, the circuit of FIG. **1** attains a new non-quiescent equilibrium condition in which the phase lag between the waveforms at detector inputs **36***a*–**36***b* and **36***x*–**36***y* is less than 90° and the frequency error signal at **36***c* has a constant negative value proportional to the average value of the voltage at amplifier input **64***a*.

In view of the foregoing, it will be seen that as the frequency of the input voltage varies in either direction from its nominal value, detector **36** operates in accordance with signals derived from the a-c input voltage and reference oscillator **37** to generate a frequency error signal which causes the frequency of reference oscillator **37** to follow that of the a-c line. Additionally, it will be seen that the amount by which the frequency error voltage at detector output **36***c* differs from +15 bolts (virtual ground) is proportional to the amount by which the input voltage frequency differs from its nominal value.

To the end that the pulses generated by oscillator **37** may be converted to squarewaves suitable for application to detector inputs **36***x* and **36***y*, there is provided a waveshaping circuit **70** including a flip-flop **72**, inverters **73**, **74** and **75** and resistors **76** and **77**. Flip-flop **72** serves to apply complementary squarewaves of voltage to inverters **74** and **75**, each squarewave having transitions which are initiated by the output pulses which oscillator **37** applies to flip-flop **72** through a conductor **79**. Resistors **76** and **77** serve as pull-up resistors, that is, resistors which set the amplitude of pulse trains from inverters **74** and **75** at a higher than usual value, in this case 15 volts, the latter being an amplitude sufficient to assure conduction through field-effect transistors **62** and **63**. Inverter **73** serves merely to compensate for the polarity reversals introduced by inverters **74** and **75**.

In accordance with an important feature of the present invention, a frequency error signal equal to the frequency error signal applied to reference oscillator **37** is applied to control oscillator **23** through a resistor **29***b*. Since the latter oscillator is substantially similar to reference oscillator **37**, the frequency of oscillator **23** varies with input frequency in the same manner as oscillator **37**. As a result, the frequency control pulses which oscillator **23** applies to shunt regulating network **17** follow line frequency variations even though oscillator **23** is not a part of the phase-lock loop including networks **35**, **36**, **37** and **70**. Thus, the circuit of FIG. **1** is not subject to the frequency drift problems which have existed in a-c voltage regulator circuits prior to the present invention.

It will be understood, of course, that the variations in the frequency of control oscillator **23** which result from variations in the input voltage frequency do not affect the ability of output sensing circuit **30** to further vary the frequency of control oscillator **23**, as required, to regulate the output voltage with respect to changes in the amplitude of the input voltage and the output current. This simultaneous control is possible because oscillator **23** is not an active part of the previously described phase-lock loop. As a result, frequency adjustments due, for example, to voltage error signals from network **30** are also treated. Thus, the regulator control circuitry of FIG. **1** is regulated both with respect to input voltage and with respect to input frequency.

In view of the foregoing, it will be seen that circuitry embodying the present invention is adapted to vary the frequency of an oscillator, as required, to compensate for variations in the amplitude of the input voltage and is also adapted to vary the frequency of an oscillator, as required, to compensate for variations in the frequency of that input voltage. Thus, the circuit of the invention eliminates the frequency-induced voltage drifts which have limited the usefulness of prior art voltage regulators.

It will be understood that the above embodiment is for descriptive purposes only and may be changed or modified without departing from the spirit and scope of the appended claims.

What is claimed is:

1. In a control circuit for a voltage regulator having and a-c input voltage of variable frequency, in combination, first means for generating a frequency error signal which signal assumes a quiescent value when the frequency of the a-c input voltage is at its nominal value and which signal varies from said quiescent value when the frequency of the a-c input voltage varies from said nominal value, second means for generating a voltage error signal which signal assumes a quiescent value when the output voltage of the voltage regulator is at its regulated value and which varies from said quiescent value when the output voltage of the voltage regulator varies from said regulated value, a control oscillator having a quiescent operating frequency and having first and second signal inputs whereby the frequency of said control oscillator may be varied from said quiescent operating frequency, means for applying said frequency error signal to said first signal input, means for applying said voltage error signal to said second signal input, said control oscillator being adapted to operate at its quiescent operating frequency when said error signals are at their quiescent values, and means for connecting said control oscillator to the voltage regulator to control the regulating activity thereof.

2. A control circuit as set forth in claim **1** in which said control oscillator includes a relaxation oscillator, first variable conducting means for controlling the firing frequency of said relaxation oscillator and second variable conducting means for biasing said relaxation oscillator with a bias voltage equal to the quiescent voltage of said error signals.

3. A control circuit as set forth in claim 1 in which said first generating means includes a phase detector comprising an averaging network for generating a signal voltage proportional to the voltages applied to the inputs of said averaging network, variable conducting means having power circuit means and control circuit means, means for connecting said power circuit means in series with the input of said averaging network and means for alternately and severally energizing said control circuit means.

4. In a control circuit for a voltage regulator having an a-c input voltage of variable frequency, in combination, a phase-lock network including a reference oscillator having a fixed quiescent operating frequency, said phase-lock network being arranged to apply to said reference oscillator a frequency error signal sufficient to vary the frequency of said reference oscillator from said quiescent frequency in accordance with variations in the frequency of the a-c input voltage from a nominal value, means for connecting said phase-lock network to the source of a-c input voltage, a control oscillator having a fixed quiescent operating frequency and having response characteristics which are substantially similar to those of said reference oscillator, means for connecting said phase-lock network to said control oscillator to apply thereto a frequency error signal substantially equal to the frequency error signal applied to said reference oscillator, means for varying the frequency of said control oscillator from said quiescent frequency in accordance with variations in the output voltage of said voltage regulator from a regulated value and means for connecting said control oscillator to said voltage regulator to control the regulating activity thereof.

5. In a control circuit for a voltage regulator having an a-c input voltage of variable frequency, in combination, a reference oscillator having a predetermined quiescent operating frequency and having a signal input whereby the operating frequency of said reference oscillator may be varied from said quiescent operating frequency, a phase-detector for generating a frequency error signal for varying the operating frequency of said reference oscillator from said quiescent value as the frequency of the a-c input voltage varies from a predetermined nominal value, means for connecting said phase-detector to said reference oscillator to apply thereto said frequency error signal, means for connecting said reference oscillator to said phase-detector to apply thereto a feedback signal, means for connecting said phase-detector to the source of input voltage, a control oscillator having response characteristics which are similar to the characteristics of said reference oscillator, said control oscillator having a predetermined quiescent frequency and having a first signal input whereby the operating frequency of said control oscillator may be varied from said quiescent frequency in accordance with said frequency error signal and a second signal input whereby the operating frequency of said control oscillator may be varied from said quiescent frequency in accordance with the output voltage of said voltage regulator, means for applying to said first signal input a frequency error signal similar to the frequency error signal applied to said reference oscillator, means for applying to said second signal input a voltage error signal which varies in accordance with the output voltage of said voltage regulator, and means for connecting said control oscillator to said voltage regulator to control the voltage regulating activity thereof.

6. A control circuit as set forth in claim 5 in which said phase-detector includes an averaging network for generating a signal voltage proportional to the average value of the voltage applied to the input of said averaging network, variable conducting means having power circuit means and control circuit means, means for connecting said power circuit means in series with the input of said averaging network and means for connecting said control circuit means to said reference oscillator.

7. A control circuit as set forth in claim 5 in which said means for connecting said phase-detector to the source of input voltage includes at least one saturable core transformer for generating positive and negative switching pulses in accordance with the input voltage and two-state switching means for generating complementary squarewaves in accordance with said positive and negative switching pulses.

8. In a control circuit for a voltage regulator having an a-c input voltage of variable frequency, in combination, first waveshaping means for generating a first squarewave signal in accordance with the a-c input voltage, a reference oscillator for generating pulses having a fixed quiescent frequency, second waveshaping means for generating a second squarewave signal in accordance with pulses from said reference oscillator, phase detecting means for generating an error signal which varies in accordance with the phase difference between said first and second squarewave signals, means for connecting said phase detecting means to said reference oscillator to vary the frequency of said reference oscillator, from said quiescent frequency, in accordance with said error signal, a control oscillator having response characteristics similar to those of said reference oscillator, means for connecting said phase detecting means to said control oscillator to apply thereto an error signal similar to the error signal applied to said reference oscillator, and means for connecting said control oscillator to the voltage regulator to compensate the latter for input frequency variations.

9. A control circuit as set forth in claim 8 in which the squarewave signals applied to said phase-detecting means are 90° out-of-phase when the frequency of the input voltage is at its nominal value.

10. A control circuit as set forth in claim 8 in which said control oscillator includes a unijunction oscillator, first variable conducting means for controlling the firing frequency of said unijunction oscillator and second variable conducting means for biasing said unijunction oscillator with a bias voltage equal to the quiescent voltage of said error signal.

11. In a control circuit for a voltage regulator having an a-c input voltage of variable frequency, in combination, first waveshaping means for generating a first pair of complementary squarewaves each having transitions which occur at predetermined times during each cycle of the a-c input voltage, reference oscillating means for generating a second pair of complementary squarewaves having a predetermined quiescent frequency, said reference oscillating means including a signal input whereby the frequency of said second pair

of squarewaves may be varied from said quiescent frequency, phase detecting means for generating a frequency error signal which varies in accordance with the phase angle between said first and second pairs of squarewaves, means for applying said frequency error signal to said signal input to equalize the frequencies of said pairs of squarewaves, a control oscillator having a predetermined quiescent frequency and having first and second signal inputs whereby the frequency of said control oscillator may be varied from said quiescent frequency, output sensing means for establishing a voltage error signal which varies in accordance with the difference between the output voltage of the voltage regulator and the desired output voltage thereof, means for applying said frequency error signal and said voltage error signal to said first and second signal inputs, respectively, and means for connecting said control oscillator to said voltage regulator to control the regulating activity thereof.

12. A control circuit as set forth in claim **11** in which the phase angle between said first and second pairs of squarewaves has a quiescent value of 90°.

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