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(71) Applicant *(for all designated States except US)*: **QUANTUM SEMICONDUCTOR LLC** [US/US]; 4320 Stevens Creek Blvd., #212, San Jose, CA 95129 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **AUGUSTO, Carlos** [PT/US]; Quantum Semiconductor LLP, 4320 Stevens Creek Blvd., Suite 212, San Jose, CA 95129 (US).

(74) Agent: **VANDERPERRE, Robert**; European Patent Attorney, Avenue de la Charmille 6/8, B-1200 Bruxelles (BE).

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(54) **Title**: PIXEL CIRCUITRY FOR ULTRA WIDE DYNAMIC RANGE

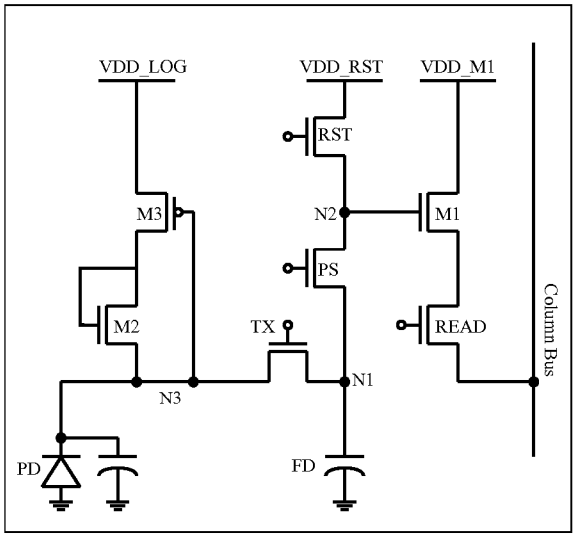


FIG. 10A

(57) **Abstract**: The pixel circuitry of the invention enables light sensing through a photo-current mode with logarithmic compression and through accumulation of charges, with a seamless transition between the modes that depends only on the light signal strength, and not on external control signals. The pixel circuitry of the invention also allows said photo-current mode for a pixel matrix operated in the electronic global shutter mode, provides anti-blooming capability, and allows for sharing of certain pixel circuit elements between a plurality of pixels.

Pixel Circuitry for Ultra Wide Dynamic Range

Background of the Invention

The present invention relates to image sensors in general, and in particular to new pixel circuitry for CMOS Image Sensors (CIS), that enable an Ultra Wide Dynamic Range (UWDR). By UWDR it is meant an intrascene dynamic range that comprises the full range of photon fluxes provided by natural illumination, that is to say, that comprises pixels that do not receive any light and pixels receiving a photon flux equivalent of staring directly into sunlight, i.e., a photon flux of roughly 1E9 photons per square micron, per second. This difference in photon flux can be roughly translated into 32 bits per square micron per second, or equivalently, around 200 dB per square micron per second.

With an image sensor that is able to handle the full intracene dynamic range of natural illumination, a camera incorporating such image sensor does not need an iris or diaphragm, exposure metering etc.

The current invention is applicable, to different types of photo-diodes, including the conventional CMOS photo-diode of 3-transistor (3T) Active Pixel Sensors (APS) and Logarithmic pixels, the Pinned Photo-Diode (PPD) of 4T APS, Avalanche Photo-Diodes (APDs), such as the SiGeC APD of U. S. Patent 6,943,051; U. S. Patent 7,265,006; U.S. Patent Application No. 11/781,544.

There are two main approaches to measure the amount of light captured by the photo-diode in CMOS pixel:

(1) Time-integration of the photo-current, also known as accumulation of charges, in which the charges generated by the photo-diode are accumulated during the exposure time.

(2) Measurement of the current flux generated by photo-generation, and convert said flux into a voltage. The typical solution for photo-current measurements is to sense the voltage at the source of a MOSFET in the weak inversion mode, in which said voltage is proportional to the logarithm of the current flowing through said MOSFET.

Each of these two approaches has advantages and disadvantages regarding the ability to better sense low light levels or strong illumination. It is widely acknowledge that the logarithmic compression of the photo-current is perhaps the most elegant and compact method of sensing photo-generated signals across many orders of magnitude of signal strength. However the 3T Log pixel is also acknowledged to be less sensitive to low light levels, that is, as the photo-current level is decreased, it becomes less sensitive to variations in said photo-current level. Also, small variations on the voltage being measured, translate into exponentially large variations of the photo-current, which translate into large fixed pattern noise at the pixel level.

The method of accumulation of charges is recognized to perform better under low light levels, but it has an upper limit to the number of charges that it can accumulate before it reaches a saturation level. Several proposals have been made to extend the dynamic range of pixels operating only with the method of accumulation of charges.

One approach is to have different integration times in different pixels, with the integration time being increased for low light levels, while the integration time is reduced for strong illumination.

Another approach is to have a pixel with multiple gain levels, a higher integration gain for weaker signals and a lower integration gain for larger signals.

Another approach, is to have pixels with two photo-diodes, one with high sensitivity and the other with low sensitivity. Typically the "floating diffusion" region of 4T pixels, is used as the low sensitivity photo-diode.

Yet another approach, consists in providing a cascade of capacitors to increase the total amount of charge

possible to accumulate in a pixel before reaching saturation. When the first capacitor is filled up, it spills over to a second capacitor, which once it it fils up, spills into a third capacitor, etc.

There have been several attempts to improve the low light sensing capability of the Logarithmic pixel, using different approaches to increase the sensitivity to variations in very small photo-currents, as well as reducing its high fixed pattern noise. The typical proposed solutions consist in combining linear and logarithmic modes of operation for the logarithmic pixel, that is, using light sensing through photo-current mode only.

One approach was suggested by N. Tu, R. Hornsey, and S. Ingram, "CMOS active pixel image sensor with combined linear and logarithmic mode operation," in Proc. IEEE Canadian Conf. Electrical and Computer Engineering, 1998, pp. 754–757.

Another approach is given by Graeme Storm, Robert Henderson, J. E. D. Hurwitz, David Renshaw, Keith Findlater, and Matthew Purcell, "Extended Dynamic Range From a Combined Linear-Logarithmic CMOS Image Sensor", in IEEE J. of Solid-State Circuits, Vol. 41, No. 9, Sep. 2006, pp. 2095-2106.

Yet another pixel design conceived to extend the dynamic range has been proposed, in which the signal from the photo-diode can be connected to either one block of circuitry performing light sensing in the accumulation of charges mode, or to another block of circuitry that performs current amplification and that is suitable for light sensing in a photo-current mode.

Nana Akahane, Rie Ryuzaki, Satoru Adachi, Koichi Mizobuchi, Shigetoshi Sugawa, "A 200dB Dynamic Range Iris-less CMOS Image Sensor with Lateral Overflow Integration Capacitor using Hybrid Voltage and Current Readout Operation", ISSCC 2006 / SESSION 16 / MEMS AND SENSORS / 16.7. It must be noted that with this pixel design, the photo-current mode does not comprise an in-pixel logarithmic conversion of the photo-current into a voltage. Rather, such conversion is performed by column-parallel circuitry. This is a very important point to consider because it does not allow for "global shutter" operation of the pixel matrix.

Yet another approach was suggested by Atsushi Hamasaki, Mamoru Terauchi, and Kenju Horii, "A Wide-Dynamic-Range Photodiode-Type Active Pixel Sensor Cell with Seamlessly Combined Logarithmic–Linear–Logarithmic Response", in Japanese Journal of Applied Physics Vol. 46, No. 7A, 2007, pp. 4050–4053. This logarithmic pixel design has 2 different transistors performing the logarithmic function of the photo-current for different light intensities. In its implementation with 5 transistors (FIG. 5A), it requires a depletion type MOSFET, which is not available as a standard device in the typical CMOS processe. This type of device is normally in the "ON" state, thereby allowing current to flow even when gate to source voltage (VGS) is zero. This depletion-mode MOSFET is connected in series between the MOSFET performing the logarithmic conversion of the photo-current into a voltage, and VDD. With a depletion mode MOSFET in series with the transistor that performs the logarithmic conversion of photo-current into a voltage, photo-current is always flowing through both transistors, and that a time-integration mode ("accumulation of charges") is not possible. This is an very important difference with respect to the present invention. A second implementation, using 7 transistors (FIG. 5B), in which the depletion-type MOSFET is replaced by an enhancement-type MOSFET of the opposite polarity (PMOS), together with a CMOS inverter (5 NMOS and 2 PMOS devices). It must also be noted that none of these implementations enables a pixel matrix to operate in the Electronic Global Shutter, since this would require a transfer gate to decouple the photo-diode is not decoupled from a capacitor (typically a floating diffusion), which are not part of either of these two implementations.

Brief Description of the Drawing Figures

FIG. 1A & 1B (Prior Art) - schematic circuit diagram of conventional 3T APS pixel cells.

FIG. 2A & 2B (Prior Art) - schematic circuit diagram of conventional 3T Logarithm pixel cells.

FIG. 3A & 3B (Prior Art) - schematic circuit diagram of conventional 4T APS pixel cells.

FIG. 4A & 4B (Prior Art) -schematic circuit diagram of 1T APD pixel cells.

FIG. 5A & 5B (Prior Art) -schematic circuit diagram of 5T and 7T pixels for Linear-Log mixed-mode operation.

FIG. 6A - schematic circuit diagram of a first implementation of the 5T pixel cells of the present invention, coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 6B - schematic circuit diagram of a first implementation of the 5T pixel cells of the present invention, coupled to CMOS-based APDs.

FIG. 7A - schematic circuit diagram of a second implementation of the 5T pixel cells of the present invention, coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 7B - schematic circuit diagram of a second implementation of the 5T pixel cells of the present invention, coupled to CMOS-based APDs.

FIG. 8A - schematic circuit diagram of a first implementation of the 6T pixel cells of the present invention, coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 8B - schematic circuit diagram of a first implementation of the 6T pixel cells of the present invention, coupled to CMOS-based APDs.

FIG. 9A - schematic circuit diagram of a first implementation of the 7T pixel cells of the present invention, coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 9B - schematic circuit diagram of a first implementation of the 7T pixel cells of the present invention, coupled to CMOS-based APDs.

FIG. 10A - schematic circuit diagram of a second implementation of the 7T pixel cells of the present invention, coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 10B - schematic circuit diagram of a second implementation of the 7T pixel cells of the present invention, coupled to CMOS-based APDs.

FIG. 11A - schematic circuit diagram of an implementation of a shared 2.25T pixel cell according to the present invention, wherein 4 pixels as implemented in FIG. 7A, comprising 9 transistors, are coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 11B - schematic circuit diagram of an implementation of a shared 2.25T pixel cell according to the present invention, wherein 4 pixels as implemented in FIG. 7B, comprising 9 transistors, are coupled to CMOS-based APDs.

FIG. 12A - schematic circuit diagram of an implementation of a shared 2T pixel cell according to the present invention, wherein 8 pixels as implemented in FIG. 7A, comprising 16 transistors, are coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 12B - schematic circuit diagram of an implementation of a shared 2T pixel cell according to the present invention, wherein 8 pixels as implemented in FIG. 7B, comprising 16 transistors, are coupled to CMOS-based APDs.

FIG. 13A - schematic circuit diagram of an implementation of a shared 4.75T pixel cell according to the

present invention, wherein 4 pixels as implemented in FIG. 10A, comprising 19 transistors, are coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 13B - schematic circuit diagram of an implementation of a shared 4.75T pixel cell according to the present invention, wherein 4 pixels as implemented in FIG. 10B, comprising 19 transistors, are coupled to CMOS-based APDs.

FIG. 14A - schematic circuit diagram of an implementation of a shared 4.5T pixel cell according to the present invention, wherein 8 pixels as implemented in FIG. 10A, comprising 15 transistors, are coupled to standard CMOS photo-diodes or pinned photo-diodes (PPDs).

FIG. 14B - schematic circuit diagram of an implementation of a shared 4.5T pixel cell according to the present invention, wherein 8 pixels as implemented in FIG. 10B, comprising 15 transistors, are coupled to CMOS-based APDs.

Detailed Description of the Invention

The present invention discloses new pixel circuitry enabling a combined linear-logarithmic operation, in which the linear operation is achieved with an accumulation of charges mode, while the logarithmic operation is achieved with a photo-current mode, with an in-pixel conversion of photo-current into voltage.

The transition between modes is seamless, with the pixel operating in the accumulation of charges mode for low light levels, automatically switching to a photo-current level if/when the amount of accumulated charges overcomes a certain threshold value, which is to say, if/when the number of photons (light intensity) impinging on the photo-diode exceed a certain intensity value.

The present invention combines into a single and compact pixel design the best features and advantages of the 3T APS and of the 3T Logarithmic pixel, simultaneously avoiding their drawbacks, namely, it has the advantages of the 3T APS for sensing low light levels, and the advantages of the 3T Logarithmic for sensing intense illumination. The present invention uses enhancement-type only MOSFETs.

The invention can be embodied through different combinations of circuit topology and mode of operation.

First Embodiment

A first embodiment is shown in **FIG. 6A and 6B**, where one finds a modified 3T APS, having 2 extra transistors: M2 and M3 (PMOS). M2 performs the logarithmic conversion of photo-current to voltage, and M3 is a switch. The source of M2 and the gate of M3 are connected to the storage node N1, which is also linked to the source of the RST. The source of M3 is connected to a voltage source (Voffset) that maybe varied from the periphery.

In **FIG. 6A** the RST gate, the RST voltage level (VRST), and the Voffset level, are presented as signals that could be distributed on a column-parallel fashion, row-parallel fashion, or on a matrix wide fashion.

The choice of VRST and Voffset and suitable biasing of the N-Well of M3 (PMOS), can be used to fine tune the "stitching point" between the modes, for a seamless transition from accumulation of charges mode to logarithm of photo-current mode. This fine tuning can also be aided by a suitable choice for the capacitance of N1.

The configuration shown **FIG. 7A** is the more likely scenario for an actual implementation, in which VRST, Voffset and VDD are all distributed on a matrix-wide fashion, that is, identical and simultaneous for all pixels in the matrix matrix, and in which VRST is identical to VDD.

Operation of Pixel of FIG. 6A (non-avalanche photo-diodes):

Signal acquisition and readout are performed on a row-by-row basis.

For one row, do the following:

Signal Acquisition & Readout:

(A) At time = 0: RS is "OFF", and RST is "ON".

(B) Begin signal acquisition (begin shutter time) by turning RST "OFF" and RS "ON".

(C) Capacitor N1 is now floating.

(D) Charges generated at the photo-diode begin to accumulate at capacitor N1, and the voltage at N1 begins to decrease.

(E) If the voltage at N1 decreases enough, M3 turns ON. If/when M3 turns ON, capacitor N1 is no longer floating, as M2 and M3 are conducting, and therefore a conductive path is established to Voffset. The voltage at the capacitor becomes the Logarithm of the current flowing through M2, with M3 acting as a resistive load. If photo-current sufficiently small, voltage at N1 increases up to the value at which M3 is switched OFF again.

(F) Column circuitry reads the "photo-signal" value, put out by M1, for the pixel:

(F1) If the voltage level put out by M1 corresponds to a value at N1 for which M3 remains OFF, then the measured signal was acquired by the accumulation of charges mode (Linear Mode).

(F2) If the voltage level put out by M1 corresponds to a value at N1 that is equal or larger than that for which M3 turns ON, then it will assumed that the measured signal was acquired by the photo-current mode (Log Mode).

(G) End signal acquisition (end shutter time) by turning "ON" the RST of selected row only, so that the "dark-current" level is readout immediately after the acquired signal has been readout. This also turns M3 "OFF".

(H) Turn "OFF" the RS transistor.

Repeat steps (A) through (H) for all other rows in the matrix.

Operation of Pixel of FIG. 6B (avalanche photo-diodes):

The pixel design of **FIG. 6A** is applicable to any photo-diode, including avalanche photo-diodes, and in particular to the APDs of U. S. Patent 6,943,051; U. S. Patent 7,265,006; U.S. Patent Application No. 11/781,544.

APDs require an avalanche inducing voltage to be applied to their terminals, and **FIG. 5B**, shows a particular configuration in which such voltage is distributed independently to each column. Other configurations for the avalanche voltage distribution are also possible, for example, distributed in parallel to all pixels in the matrix.

In **FIG. 6B** the RST voltage level (VRST), and the Voffset level, are presented as signals that could be distributed on a column-parallel fashion, row-parallel fashion, or on a matrix wide fashion.

The configuration shown **FIG. 7B** is the more likely scenario for an actual implementation, in which VRST, Voffset and VDD are all distributed on a matrix-wide fashion, that is, identical and simultaneous for all pixels in the matrix matrix, and in which VRST is identical to VDD.

With avalanche photo-diodes (APDs), the voltage applied to the APDs can be used as another controllable parameter for the operation of the pixel. In the absence of that voltage, there is no avalanche gain, and therefore one photon generates only one electron-hole pair. When the voltage is applied, the avalanche multiplication may generate 100 electron-hole pairs, for example. Therefore a pulsed avalanche voltage can be used to define an time interval during which the photo-generated signal is multiplied by the avalanche gain, while photons absorbed outside that exposure time interval generate an electrical signal that is much weaker. This time interval, defined by the duration of the voltage pulse applied to the APDs,

can be used as a "shutter time", since the photo-generated signal outside this interval is negligible. Using the duration of the voltage pulse applied to the APDs as a way to defined a shutter time, works for the accumulation charges mode. However it cannot be used to define a shutter time for a photo-current mode because it is not possible to take a "snapshot" of the current level and preserve it until the readout procedure. Therefore, the combined linear-logarithmic mode of the 5-transistor pixel design can only be operated in the ERS.

Signal acquisition and readout are performed on a row-by-row basis. During the procedure described below, the voltage applied to the APDs will remain constant at a value suitable for avalanche gain.

For one row, do the following:

Signal Acquisition & Readout:

(A) At time = 0: RS is "OFF", and RST is "ON".

(B) Begin signal acquisition (begin shutter time) by turning RST "OFF" and RS "ON".

(C) Capacitor N1 is now floating.

(D) Charges generated at the photo-diode begin to accumulate at capacitor N1, and the voltage at N1 begins to decrease.

(E) If the voltage at N1 decreases enough, M3 turns ON. If/when M3 turns ON, capacitor N1 is no longer floating, as M2 and M3 are conducting, and therefore a conductive path is established to Voffset. The voltage at the capacitor becomes the Logarithm of the current flowing through M2, with M3 acting as a resistive load. If photo-current sufficiently small, voltage at N1 increases up to the value at which M3 is switched OFF again.

(F) Column circuitry reads the "photo-signal" value, put out by M1, for the pixel:

(F1) If the voltage level put out by M1 corresponds to a value at N1 for which M3 remains OFF, then the measured signal was acquired by the accumulation of charges mode (Linear Mode).

(F2) If the voltage level put out by M1 corresponds to a value at N1 that is equal or larger than that for which M3 turns ON, then it will assumed that the measured signal was acquired by the photo-current mode (Log Mode).

(G) End signal acquisition (end shutter time) by turning "ON" the RST of selected row only, so that the "dark-current" level is readout immediately after the acquired signal has been readout. This also turns M3 "OFF".

(H) Turn "OFF" the RS transistor.

Repeat steps (A) through (H) for all other rows in the matrix.

It should be noted that with an ERS, and with column-parallel circuitry that is able to sense in real-time whether the strength of electrical signal produced by a pixel, it is possible to provide feedback to the voltage source applied to the APD of the respective column, and change the voltage value, and thus the avalanche gain value. This is only possible when there is a column-parallel control of the voltage applied to the photo-diodes during signal acquisition.

Second Embodiment

Referring to **FIG. 8A**, one finds a 7-transistor pixel based on a modified 4T APS, having 3 more transistors: TX, M2 and M3 (PMOS) and M4. TX is the transfer gate typical of 4T PPD APS designs, which separates the photo-diode from the storage node N1. Transistor M2 performs the logarithmic

conversion of photo-current to voltage, transistor M3 is a switch, and transistor M4 is also a switch.

The source of M2 and the gate of M3 are connected to the storage node N1, which is also linked to the source of the RST. The source of M3 is connected to the drain of M4, whose source is connected to voltage source (Voffset) that maybe varied from the periphery. The gate of M4 is linked to a control signal.

The transfer gate (TX) between the photo-diode and the storage node (N1) is the classic method to enable an EGS for the accumulation of charges mode: when the shutter time ends, and no more charges are to be accumulated, the transfer gate isolates the photo-diode from the storage node (N1).

A transfer gate (TX) alone is not enough to enable a EGS using the photo-current mode. It can be seen that, for example, under intense illumination, there is a significant photo-current flowing through M2 and M3 and the voltage level at node N1 is significantly below its reset value. In this case, turning OFF the transfer gate, would impede the transfer of charges from the photo-diode to node N1, but charges would escape from N1 through M2 and M3 until almost all charges would have escaped from N1.

Therefore, in order to have an EGS for photo-current, it is necessary to block the photo-current path at the same time that the transfer gate between the photo-diode and node N1 is turned OFF, and that is the purpose of M4.

Operation of Pixel of FIG. 8A (non-avalanche photo-diodes):

In **FIG. 8A** the RST gate, the RST voltage level (VRST), and the Voffset level, are presented as signals that could be distributed on a column-parallel fashion, row-parallel fashion, or on a matrix wide fashion.

The choice of VRST and Voffset and suitable biasing of the N-Well of M3 (PMOS), can be used to fine tune the "stitching point" between the modes, for a seamless transition from accumulation of charges mode to logarithm of photo-current mode. This fine tuning can also be aided by a suitable choice for the capacitance of N1.

The configuration shown **FIG. 9A** is the more likely scenario for an actual implementation, in which VRST, Voffset and VDD are all distributed on a matrix-wide fashion, that is, identical and simultaneous for all pixels in the matrix matrix, and in which VRST is identical to VDD.

The main advantage of the 7-transistor pixel over the 5-transistor pixel, is the ability to operate with an **EGS**, in which, signal acquisition and signal readout are performed separately. Signal acquisition is performed simultaneously for all pixels in the matrix, while readout takes place on a row-by-row fashion.

Signal Acquisition:

For all rows in the matrix, do the following:

(A) At time = 0: RS, TX, M4 are "OFF", and RST is "ON".

(B) Begin signal acquisition (begin shutter time) by turning RST "OFF" and TX & M4 "ON".

(C) Capacitor N1 is now floating.

(D) Charges generated at the photo-diode begin to accumulate at capacitor N1, and the voltage at N1 begins to decrease.

(E) If the voltage at N1 decreases enough, M3 turns ON. If/when M3 turns ON, capacitor N1 is no longer floating, as M2 and M3 are conducting, and therefore a conductive path is established to Voffset. The voltage at the capacitor becomes the Logarithm of the current flowing through M2, with M3 acting as a resistive load. If photo-current sufficiently small, voltage at N1 increases up to the value at which M3 is switched OFF again.

(F) End signal acquisition (end shutter time) by turning TX & M4 "OFF". With TX "OFF" photo-generated charges cannot flow from the photo-diode to N1. With T4 "OFF", charges cannot flow from N1, through M2, M3 and M4, into Voffset, thereby preserving the voltage level of N1, regardless whether that voltage level was such that M3 was "OFF" or "ON".

Signal Readout:

For one row, do the following:

(G) Turn RS "ON".

(H) Column circuitry reads the "photo-signal" value, put out by M1, for the pixel:

(H1) If the voltage level put out by M1 corresponds to a value at N1 for which M3 remains OFF, then the measured signal was acquired by the accumulation of charges mode (Linear Mode).

(H2) If the voltage level put out by M1 corresponds to a value at N1 that is equal or larger than that for which M3 turns ON, then it will assumed that the measured signal was acquired by the photo-current mode (Log Mode).

(I) Turn "ON" the RST of selected row only, so that the "dark-current" level is readout immediately after the acquired signal has been readout. This also turns M3 "OFF".

(J) Turn RS "OFF".

Repeat steps (G) through (J) for all other rows in the matrix.

Operation of Pixel of FIG. 8B (avalanche photo-diodes):

The pixel design of **FIG. 8A** is applicable to any photo-diode, including avalanche photo-diodes, and in particular to the APDs of U. S. Patent 6,943,051; U. S. Patent 7,265,006; U.S. Patent Application No. 11/781,544.

APDs require an avalanche inducing voltage to be applied to their terminals, and **FIG. 8B**, shows a particular configuration in which such voltage is distributed independently to each column. Other configurations for the avalanche voltage distribution area also possible, for example, distributed in parallel to all pixels in the matrix.

The operation of the **EGS** and of the voltage applied o the APDs, can be combined into different arrangements.

For example, the voltage applied to the APDs can remain constant through the signal acquisition and readout, or can be switched ON and OFF at certain moments. The procedure described below assumes that the voltage is applied to the APDs during the signal acquisition, that is, during the shutter time interval, but that is not applied outside that time interval.

In **FIG. 8B** the RST voltage level (VRST), and the Voffset level, are presented as signals that could be distributed on a column-parallel fashion, row-parallel fashion, or on a matrix wide fashion.

The configuration shown **FIG. 9B** is the more likely scenario for an actual implementation, in which VRST, Voffset and VDD are all distributed on a matrix-wide fashion, that is, identical and simultaneous for all pixels in the matrix matrix, and in which VRST is identical to VDD.

Signal Acquisition:

For all rows in the matrix, do the following:

(A) At time = 0: RS, TX, M4 are "OFF", and RST is "ON". Avalanche voltage is applied to APDs

(B) Begin signal acquisition (begin shutter time) by turning RST "OFF" and TX & M4 "ON".

(C) Capacitor N1 is now floating.

(D) Charges generated at the photo-diode begin to accumulate at capacitor N1, and the voltage at N1 begins to decrease.

(E) If the voltage at N1 decreases enough, M3 turns ON. If/when M3 turns ON, capacitor N1 is no longer floating, as M2 and M3 are conducting, and therefore a conductive path is established to Voffset. The voltage at the capacitor becomes the Logarithm of the current flowing through M2, with M3 acting as a resistive load. If photo-current sufficiently small, voltage at N1 increases up to the value at which M3 is switched OFF again.

(F) End signal acquisition (end shutter time) by turning OFF the voltage applied to the APDs, and turning TX & M4 "OFF". With TX "OFF" photo-generated charges cannot flow from the photo-diode to N1. With T4 "OFF", charges cannot flow from N1, through M2, M3 and M4, into Voffset, thereby preserving the voltage level of N1, regardless whether that voltage level was such that M3 was "OFF" or "ON".

Signal Readout:

For one row, do the following:

(G) Turn RS "ON".

(H) Column circuitry reads the "photo-signal" value, put out by M1, for the pixel:

(H1) If the voltage level put out by M1 corresponds to a value at N1 for which M3 remains OFF, then the measured signal was acquired by the accumulation of charges mode (Linear Mode).

(H2) If the voltage level put out by M1 corresponds to a value at N1 that is equal or larger than that for which M3 turns ON, then it will assumed that the measured signal was acquired by the photo-current mode (Log Mode).

(I) Turn "ON" the RST of selected row only, so that the "dark-current" level is readout immediately after the acquired signal has been readout. This also turns M3 "OFF".

(J) Turn RS "OFF".

Repeat steps (G) through (J) for all other rows in the matrix.

Third Embodiment

Referring to **FIG. 10A**, describes a 7-transistor pixel based on a modified 4T APS, with 3 additional transistors: M2 (Log) and M3 (PMOS) and PS (Pixel Select). Transistor M2 performs the logarithmic conversion of photo-current to voltage, transistor M3 is a PMOS switch. PS is a pass transistor that isolates the Floating Diffusion N1, from the RST and M1 devices (node N2).

The source of M2, the gate of M3, and the source of TX are connected to node N3, which is also connected to the anode of the photo-diode (PD) where the photo-generated electrons accumulate. The drain of the transfer gate connects to the storage node N1, which is also linked to the source of the PS transistor. The drain of M3 is connected to voltage source (VDD_LOG) that maybe varied from the periphery.

The transfer gate (TX) between the photo-diode (node N3) and the storage node (N1) is the classic method to enable an Electronic Global Shutter (EGS) for the accumulation of charges mode: when the shutter time ends, the transfer gate is turned ON to allow signal at N3 to propagate to the storage node N1, after which the transfer gate is turned OFF again, and those nodes become isolated from each other.

The signal at N3 may have been acquired in two different modes:

A. In the accumulation of charges mode, if the number of accumulated charges at N3 were not

sufficient to lower the voltage at the gate of M3 to the point of M3 being switched ON.

B. Photo-current mode, if the illumination intensity was such that the number of accumulated charges at N3 were sufficient to lower the voltage at the gate of M3, so that M3 was switched ON. If/when M3 is switched ON, photo-current flows through M2, at which point, the voltage at the source of M2 is proportional to the (natural) logarithm of the photo-current flowing through M2.

The voltage level at N3, that is transfered to and stored at N1, already contains the information on whether it is a linear signal proportional to the number of accumulated charges, or whether it is a compressed signal proportional to the logarithm of the photo-current flowing through M2.

Therefore, this pixel enables an Electronic Global Shutter (EGS) for signals acquired through combined accumulation of charges and photo-current.

In **FIG. 10A** the VDD_LOG voltage level, the RST voltage level VDD_RST, and the VDD_M1 voltage level, are presented as signals that are independent from each other, and can be distributed on a column-parallel fashion, row-parallel fashion, or on a matrix wide fashion.

In a standard implementations for 3T APS, 4T APS and 3T Log pixels, VDD_RST and VDD_M1 are the same a simply marked as VDD.

However, for the operation as a Solar Cell discussed further below, it is useful to keep this buses separate and independent.

The choice of VDD_RST and VDD_LOG and suitable biasing of the N-Well of M3 (PMOS), can be used to fine tune the "stitching point" for a seamless transition from accumulation of charges mode to logarithm of photo-current mode.

The following is a sequence of operations for image acquisition and readout, that is compatible with an Electronic Global Shutter (EGS) and with Correlated Double Sampling (CDS). The list of operations specifies the sequence of switching ON and OFF of the transistors inside the pixel shown in FIG. 4.

Signal Acquisition for Electronic Global Shutter (EGS):

For all rows in the matrix, do the following:

A. At time = 0: RST, PS, and TX, are "ON": N1 and N3 are set at VDD.
B. Begin signal acquisition (begin shutter time) by turning "OFF" PS & TX.
C. Nodes N1 and N3 are now floating.
D. Charges are generated and accumulated at the photo-diode (PD), thereby decreasing the voltage at N3.
E. If the voltage at N3 decreases enough, M3 turns ON. If/when M3 turns ON, node N3 is no longer floating, as M2 and M3 are conducting, and therefore a conductive path is established to VDD_LOG, and the voltage at N3 becomes the logarithm of the current flowing through M2, with M3 acting as a resistive load. If the photo-current is sufficiently small, voltage at N3 increases up to the value at which M3 is switched OFF again.
F. End signal acquisition (end shutter time) by turning "ON" TX for the time interval sufficient and necessary to transfer the signal from N3 to N1. Turn "OFF" TX.

Signal Readout with Correlated Double Sampling (CDS):

For one row, do the following:

(G) At time = 0, for all rows in the matrix: TX, PS and READ are "OFF".
(H) Begin readout of first row by turning "ON" the "READ" transistor, while RST remains "ON". The signal injected into the Column Bus is the dark current level (VDD) amplified through M1. A capacitor connected to the Column Bus, and that is part of the column circuitry, is charged with this (dark current) signal.

(I) Switch "OFF" the RST device.
(J) Switch "ON" the "PS" device, to allow the signal stored at N1 to be transferred to N2, thus amplified by M1, injected into the Column Bus.
(K) Column circuitry reads the "photo-signal" value, put out by M1, for the pixel:
(K1) If the voltage level put out by M1 corresponds to a value at N1 for which M3 remains OFF, then the measured signal was acquired by the accumulation of charges mode (Linear Mode).
(K2) If the voltage level put out by M1 corresponds to a value at N1 that is equal or larger than that for which M3 turns ON, then it will assumed that the measured signal was acquired by the photo-current mode (Log Mode).
(L) Expose the capacitor that had previously been charged with the "dark-current" signal, to the photo-generated signal, thus resulting in a stored value that is the difference between the two signals, thus realizing a correlated double sampling (CDS).
(M) Turn "OFF" the "READ" device.
Repeat steps (G) through (M) for all other rows in the matrix.

The same pixel architecture and mode of operation can be used with Avalanche Photo-Diodes (APDs), as shown in **FIG. 10B**.

The avalanche operation of the photo-diode leads to more electrons being generated per photon absorbed, and thus for the same amount of light absorbed, the number of accumulated charges increases according to the multiplication factor of the avalanche. This will cause the switching "ON" of M3 for less intense illumination than with a normal photo-diode. At the same time the Signal-to-Noise Ratio is increased, regardless of whether the signal is acquired in the accumulation of charges mode or in the photo-current mode.

An additional possibility, is to synchronize the VEE voltage pulse with the duration of the "shutter time", so that avalanche multiplication (and thus power consumption) only occurs during signal acquisition.

The pixels shown in **FIG. 10A** and **FIG. 10B** enable a pixel matrix to be operated in the Electronic Global Shutter (EGS), and therefore the images are free from "smearing" or motion artifacts, that are due to a continued signal acquisition during the readout phase. These artifacts occur in all un-shuttered sensor/camera designs, and essentially prevent high quality images of fast moving objects.

The pixels shown in **FIG. 10A** and **FIG. 10B** have a built-in anti-blooming capability. Blooming occurs when a charge collector overflows into its neighbor. By definition this does not occur in this pixel, and in the standard 3T Log pixels, in which the photo-current mode removes the possibility of such problem to take place.

While existing pixel architectures achieve one or more desirable features, none achieves all those listed below simultaneously:

1. Combined modes of light sensing, with a seamless transition between modes:
1a. Sensing of low light levels with an in-pixel linear operation through the accumulation of charges mode.
1b. Sensing of intense light levels with an in-pixel logarithmic conversion into voltage of photo-current.
2. Seamless transition from accumulation of charges to logarithm of photo-current, without external control signals, dependent only on the strength of the optical signal itself, and within a single signal (image) acquisition operation. This is transparent to, and does not require the interaction of, circuitry outside the pixel.
3. Possibility, during readout, for the column circuitry to discriminate which mode of operation was used to acquire the signal. The discrimination is based on the value of the output signal itself,

thereby making it straightforward to decode the readout signal by circuitry at the periphery:

3a. When the output of the pixel is above a certain voltage value, light was sensed in the accumulation of charges mode, and the signal is linearly proportional to the number of accumulated charges;

3b. When the output of the pixel is below a certain voltage value, light was sensed in the photo-current mode, and the pixel output voltage signal is a logarithmic compression of the photo-current;

4. Capability to store inside each pixel the value of the acquired signal, thereby enabling an Electronic Global Shutter (EGS), even when the signal is acquired through a photo-current mode.

5. Readout with Correlated Double Sampling (CDS) when pixel matrix operates in an EGS, because the acquired signal is stored in a capacitor ("floating diffusion") that is decoupled fromthe photo-diode by a first transfer gate, and decoupled from any other circuit elements by second transfer gate, which is missing from all other pixels designed for high dynamic range and which were discussed in this document.

6. Built-in anti-blooming capability (as in any pixel with photo-current mode).

7. Requires only Enhancement-MOSFETs and is thus fully compatible with standard CMOS.

8. Pixel circuitry sharing scheme that reduces the transistor count per pixel from 7T to 4.75T, without any loss of features and/or functionality, and that allows 2x2 binning.

9. Applicable to many types of photo-diodes, including conventional CMOS photo-diode, Pinned Photo-Diodes (PPDs) and Avalanche Photo-Diodes (APDs).

Fourth Embodiment

The configuration shown **FIG. 11A** presents a likely scenario for an actual implementation, in which VRST, Voffset and VDD are all distributed on a matrix-wide fashion, that is, identical and simultaneous for all pixels in the matrix matrix, and in which VRST is identical to VDD.

As with all arrangements in which several pixels share some transistors, each photo-diode is coupled to a transfer gate, which allow the multiplexing of the signals from each photo-diode into the shared circuitry. In this case, transfer gates are used solely for multiplexing and not for the purpose of an EGS, and only ERS operation is possible. Therefore, transistor M4 is not necessary, and the schematic of **FIG. 11A**, shows a 4 pixel cell with a total of 9 transistors, which results in a 2.25T per pixel.

Because of the multiplexing functionality of the transfer gates (TX), the conventional row-select transistor is now called the READ transistor, since it no longer selects a row, but rather controls the access of a pixel cell (with 4 pixels) to the column bus line.

The operation of the pixel cell depicted in **FIG. 11A**, is similar to that described for the pixel cell of **FIG. 6A**, with the particularity that each transfer gate (TX) in the cell, must be controlled independently from the others, which means that there must be 2 row-select signals for each row of pixels.

The pixel design of **FIG. 11A** is applicable to any photo-diode, including avalanche photo-diodes, and in particular to the APDs of U. S. Patent 6,943,051; U. S. Patent 7,265,006; U.S. Patent Application No. 11/781,544.

APDs require an avalanche inducing voltage to be applied to their terminals, and **FIG. 11B**, shows a particular configuration in which such voltage is distributed independently to each column. Other configurations for the avalanche voltage distribution are also possible, for example, distributed in parallel to all pixels in the matrix.

The operation of the pixel cell depicted in **FIG. 11B**, is similar to that described for the pixel cell of **FIG. 6B**, with the particularity that each transfer gate (TX) in the cell, must be controlled independently from the others, which means that there must be 2 row-select signals for each row of pixels.

Fifth Embodiment

The configuration shown **FIG. 12A** presents a likely scenario for an actual implementation, in which VRST, Voffset and VDD are all distributed on a matrix-wide fashion, that is, identical and simultaneous for all pixels in the matrix matrix, and in which VRST is identical to VDD.

As with all arrangements in which several pixels share some transistors, each photo-diode is coupled to a transfer gate, which allow the multiplexing of the signals from each photo-diode into the shared circuitry. In this case, transfer gates are used solely for multiplexing and not for the purpose of an EGS, and only ERS operation is possible. Therefore, transistor M4 is not necessary.

The schematic of **FIG. 12A**, shows a 8 pixel cell with a total of 16 transistors, which results in a 2T per pixel. This cell design also removes the READ transistor (existent in **FIG. 11A**).

The new cell, comprising 8 pixels, has two row-select lines, TX1 & TX2, and two column bus lines. The two blocks of 4 pixels has each one RST transistor whose gate (RST1 & RST2) and source voltages (VRST1 & VRST2) are controlled from the periphery.

The pixel design of **FIG. 12A** is applicable to any photo-diode, including avalanche photo-diodes, and in particular to the APDs of U. S. Patent 6,943,051; U. S. Patent 7,265,006; U.S. Patent Application No. 11/781,544.

APDs require an avalanche inducing voltage to be applied to their terminals, and **FIG. 12B**, shows a particular configuration in which such voltage is distributed independently to each column. Other configurations for the avalanche voltage distribution are also possible, for example, distributed in parallel to all pixels in the matrix.

Sixth Embodiment

The pixels shown in **FIG. 10A** and **FIG. 10B** can be arranged to share transistors, thereby lowering the number of transistors per pixel. In turn this allows a larger fill factor and/or smaller pixels.

FIG. 13A and FIG. 13B show a possible arrangement, which preserves all the characteristics of the non-shared 7T design of **FIG. 10A and FIG. 10B**, respectively.

In **FIG. 13A**, the central area shows the 3 transistors that are shared between 4 adjacent pixels: RST, M1, and READ, which means that each individual pixel has 4 transistors that are not shared., for a total of 4x4+3=19 transistors for 4 pixels. This results in 4.75 transistors per pixel.

The principles of operation are identical to those outlined for the pixel of **FIG. 10A and FIG. 10B**. If the readout phase is carried out for all pixels in parallel, then one has a 2x2 binning. If the readout phase is carried out in a time-switched sequence for each pixel, then the resolution is preserved

With the sharing scheme of **FIG. 13A and FIG. 13B**, all pixels operate independently during the signal acquisition phase, and since each pixel possesses an independent storage node N1, decoupled from the shared circuitry by the pass transistor PS (Pixel Select), the pixel matrix can still be operated in an EGS.

All the advantages for the pixel of **FIG. 10A and FIG. 10B**, listed further below, are also applicable to the sharing scheme of **FIG. 14A and FIG. 10B**.

Seventh Embodiment

The pixels shown in **FIG. 14A** and **FIG. 14B** provide another sharing arrangement for the non-shared pixel shown in **FIG. 10A and FIG. 10B**. This sharing arrangement for the pixel depicted in **FIG. 10A and FIG. 10B** is similar to the sharing arrangement show in **FIG. 12A and FIG. 12B** for the pixel

depicted in **FIG. 7A and FIG. 7B**.

The schematic of **FIG. 14A**, shows a 8 pixel cell with a total of 3636 transistors, which results in a 4.5T per pixel. This cell design also removes the READ transistor (existent in **FIG. 13A**).

The new cell, comprising 8 pixels, has two row-select lines, TX1 & TX2, and two column bus lines. The two blocks of 4 pixels has each one RST transistor whose gate (RST1 & RST2) and source voltages (VRST1 & VRST2) are controlled from the periphery.

The pixel design of **FIG. 14A** is applicable to any photo-diode, including avalanche photo-diodes, and in particular to the APDs of U. S. Patent 6,943,051; U. S. Patent 7,265,006; U.S. Patent Application No. 11/781,544.

APDs require an avalanche inducing voltage to be applied to their terminals, and **FIG. 14B**, shows a particular configuration in which such voltage is distributed independently to each column. Other configurations for the avalanche voltage distribution are also possible, for example, distributed in parallel to all pixels in the matrix.

Solar Cell Operation

The pixel cells of **FIGs. 6A & 6B**, **FIGs. 8A & 8B**, **FIGs. 10A & 10B**, **FIG. 12A** & **12B**, **FIG. 13A** & **13B**, **FIG. 14A** & **14B**, can be operated in a mode in which the photo-current is guided into the periphery though the RST transistor. This can be done by connecting the VDD_RST (or VRST1 and VRST2) line, at the periphery of the pixel matrix, to two pass transistors:

A. A first pass-transistor connects to a standard VDD voltage source, in which case the pixels operate in the normal imaging mode, or

B. A second pass-transistor allows the photo-current, originated at the pixels, to flow to circuit that will process it for either battery storage or powering other circuits.

The image sensor can be used as a "pixelated solar cell" when not in use to acquire images. There are certain control signals necessary to acquire images, and when those are not activated, it could automatically mean that the circuitry that uses the energy generated as a solar cell, is activated. This concept can be applied to CCDs and the most common CIS, such as the 3T and 4T APS.

For example, the circuit of FIG. 12A operates as a solar cell, when TX and PS and RST are ON for all pixels, while the VDD_LOG and VDD_M1 lines are connected (at the periphery), through pass transistors, to blocks of circuitry that will process the photo-current for the purpose of power generation and/or storage.

The top electrode is the interconnect line VDD_RST, which may be connected in a column-parallel configuration, or on a matrix-wide configuration. In any case, all photo-diodes are connected in parallel.

Solar cell operation is also possible when the photo-diode is an APD, with the advantage that the bottom electrode in a N-Well, which is decoupled from adjacent N-Wells. Because the top electrodes of the APDs are also connected on a column-parallel fashion, one column of pixels can be connected in a series arrangement, thereby enabling the doubling of the open circuit voltage, which may be beneficial in the sense that DC-DC voltage conversion at the periphery might no longer be necessary.

Claims

Claim 1: A pixel circuit comprising,

a photo-diode whose cathode is connected to a first node,

a first NMOS device whose gate is connected to said first node, its drain is connected to a voltage source, and its source is connected to a source/drain region of second NMOS,

a second NMOS with one source/drain region connected to said first NMOS device, and the other source/drain region connected to an output line, and its gate connected to a "read" control signal,

a third NMOS device whose gate is connected to a reset control signal, its drain is connected to a voltage source, and its source is connected to said first node,

a fourth NMOS device whose source is connected to said first node, its gate is connected to its drain, and its drain is connected to the source of a PMOS device

a PMOS device whose drain is connected to a voltage source, its drain is connected to the drain of said fourth NMOS device and whose gate is connected to said first node, wherein said PMOS device is on N-Well that can be independently biased, and said bias can be dynamically changed by control signals to adjust the threshold of said PMOS.

Claim 2: A pixel circuit comprising,

a photo-diode whose cathode is connected to a first node,

a capacitor connected to said first node and to a voltage source,

a first NMOS device whose gate is connected to said first node, its drain is connected to a voltage source, and its source is connected to a source/drain region of second NMOS,

a second NMOS with one source/drain region connected to said first NMOS device, and the other source/drain region connected to an output line, and its gate connected to a "read" control signal,

a third NMOS device whose gate is connected to a reset control signal, its drain is connected to a voltage source, and its source is connected to said first node,

a fourth NMOS device whose source is connected to said first node, its gate is connected to its drain, and its drain is connected to the source of a PMOS device

a PMOS device whose drain is connected to a voltage source, its drain is connected to the drain of said fourth NMOS device and whose gate is connected to said first node, wherein said PMOS device is on N-Well that can be independently biased, and said bias can be dynamically changed by control signals to adjust the threshold of said PMOS.

Claim 3: A pixel circuit comprising,

a photo-diode whose cathode is connected to the source region of a first NMOS device (transfer gate), whose gate is connected to a control signal, and whose drain is connected to a first node,

a capacitor connected to said first node and to a voltage source,

a second NMOS device whose gate is connected to said first node, its drain is connected to a voltage source, and its source is connected to a source/drain region of third NMOS,

a third NMOS with one source/drain region connected to said second NMOS device, and the other source/drain region connected to an output line, and its gate connected to a "read" control signal,

a fourth NMOS device whose gate is connected to a reset control signal, its drain is connected to a voltage source, and its source is connected to said first node,

a fifth NMOS device whose source is connected to said first node, its gate is connected to its drain, and its drain is connected to the source of a PMOS device,

a PMOS device whose drain is connected to a voltage source, its drain is connected to the drain of said fifth NMOS device and whose gate is connected to said first node, wherein said PMOS device is on N-Well that can be independently biased, and said bias can be dynamically changed by control signals to adjust the threshold of said PMOS.

Claim 4: A pixel circuit comprising,

a photo-diode whose cathode is connected to the source region of a first NMOS device (transfer gate), whose gate is connected to a control signal, and whose drain is connected to a first node,

a capacitor connected to said first node and to a voltage source,

a second NMOS device whose gate is connected to said first node, its drain is connected to a voltage source, and its source is connected to a source/drain region of third NMOS,

a third NMOS with one source/drain region connected to said second NMOS device, and the other source/drain region connected to an output line, and its gate connected to a "read" control signal,

a fourth NMOS device whose gate is connected to a reset control signal, its drain is connected to a voltage source, and its source is connected to said first node,

a fifth NMOS device whose source is connected to said first node, its gate is connected to its drain, and its drain is connected to the source of a PMOS device,

a PMOS device whose drain is connected to the source of a sixth NMOS device, its drain is connected to the drain of said fifth NMOS device and whose gate is connected to said first node,

A sixth NMOS device whose drain is connected to a voltage source, its source is connected to drain of said PMOS device, and whose gate is connected to a control signal, wherein said PMOS device is on N-Well that can be independently biased, and said bias can be dynamically changed by control signals to adjust the threshold of said PMOS.

Claim 5: A pixel circuit comprising,

a photo-diode whose cathode is connected to a node N3,

a first NMOS device, whose source is connected to said node N3, whose gate is connected to a control signal, and whose drain is connected to a node N1,

a capacitor connected to said node N1 and to a voltage source,

a second NMOS device (transfer gate) whose gate is connected to a control signal, whose source is connected to node N1 and whose drain is connected to node N2.

a third NMOS device whose gate is connected to node N2, its drain is connected to a voltage source, and its source is connected to a source/drain region of third NMOS,

a fourth NMOS with one source/drain region connected to said second NMOS device, and the other source/drain region connected to an output line, and its gate connected to a "read" control signal,

a fifth NMOS device whose gate is connected to a reset control signal, its drain is connected to a voltage source, and its source is connected to said node N2,

a sixth NMOS device whose source is connected to said node N3, its gate is connected to its drain, and its drain is connected to the source of a PMOS device,

a PMOS device whose drain is connected to a voltage source, its source is connected to the drain of said sixth NMOS device and whose gate is connected to said node N3, wherein said PMOS device is on N-Well that can be independently biased, and said bias can be dynamically changed by control signals to adjust the threshold of said PMOS.

Claim 6: The pixel circuit of claim 3 wherein,

the photo-diode and NMOS transfer gate of a plurality of pixels are connected in parallel to said first node, and wherein all other MOSFET devices connected to that node are shared by said plurality of pixels.

Claim 7: The pixel circuit of claim 4 wherein,

the photo-diode and NMOS transfer gate of a plurality of pixels are connected in parallel to said first node, and wherein all other MOSFET devices connected to that node are shared by said plurality of pixels.

Claim 8: The pixel circuit of claim 5 wherein,

the photo-diode and NMOS transfer gate of a plurality of pixels are connected in parallel to said node N2, and wherein all other MOSFET devices connected to that node are shared by said plurality of pixels.

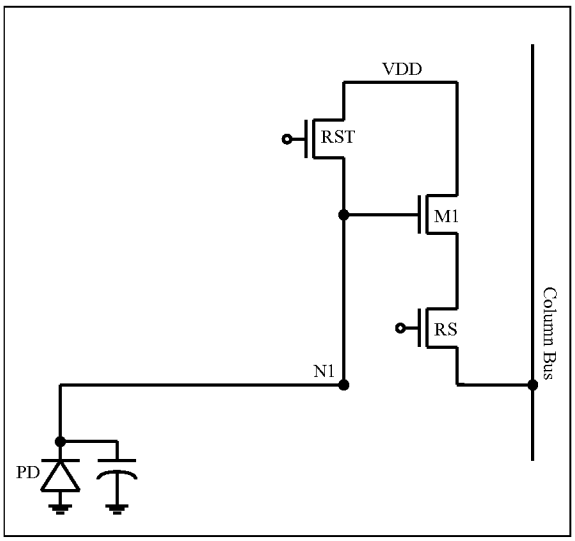


FIG. 1

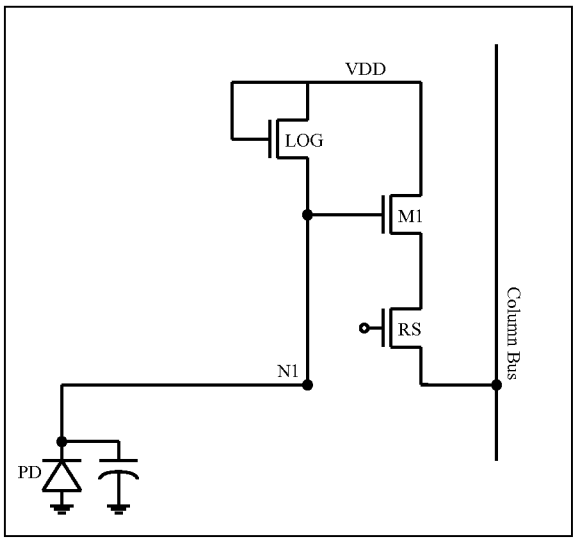


FIG. 2

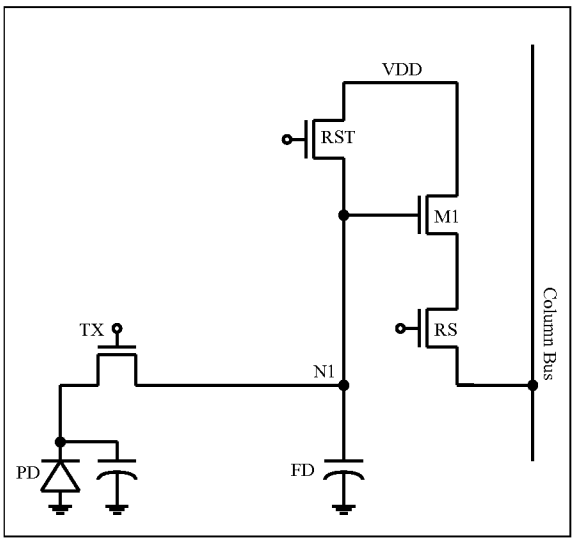


FIG. 3

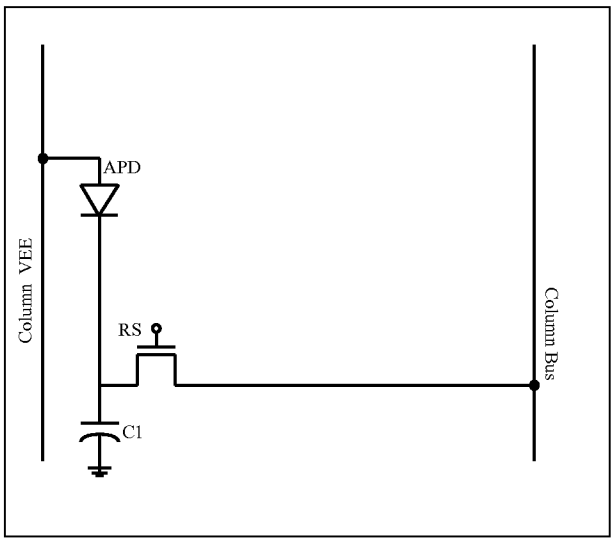


FIG. 4

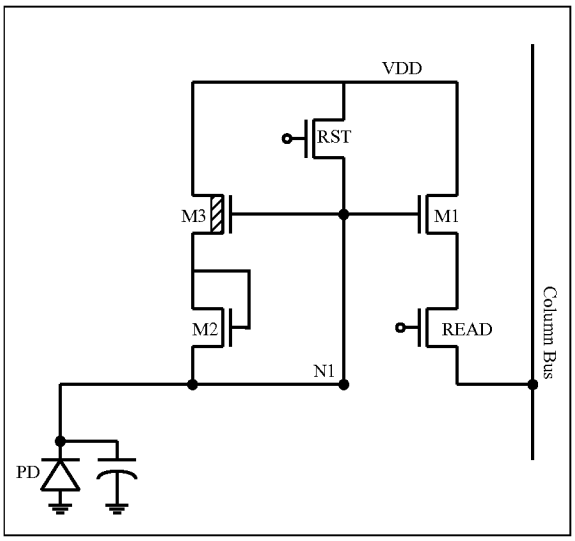


FIG. 5A

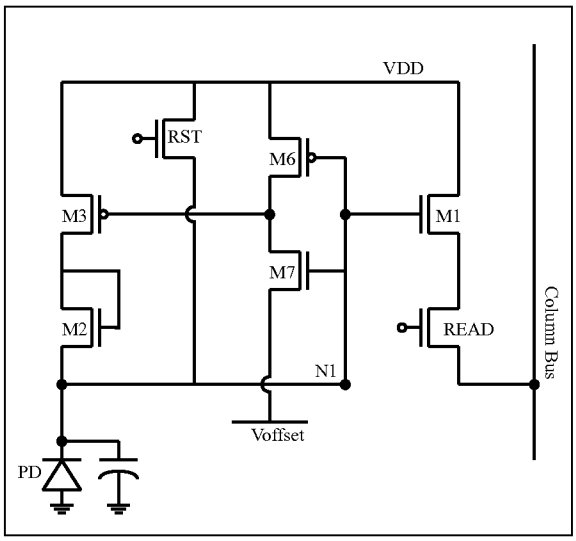


FIG. 5B

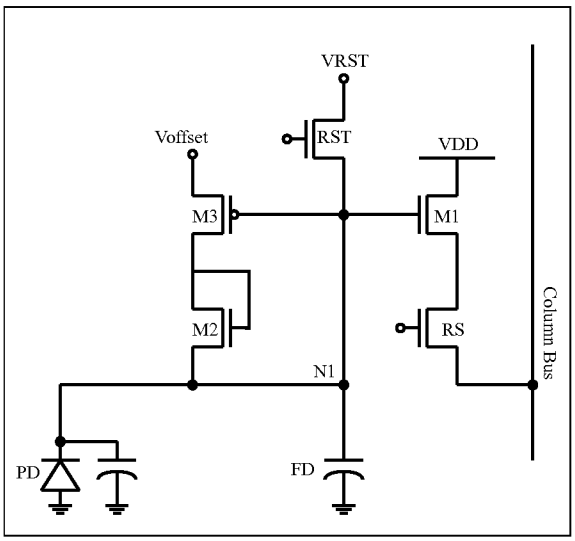


FIG. 6A

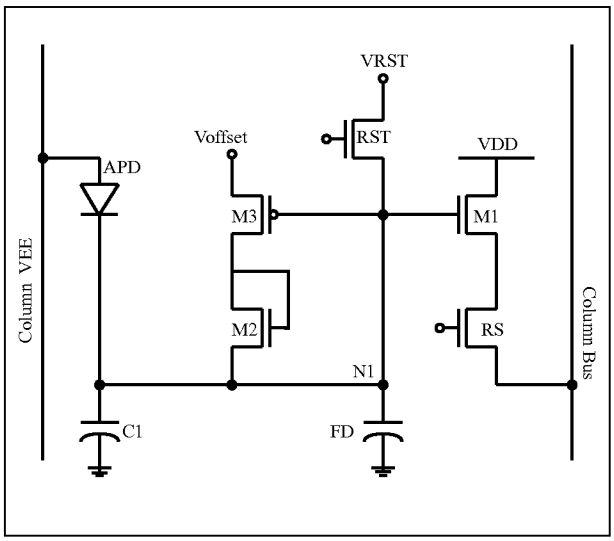


FIG. 6B

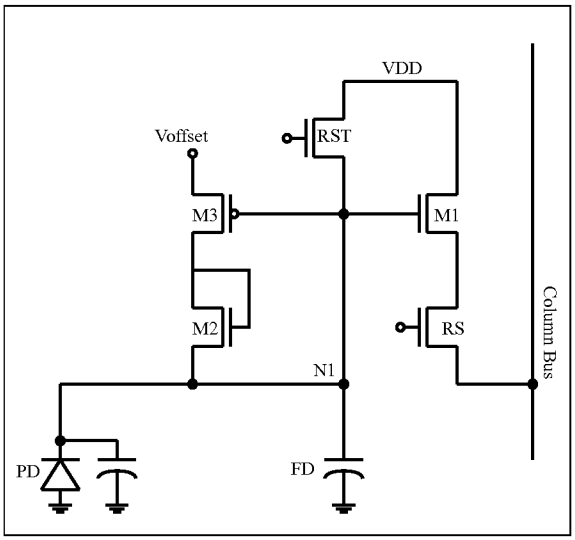


FIG. 7A

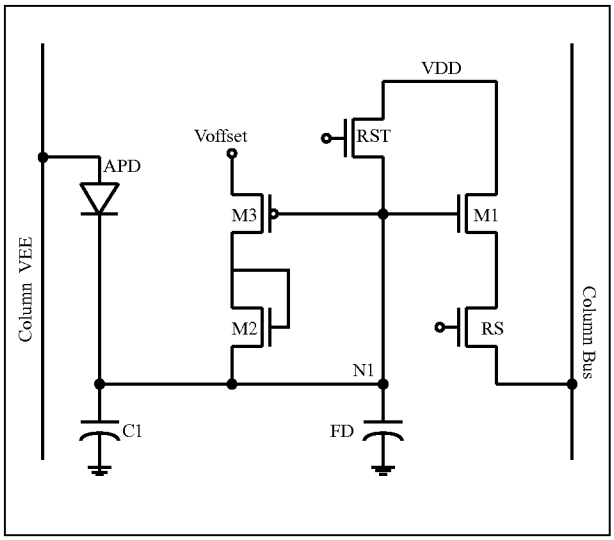


FIG. 7B

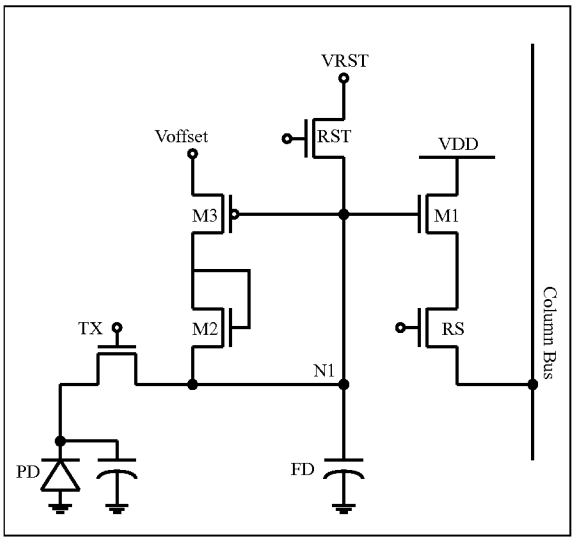


FIG. 8A

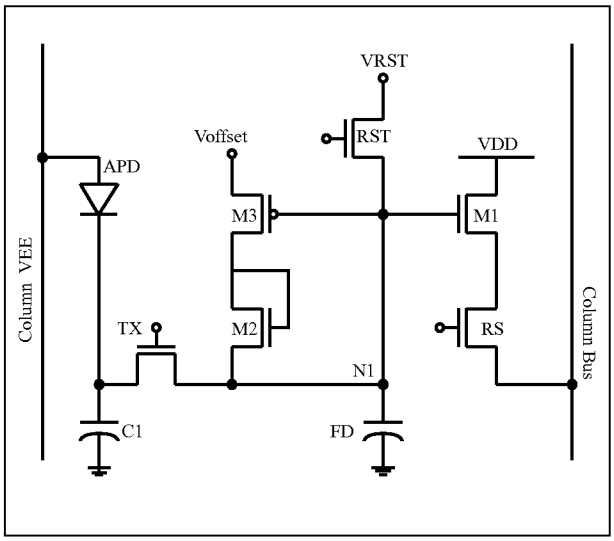


FIG. 8B

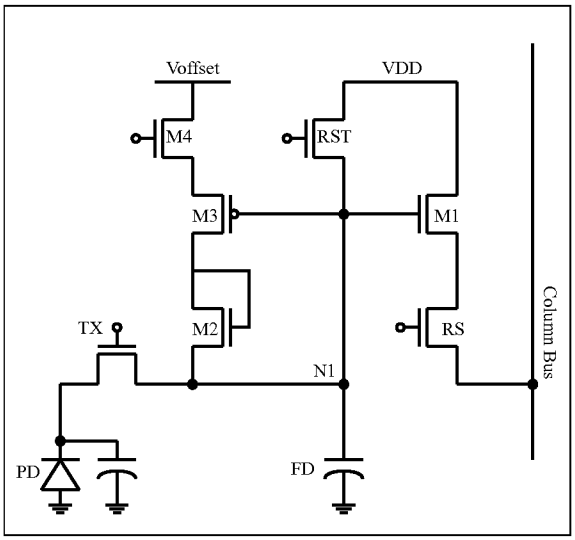


FIG. 9A

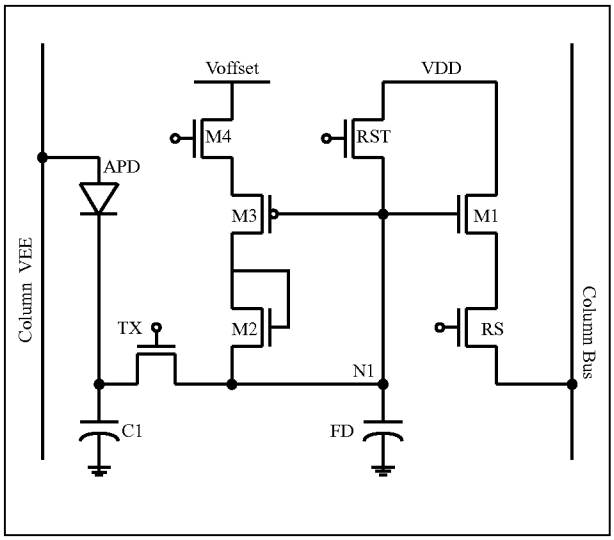


FIG. 9B

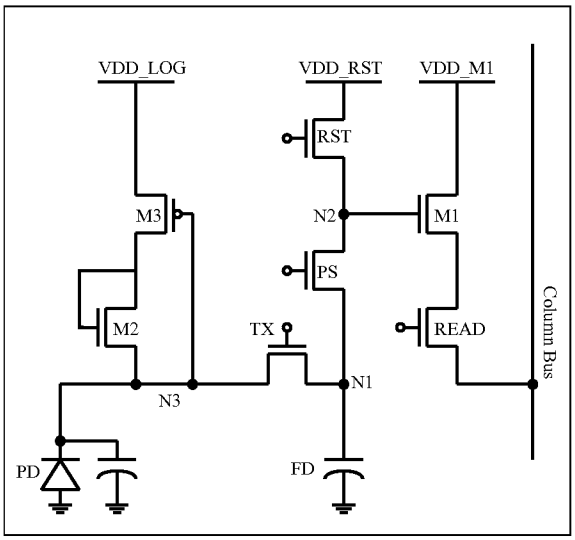


FIG. 10A

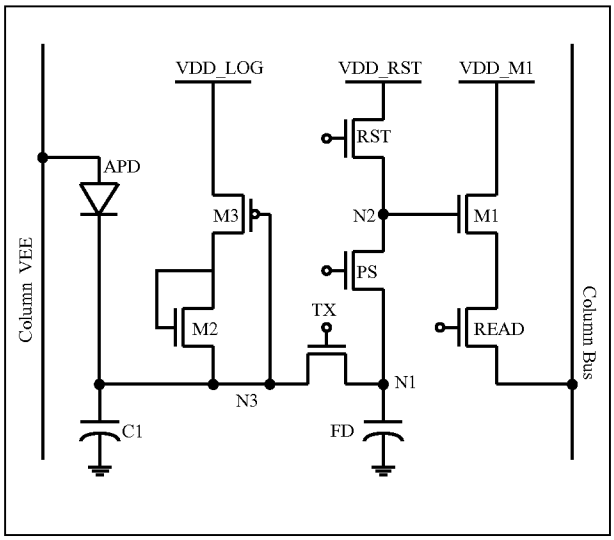


FIG. 10B

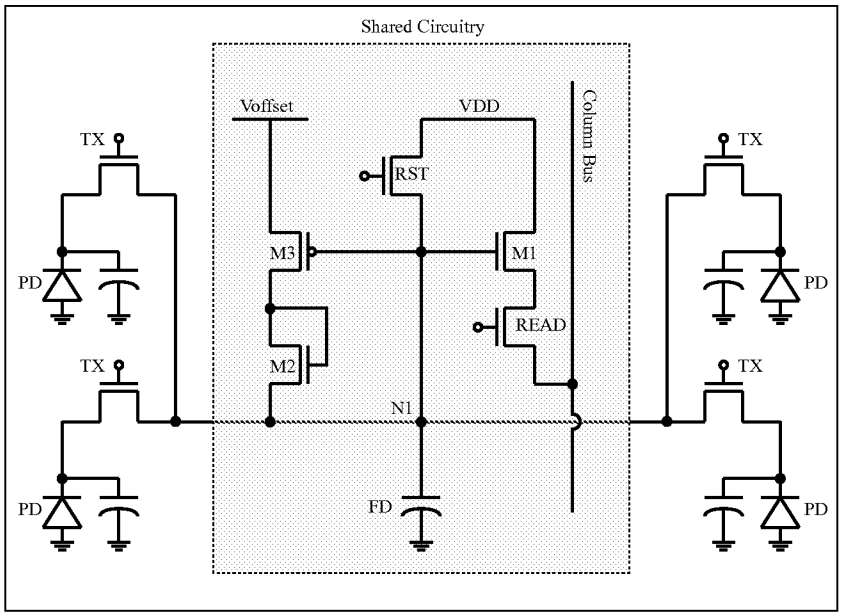


FIG. 11A

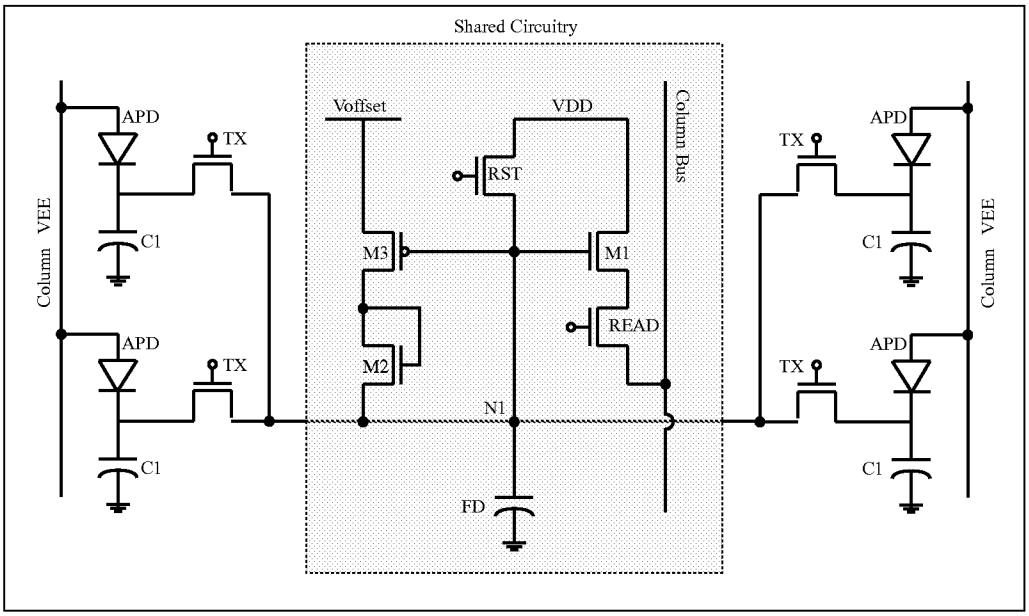


FIG. 11B

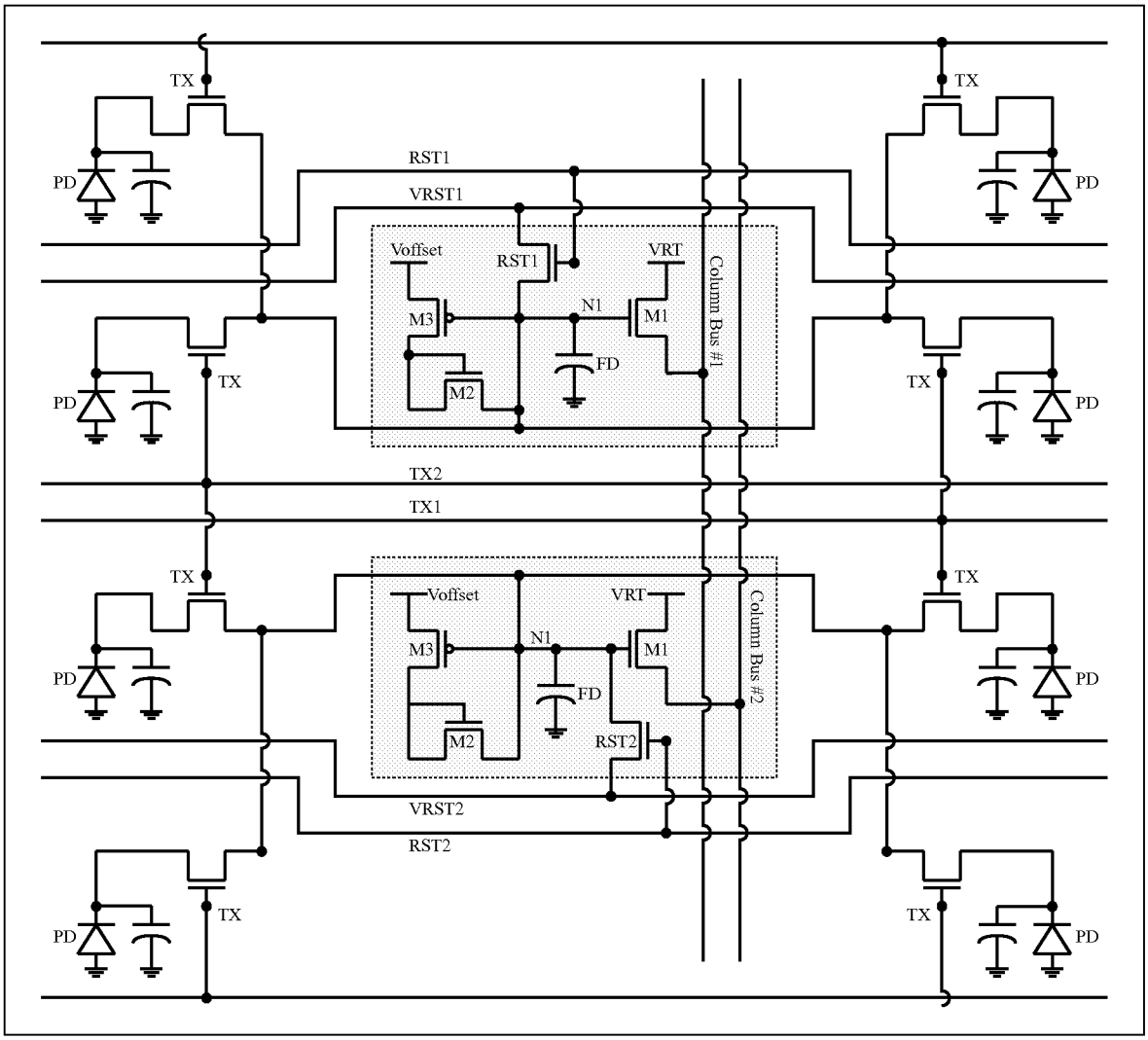
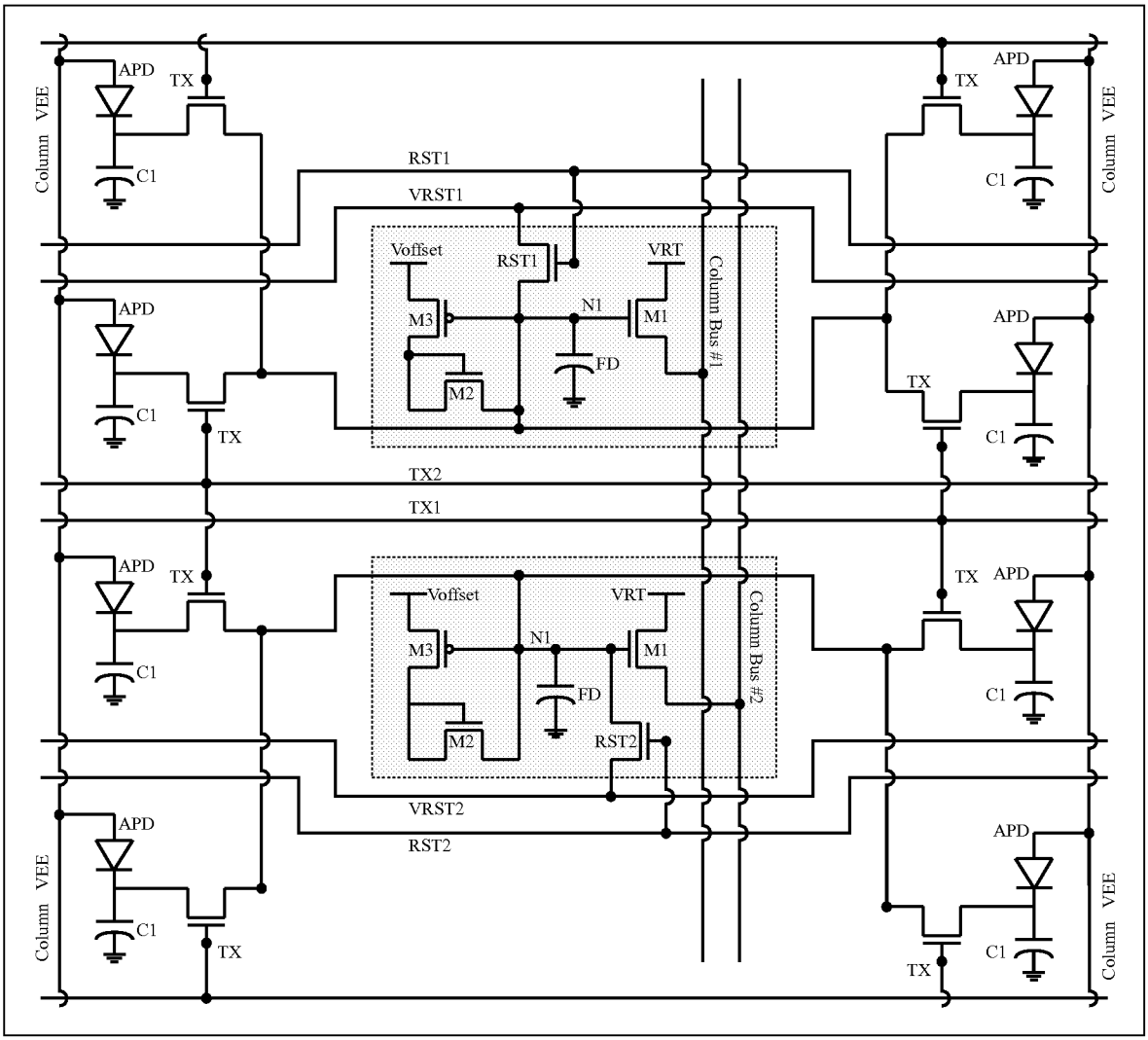

TX
PD
RST1
VRST1
Voffset
RST1
VRT
M3
N1
M1
FD
M2
Column Bus #1
TX2
TX1
RST2
VRST2
Column Bus #2

FIG. 12A


APD
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C1
Column VEE
RST1
VRST1
Voffset
VRT
M3
M2
N1
M1
FD
Column Bus #1
TX2
TX1
RST2
VRST2
Column Bus #2

FIG. 12B

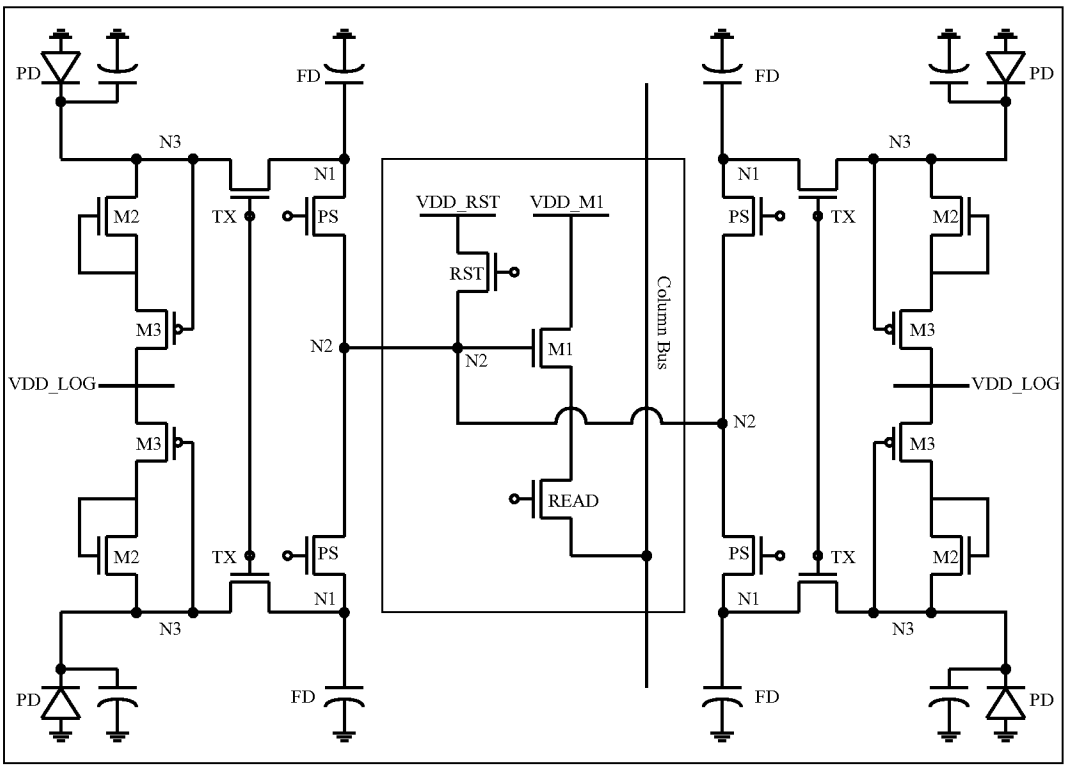


FIG. 13A

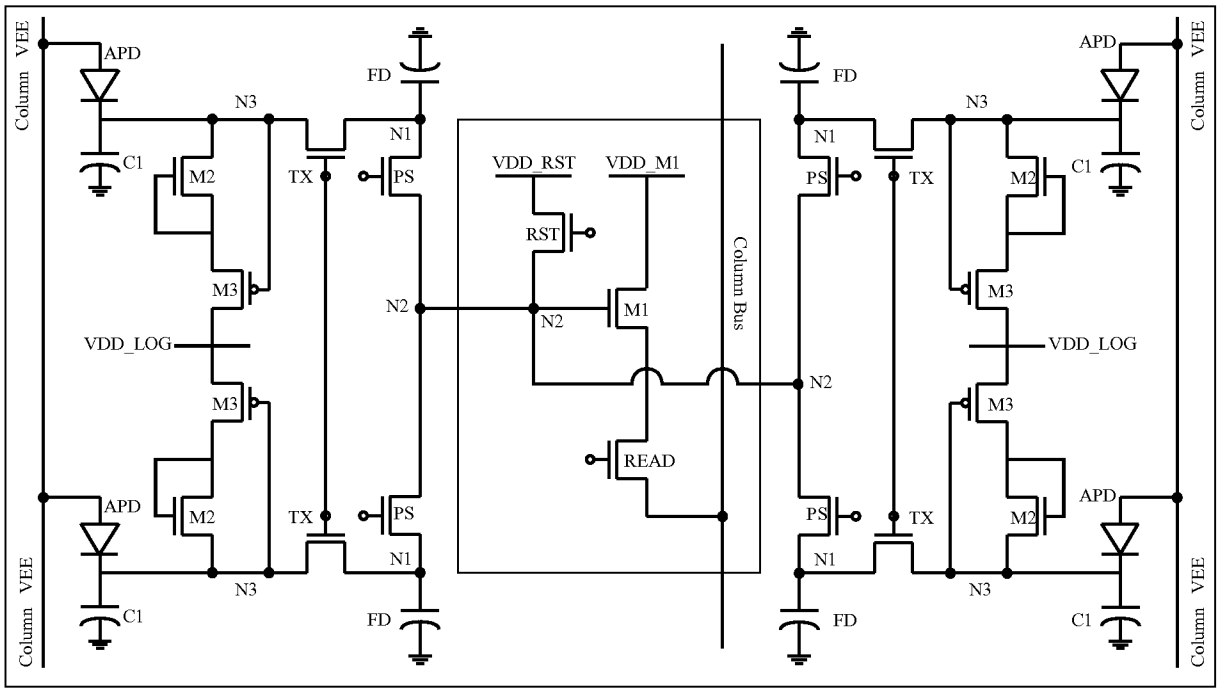
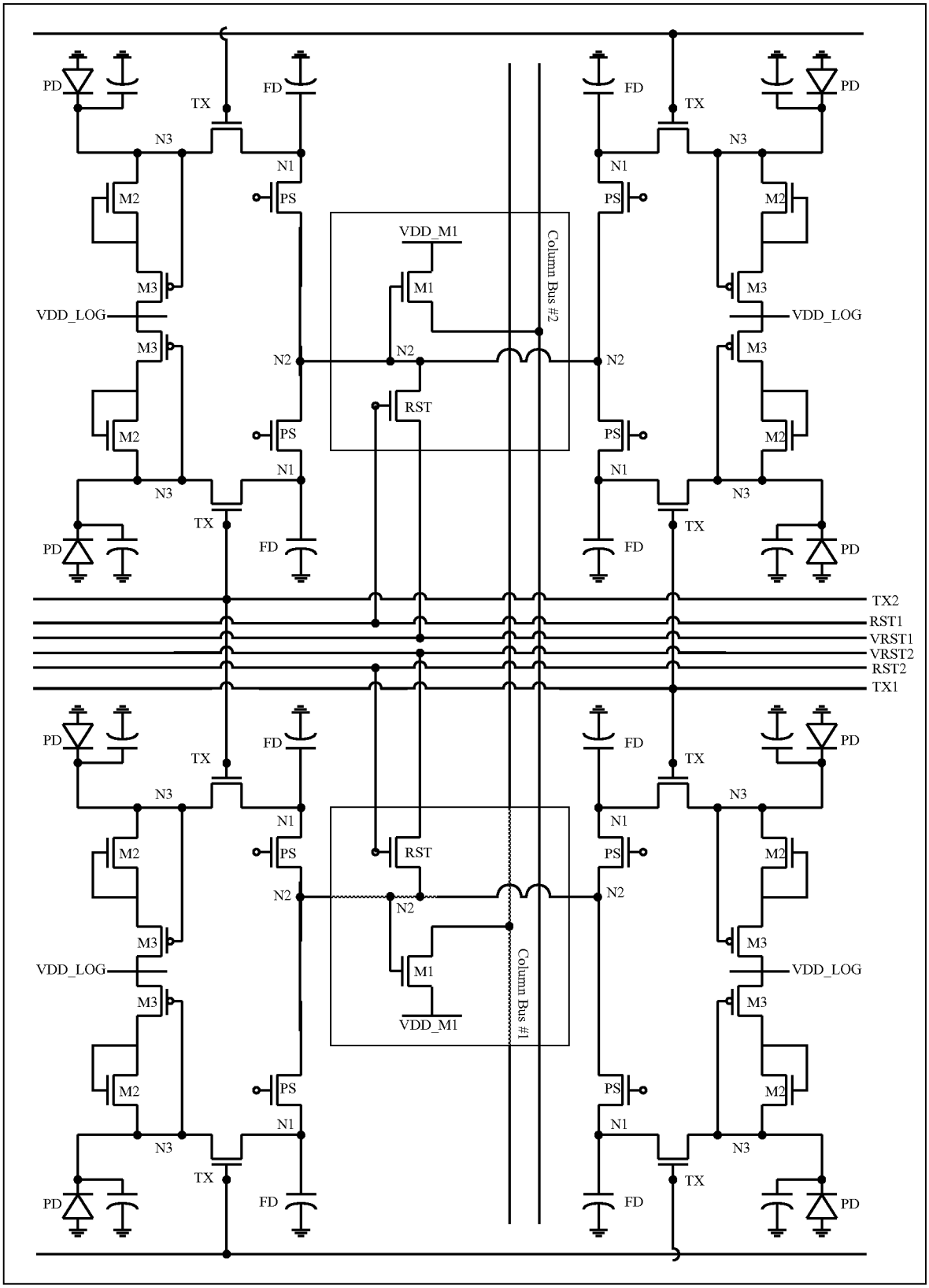


FIG. 13B


PD
TX
FD
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N1
M2
PS
VDD_M1
Column Bus #2
M1
M3
VDD_LOG
N2
RST
TX2
RST1
VRST1
VRST2
RST2
TX1
Column Bus #1

FIG. 14A

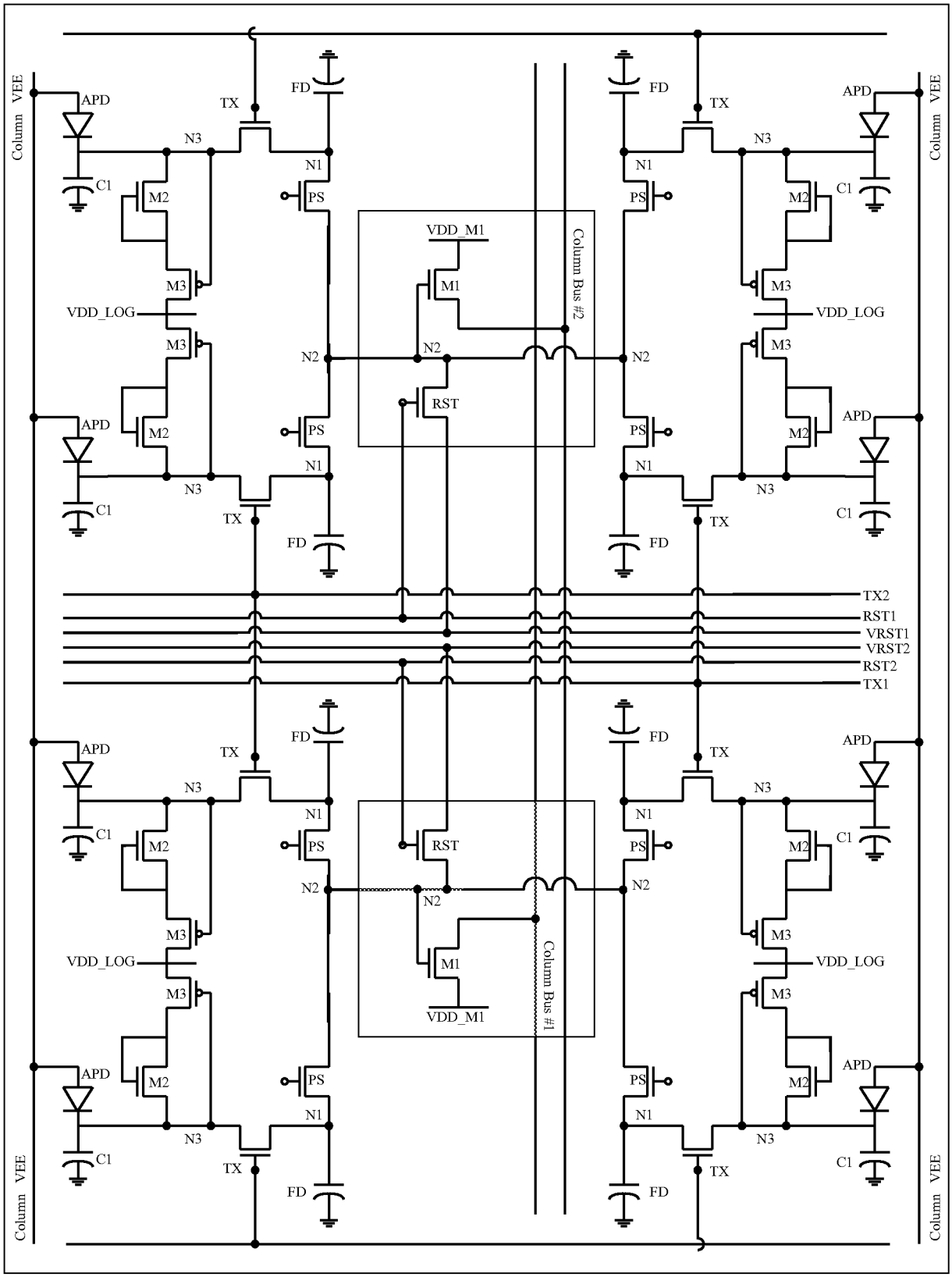
Column VEE
APD
C1
TX
FD
N3
N1
M2
PS
M3
VDD_LOG
N2
VDD_M1
M1
RST
Column Bus #2
Column Bus #1
TX2
RST1
VRST1
VRST2
RST2
TX1

FIG. 14A