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(71) Applicant: **ARCELIK ANONIM SIRKETI** [TR/TR]; E5 Ankara Asfalti Uzeri, Tuzla, 34950 Istanbul (TR).

(72) Inventors: **ECEVIT, Ahmet Berkant**; E5 Ankara Asfalti Uzeri, Tuzla, 34950 Istanbul (TR). **TURK, Reyhan**; E5 Ankara Asfalti Uzeri, Tuzla, 34950 Istanbul (TR). **YARDIBI, Hakan Suleyman**; E5 Ankara Asfalti Uzeri, Tuzla, 34950 Istanbul (TR).

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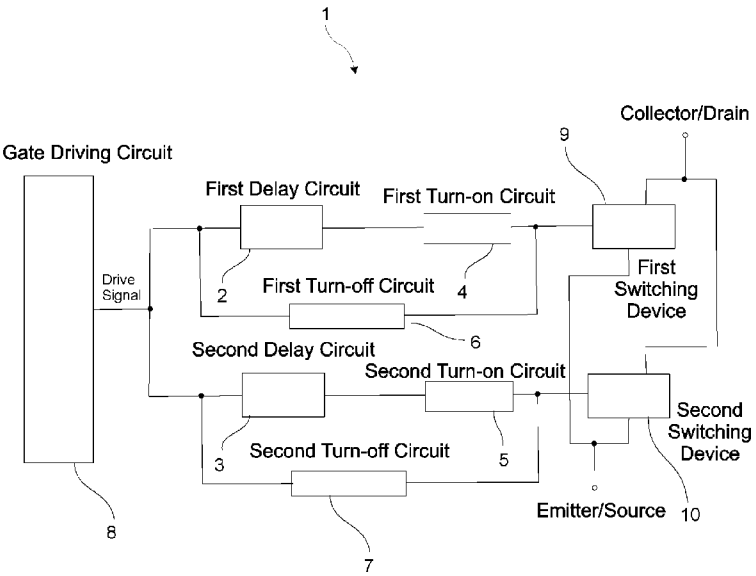
(54) Title: PARALLEL-COUPLED SWITCHING DEVICES AND SWITCH-MODE POWER CONVERTER

Fig. 1



(57) Abstract: The present invention relates to a power electrical switching circuit and more particularly to parallel-coupled switching devices and an associated switched-mode power converter (1). The present invention more particularly relates to a switched-mode power converter (1) comprising a first switching device (9) connected electrically in parallel to a second switching device (9), the first and second switching devices (9 and 10) being driven by a gate driving circuit (8).

Description

PARALLEL-COUPLED SWITCHING DEVICES AND SWITCH-MODE POWER CONVERTER

[0001] The present invention relates to an electrical power switching circuit and more particularly to parallel-coupled switching devices and an associated switch-mode power converter.

[0002]

Switching devices such as IGBTs (Insulated Gate Bipolar Transistor) are capable of high switching speeds needed for certain loads such as electrical motors. Instantaneous power dissipation occurs in a switching device during the turn-on and turn-off intervals. Since the switching power loss is linearly dependent on the switching frequency, a switching device with shorter switching times will substantially limit the switching power loss.

[0003] On the other hand, it is also to be noted that the power loss of the switching device during conduction also adds to the power dissipation during the on-state. The on-state voltage is decisive in determining conduction losses.

[0004]

[0005] Among others, a prior art publication in the technical field of the invention may be referred to as US4532443, which discloses a power switching circuit for switching power from a DC supply to a regenerative load, comprising: a plurality of power MOSFETs each having source, drain and gate elements with the source-drain circuits parallel connected between the DC supply and the regenerative load, each of the MOSFETs having an inherent reverse diode junction between the source and drain elements; a control signal source having a switching control signal output connected with the gate element of each MOSFET, switching the MOSFET source-drain circuits on and off at a selected rate; a first diode connected in parallel with the source-drain circuits of the power MOSFETs and poled to conduct reverse current from the load; and a second diode connected in series with the source-drain circuits of the power MOSFETs and poled to block current flow through the reverse diode junctions of the MOSFETs,

the series combination of the second diode and the source-drain circuits of the power MOSFETs being shunted by the first diode.

[0006] The present invention provides a switched-mode power converter having parallel-coupled switching devices operable so as to feature decreased switching and conduction losses as provided by the characterizing features defined in Claim 1.

[0007] Primary object of the present invention is to provide a switched-mode power converter having parallel-coupled switching devices operable so as to feature decreased switching and conduction losses.

[0008] The present invention proposes a switched-mode power converter comprising parallel switching devices such that a first delaying circuit in electrical connection with a gate driving circuit and a first switching device delays turn-off of the first switching device. Further a second delaying circuit in electrical connection with the gate driving circuit and a second switching device delays turn-on of the second switching device.

[0009] The first switching device is faster than the second switching device in the sense that it has shorter turn-on and turn-off crossover intervals in comparison to the second switching device.

[0010] In sum, the first faster switching device with lower turn-on power loss starts conducting prior to the second switching device so that it conducts a greater proportion of the current being shared. On the other hand, it continues to conduct current while the second switching device is being turned off as a result of which a greater proportion of the switching off current switches to the faster switching device.

[0011] Accompanying drawings are given solely for the purpose of exemplifying a switch-mode power converter whose advantages over prior art were outlined above and will be explained in brief hereinafter.

[0012] The drawings are not meant to delimit the scope of protection as identified in the claims nor should they be referred to alone in an effort to interpret the scope identified in the claims without recourse to the technical disclosure in the description of the present invention.

[0013] Fig. 1 demonstrates a simplified block diagram of a switched-mode power converter driving circuit according to the present invention.

[0014] Fig. 2 demonstrates a circuit diagram of a switched-mode power converter driving signal adjustment circuit according to the present invention.

[0015] The following numerals are assigned to different parts being referred to in the detailed description:

1. Switched-mode power converter
2. First delay circuit
3. Second delay circuit
4. First turn-on circuit
5. Second turn-on circuit
6. First turn-off circuit
7. Second turn-off circuit
8. Gate driving circuit
9. First switching device
10. Second switching device

[0016] The present invention proposes a switched-mode power converter designated generally by the numeral 1. The switched-mode power converter (1) comprises parallel-coupled first and second switching devices (9 and 10) such as for instance IGBTs (Insulated Gate Bipolar Transistor).

[0017] A switching device causes Instantaneous power dissipation during the turn-on and turn-off intervals. When a switching device is turned on, the current flows through the switching device while a parallel diode remains reverse biased. On the other hand, when the switching device is turned off, an input voltage appears across the switching device.

[0018] During the turn-on transition of the switching device, a delay time will be followed by a current rise time upon which the voltage across the terminals of the switching device falls to a certain on-state value. As the switching device will remain in conduction during a conduction time, which can typically be larger than the turn-on and turn-off transition times, the energy losses during the conduction time will be dependent on the on-state voltage and current.

[0019] Likewise, during the turn-off transition of the switching device, a turn-off delay will be followed by a voltage rise upon which the parallel diode

becomes forward biased and conducts current.

[0020] According to the present invention, a first switching device (9) with shorter turn-on and turn-off crossover intervals in comparison to a second switching device (10) is connected in parallel to the first switching device (9). In other words, the second switching device (10) has larger turn-on and turn-off transition times compared to the first switching device (9). Therefore, the first switching device (9) according to the invention is faster compared to the second switching device (10) connected in parallel.

[0021] While a first turn-on circuit (4) effectuates turning on of the first switching device (9), a first turn-off circuit (6) accordingly turns off the first switching device (9). Likewise, second turn-on and turn-off circuits (5, 7) function so as to initiate and terminate the conduction state of the second switching device (10). According to the present invention, first and second delay circuits (2, 3) provide that the first and second switching devices (9, 10) are biased to conduction and non-conduction modes.

[0022] The first and second delay circuits (2, 3) serve to the purpose of lowering power losses and increasing power conversion efficiency by way of delaying turning-on and turning-off of the first and second switching devices (9, 10) as will be delineated hereinafter.

[0023] Turn-on of the second switching device (10), which is slower compared to the first switching device (9), is delayed by the second delay circuit (3). Therefore, the first switching device (9) with lower turn-on power loss starts conducting prior to the second switching device (10) and by the time the second switching device (10) is turned on, the first switching device (9) conducts a greater proportion of the current, thereby contributing to lowering overall switching power losses.

[0024] Likewise, the first delay circuit (2) serves to the purpose of delaying turning-off of the first switching device (9). Therefore, the first switching device (9) continues to conduct current while the second switching device (9) is being turned off and therefore transitions between conduction and non-conduction modes of the switched-mode power converter (1) is substantially effectuated by the first switching device (9), which is faster and thereby incurring lower switching losses.

[0025] According to the present invention, while the faster switching device (the first switching device, 9) with lower turn on power loss switches a greater proportion of the current on and off, the slower parallel switching device (the second switching device, 10) having lower on-state loss characteristics shares the conduction current during the on-state duration so that a lower overall conduction loss occurs compared to the situation where the faster switching device (the first switching device, 9) operates alone.

[0026] As the power loss of the switching devices during the on-state also adds to the overall power dissipation, the on-state voltage drop of the switching devices is decisive in determining conduction losses. Therefore, the circuit arrangement according to the present invention advantageously lowers conduction losses by the second switching device (10) while at the same time lowering switching losses thanks to the first switching device (9).

[0027] It is established that the circuit topology with the first and second switching devices (9, 10) being in parallel offers increased efficiency by 2,5% compared to the faster switching device (the first switching device, 9) operating alone and by 8,1 percent compared to the slower switching device (the second switching device, 10) if operated alone. It is to be noted that the efficiency of the converter will increase even further depending on the switching frequency of the switched-mode power converter (1) since the switching power loss is linearly dependent on the switching frequency and a switching device with shorter switching times will substantially limit switching losses.

[0028] Referring to Fig. 2 depicting an exemplary embodiment according to the present invention, the first delay circuit (2) generating the “faster switch” output can be realized by way of changing the values of the resistor R_4 and capacitor C_1 so as to adjust the turn-on time of the transistor Q_2 so that the turn-off time of the first switching device (9) connected to the “faster switch” output can be delayed.

[0029] Likewise, the second delay circuit (3) generating the “slower switch” output can be realized by way of changing the values of the resistor R_1 and capacitor C_2 so as to adjust the turn-on time of the transistor Q_1 so that

the turn-on time of the second switching device (10) connected to the "slower switch" output can be delayed. Therefore, the first and second delay circuits (2, 3) respectively delay turn-off of the first switching device (9) and turn-on of the second switching device (10).

[0030] According to the invention, a first delaying circuit (2) is connected between a gate driving circuit (8) and the first switching device (9) in the manner that the first delaying circuit (2) delays turn-off of the first switching device (9) and a second delaying circuit (3) is connected between the gate driving circuit (8) and the second switching device (10) in the manner that the second delaying circuit (3) delays turn-on of the second switching device (10).

[0031] In summary, the present invention proposes a switched-mode power converter (1) comprising a first switching device (9) connected electrically in parallel to a second switching device (10), the first and second switching devices (9 and 10) being driven by a gate driving circuit (8).

[0032] In one embodiment of the present invention, a first delaying circuit (2) is connected between the gate driving circuit (8) and the first switching device (9) in the manner that the first delaying circuit (2) delays turn-off of the first switching device (9) and a second delaying circuit (3) is connected between the gate driving circuit (8) and the second switching device (10) in the manner that the second delaying circuit (3) delays turn-on of the second switching device (10).

[0033] In a further embodiment of the present invention, the first switching device (9) has shorter turn-on and turn-off crossover intervals in comparison to the second switching device (10).

[0034] In a further embodiment of the present invention, a first turn-on circuit (4) provides that the first switching device (9) is biased to conduction and a first turn-off circuit (6) provides that the first switching device (9) is biased to non-conduction modes.

[0035] In a further embodiment of the present invention, a second turn-on circuit (5) provides that the second switching device (10) is biased to conduction and a second turn-off circuit (7) provides that the second switching device (10) is biased to non-conduction modes.

[0036] In a further embodiment of the present invention, the first switching device (9) with lower turn-on and turn-off power loss starts conducting prior to the second switching device (10) and by the time the second switching device (10) is turned on, the first switching device (9) conducts a greater proportion of the current being shared.

[0037] In a further embodiment of the present invention, the first switching device (9) continues to conduct current while the second switching device (9) is being turned off.

[0038] In a further embodiment of the present invention, transitions between conduction and non-conduction modes of the switched-mode power converter (1) is substantially effectuated by the first switching device (9).

[0039] The present invention therefore provides a switched-mode power converter (1) having parallel-coupled first and second switching devices (9, 10) operable so as to feature decreased switching and conduction losses. While the first switching device (9) provides lowering of the switching losses, the second switching device (10) is advantageous in lowering on-state losses.

Claims

1. A switched-mode power converter (1) comprising a first switching device (9) connected electrically in parallel to a second switching device (9), the first and second switching devices (9 and 10) being driven by a gate driving circuit (8), **characterized in that**

   a first delaying circuit (2) is connected between the gate driving circuit (8) and the first switching device (9) in the manner that the first delaying circuit (2) delays turn-off of the first switching device (9) and a second delaying circuit (3) is connected between the gate driving circuit (8) and the second switching device (10) in the manner that the second delaying circuit (3) delays turn-on of the second switching device (10).
2. A switched-mode power converter (1) as in Claim 1, **characterized in that** the first switching device (9) has shorter turn-on and turn-off crossover intervals in comparison to the second switching device (10).
3. A switched-mode power converter (1) as in Claim 1 or 2, **characterized in that** a first turn-on circuit (4) provides that the first switching device (9) is biased to conduction and a first turn-off circuit (6) provides that the first switching device (9) is biased to non-conduction modes.
4. A switched-mode power converter (1) as in Claim 1 or 2, **characterized in that** a second turn-on circuit (5) provides that the second switching device (10) is biased to conduction and a second turn-off circuit (7) provides that the second switching device (10) is biased to non-conduction modes.
5. A switched-mode power converter (1) as in Claim 2, **characterized in that** the first switching device (9) with lower turn-on power loss starts conducting prior to the second switching device (10) and by the time the second switching device (10) is turned on, the first switching device (9) conducts a greater proportion of the current being shared.
6. A switched-mode power converter (1) as in Claim 2 or 5, **characterized in that** the first switching device (9) continues to conduct current while the second switching device (9) is being turned off.
7. A switched-mode power converter (1) as in Claim 6, **characterized in that** transitions between conduction and non-conduction modes of the switched-mode power converter (1) is substantially effectuated by the first

switching device (9).

Fig. 1

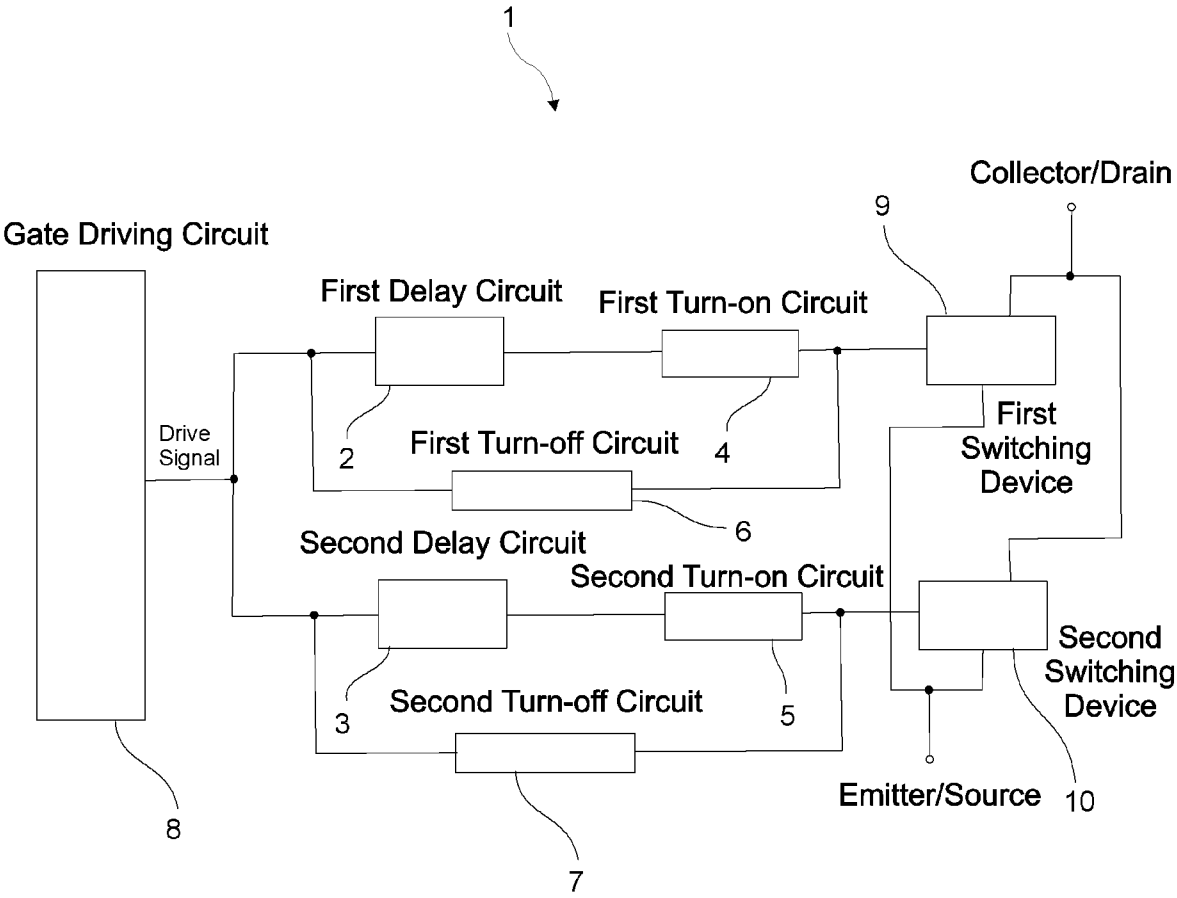
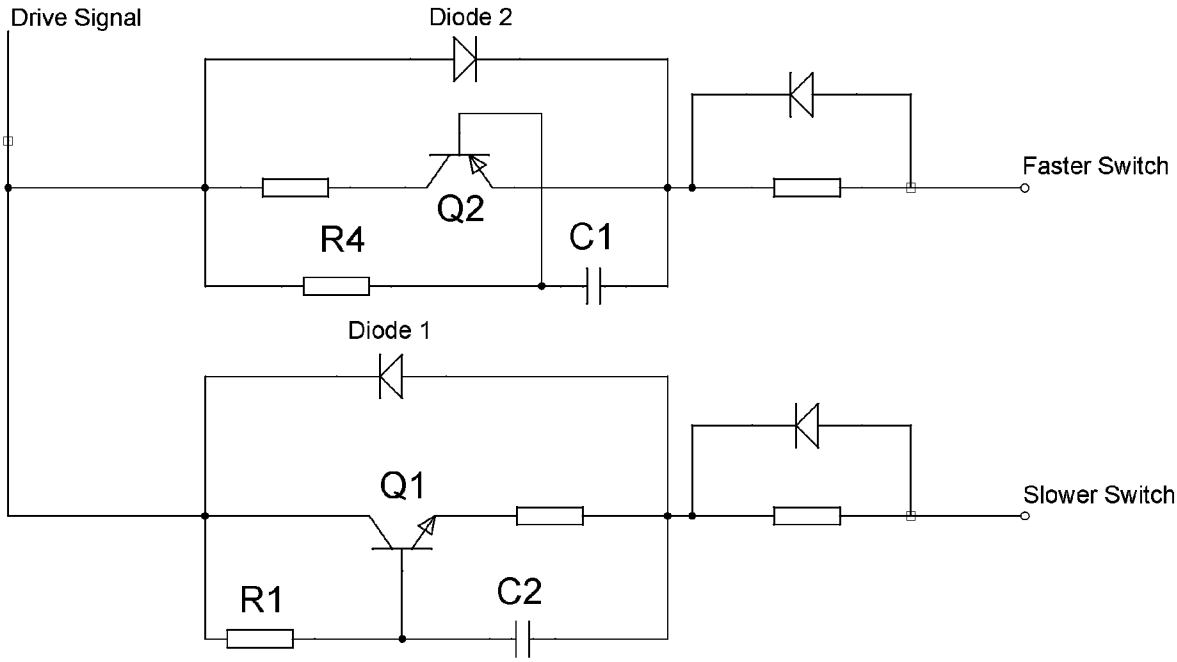

1
Collector/Drain
9
Gate Driving Circuit
First Delay Circuit
First Turn-on Circuit
Drive Signal
2
First Turn-off Circuit
4
First Switching Device
6
Second Delay Circuit
Second Turn-on Circuit
Second Switching Device
3
Second Turn-off Circuit
5
Emitter/Source
10
8
7

Fig. 2


Drive Signal
Diode 2
Faster Switch
Q2
R4
C1
Diode 1
Q1
Slower Switch
R1
C2

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/062481

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/088 H03K17/12
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 581 016 A1 (KOLLMORGEN CORP [US]) 2 February 1994 (1994-02-02) column 5 - lines 5-39; figures 1,3 column 2 - lines 30-36 claim 1	1-7
X	WO 2015/022860 A1 (NISSAN MOTOR [JP]) 19 February 2015 (2015-02-19) abstract figures 1,4,9,10	1-7
A	US 2008/265851 A1 (ZHANG JASON [US]) 30 October 2008 (2008-10-30) paragraphs [0017] - [0023]; figures 2,4,5	1-7
A	EP 2 117 121 A1 (SCHLEIFRING UND APPBAU GMBH [DE]) 11 November 2009 (2009-11-11) figures 2,7	1-7

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Marannino, M

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2015/062481

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