US 20180301418A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2018/0301418 A1**

Chang Chien et al. (43) **Pub. Date: Oct. 18, 2018**

(54) **PACKAGE STRUCTURE AND MANUFACTURING METHOD THEREOF**

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(21) Appl. No.: **15/717,923**

(22) Filed: **Sep. 27, 2017**

Related U.S. Application Data

(60) Provisional application No. 62/484,907, filed on Apr. 13, 2017.

Publication Classification

(51) **Int. Cl.**

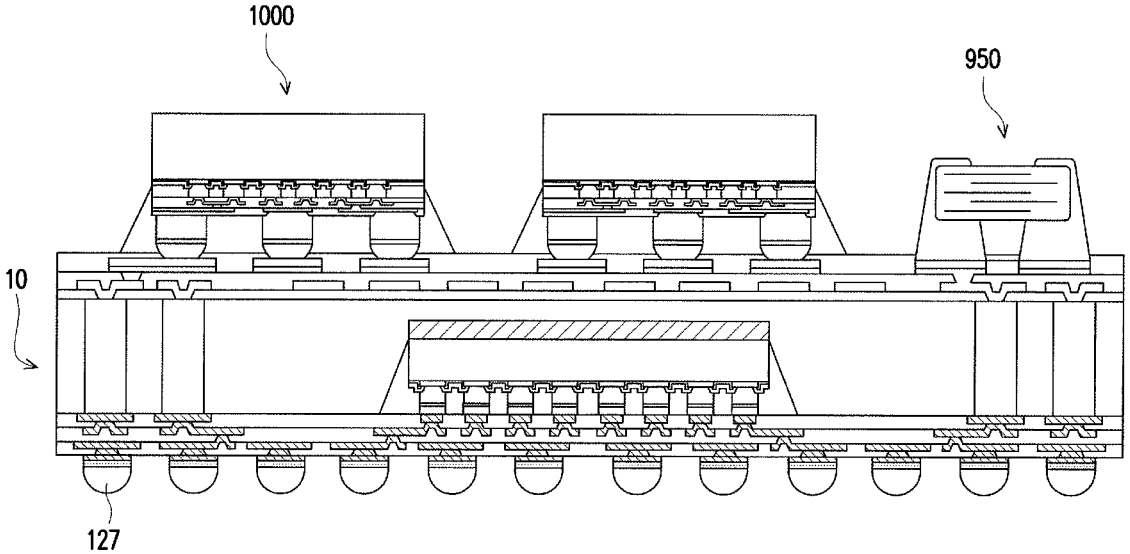
H01L 23/538	(2006.01)
H01L 23/31	(2006.01)
H01L 23/00	(2006.01)
H01L 21/48	(2006.01)
H01L 21/683	(2006.01)
H01L 21/56	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/5389*** (2013.01); *H01L 25/105* (2013.01); ***H01L 23/3128*** (2013.01); ***H01L 23/3135*** (2013.01); ***H01L 23/5383*** (2013.01); ***H01L 24/16*** (2013.01); ***H01L 23/5384*** (2013.01); ***H01L 24/32*** (2013.01); ***H01L 21/4857*** (2013.01); ***H01L 21/6835*** (2013.01); ***H01L 21/568*** (2013.01); ***H01L 21/486*** (2013.01); ***H01L 24/81*** (2013.01); ***H01L 24/73*** (2013.01); *H01L 2221/68345* (2013.01); *H01L 2221/68359* (2013.01); *H01L 2224/16227* (2013.01); *H01L 2224/32225* (2013.01); *H01L 2224/73204* (2013.01); ***H01L 23/5386*** (2013.01)

(57) **ABSTRACT**

A package structure includes a first redistribution structure, a chip, an insulation encapsulation and a protection layer. The first redistribution structure has a first surface and a second surface opposite to the first surface. The chip is disposed on the first surface of the first redistribution structure and has an active surface and a rear surface opposite to the active surface. The insulation encapsulation encapsulates the chip and the first surface of the first redistribution structure. The protection layer is directly disposed on the rear surface of the chip.



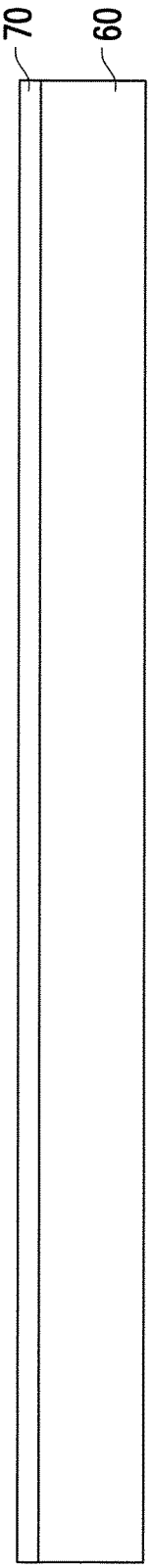

70
60

FIG. 1A

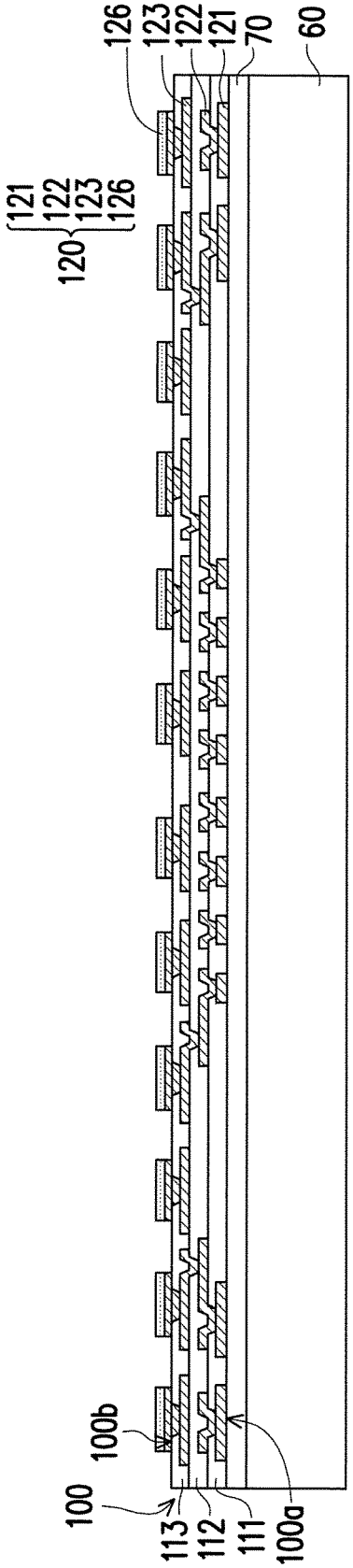

126
123
122
121
70
60
121
122
123
126
120
100b
100
113
112
111
100a

FIG. 1B

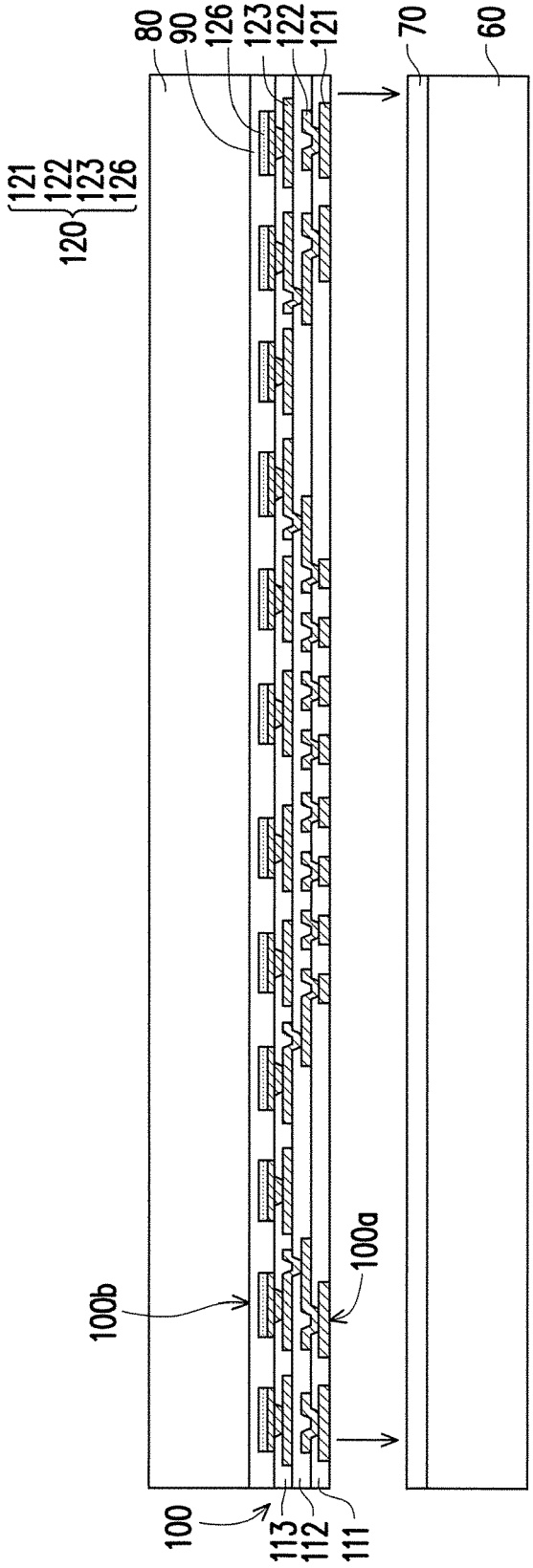

80
90
126
123
122
121
70
60
121
122
123
126
120
100b
100a
100
113
112
111

FIG. 1C

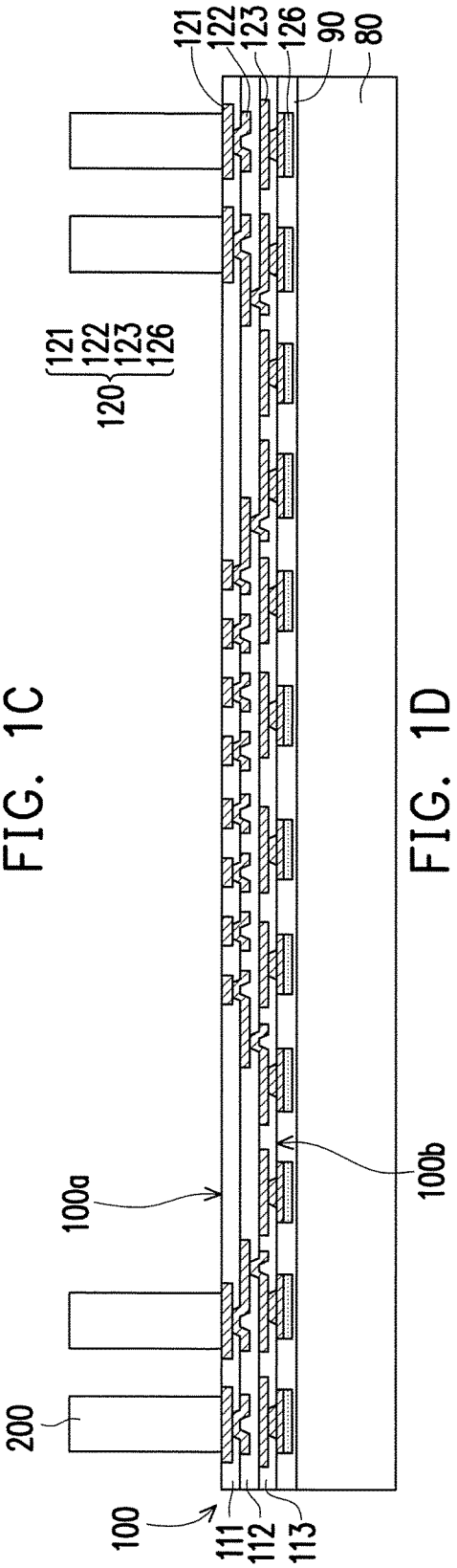

121
122
123
126
90
80
121
122
123
126
120
100a
100b
200
100
111
112
113

FIG. 1D

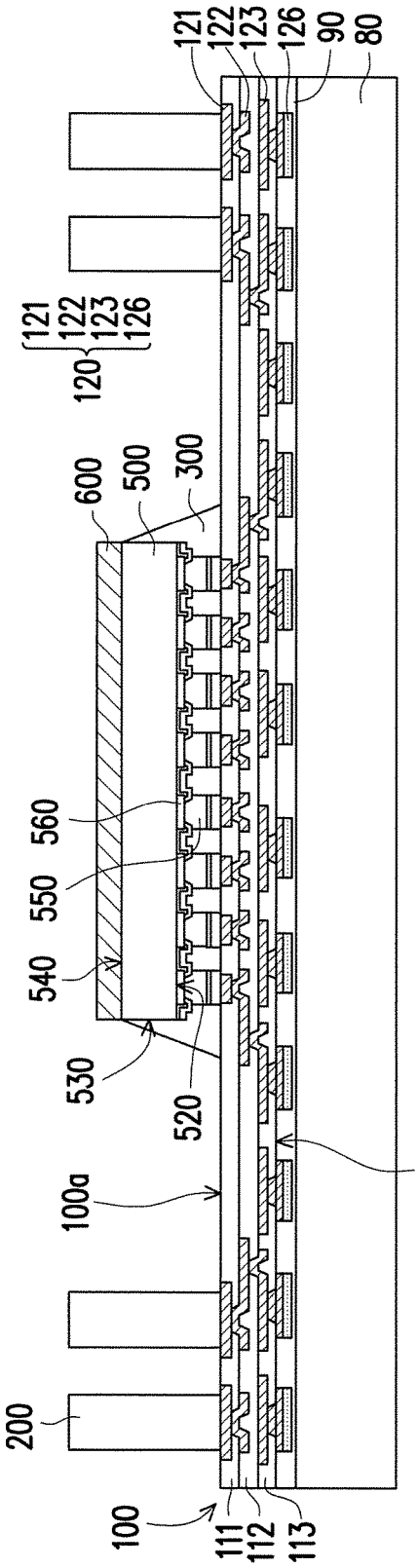

121
122
123
126
90
80
120
600
500
300
560
550
540
530
520
100a
100b
200
100
111
112
113

FIG. 1E

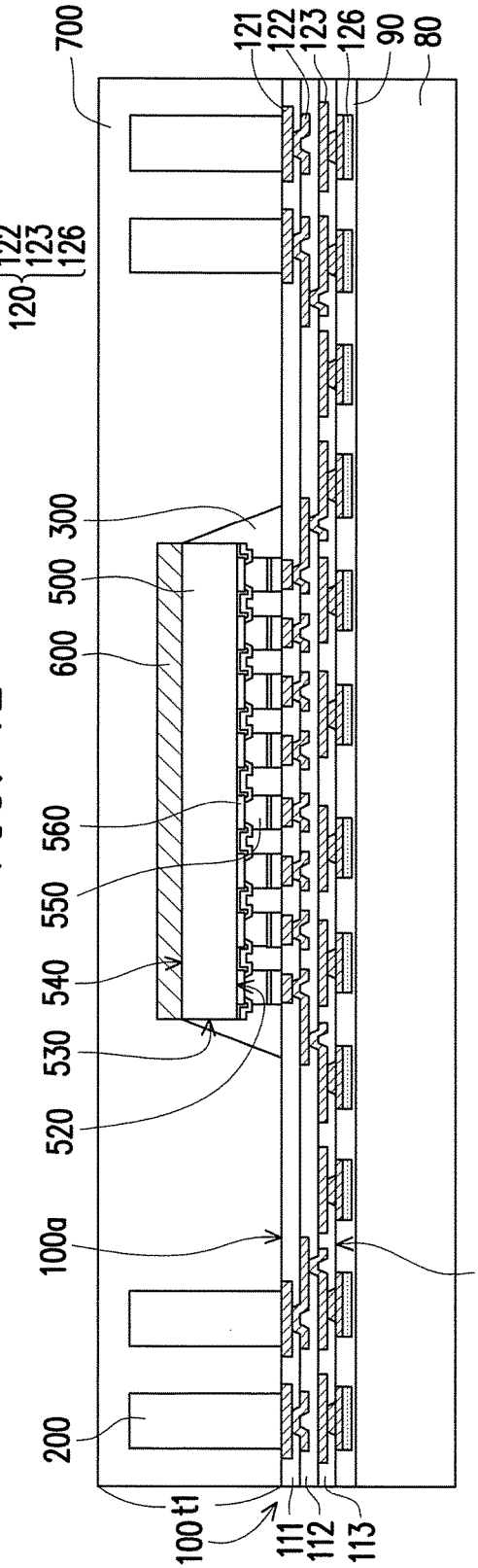

700
121
122
123
126
90
80
120
300
500
600
560
550
540
530
520
100a
100b
200
100t1
111
112
113

FIG. 1F

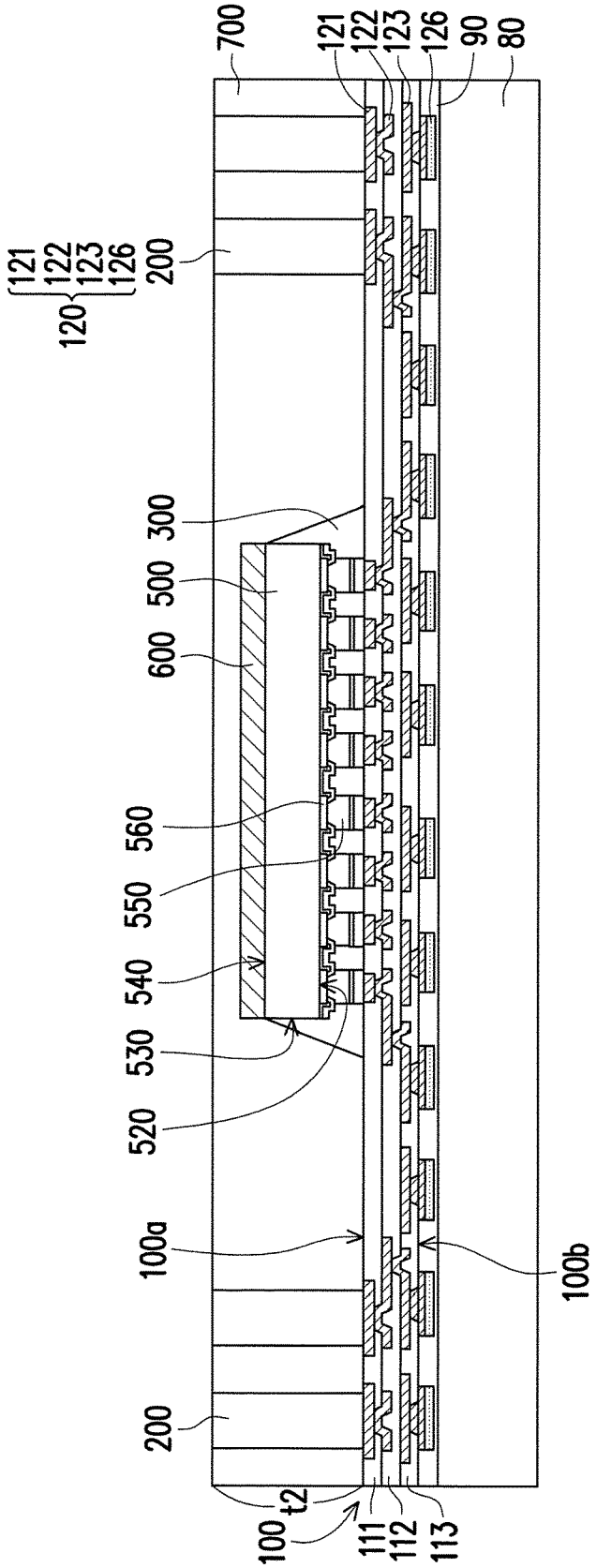

700
121
122
123
126
90
80
121
122
123
126
120
200
300
500
600
560
550
540
530
520
100a
100b
200
100
t2
111
112
113

FIG. 1G

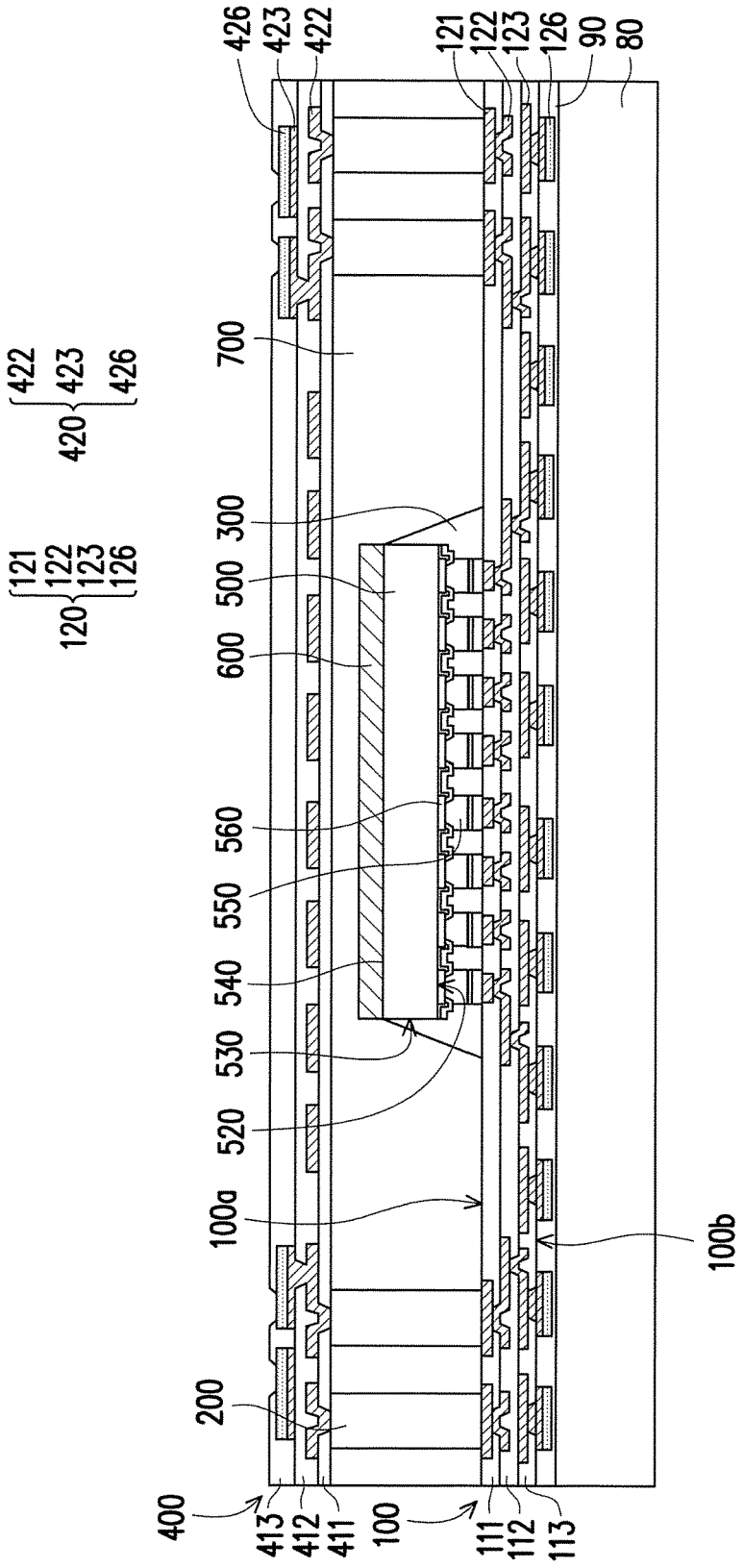

426
423
422
121
122
123
126
90
80
700
422
423
426
420
300
121
122
123
126
120
500
600
560
550
540
530
520
100a
100b
200
400
413
412
411
100
111
112
113

FIG. 1H

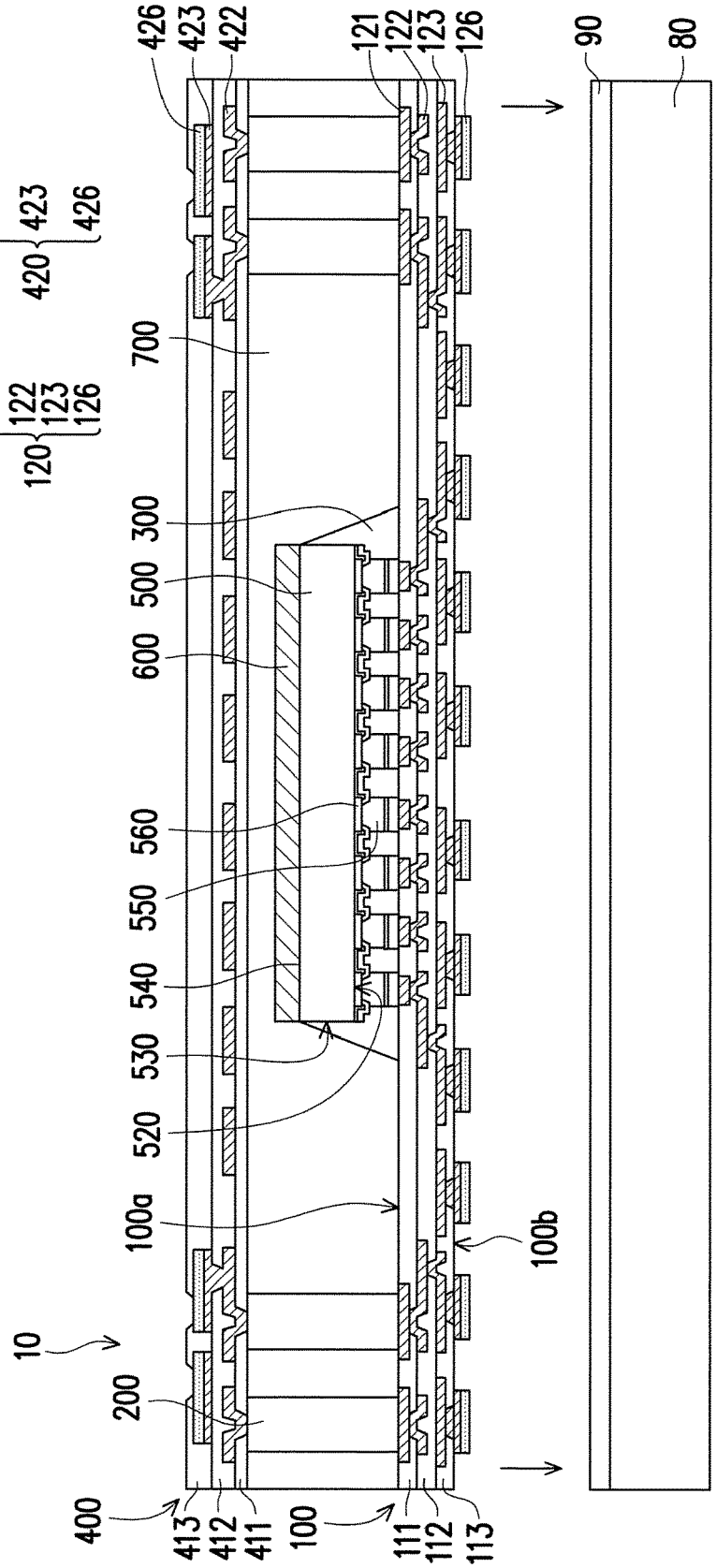

426
423
422
121
122
123
126
90
80
422
423
426
420
700
121
122
123
126
120
300
500
600
560
550
540
530
520
100a
100b
10
200
400
413
412
411
100
111
112
113

FIG. 1I

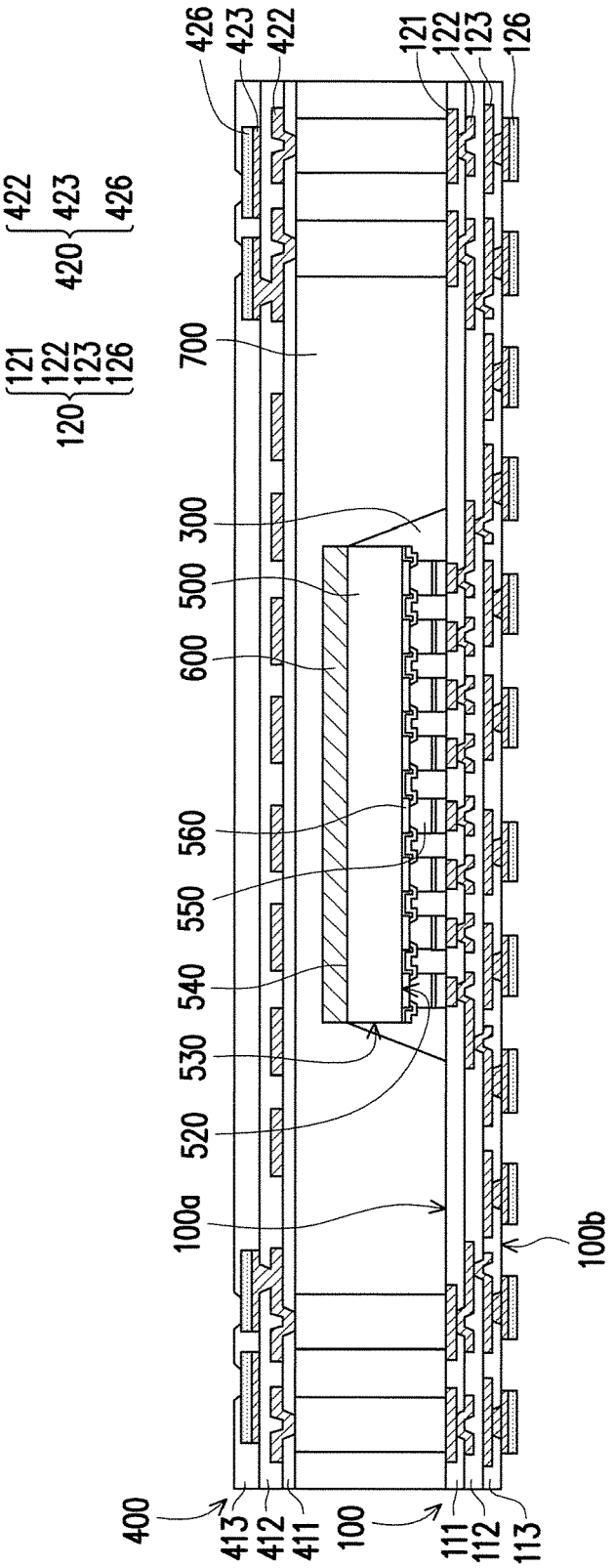

426
423
422
121
122
123
126
422
423
426
420
121
122
123
126
120
700
300
500
600
560
550
540
530
520
100a
100b
400
413
412
411
100
111
112
113

FIG. 1J

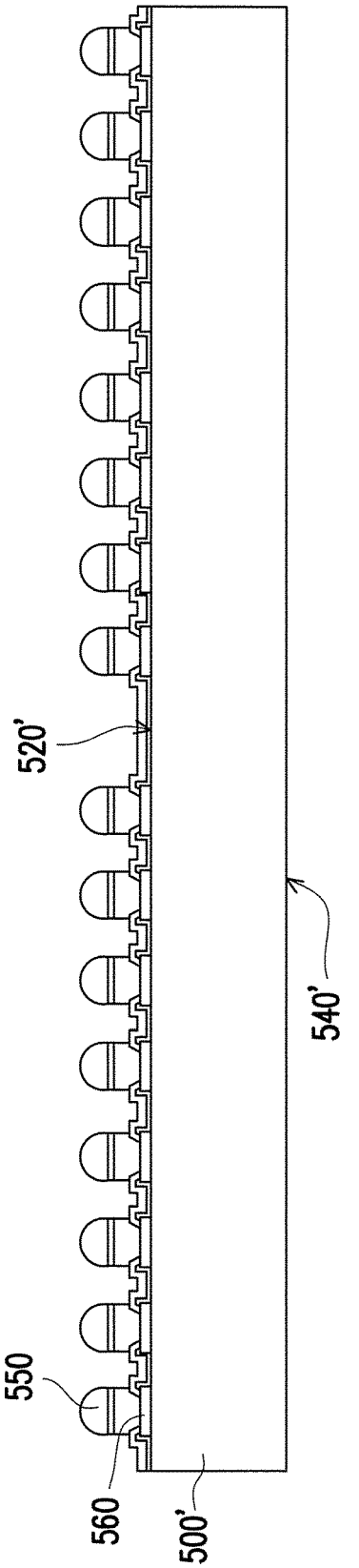


FIG. 2A

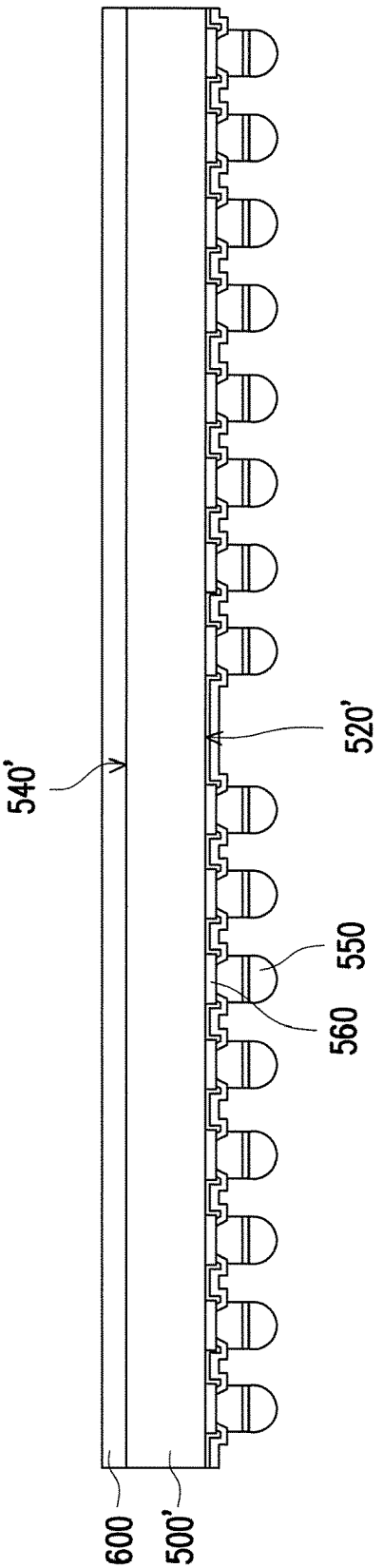


FIG. 2B

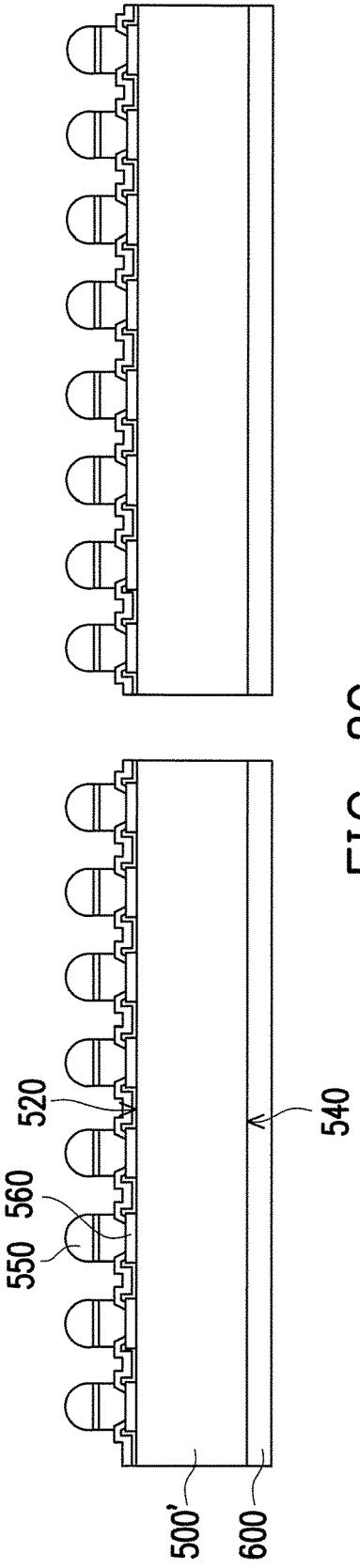


FIG. 2C

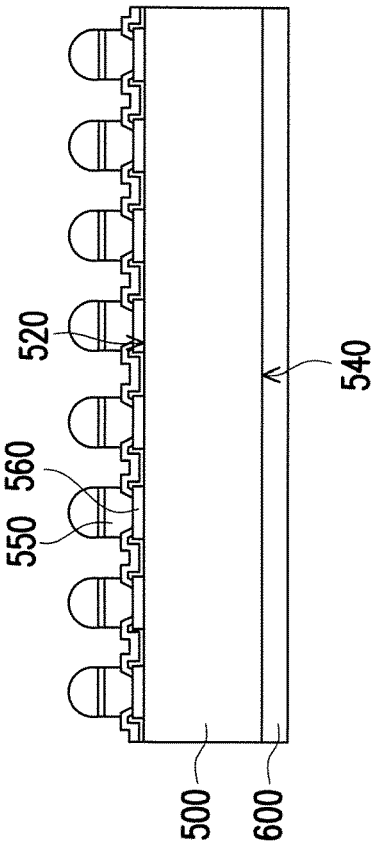


FIG. 2D

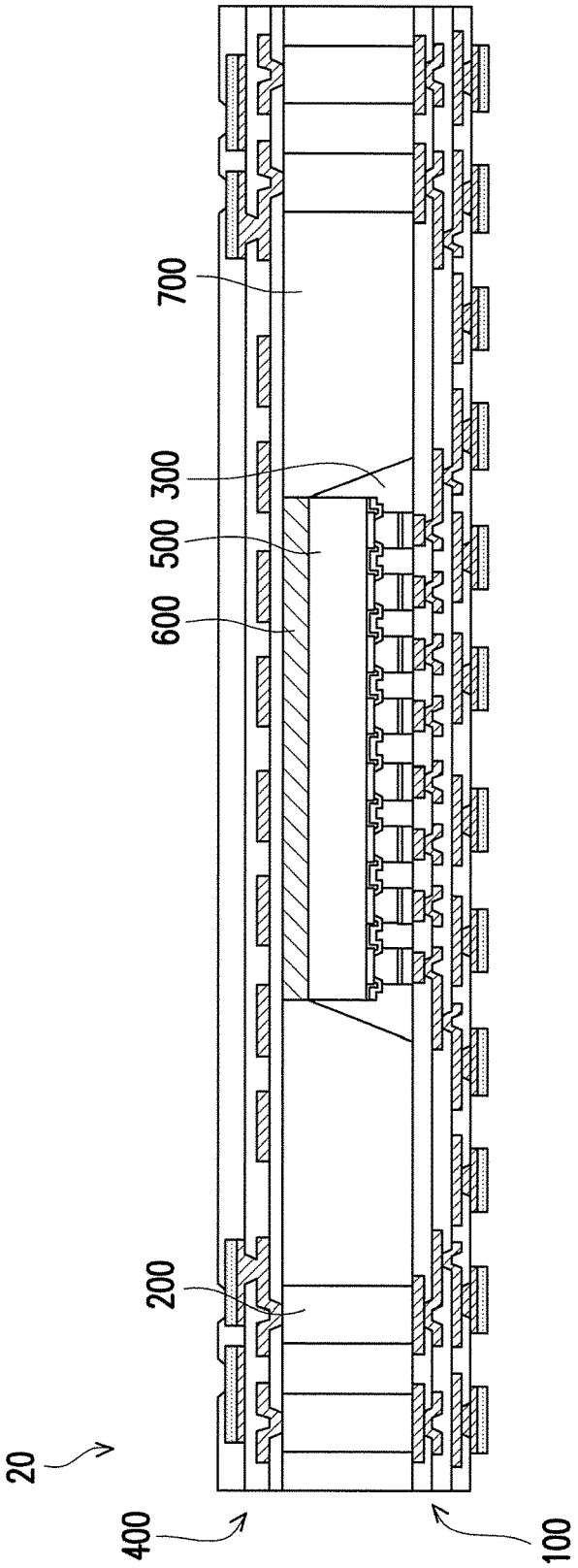


FIG. 3

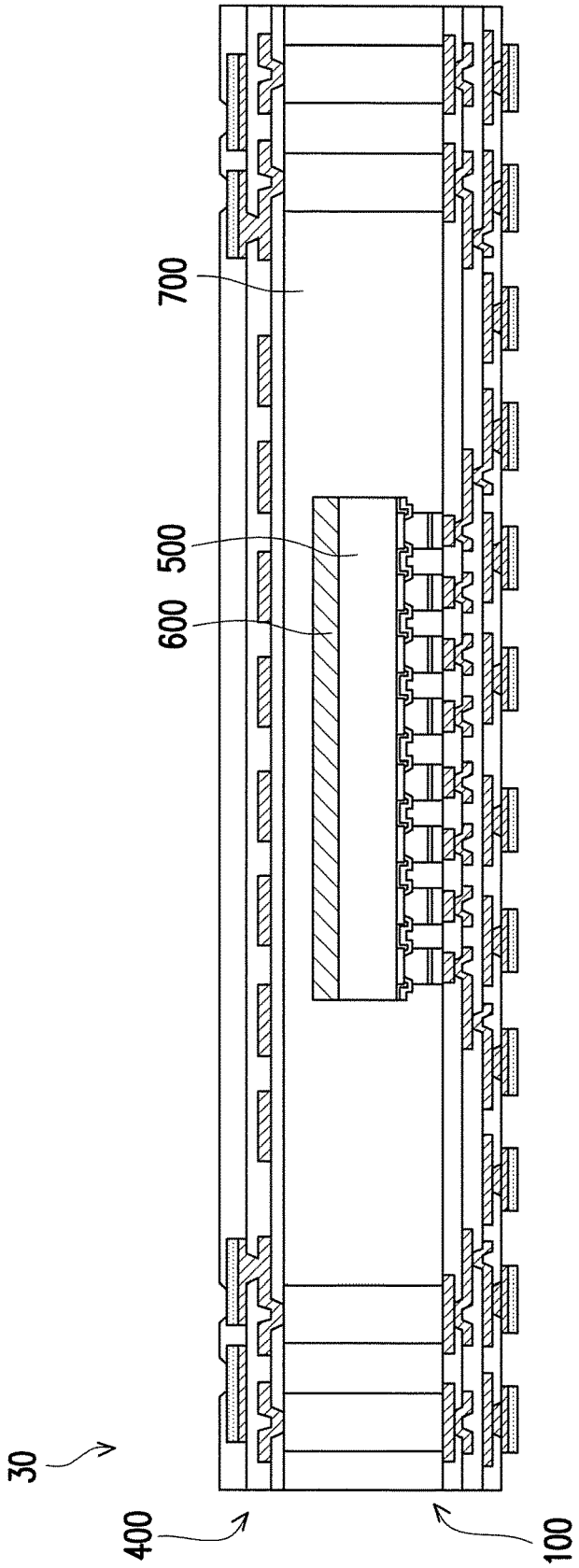


FIG. 4

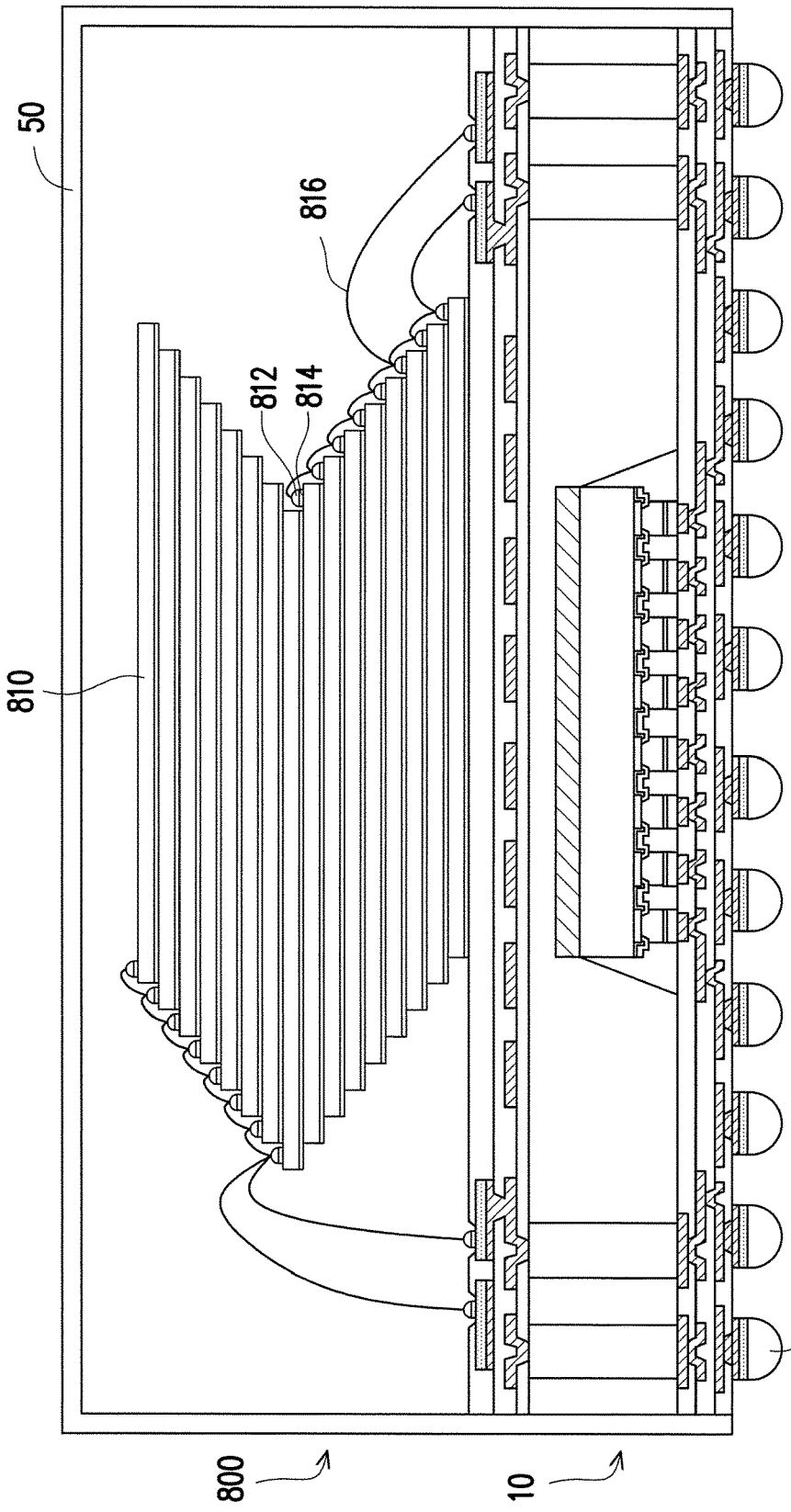


FIG. 5A

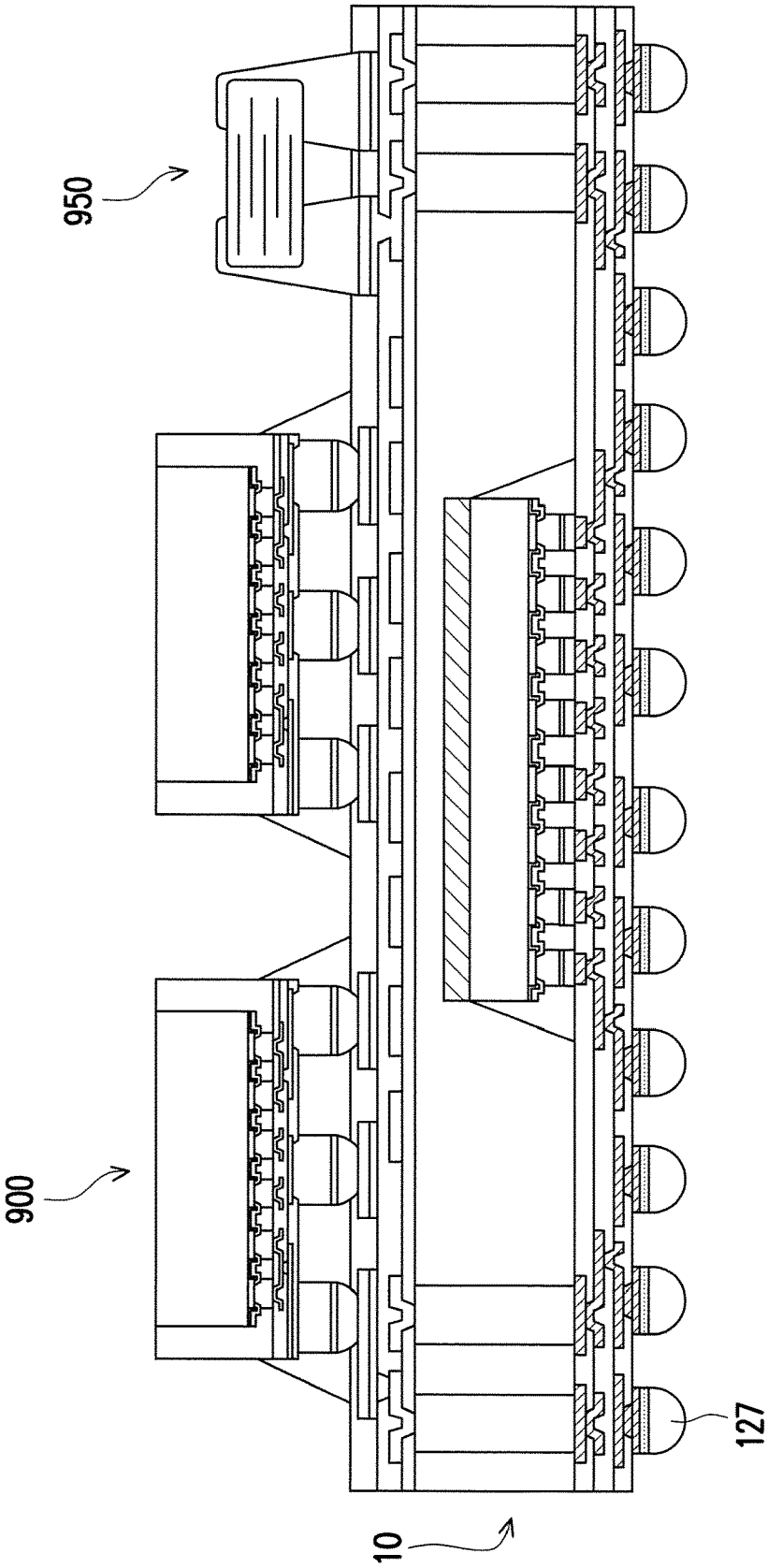


FIG. 5B

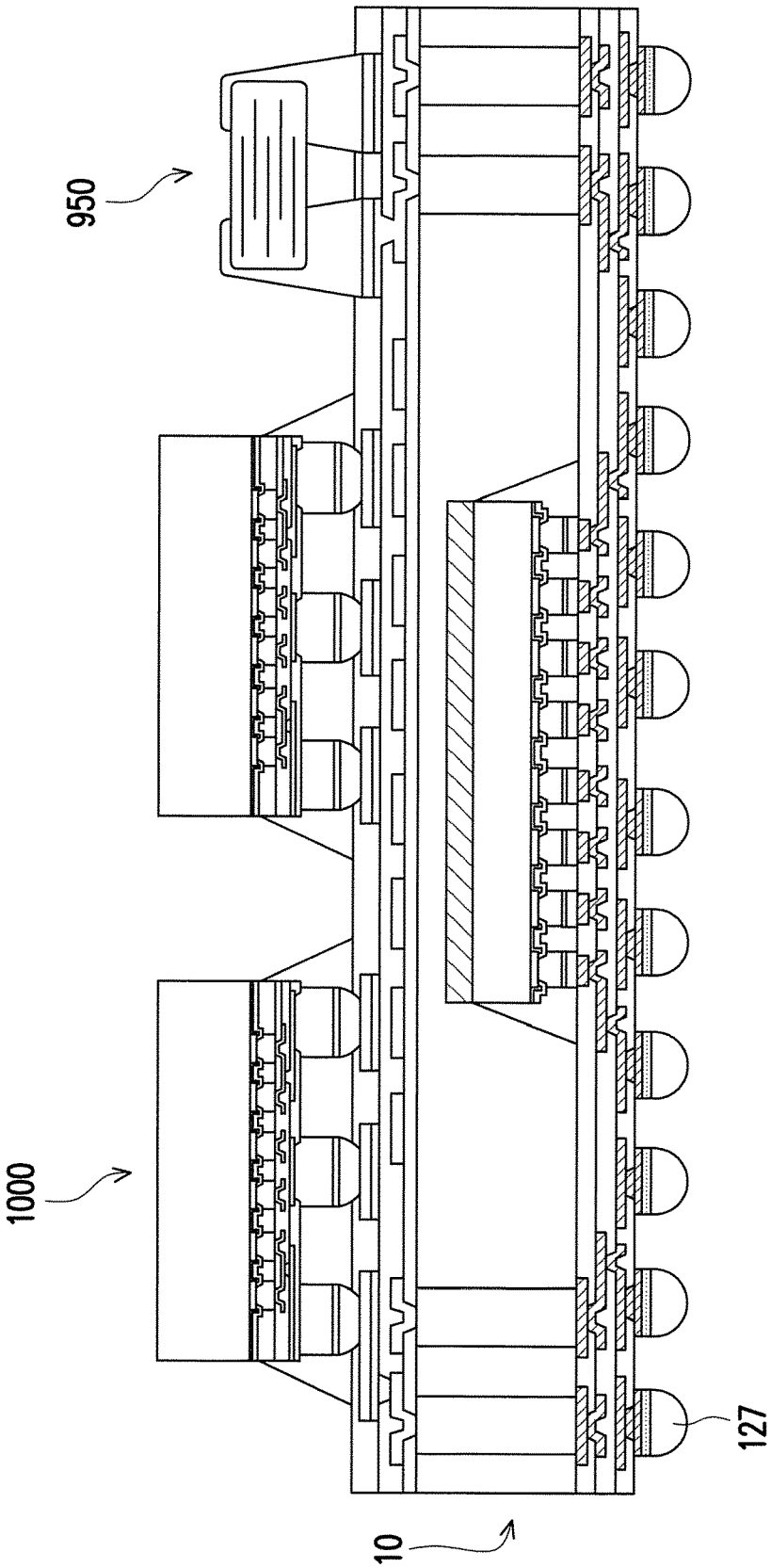


FIG. 5C

PACKAGE STRUCTURE AND MANUFACTURING METHOD THEREOF

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the priority benefit of U.S. provisional application Ser. No. 62/484,907, filed on Apr. 13, 2017. The entirety of the above-mentioned patent application is hereby incorporated by reference herein and made a part of specification.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention generally relates to a package structure and a display, in particular, to a package structure having a protection layer.

2. Description of Related Art

[0003] With advancement of the technology, the electronic product has been designed to achieve being light, slim, short, and small, so as to develop products that are smaller in volume, lighter in weight, higher in integration, and more competitive in the market. As the products gradually shrinkage in volume, the risk of malfunction or failure of the electronic chip due to crack or warpage is increased accordingly. As such, how to miniature the package structure while maintaining the reliability and the functionality of the package, so as to lower the risk of failure of the final products, has become a challenge to those researchers in the field.

SUMMARY OF THE INVENTION

[0004] Accordingly, the present invention is directed to a package structure and a manufacturing method thereof, which can lower the risk of malfunction or failure of a package structure of the chip and enhance the reliability thereof.

[0005] The present invention provides a package structure including a first redistribution structure, a chip, an insulation encapsulation, a protection layer. The first redistribution structure has a first surface and a second surface opposite to the first surface. The chip is disposed on the first surface of the first redistribution structure and has an active surface and a rear surface opposite to the active surface. The insulation encapsulation encapsulates the chip and the first surface of the first redistribution structure. The protection layer is directly disposed on the rear surface of the chip.

[0006] The present invention provides a manufacturing method of a package structure. The method includes at least the following steps. A first carrier substrate is provided. A first redistribution structure having a first surface and a second surface opposite to the first surface is formed on the first carrier substrate. The first surface is attached to the first carrier substrate. A second carrier substrate attached to the second surface of the first redistribution structure is provided. The first redistribution structure is separated from the first carrier substrate. A chip is disposed onto the first surface of the first redistribution structure. The chip has an active surface and a rear surface opposite to the active surface. A protection layer is formed on the rear surface, and the active surface is adhered to the first surface of the first redistribution structure.

[0007] Base on the above, the protection layer is formed on the rear surface of the chip. Accordingly, the chip is strengthened to sufficiently alleviate the warpage issues during the manufacturing process of the package structure. Moreover, since the issues of the warpage of the chip are alleviated, the flip-chip bonding yield may be improved to avoid the non-joint issue. As result, the overall strength of the chip having the protection layer disposed thereon is enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0009] FIG. **1**A to FIG. **1**J are schematic cross-sectional view illustrating a manufacturing method of package structure according to an embodiment of the present invention.

[0010] FIG. **2**A to FIG. **2**D are schematic cross-sectional view illustrating a manufacturing method of the chip and the protection layer of the package structure according to an embodiment of the present invention.

[0011] FIG. **3** is a cross-sectional view illustrating a package structure according to another embodiment of the present invention.

[0012] FIG. **4** is a cross-sectional view illustrating a package structure according to another embodiment of the present invention.

[0013] FIG. **5**A to FIG. **5**C are a schematic views illustrating some exemplary embodiments of the semiconductor packages wherein the package structure of FIG. **1**J is applied.

DESCRIPTION OF THE EMBODIMENTS

[0014] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0015] FIG. **1**A to FIG. **1**J are schematic cross-sectional view illustrating a manufacturing method of package structure according to an embodiment of the present invention. Referring to FIG. **1**A, a first carrier substrate **60** is provided. In the embodiment, the first carrier substrate **60** may be made of silicon, polymer or other suitable materials. A first release layer **70** is formed on the first carrier substrate **60** to enhance the adhesion between the first carrier substrate **60** and the other structures subsequently formed thereon, and to improve the rigidity of the overall package structure during the manufacturing process. The first release layer **70** is, for example, a light to heat conversion (LTHC) adhesive layer or other suitable adhesive layers.

[0016] Referring to FIG. **1**B, a first redistribution structure **100** is formed on the first carrier substrate **60** and the first release layer **70**. In the embodiment, the first redistribution structure **100** has a first surface **100***a* and a second surface **100***b* opposite to the first surface **100***a*. The first redistribution structure **100** may include a plurality of dielectric layers and a plurality of conductive elements disposed therein. As illustrated in FIG. **1**B, the first conductive elements **120** includes three trace layers **121**, **122**, **123**, respectively dis-

posed in the three dielectric layers **111**, **112**, **113**. The first conductive elements **120** include a plurality of interconnect structures connecting the trace layers **121**, **122**, **123**. A plurality of ball pads **126** formed on the second surface **100***b* are included in the first conductive elements **120** and electrically connected to the trace layers **121**, **122**, **123** through the interconnect structures. For example, the trace layer **121** may be first formed on the first carrier substrate **60**. Next, the dielectric layer **111** including a plurality of openings may be formed over the first carrier substrate **60** to cover the trace layer **121** and the openings of the dielectric layer **111** may expose at least a portion of the trace layer **121**. Subsequently, the trace layer **122** may be formed in the openings and on the dielectric layer **111** and the trace layer **122** is electrically connected to the trace layer **121**. The abovementioned steps may be performed multiple times to sequentially form the dielectric layer **112**, the trace layer **123**, the dielectric layer **113** and the ball pads **126**.

[0017] As shown in FIG. **1**B, the dielectric layer **113** exposes the trace layer **123** and the interconnect structures disposed thereon, such that the trace layer **123** may electrically connect to other trace layers or package structures through the interconnect structures. The patterned circuits may be formed from the trace layer **122** with a fine-pitch pattern located in the dielectric layer **112** to the trace layer **121** with a large pattern located on the first surface **100***a* for obtaining a better fine line-and-space (L/S) RDL (redistribution layer) yield. In addition, the ball pads **126** may be made of copper, nickel, tin, gold, silver or a combination thereof.

[0018] Referring to FIG. **1**C, a second carrier substrate **80** is attached to the second surface **100***b* of the first redistribution structure **100**. Moreover, a second release layer **90** is formed between the second carrier substrate **80** and the first redistribution structure **100**. The ball pads **126** may be embedded within the second release layer **90**. The first carrier substrate **60** is detached and separated from the first surface **100***a* of the first redistribution structure **100** through the first release layer **70** following a direction pointed by the direction arrows in FIG. **1**C.

[0019] Referring to FIG. **1**D, after the first redistribution structure **100** is separated from the first carrier substrate **60**, the first surface **100***a* of the first redistribution structure **100** may have desired surface coplanarity for the subsequent flip-chip bonding processes. In the present embodiment, the surface of the trace layer **121** exposed on the first surface **100***a* may be lower than that of the dielectric layer **111**. A height level difference between the surface of the dielectric layer **111** and the surface of the trace layer **121** may be smaller than 3 μm. Moreover, a plurality of conductive pillars **200** is formed on the first surface **100***a* of the first redistribution structure **100** and electrically connected to the trace layer **121**. In the present embodiment, the conductive pillars **200** may be made of copper, nickel, tin, gold, silver or a combination thereof.

[0020] Referring to FIG. **1**E, a chip **500** is disposed on the first surface **100***a* of the first redistribution structure **100** through a flip-chip bonding process. However, it construes no limitation in the invention. The number of the chip **500** is not limited and may depend on circuit design. As illustrated in FIG. **1**E, the conductive pillars **200** may surround the chip **500**. The chip **500** has an active surface **520** and a rear surface **540** opposite to the active surface **520**. A protection layer **600** may be directly formed on the rear surface **540** before the chip **500** is disposed on the first surface **100***a*. The protection layer **600** can prevent the chip **500** from cracking during the flip-chip bonding process. In addition, with the aid of the protection layer **600**, especially for a large-sized chip, the issue of chip warpage may be eliminated and the flip-chip bonding yield may be improved to avoid the non joint issue, thereby enhancing the overall strength of the subsequently formed package structure **10** (as shown in FIG. **1**J). A Capillary Underfill (CUF) **300** is formed between the active surface **520** of the chip **500** and the first surface **100***a* of the first redistribution structure **100** and surrounds a lateral side **530** of the chip **500**. The protection layer **600** on the rear surface **540** of the chip **500** may prevent the CUF **300** from overflowing to the rear surface **540**. The CUF **300** may be formed using insulating materials, such as epoxy or other suitable resins. Furthermore, a plurality of bumps **550** and pads **560** are formed between the active surface **520** and the first surface **100***a* of the first redistribution structure **100** as the interconnection structures for electrically connecting the chip **500** to the conductive elements **120** of the first redistribution structure **100**.

[0021] Referring to FIG. **1**F, the chip **500**, the protection layer **600**, and the conductive pillars **200** are encapsulated by an insulation encapsulation **700**. As shown in FIG. **1**F, the insulation encapsulation **700** is formed over the chip **500**, the protection layer **600**, and the conductive pillars **200**, such that the insulation encapsulation **700** completely covers all conductive pillars **200**, the chip **500**, and the protection layer **600**. The insulation encapsulation **700** may include molding compounds disposed on the first redistribution structure **100** using a molding process. As illustrated in FIG. **1**F, the insulation encapsulation **700** may have a thickness t**1**, which is larger than the height of the conductive pillars **200**.

[0022] Referring to FIG. **1**G, the thickness of the insulation encapsulation **700** is thinned from thickness t**1** to thickness t**2** to expose top surfaces of the conductive pillars **200** for subsequent processes of forming, for example, another redistribution structure thereon. The insulation encapsulation **700** may still be covering the protection layer **600** after the thinning process. After the thinning process, a surface roughness of the insulation encapsulation **700** and the conductive pillars **200** may be enhanced, thereby increasing an adhesive property with layers subsequently formed thereon. The thinning process may be performed using mechanical grinding, Chemical-Mechanical Polishing (CMP), etching, or other suitable methods. The etching process for the conductive pillars **200** may include anisotropic etching or isotropic etching.

[0023] Referring to FIG. **1**H, a second redistribution structure **400** is formed above the insulation encapsulation **700**. The second redistribution structure **400** may include at least a dielectric layer and at least a conductive element. As shown in FIG. **1**H, the second redistribution structure **400** includes the second conductive elements **420**. The second conductive elements may include trace layers **422**, **423**, respectively disposed in the dielectric layers **412**, **413**. In addition, the trace layers **422**, **423** are electrically connected to the conductive pillars **200**.

[0024] Referring to **1**I and **1**J, the second carrier substrate **80** is detached from the second surface **100***b* of the first redistribution structure **100** through the release layer **90** to form a package structure **10** as shown in FIG. **1**J.

[0025] FIG. **2**A to FIG. **2**D are schematic cross-sectional view illustrating a manufacturing method of the chip and the protection layer according to an embodiment of the present invention. Referring to FIG. **2**A, a wafer **500'** has an active surface **520'** and a rear surface **540'** opposite to the active surface **520'** is provided. The active surface **520'** have a plurality of the bumps **550** and pads **560** formed thereon. Referring to FIG. **2**B, the protection layer **600** is formed on the rear surface **540'**. Referring to FIG. **2**C, a singulation process is performed on the wafer **500'** to form a plurality of chips **500** as illustrated in FIG. **2**C and FIG. **2**D. The singulation process includes, for example, cutting with rotating blade or laser beam.

[0026] In the embodiment, a coefficient of thermal expansion (CTE) of the protection layer **600** is smaller than polyimide but larger than molding compound and silicon materials. For example, the CTE of the protection layer **600** ranges between 5 ppm/° C. and 40 ppm/° C. Accordingly, the protection layer **600** can reduce the risk of chip cracking or chipping during the sawing process of the wafer **500'**. In addition, the protection layer **600** can be used as a buffer layer to reduce the chip **500** warpage and enhance the flip-chip bonding process yield to avoid non-joint risk, especially for a large-sized chip. Specifically, as the issues of the warpage of the chip **500** is alleviated, the chip **500** may be bonded to the trace layer **121** of the first redistribution structure **100** with fine-pitch line and space patterns by the aid of the alignment processes.

[0027] FIG. **3** is a cross-sectional view illustrating a package structure according to another embodiment of the present invention. The structure of the package structure **20** is similar to the package structure **10** in FIG. **1**J. Thus, the identical components will be denoted with the same numerals and not repeated herein. The difference between the package structure **20** and the package structure **10** is that the insulation encapsulation **700** may be further thinned to remove the insulation encapsulation **700** disposed above the protection layer **600** to expose the protection layer **600**. Accordingly, the top surface of the protection layer **600** may be coplanar with the top surface of the insulation encapsulation **700** and the top surfaces of the conductive pillars. Therefore, the second redistribution structure **400** can be directly in contact with the protection layer **600**. In this embodiment, the protection layer **600** may serve as a buffer layer to avoid delamination between the second redistribution structure **400** and the chip **500** during the manufacturing process of the package structure **20**.

[0028] In the present embodiment, the protection layer **600** may be made of materials similar to the insulation encapsulation **700**, such as molding compound. Therefore, the protection layer **600** and the insulation encapsulation **700** may have similar properties. As such, the life time of the mold grinding wheel applying in the thinning/grinding process of the insulation encapsulation **700** and the protection layer **600** may be elongated. Furthermore, the protection layer **600** may have good thermal conductivity, which ranges between 2 W/m-k and 5 W/m-k, to enhance the thermal dissipation performance of the package structure **20**.

[0029] FIG. **4** is a cross-sectional view illustrating a package structure according to another embodiment of the present invention. The structure of the package structure **30** is similar to the package structure **10** in FIG. **1**J. Thus, the identical components will be denoted with the same numerals and not repeated herein. The difference between the package structure **30** and the package structure **10** is that a Molded Underfill (MUF) can be applied to replace the CUF **300**. For example, the insulation encapsulation **700** may be a molding compound, sometimes called the MUF. The MUF may encapsulate the chip **500** and fill the gap between the chip **500** and the first redistribution structure **100**, thereby improving the reliability of the package structure **30**. Different underfills may be utilized according to the practical needs of the different package structures.

[0030] FIG. **5**A to FIG. **5**C are schematic views illustrating some exemplary embodiments of the semiconductor packages wherein the package structure **10** of FIG. **1**J is applied. Referring to FIG. **5**A, a stacking structure **800** may be formed above the package structure **10**. A plurality of bumps **127** may be disposed on the bottom surface of the package structure **10** for bonding the package structure **10** on a circuit substrate or an interposer. In the embodiment, a plurality of the pads **814** may be formed on the surface of each chip **810** of the stacking chip structure **800**. The pads **814** on the surfaces of the different chips **810** may be mutually bonded and electrically connected through a plurality of bumps **812** and wires **816**. Each chip **810** of the stacking chip structure **800** may be also electrically connected and bonded to the package structure **10** and the chip **500** through the bumps **812** and the wires **816**. As illustrated in FIG. **5**A, an electromagnetic interference (EMI) shielding structure **50** may be disposed to surround and protect the package structure **10** and the stacking chip structure **800**.

[0031] Referring to FIG. **5**B, a plurality of fan-out structures **900** and a plurality of passive components **950**, such as capacitors, inductors or antennas, may also be disposed above the package structure **10**.

[0032] Referring to FIG. **5**C, a plurality of wafer level chip scale package (WLCSP) structures **1000** and the passive components **950** may be disposed above the package structure **10**. Accordingly, as illustrated in FIG. **5**A, FIG. **5**B and FIG. **5**C, the configurations of the package structure **10** can be adjusted based on the practical needs of different functions or different kinds of applications.

[0033] In light of the foregoing, the package structure may include the first redistribution structure, the second redistribution structure and the chip. The second redistribution structure is disposed above the first redistribution structure. The chip is disposed and encapsulated between the first redistribution structure and the second redistribution structure and has an active surface and a rear surface opposite to each other. In addition, the package structure includes a package layer disposed on the rear surface of the chip.

[0034] In the manufacturing process of the package structure, the protection layer can prevent the chip from cracking or chipping during the wafer sawing process. In addition, as the chip is flip-chip bonded to the first redistribution structure, the protection layer can alleviate the issues of chip cracking and chip warpage, and the flip-chip bonding yield may be improved to avoid the non-joint issue, thereby enhancing the overall strength of the package structure.

[0035] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A package structure comprising:

a first redistribution structure having a first surface and a second surface opposite to the first surface;

a chip, disposed on the first surface of the first redistribution structure and having an active surface and a rear surface opposite to the active surface;

an insulation encapsulation, encapsulating the chip and the first surface of the first redistribution structure; and

a protection layer, directly disposed on the rear surface of the chip.

2. The package structure according to claim **1**, wherein the first redistribution structure comprises at least one dielectric layer and a plurality of first conductive elements disposed in the at least one dielectric layer, and the chip is electrically connected to the first conductive elements exposed on the first surface.

3. The package structure according to claim **2**, further comprising a plurality of bumps, disposed between the active surface and the first surface of the first redistribution structure and electrically connected to the first conductive elements respectively.

4. The package structure according to claim **3**, wherein the surfaces of the bumps facing the first surface are substantially coplanar with a surface of the insulation encapsulation.

5. The package structure according to claim **1**, further comprising a second redistribution structure, disposed above the rear surface of the chip, the protection layer, and the insulation encapsulation.

6. The package structure according to claim **5**, further comprising a plurality of conductive pillars, surrounding the chip and disposed between the first redistribution structure and the second redistribution structure.

7. The package structure according to claim **6**, wherein the second redistribution structure comprises at least one dielectric layer and a plurality of second conductive elements disposed in the at least one dielectric layer, and the chip is electrically connected to the second conductive elements through the first redistribution structure and the conductive pillars.

8. The package structure according to claim **1**, further comprising an underfill, disposed between the first surface of the first redistribution structure and the active surface of the chip.

9. The package structure according to claim **1**, wherein a thickness of the protection layer ranges between 5 μm and 30 μm.

10. The package structure according to claim **1**, wherein the chip is electrically connected to the first redistribution structure through a flip-chip bonding process.

11. A manufacturing method of a package structure, comprising:

providing a first carrier substrate;

forming a first redistribution structure having a first surface and a second surface opposite to the first surface on the first carrier substrate, wherein the first surface is attached to the first carrier substrate;

providing a second carrier substrate attached to the second surface of the first redistribution structure;

separating the first redistribution structure from the first carrier substrate; and

disposing a chip on the first surface of the first redistribution structure, wherein the chip has an active surface and a rear surface opposite to the active surface, a protection layer is directly formed on the rear surface, and the active surface of the chip is adhered to the first surface of the first redistribution structure.

12. The method according to claim **11**, further comprising forming a first release layer between the first carrier substrate and the first redistribution structure.

13. The method according to claim **11**, further comprising forming a second release layer between the second carrier substrate and the second surface of the first redistribution structure for separating the second carrier substrate from the first redistribution structure.

14. The method according to claim **11**, wherein the step of forming the first redistribution structure further comprises forming at least one dielectric layer and a plurality of first conductive elements, and the chip is electrically connected to the first conductive elements.

15. The method according to claim **14**, further comprising forming a plurality of conductive pillars on the first surface of the first redistribution structure, wherein the conductive pillars surround the chip.

16. The method according to claim **15**, further comprising encapsulating the chip, the protection layer, and the conductive pillars by utilizing an insulation encapsulation.

17. The method according to claim **16**, wherein the step of encapsulating the chip, the protection layer and the conductive pillars comprises:

disposing the insulation encapsulation over the chip, the protection layer, and the conductive pillars; and

reducing a thickness of the insulation encapsulation to expose top surfaces of the conductive pillars.

18. The method according to claim **17**, further comprising forming a second redistribution structure above the insulation encapsulation.

19. The method according to claim **18**, wherein the step of forming the second redistribution structure comprises forming at least one dielectric layer and a plurality of second conductive elements, and the conductive pillars are electrically connected between the first conductive elements and the second conductive elements respectively.

20. The method according to claim **11**, wherein the step of disposing the chip on the first surface of the first redistribution structure comprises forming a plurality of bumps between the active surface of the chip and the first surface of the first redistribution structure.

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