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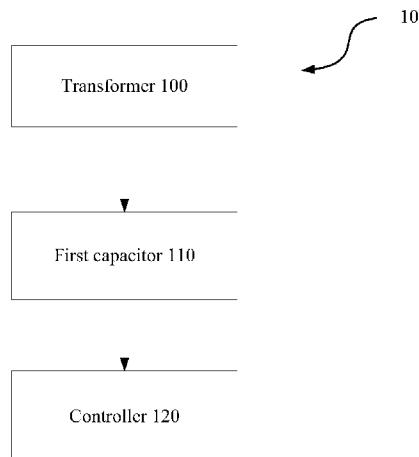


FIG. 1

(57) **Abstract:** Provided are a driving circuit (10) and a driving method. The driving circuit (10) comprises a transformer (100), a first capacitor (110) and a first controller (120). The transformer (100) includes a primary winding and a secondary winding. The secondary winding is located in a secondary side and configured to generate a power. The first capacitor (110) is connected in series to the primary winding, wherein the first capacitor (110) and the transformer (100) are configured to form a resonance unit. The first controller (120) is configured to obtain a feedback current from the secondary side, and change a working frequency of the resonance unit based on the feedback current so as to change the power. Provided also are a lighting device and a method of controlling LED device.



## DRIVING CIRCUIT, LIGHTING DEVICE AND METHOD OF REDUCING POWER DISSIPATION

### TECHNICAL FIELD

**[0001]** The present disclosure relates to a driving circuit, and more specifically, but not exclusively limited to a driving circuit, lighting device and method for reducing power dissipation.

### BACKGROUND

**[0002]** Conventional LEDs operating under a constant current do not emphasize solving thermal power dissipation of the LEDs. The heat generated by LEDs is dissipated via heat dissipation devices made from metals with excellent heat conductivity. LEDs positioned in different environments will eventually reach thermal equilibrium with the ambient air. High thermal power dissipation results in the LEDs working at a high temperature, which, in turn, results in a negative impact on the service life of the LEDs, which causes a reduction of their working reliability and a waste of energy. Furthermore, many metals will be consumed in heat dissipation elements for heat dissipation. Thus, there exists the need for a new driving circuit and devices to overcome the heat dissipation of LEDs.

### SUMMARY OF THE INVENTION

**[0003]** An embodiment of the invention discloses a driving circuit which comprises a transformer, including a primary winding and a secondary winding; the secondary winding is located on a secondary side and configured to generate power; a first capacitor is connected in series to the primary winding, wherein the first capacitor and the transformer are configured to form a resonance unit; one controller is configured to obtain a feedback current from the secondary side, and change the working frequency of the resonance unit based on the feedback current, so as to change the power.

**[0004]** Alternatively, the driving circuit further comprises a first MOSFET and a second MOSFET, wherein the first MOSFET and the second MOSFET are configured to be alternately on and to control the resonance unit to charge or discharge with the

changed working frequency.

**[0005]** Alternatively, a gate of the first MOSFET is connected to a first output port of the first controller, a gate of the second MOSFET is connected to a second output port of the controller, a drain of the first MOSFET is connected to an input voltage, a source of the first MOSFET is connected to both a drain of the second MOSFET and the primary winding, a source of the second MOSFET is connected to ground, wherein the first output port and second output port of the first controller are configured to output a complementary square wave.

**[0006]** Alternatively, the first controller is further configured to obtain a working current of the resonance unit, and change the working frequency of the resonance unit based on the feedback current and the working current.

**[0007]** Alternatively, the first controller is further configured to obtain a change of input voltage, and change the working frequency of the resonance unit based on the feedback current, the change of the input voltage and the working current.

**[0008]** Alternatively, the driving circuit further comprises a second capacitor connected between a connection point of the primary winding and the first capacitor and a first input port of the first controller, the second capacitor being configured to detect the working current.

**[0009]** Alternatively, the secondary side further comprises a first rectifier connected to the secondary winding, and the first rectifier is configured to cut off the power when a voltage on the first rectifier is lower than a first voltage threshold, wherein the first rectifier comprises a Metal-Oxide-Semiconductor Field Effect Transistor.

**[0010]** Alternatively, the secondary side further comprises a second controller; configured to turn on the first rectifier if the voltage during a duration is larger than a second voltage threshold, and the duration is larger than a time threshold.

**[0011]** Alternatively, the second controller further comprises a timer, a RS trigger, a first comparator, a second comparator, a third comparator, and an amplifier, wherein one input port of each of the first comparator, the second comparator and the third comparator is configured to receive an input voltage, the other input port of the first

comparator, the second comparator and the third comparator is configured to obtain a third voltage threshold, a fourth voltage threshold, and a fifth voltage threshold respectively, wherein an output port of the first comparator is connected to a S port of the RS trigger, an output port of the second comparator is connected to a R port of the RS trigger, an output port of the third comparator is connected to a first input port of the amplifier, an input port of the timer is connected to a Q port of the RS trigger, a first output port of the timer is connected to a control port of the RS trigger, a second output port of the timer is connected to a second input port of the amplifier.

**[0012]** Alternatively, the secondary side further comprises a first diode, a third capacitor, wherein an anode of the first diode is connected to a first tap of the secondary winding, the third capacitor is connected between a cathode of the first diode and a second tap of the secondary winding, and the first rectifier is connected to a connection point of the second tap and the third capacitor.

**[0013]** Alternatively, the secondary side further comprises a second rectifier connected to the secondary winding, wherein the first rectifier and the second rectifier are alternately on to perform a full wave rectification.

**[0014]** Alternatively, the driving circuit further comprises an optocoupler connected between the secondary side and the first controller, wherein the optocoupler is configured to provide the feedback current.

**[0015]** Alternatively, the driving circuit further comprises a third rectifier configured to rectify an alternate input current to direct current; a power factor controller connected to the third rectifier and configured to adjust a power factor of the driving circuit.

**[0016]** Another embodiment of the invention discloses a lighting device, comprising a driving circuit, which comprises a transformer, a primary winding and a secondary winding; the secondary winding is located on a secondary side and configured to generate power; a first capacitor is connected in series to the primary winding, wherein the first capacitor and the transformer are configured to form a resonance unit - a first controller configured to obtain a feedback current from the secondary side, and change the working frequency of the resonance unit based on the feedback current; and

wherein the resonance unit is configured to oscillate on the changed working frequency so as to output that changed power; a plurality of LED elements connected to the secondary side of the driving circuit, wherein the LED elements work in a range between about a normal working current and about a peak pulse current.

**[0017]** Alternatively, the normal working current comprises rated working current.

**[0018]** Alternatively, the LED elements work at about the peak pulse current.

**[0019]** Alternatively, the plurality of LED elements are arranged in columns, and the columns are connected in parallel.

**[0020]** Alternatively, the lighting device further comprises a second controller configured to control the columns of LED elements to light in turns.

**[0021]** Alternatively, the driving circuit further comprises a first MOSFET and a second MOSFET, wherein the first MOSFET and the second MOSFET are configured to be alternately on and to control the resonance unit to charge or discharge with the changed working frequency.

**[0022]** Alternatively, a gate of the first MOSFET is connected to a first output port of the first controller, a gate of the second MOSFET is connected to a second output port of the controller, a drain of the first MOSFET is connected to an input voltage, a source of the first MOSFET is connected to both a drain of the second MOSFET and the primary winding, a source of the second MOSFET is connected to ground, wherein the first output port and second output port of the first controller are configured to output complementary square wave.

**[0023]** Alternatively, the first controller is further configured to obtain a working current of the resonance unit, and change the working frequency of the resonance unit based on the feedback current and the working current.

**[0024]** Alternatively, the first controller is further configured to obtain a change of input voltage, and change the working frequency of the resonance unit based on the feedback current, the change of the input voltage and the working current.

**[0025]** Alternatively, the driving circuit further comprises a second capacitor connected between a connection point of the primary winding and the first capacitor and a first input port of the first controller, the second capacitor being configured to detect the working current.

**[0026]** Alternatively, the secondary side further comprises a first rectifier connected to the secondary winding, and the first rectifier is configured to cut off the power when a voltage on the first rectifier is lower than a first voltage threshold, wherein the first rectifier comprises a Metal-Oxide -Semiconductor Field Effect Transistor.

**[0027]** Alternatively, the secondary side further comprises a third controller, configured to turn on the first rectifier if the voltage during a duration is larger than a second voltage threshold, and the duration is larger than a time threshold.

**[0028]** Alternatively, the third controller further comprises a timer, a RS trigger, a first comparator, a second comparator, a third comparator, and an amplifier, wherein one input port of each of the first comparator, the second comparator and the third comparator is configured to receive an input voltage, the other input port of the first comparator, the second comparator and the third comparator is configured to obtain a third voltage threshold, a fourth voltage threshold, and a fifth voltage threshold respectively, wherein an output port of the first comparator is connected to a S port of the RS trigger, an output port of the second comparator is connected to a R port of the RS trigger, an output port of the third comparator is connected to a first input port of the amplifier, an input port of the timer is connected to a Q port of the RS trigger, a first output port of the timer is connected to a control port of the RS trigger, a second output port of the timer is connected to a second input port of the amplifier.

**[0029]** Alternatively, the secondary side further comprises a first diode, a third capacitor, wherein an anode of the first diode is connected to a first tap of the secondary winding, the third capacitor is connected between a cathode of the first diode and a second tap of the secondary winding, and the first rectifier is connected to a connection point of the second tap and the third capacitor.

**[0030]** Alternatively, the secondary side further comprises a second rectifier connected to the secondary winding, wherein the first rectifier and the second rectifier are alternately on to perform a full wave rectification.

**[0031]** Alternatively, the driving circuit further comprises an optocoupler connected between the secondary side and the first controller, wherein the optocoupler is configured to provide the feedback current.

**[0032]** Alternatively, the driving circuit further comprises a third rectifier configured to rectify an alternate input current to direct current; a power factor controller connected to the third rectifier and configured to adjust a power factor of the driving circuit.

**[0033]** Another embodiment of the invention discloses a driving method, comprising: generating a power by a transformer including a primary winding and a secondary winding, which is located on the secondary side; oscillating by a capacitor and the transformer at a working frequency; obtaining a feedback current from the secondary side, changing the working frequency based on the feedback current; and changing the power based on the changed working frequency.

**[0034]** Alternatively, the method further comprises obtaining a working current of the resonance unit, and changing the working frequency of the resonance unit based on the feedback current and the working current.

**[0035]** Alternatively, the method further comprises obtaining a change of input voltage, and changing the working frequency of the resonance unit based on the feedback current, the change of the input voltage and the working current.

**[0036]** Alternatively, the method further comprises converting feedback voltage to the feedback current with optocoupler; obtaining working current with detection capacitor; determining whether the working current is larger than a current-limiting threshold; changing the working frequency of the resonance unit according to the feedback current if not larger than the current-limiting threshold; increasing the working frequency so as to reduce output voltage if larger than the current-limiting threshold.

**[0037]** Another embodiment of the invention discloses a method of controlling LED device, comprising: detecting the temperature of the LED device; determining the off

time in a cycle of the LED device based on the temperature; and switching the LED device on and off periodically, wherein the LED device is off for the determined off time in each cycle.

**[0038]** Alternatively, the method further comprises supplying a voltage to the LED device, such that the LED device works in a range between about a normal working current and about a peak pulse current.

**[0039]** Alternatively, the method further comprises supplying a voltage to the LED device, such that the LED device works at about the peak pulse current.

**[0040]** Another embodiment of the invention discloses a computer-readable medium containing instructions that, when executed by a processor, are configured for performing: detecting the temperature of the LED device; determining the off time in a cycle of the LED device based on the temperature; and switching the LED device on and off periodically, wherein the LED device is off for the determined off time in each cycle.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0041]** The present invention is illustrated in an exemplary manner by the accompanying drawings. The drawings should be understood as exemplary rather than limiting, as the scope of the invention is defined by the claims. In the drawings, the identical reference signs represent the same elements.

**[0042]** FIG. 1 is a device block diagram illustrating an embodiment of the driving circuit.

**[0043]** FIG. 2 is a circuit diagram illustrating another embodiment of the driving circuit.

**[0044]** FIG. 3 is a circuit diagram illustrating another embodiment of the driving circuit.

**[0045]** FIG. 4 is a circuit diagram illustrating another embodiment of the driving circuit.



- [0046]** FIG. 5 is a circuit diagram illustrating another embodiment of the driving circuit.
- [0047]** FIG. 6 is a circuit diagram illustrating another embodiment of the driving circuit.
- [0048]** FIG. 7 is a diagram of an embodiment of a sensing circuit for the secondary output voltage and the FB feedback pin.
- [0049]** FIG. 8 is a circuit diagram illustrating an embodiment of the rectifier circuit.
- [0050]** FIG. 9 is an internal block diagram of the chip IC3 and IC4 shown in FIG. 8.
- [0051]** FIG. 10 is a block diagram illustrating an embodiment of the lighting circuit.
- [0052]** FIG. 11 is a block diagram illustrating an embodiment of the LED circuit.
- [0053]** FIG. 12 is a circuit diagram illustrating an embodiment of the LED device including a driving circuit.
- [0054]** FIG. 13 is a flow chart illustrating an embodiment of a driving method.
- [0055]** FIG. 14A and 14B are flow charts illustrating an embodiment of a method of light controlling.
- [0056]** FIG. 15 is a method flow chart illustrating a method of controlling chip U1.
- [0057]** FIG. 16 is a method flow chart illustrating another method of controlling chip U1.
- [0058]** FIG. 17A is an equivalent circuit diagram illustrating the LC series resonance circuit.
- [0059]** FIG. 17B is a graph illustrating a test of resonance gain.
- [0060]** FIG. 18 is a diagram illustrating an embodiment of the waveform of the LC series resonance circuit.

#### DETAILED DESCRIPTION

**[0061]** Various examples of the invention will now be described. The following description provides specific details for a thorough understanding and enabling

description of these examples. One skilled in the relevant art will understand, however, that the invention may be practiced without many of these details. Additionally, some well-known structures or functions may not be shown or described in detail below, so as to avoid unnecessarily obscuring of the relevant description.

**[0062]** Driving the LED devices is only one application of the embodiment of the driving circuit. The embodiments of the invention can also be applied to audio amplifier, power supply for printer, power supply for LCD TV, or any other electrical device.

**[0063]** FIG. 1 is a device block diagram illustrating an embodiment of the driving circuit. The driving circuit 10 comprises a transformer 100, a first capacitor 110 and a controller 120. The transformer 100 includes a primary winding and a secondary winding, and the secondary winding is configured to generate a power. The secondary winding is located at a second side. The primary winding and the secondary winding will be specifically described in FIG. 2. The first capacitor 110 is connected in series to the primary winding, wherein the first capacitor 110 and the transformer 100 are configured to form a resonance unit. The controller 120 is configured to obtain a feedback current from the secondary side, and changes the working frequency of the resonance unit based on the feedback current. The resonance unit operates at a changed working frequency, such that the output power is changed. Alternatively, the controller 120 is also configured to obtain the working current of the primary winding, that is, the working current of the resonance unit, and changes the working frequency of the resonance unit based on the feedback current and the working current of the resonance unit. Alternatively, the controller 120 is also configured to obtain the change of input voltage, and changes the working frequency of the resonance unit based on the feedback current, the change of the input voltage and the working current.

**[0064]** FIG. 2 is a circuit diagram illustrating another embodiment of the driving circuit. The driving circuit includes a bi-directional passive EMI (Electro Magnetic Interference) suppressor 200, a boost power factor controller PFC 210, an LC resonance frequency converter 220 and a synchronous rectifier 230. The LC resonance frequency converter 220 and the synchronous rectifier 230 will be described in more detail below.

**[0065]** FIG. 3 is a circuit diagram illustrating an embodiment of the driving circuit. The driving circuit 20 comprises a transformer TS, a first capacitor C1 and a controller U1, and further comprises a first MOSFET Q1 and a second MOSFET Q2. The transformer TS includes a primary winding PW and a secondary winding SW. The first MOSFET Q1 and the second MOSFET Q2 are configured to be alternately on and control the resonance unit to charge or discharge.

**[0066]** The controller U1 includes multiple outputs, for example, a first output port out1 and a second output port out2. A gate of the first MOSFET Q1 is connected to the first output port out1 of the controller U1, and a gate of the second MOSFET Q2 is connected to the second output port out2 of the controller U1. A drain of the first MOSFET Q1 is connected to a power supply voltage V1. For example, V1 may be 380 VDC (direct current). A source of the first MOSFET Q1 is connected to both a drain of the second MOSFET Q2 and the primary winding. A source of the second MOSFET Q2 is connected to ground, wherein the first output port and second output port of the controller U1 are configured to output complementary square wave.

**[0067]** When the first MOSFET Q1 is on and the second MOSFET Q2 is off, a current path is shown in FIG. 3. A power supply V1 flows through the transformer TS via the first MOSFET Q1 to charge the capacitor C1 and therefore the electrical energy is stored in the first capacitor C1. When the second MOSFET Q2 is on and the first MOSFET Q1 is off, a current path is shown in FIG. 4. The electrical energy stored in the first capacitor C1 is discharged through the transformer TS. The transformer TS and the first capacitor C1 form a resonance circuit. The resonance frequency  $f_R$  of the resonance circuit, also called local frequency, can be represented as

**[0068]** 
$$f_R = \frac{1}{2\pi\sqrt{L_L \times C_1}} = \frac{1}{6.28\sqrt{L_L \times C_1}}$$

**[0069]** In the above expression,  $f_R$  is the series resonance frequency (Hz),  $L_L$  is the leakage inductance (H) of the transformer TS, and  $C_1$  is the value of the resonance capacitor C1 (F). In the actual application, the maximum variable frequency may be 0.8  $f_R$ .

**[0070]** The controller U1 changes the switching frequency of the first MOSFET Q1 and the second MOSFET Q2 by changing the frequency of the output square wave of the first output port and the second output port. Thus the working frequency of the resonance unit changes accordingly. That is, the charge and discharge periods of the resonance unit which comprises the first capacitor C1 and the transformer TS are also changed. Therefore the induced electrical energy induced by the secondary winding SW of the transformer TS changes accordingly. As a result, power provided by the secondary winding SW of the transformer TS changes consequently.

**[0071]** As shown in FIG. 3, the driving circuit 20 further comprises a second capacitor C2 connected between a connection point of the primary winding PW and the first capacitor C1 and a first input port in1 of the controller U1 and configured to detect the working current of the resonance unit.

**[0072]** FIG. 3 also shows an optocoupler OC connected between the secondary winding SW and the controller U1. The optocoupler OC is configured to provide the feedback current. The left side of the optocoupler OC is a phototransistor and the right side is a light emitting diode (LED). The light emitting diode (LED) converts an electrical signal representing a voltage of the secondary side into an optical signal. The phototransistor detects an incident optical signal and generates a current corresponding to the voltage of the secondary side. The optocoupler may be a linear optocoupler. The higher the voltage on the secondary side, the larger the current generated by the optocoupler OC.

**[0073]** The driving circuit 20 shown in FIG. 3 further comprises a third rectifier REC. The third rectifier REC is configured to rectify an alternate input current to direct current. As shown in FIG. 3, the REC can be implemented as a bridge. The driving circuit 20 further comprises a power factor controller configured to be connected to the third rectifier REC and adjust a power factor of the driving circuit.

**[0074]** FIG. 18 is a diagram illustrating an embodiment of the waveform of the LC series resonance circuit.

**[0075]** The voltage of the first output port out1 of U1 can be expressed as VGS1, and the voltage of the second output port out2 of U1 can be expressed as VGS. As shown in FIG. 18, the square-waves outputted by the first output port and the second output port are complementary. Therefore, the gate voltages of the first MOSFET Q1 and the second MOSFET Q2 are opposite. When the first output port outputs VGS1 at a high voltage level, the second output port outputs VGS2 at a low voltage level. Conversely, when the first output port outputs VGS1 at a low voltage level, the second output port outputs VGS2 at a high voltage level. Therefore, the first MOSFET Q1 and second MOSFET Q2 are alternately on. From FIG. 18, it can be seen that there is a gap between rising and falling edges of VGS1 and VGS2, so as to avoid Q1 and Q2 being on at the same time, and destroy the circuit. From FIG. 18, it can also be seen that the voltage output by U1 is a pulse sequence in square wave, but the LC resonance current is harmonic wave. IS1 represents the source current of Q1, and IS2 represents the source current of Q2.

**[0076]** FIG. 17A is an equivalent circuit diagram illustrating the LC series resonance circuit. R represents an equivalent resistance of the MOSFET. L represents an inductor of the transformer. C represents the resonance capacitor.

**[0077]** FIG. 17B is a graph illustrating a test of resonance gain. Fs represents working frequency, and Fr represents the resonance frequency. Fs/Fr represents the ratio of working frequency and resonance frequency. Its maximum value is 1. Optionally, the working frequency Fs may be selected on the right side of the resonance point, as the gains on the right side of the resonance point are higher than the gains on the left side of the resonance point. That is, the operational region may be selected on the right side of the resonance point. Q represents quality factor, and Gain represents gain. When the working frequency Fs varies, gains for resonance voltage or current are different. From the resonance frequency to its right, the higher the frequency, the smaller the gain, thus the output voltage and current are reduced.

**[0078]** According to an embodiment of the present invention, the advantage of designing a driving circuit as a resonance frequency converter includes the minimum thermal power dissipation in transformation, and the output power can automatically

match the load of the lighting sets in order to achieve the maximum efficiency. It can be well matched in the circumstances of an open circuit (including standby), short circuit, a maximum load and a proportional load. The design of match between the power circuit and the LED circuit includes a thermal dynamic equilibrium of the circuit during operation, which enables the circuit to work with optimal efficiency, and reduces heat dissipation.

**[0079]** The driving circuit is not limited to driving an LED device; it can also be used for driving electrical or electric equipment such as air conditioners. Further, an embodiment of the drive circuit is an efficient driving power supply. As the embodiments solve the problem of thermal power dissipation of a power supply, the embodiments may also be applied, but not limited to, LED street lamps and outdoor lighting, audio amplifier, printer power supply, LCD TV power supply and other electrical devices.

**[0080]** FIG. 4 is a circuit diagram illustrating another embodiment of the driving circuit 40. Details are omitted for the elements already discussed with respect to FIG.3. As shown in FIG. 4, the secondary side of the transformer TS further comprises the first rectifier 400 connected to the secondary winding SW. The secondary winding SW is located on the secondary side. The first rectifier 400 is configured to cut off power when a voltage on the first rectifier 400 is lower than a threshold, the threshold may be, for example, about -310mV. The first rectifier 400 comprises a Metal-Oxide-Semiconductor Field Effect Transistor Q3. As shown in FIG. 4, the secondary side further comprises a first diode D1 and a third capacitor C3, wherein an anode of the first diode D1 is connected to a first tap of the secondary winding SW. The third capacitor C3 is connected between a cathode of the first diode D1 and a second tap of the secondary winding SW. The first rectifier 400 is connected to the connection point of the second tap and the third capacitor C3. A third tap of the secondary winding is connected to ground. As shown in FIG. 4, the first rectifier 400 further includes a rectifier controller IC3 to detect the voltage on the first rectifier 400 and determine whether the voltage on the first rectifier 400 is higher than a threshold - the threshold may be, for example, about -310mV. If the voltage is higher than the threshold, then Q3 will be on, while if the voltage is lower than the threshold, Q3 will be off. Alternatively, the rectifier controller

IC3 can further determine the duration time of the voltage higher than the threshold. If the duration time is greater than a time threshold, for example, about 2 $\mu$ s, it means that the voltage is an input signal and the rectifier controller IC3 controls the Q3 to be turned on. If the duration time is less than the time threshold, the rectifier controller IC3 will determine that it may be interference, for example, a spike pulse, and Q3 will still be off under the control of the rectifier controller IC3. The secondary side further includes a resistor R5 and is configured to limit the current. The first rectifier 400 performs a half-wave rectification on the output waveform and outputs power discontinuously. Since Q3 is positioned in the main current path and it is a MOSFET, and the internal resistance of the MOSFET when it is on is very small compared to a diode, it can subsequently further reduce the heat dissipation.

**[0081]** FIG. 5 is a circuit diagram illustrating another embodiment of the driving circuit. A secondary side where the secondary winding SW is located further comprises a second rectifier 500 connected to the secondary winding SW, wherein the first rectifier 400 and the second rectifier 500 are alternately on to perform a full wave rectification. Specifically, the secondary side further comprises a second diode D2, a fourth capacitor C4, wherein an anode of the second diode D2 is connected to a fourth tap of the secondary winding SW. The fourth capacitor C4 is connected between a cathode of the second diode D2 and a fifth tap of the secondary winding SW. The second rectifier 500 is connected to the connection point of the fifth tap and the fourth capacitor C4. As shown in FIG. 5, the second rectifier 500 further includes a rectifier controller IC4 to detect the voltage on the second rectifier 500 and determine whether the voltage on the second rectifier 500 is higher than a threshold, the threshold may be for example, -310mV. If the voltage is higher than the threshold, Q4 will be on, while if the voltage is lower than the threshold, Q4 will be off. The secondary side further includes a resistor R6 and is configured to limit the current.

**[0082]** FIG. 6 is a circuit diagram illustrating another embodiment of the driving circuit 60. The output HB of U1 drives output transformer TS through DC blocking capacitor/resonance capacitor C14 (equivalent to the C1 in FIG. 3). TS and resonance

capacitor C14 form a primary series resonance circuit and the primary series resonance frequency can be represented as:

$$[0083] \quad f_R = \frac{1}{2\pi\sqrt{L_L \times C_{14}}} \approx \frac{1}{6.28\sqrt{L_L \times C_{14}}}$$

[0084] In the above expression,  $f_R$  is the series resonance frequency (Hz),  $L_L$  is the leakage inductance (H) of the transformer TS, and  $C_{14}$  is the value of the resonance capacitor C14 (F).

[0085] Elements D4, R12 and C12 form a boost circuit and supply power to an internal driver of U1 for the upper MOSFET, that is Q1. Elements C16, R11 and C5 provide filter and bypass to the input Vcc (about +12V). The input Vcc (about +12 V) is the VCC power supply of the controller U1, that is an aiding power supply. Voltage dividers R7, R8, R9 and R10 are used for setting the thresholds of high voltage on, off and overvoltage. When the input high voltage overvoltage cut-off point is about 473 VDC, the on-point can be set at about 360 VDC and the cut-off point of the under-voltage is set at about 285 VDC by the selected values of the voltage dividers. The input under-voltage cut-off point can be set at about 280 VDC due to the internal hysteresis characteristics. Capacitor C13 is a about +380V high frequency bypass capacitor.

[0086] Capacitors C15 and C14 together form a shunt for sampling a part of the primary current. Resistor R16 can detect the primary current (that is, the current to be fed into IS pin of the controller U1) and the generated signal is filtered by R17 and C11. The rated value of C15 can be determined according to the peak voltage occurred in the fault condition. Capacitor C15 is equivalent to the Capacitor C2 in FIG. 3. The capacitor C15 can be made from stable media with low loss such as metal film, SL ceramics or NP0/C0G ceramics, etc. The used capacitor is a discoid ceramic capacitor with a "SL" temperature characteristic and is usually used for the driver of Cold Cathode Fluorescent Lamp (CCFL). According to the following formula, the selected value can set a current-limiting for one period (high-speed) at about 5.5A and a current-limiting for seven periods (low-speed) at about 3A:



$$[0087] \quad I_{CL1} = \frac{0.5}{\left(\frac{C15}{C14 + C15}\right) \times R16}$$

[0088]  $I_{CL}$  is the current-limiting value for seven periods (A), and R16 is the current-limiting resistor (Ohms). C14 and C15 are the value of the resonance capacitor and the current sampling capacitor (nF). As to the current-limiting value for one period, about 0.5 V in above formula can be replaced with about 0.9 V. That is

$$[0089] \quad I_{CL2} = \frac{0.9}{\left(\frac{C15}{C14 + C15}\right) \times R16}$$

[0090] Resistor R17 and capacitor C11 filter the primary current signal to be transmitted to the IS pin of the controller U1. The resistor R17 may be set at the minimum suggested value of about 220 Ohms ( $\Omega$ ). The set value of the capacitor C11 can be about 1nF in order to avoid a false triggering caused by noise and the value is insufficient to influence the above-calculated current, limiting set values  $I_{CL1}$  and  $I_{CL2}$ . Elements of the resistor R17 and the capacitor C11 can be positioned near the IS pin in order to maximize their utility. The IS pin can bear a negative current, therefore the current sensing does not need to adopt a sophisticated rectification scheme.

[0091] Resistor R15 is connected to the pin DT/BF of the controller U1. The dead-time DT is set to about 330 nS and the maximum working frequency  $F_{MAX}$  of the controller U1 is set to about 773 kHz. C9 filters the input of  $F_{MAX}$  of the controller U1. The parallel connection of R15 and R18 can choose the pattern of the pulse train as "one" period for U1. In this way, the lower limit  $f_{START}$  and the upper limit  $f_{STOP}$  of the threshold frequency of the pulse train can be set to about 338 kHz and about 386 kHz respectively.

[0092] The feedback pin FB has the approximate characteristic that each  $\mu$ A current flowing into the feedback pin generates a frequency of about 2.6kHz. With the increase of the current flowing into the feedback pin FB, the working frequency of U1 is higher correspondingly, thus reducing the output voltage. R13 and R14 connected in series enables the set value of the minimum working frequency of U1 to about 115kHz.

The set value is usually a little bit lower than the required frequency to achieve voltage stabilization under the conditions of full load and the minimum large bulk capacitance voltage.

**[0093]** Resistor R13 is bypassed by C7 to provide a soft start output when starts to work. Its operation mode is as follows: when a feedback loop is open, initially a higher current is allowed to flow into the feedback pin FB. Therefore the working frequency of the controller U1 is higher, which enables Q1 and Q2 with a higher switching frequency at the beginning. Then the switching frequencies of Q1 and Q2 are reduced after the output voltage is stabilized. The set value of resistor R14 is usually the same as the resistor R15 in order that the original frequency of a soft-start is equivalent to the maximum working frequency set by the resistor R15. If the value of R14 is smaller than R15, it will cause a delay during the period between applying an input voltage and starting the switching operation.

**[0094]** The optocoupler OC drives the feedback pin FB of the controller U1 via a resistor R19. The resistor R19 can limit the maximum optocoupler current flowing into the feedback pin FB, which achieves an effect of limiting the current. Capacitor C8 is used to filter the feedback pin FB. Resistor R20 may load the output of the optocoupler in order to force it to work with a relatively higher static current and improve its gain. The resistors R19 and R20 may improve the step response of the signal and the output ripple of the pulse train mode. R20 can be isolated from the network of  $F_{MAX}$ /soft-start by a diode D5.

**[0095]** The following part will focus on the basic working principle of U1.

**[0096] - Dead-time, the maximum start-frequency, and the threshold frequency of the pulse train**

**[0097]** The resonance converter U1 requires a fixed and accurate dead-time during the half-period of switching (avoid shoot-through). The resistor voltage dividers connected among the pin DT/BF, pin VREF and grounding pin G are used for setting dead-time, the maximum start-frequency  $F_{MAX}$  and the threshold frequency of the pulse train.

**[0098] - Dead-time/pulse train frequency pin (DT/BF)**

**[0099]** The pin has the voltage-current (V-I) characteristic of the grounding diode at the same time. The resistor voltage divider connected to the pin VREF and the grounding pin G can set the dead-time, the maximum start-frequency, and the threshold frequency of the pulse train; the maximum start-frequency  $F_{MAX}$  is determined by the current flowing into the pin DT/BF through a resistor voltage divider. The ratio of the resistor can be chosen from three independent ratios of the threshold frequency of the pulse train. The three ratios are fixed fractions of  $F_{MAX}$ .

**[00100] - Changes in frequency**

**[00101]** The feedback pin FB is the input of frequency control for the feedback loop. The frequency is proportional to the current of the feedback pin FB. The voltage-current (V-I) characteristic of the feedback pin is similar to the grounding diode.

**[00102] - Pulse train mode**

**[00103]** If the controller U1 determines that the frequency controlled by the current of the feedback pin FB exceeds the upper limit of the pulse train threshold frequency ( $f_{STOP}$ ) set by the resistor voltage divider on the pin DT/BF, the output MOSFET Q1 and Q2 will be cut off. If the working frequency corresponding to the current of the feedback pin FB is lower than the lower limit of the threshold frequency of the pulse train ( $f_{START}$ ), the MOSFET Q1 and Q2 will start switching again. Generally, the pulse train mode controlling is similar to a controller with hysteresis characteristics: a progress is repeated that the frequency increases from  $f_{START}$  to  $f_{STOP}$  and then stops. The minimum and start current of the feedback pin FB is determined by the external circuit connected to the pin VREF and feedback pin FB, thus the minimum and the start frequency  $f_{START}$  is determined. The soft-start capacitor in the circuit determines the timing sequence of the soft-start.

**[00104] - Pin VREF**

**[00105]** VREF pin provides a reference voltage, for example, about 3.4 V, for the external circuit of the feedback pin FB and other function control circuits. The maximum current provided by the VREF pin must be  $\leq$  about 4mA.

**[00106] - Pin OV/UV**

**[00107]** Pin OV/UV detects the output of high voltage B+ through a resistor voltage divider. It performs a voltage ramp up, a voltage ramp down and a function of overvoltage (OV) protection with hysteresis characteristics. The ratios of these voltages are fixed. Users can choose the ratio of the resistor voltage divider and enables the ramp up voltage lower than the minimum stabilized set value for rated large capacitor (input) voltage in order to insure a start.

**[00108]** However, the restart voltage OV (lower protection threshold) is higher than the maximum set value for the rated large capacitor voltage in order to insure of a restart of LC when input voltage fluctuations triggers an upper threshold of OV. If different voltage ramp up - voltage ramp down - OV ratio are needed, an additional external circuit may need to be added around the resistor voltage dividers.

**[00109] - Pin VCC under voltage lock out (UVLO)**

**[00110]** Pin VCC has a function of internal under voltage lock out UVLO and also has hysteresis characteristics. The controller U1 will not start until the pin voltage VCC exceeds the VCC start threshold VUVLO (+). U1 will cut off when VCC drops to the cut-off threshold VUVLO(-) of VCC.

**[00111] Pin VCCH under voltage lock out (UVLO)**

**[00112]** Pin VCCH is the power supply pin of the upper-side driver. It is similar to the pin VCC and has a UVLO function, but the threshold value is lower than pin VCC. Thus the voltage of VCCH is a little bit lower than VCC, because pin VCCH is powered by VCC through boost diode D4, and a series current-limiting resistor R12.

**[00113] Start and restart automatically**

**[00114]** Before start, internal of the chip U1 pulls the voltage of the feedback pin FB up to the pin VREF in order to discharge the soft-start capacitor and keep the output MOSFET Q1 and Q2 off. After start, the internal pull-up transistor is off and the soft-start capacitor charges. The output starts switching operation at  $F_{MAX}$ . The current of the

feedback pin decreases and the switching frequency falls down. At this time, the output of the power supply goes up.

**[00115]** When the output reaches the set point of voltage, the optocoupler OC is on, which closes the feedback loop and the output is regulated to reach a stabilized voltage. Each time the pin VCC powers on, the pin DT/BF is under a high impedance mode for 500ms to detect the ratio of the voltage divider and choose the working threshold of the pulse train. Storing these settings until VCC is powered on and the settings need to be chosen again next time. Then the pin DT/BF turns into a normal mode, which is similar to a grounding diode. The sensed current will then set an  $F_{MAX}$  frequency. The threshold frequency of the pulse train is the fixed fraction of  $F_{MAX}$ . As long as the internal of the chip U1 pulls the voltage of the feedback pin FB up to start, the internal oscillator operates the internal counter at  $F_{MAX}$ .

**[00116]** When a malfunction is detected by pin IS、OV/UV or VCC (UVLO), the internal feedback pin FB pulls up the transistor and is on, for example, 131,072 clock periods in order to totally discharge the soft-start capacitor and then try to restart. The first power-on after the power supply circulation of VCC only waits for example 1024 periods, including the situation that the pin OV/UV rises above the threshold of the ramp voltage the first time after VCC powers on.

**[00117] - Remote shut off**

**[00118]** Remote shut off can be achieved by pulling the OV/UV pin voltage down to the ground or pull the IS pin up to higher than about 0.9V for activation. These two approaches can both activate for example a 131,072 cycle restart cycle.

**[00119]** It can also be achieved by pulling down the VCC to shut off the device, but when the VCC is pulled up, the voltage of feedback pin FB will be pulled up to VREF pin voltage, and the soft start capacitor is discharged for only for example 1024  $F_{max}$  clock cycles. If this solution is used, it should be guaranteed at the time that the VCC is pulled down, plus, for example, 1024 cycles are sufficient for the soft start capacitor to discharge, otherwise, it will cause the start frequency to be lower and result in a too large primary current, which may even trigger over-current protection.

**[00120] - Current sensing**

**[00121]** IS pin is used to sense the primary current. It is similar to a diode inversely connected to grounding pin G. It allows a negative voltage, with the condition that the negative current is limited to less than about 5mA. To this end, IS pin is connected to the current sensing resistor through a series current-limiting resistor of more than 220Ω (for example R17) (or through primary capacitive voltage divider and sensing resistor, such as C11 and R16). Therefore IS pin can accept AC waveform, and does not require a rectifier or peak sensing circuit. If IS pin senses a rated peak forward voltage of about 0.5 V for seven consecutive cycles, the automatic restart will be activated. IS pin also has a higher rated threshold of about 0.9 V, and when a single pulse voltage exceeds this threshold, the automatic restart will be activated. The minimum sensing pulse width to trigger the two voltage thresholds requires a rating of about 30 ns, i.e. normal threshold sensing time should be greater than 30ns.

**[00122]** The parameters for resistance and capacitance shown in FIG. 6 are as below. The following values are only for example, and those of ordinary skill in the art can select other values according to the actual practical application.

	Value	Accuracy
R7	976kΩ	1%
R8	976kΩ	1%
R9	976kΩ	1%
R10	20kΩ	1%
R11	4.7kΩ	
R12	2.2kΩ	1%
R13	36.5kΩ	
R14	7.68kΩ	1%
R15	7.68kΩ	1%
R16	24Ω	
R17	220Ω	

R18	143k $\Omega$	1%
R19	1.2k $\Omega$	
R20	4.7k $\Omega$	

	Value	Internal voltage
C5	1 $\mu$ F	25V
C6	4.7nF	200V
C7	220nF	50V
C8	4.7nF	200V
C9	4.7nF	200V
C10	1 $\mu$ F	25V
C11	1nF	200V
C12	330nF	50V
C13	220nF	630V
C14	6.2nF	1.6kV
C15	47pF	1.5kV
C16	47 $\mu$ F	35V

**[00123]** FIG. 7 is a diagram of an embodiment of a sensing circuit for the secondary output voltage and the FB feedback pin.

**[00124]** Feedback pin FB is a pin with stabilized voltage. It has a characteristic of a Thévenin's equivalent circuit with a rated voltage of about 0.65V and a resistance of about 2.5k $\Omega$ . Under normal working conditions, it absorbs current. During shut off time of automatic restart, and the clock delay period before start, it will internally pull up voltage to VREF, so as to discharge the soft start capacitor Cstart in ( equivalent to C7 in FIG. 6). The current that enters the pin determines the working frequency, that is, the

switching frequency. The greater the current, the greater the switching frequency, so as to reduce the LC resonance output voltage. In a typical application, the optocoupler to VREF pin pulls up the voltage on the feedback pin FB through the resistor network. When the output voltage rises, the optocoupler acts as a current source to inject current into the feedback pin FB, so as to increase the current on the feedback pin FB. The resistor network among the optocoupler, the feedback pin FB and VREF pin determines the minimum and maximum feedback pin current (thus determines the minimum and maximum working frequency). The optocoupler can control the current on the feedback pin FB during the duration that the current ranges from cut-off to saturation. The resistor network also includes soft start timing capacitor Cstart (see FIG. 7).

**[00125]** The network settings should be lower than the minimum frequency conversion control circuit U1 power under the minimum input voltage required by the frequency. In FIG. 7, this is decided by Rfmin and Rstart, and when the light coupling device as current feedback pin is decided by the two resistances. Under normal working conditions, Cstart is negligible.

**[00126] - Matching load**

**[00127]** Converter U1 is variable frequency resonance converter. In a smaller range, when the load is reduced, the output voltage increases, therefore feedback current on the feedback pin FB increases, and the frequency increases. Refer to the resonance curve shown in FIG. 17B, when the operational region is on the right side of the resonance point - the higher the frequency, the lower the gain - thus the output voltage is reduced accordingly, which achieves the effect of stable voltage and load matching. When the converter U1 works at a series resonance frequency, the frequency changes slightly, if at all, with the change of load. When the voltage ramps down (minimum input voltage) at full load, the working frequency will reach the required minimum working frequency (close to the resonance point).

**[00128]** The parameters for resistance, capacitance and inductance shown in FIG. 7 are as below.

	Value	Accuracy
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R23	86.6kΩ	1%
R24	7.5kΩ	
R25	1kΩ	
R26	1.5kΩ	
R27	22kΩ	
R28	10kΩ	1%
R29	47Ω	

	Value	Internal Voltage
C17	330nF	50V
C18	470μF	35V
C19	2.2nF	200V
C20	3.3nF	200V
CFB	4.7nF	

	Value
L1	150nH

**[00129]** Further, zener diode in the load voltage detection circuit, shown in FIG. 7 can use the general 431 type.

**[00130]** FIG. 15 is a method flow chart of controller U1. For U1, the hardware circuit power input and hardware detection management includes: provide the about 12V aiding power to VCC and VCCH power supply pin. When the input voltage is greater than the VCC pin voltage threshold, U1 starts. When the input voltage is lower than the VCC pin circuit off threshold, U1 does not work, and all the outputs are closed. When the input voltage is greater than the VCCH pin circuit threshold, Q1 starts working status.

**[00131]** For a software part, shown in FIG. 15, first the hardware and parameter variables of the controller U1 are initialized in block 1500. Then the controller U1 determines whether the input DC power supply (about 380V) is normal in block 1510. If abnormal, then the controller U1 is closed in block 1520, to prevent that the controller U1 from being damaged. If normal, then the controller U1 determines whether working frequency  $f_s$  is less than the maximum frequency threshold ( $f_{stop}$ ) in block 1530. If less than the maximum frequency threshold, then the controller U1 continues to determine whether the working frequency is greater than the minimum frequency threshold ( $f_{start}$ ) in block 1540. If  $f_s$  is less than or equal to the minimum frequency threshold value, or if  $f_s$  is greater than or equal to the maximum frequency threshold, simultaneously shut off both Q1 and Q2 in block 1550. If  $f_{start} < f_s < f_{stop}$ , then the Q1 and Q2 are turned on in block 1560.

**[00132]** FIG. 16 is a flow chart illustrating a method of adjusting output power. First the method detects in block 1600 the load voltage, that is, the feedback voltage. Then the optocoupler converts in block 1610 the feedback voltage to feedback current. Then in block 1620, the feedback current changes according to the change of feedback voltage. Then, the controller U1 changes in block 1630 the working frequency of the resonance unit according to the feedback current, so as to change the output voltage in block 1640. If the working current is greater than the current limit threshold, the controller U1 increases the working frequency so as to reduce the output voltage, instead of immediately closing Q1 and Q2.

**[00133]** FIG. 8 is a circuit diagram illustrating an embodiment of the rectifier circuit. FIG. 8 will be described in combination with FIGs. 4 and 5. The IC3 in FIG. 8 is equivalent to the IC3 in FIGs. 4 and 5, and IC4 in FIG. 8 is the equivalent of IC4 in FIGs. 4 and 5. As shown in FIG. 8, the IC3 and IC4 respectively have an Srsense input port and a Driver output respectively. Rsresense in FIG. 8 is equivalent to R5 and R6 in FIG. 5. Qsec is equivalent to Q3 and Q4 in FIG. 5. D3 is equivalent to D1 in FIG. 5, and D4 is equivalent to D2 in FIG. 5.

**[00134]** FIG. 9 is an internal block diagram of the chip IC3 and IC4 shown in FIG. 8. IC3 and IC4 are the same synchronous rectifier chips. Chip IC3 and IC4 each comprise

a timer, a RS trigger, a first comparator COMP1, a second comparator COMP2, a third comparator COMP3, and an amplifier AMP. One input port of each of the first comparator COMP1, the second comparator COMP2 and the third comparator COMP3 is configured to receive an input voltage. The other input port of each the first comparator COMP1, the second comparator COMP2 and the third comparator COMP3 is configured to obtain a first voltage threshold, for example, about -310mV, a second voltage threshold, for example, about -12mV, and a third voltage threshold respectively, for example, about -55mV. An output port of the first comparator COMP1 is connected to an S port of the RS trigger. An output port of the second comparator COMP2 is connected to an R port of the RS trigger. An output port of the third comparator COMP2 is connected to the first input port of the amplifier AMP. An input port of the timer is connected to a Q port of the RS trigger. The first output port of the timer is connected to a control port of the RS trigger. A second output port of the timer is connected to a second input port of the amplifier AMP. The timer is hysteresis.

**[00135]** FIG. 10 is a block diagram illustrating an embodiment of the lighting circuit.

**[00136]** When the rectifying circuit is working, its operation principle is as follows: when the SRSENSE pin senses negative voltage (typical value of about - 310mv), the driver outputs high voltage level, and the external MOSFET Qsec is on. After the SRSENSE pin voltage rises to about - 55mv, the driving output voltage will maintain the pin voltage at about - 55mv; When SRSENSE pin voltage rises to about -12mv, the drive output will be pulled down to the ground immediately.

**[00137]** After the synchronous rectifier MOSFET is on, input signal of SRSENSE pin will be interrupted for about 2ms, in order to prevent wrong turn-off caused by secondary impulse current with high-frequency.

**[00138]** When the SRSENSE pin voltage is about -55mv, the driver output voltage will be immediately reduced. When the switch current is zero, the external power switch Qsec (that is equivalent to Q3 and Q4 in FIG. 5) will turn off immediately. When SRSENSE pin voltage equals about -12mv, zero current is detected.

**[00139]** When the Timer detects a secondary pulse to be less than two microseconds ( $\mu\text{s}$ ) (typically), the driver output shuts down, which causes the circuit to work at a small duty cycle. When the secondary pulse increases to more than 2.2 microseconds ( $\mu\text{s}$ ), the driver output reopens. Those having ordinary skill in the art should appreciate that the above numericals (for example, the 2 microseconds and 2.2 microseconds) are for reference only, and those having ordinary skill in the art can adjust the actual values according to actual application.

**[00140]** The driving capacity of the gate driving circuit for the external power MOSFET Qsec includes typical drive current of about 250mA and typical reverse current of about 2.7A. The driving capacity can achieve quick open and shut off with high-efficiency. The output driving voltage is limited to about 10v. The driving voltage can drive all of the MOSFET with minimum turn-on resistance.

**[00141]** At startup ( $V_{CC} < V_{\text{startup}}$ ) and under-voltage lockout, the output driving voltage is immediately pulled low.

**[00142]** The rectifier circuit may have at least the following advantages:

**[00143]** Precise synchronous rectifying function; wide voltage power supply (about 8.6 V ~ about 38 V); Accurate internal reference voltage (accuracy of 1%); 10V voltage with high driving capacity and low turn-on resistance can drive all the MOSFET; Green features: low current consumption, high system efficiency from no load to full load; Protection features: under-voltage protection, when VCC voltage reaches about 8.6 V (typical), under-voltage lockout is removed, and the synchronous rectifier circuit is activated. When the VCC voltage drops below 8.1V, the IC enters under-voltage lockout state again, and the synchronous rectifier outputs low level voltage.

**[00144]** FIG. 11 is a diagram illustrating an embodiment of the LED circuit. The lighting circuit includes a LED array controller 5 and a LED array 6.

**[00145]** FIG.12 is a diagram illustrating an embodiment of the circuit of the LED device including a driving circuit. The lighting device 50 includes the driving circuit. The driving circuit further includes a transformer TS, a capacitor C1, and a controller U1. The lighting device also includes a plurality of LED elements connected to the

secondary side of the driving circuit. These LED elements are arranged in several groups, namely into several columns, and the several groups are connected in parallel, wherein the LED elements work between about a rated working current and about a peak pulse current. Alternatively, the LED elements may work at about the peak pulse current. Generally speaking, the peak pulse current of the LED elements is equal to the peak current, and is 3 times that of the normal working current. The normal working current comprises the rated working current.

**[00146]** The number of the LED elements in the LED array can be one high-power (integrated optical source, COB etc.) or multiple. The maximum total power of the LED elements can be up to hundreds of watts. Series connection (i.e., channel CH1, CH2,...) or parallel connection (column number of like strings) can be adopted according to the power parameters of the power supply and LED element parameter. The parameter of each string is the same and the operating principles are similar as well. LED array may be designed as a surface, instead of a point. The LED array may be well ventilated, and the LED elements are first connected in series, then the strings are connected in parallel.

**[00147]** When many LED elements are needed to build a high-power LED array LED, a plurality of channels are formed first by being connected in series. (In the embodiment, there are four channels CH1-CH4). Each array is controlled independently. Differentiation will be created if all of the four strings are connected in parallel, which will result in additional heat dissipation.

**[00148]** Q5~Q8 in FIG. 12 is the current driver for the controller U2. R21, R22, R23 and R24 are the sample resistors employed by U2 to detect the value of turn-on current of each channel. Sample resistors can also function as the current-limiting resistor for respective channels CH1, and CH2. The sample resistors can be adjusted to determine the maximum current. The current of each channel can take the value of peak pulse current value of the LED product parameter provided by the manufacturer. Advantage of using the peak pulse current value is to establish a thermal power fluctuation mode, and heat fluctuation transfer is far better than the constant current heat transfer. Under an appropriate enough frequency, and by taking advantage of the human eye's ability to

sense the brightness of an object, the thermal fluctuation mode substantially reduces power consumption, while achieving the same effect.

**[00149]** In addition to detecting the current of each channel (CH1 and CH2, as examples), and protecting each channel, the controller U2 further determines the on/off time period of the LED array to eliminate flickers, and determines the value of off time  $T_{off}$ . The off-time  $T_{off}$  determines the operating temperature and overall brightness of the LED array. When the LED device works discontinuously, and when the LED elements are instantly on, the LED elements will have the maximum brightness (when operating at the peak pulse current) which can effectively enhance the subjective brightness of sensitization of human eyes so as to be more energy-efficient. The enhanced instant temperature difference will facilitate conducting the heat to the outside because the conductive heat is proportional to the temperature difference. Distortion-less dimming is easy to be achieved through increasing a few elements, which greatly reduces the light attenuation and aging of the LED elements so as to enable the LED device lifetime to be normally 50,000~100,000 hours. If the operational parameters of the circuit and the space structure of the LED device are carefully adjusted, the LED device can use quite few nonferrous metal heat sinks, or even none at all.

**[00150]** FIG. 13 is a diagram illustrating an embodiment of a driving method. The driving method can be used to adjust power dissipation. The method comprises generating in block 1300, a power by a transformer. The transformer includes a primary winding and a secondary winding, and the secondary winding is located in a secondary side; oscillating, in block 1310, at a working frequency by a resonance unit formed by a capacitor and the transformer; obtaining, in block 1320, a feedback current from the secondary side, and changing in block 1330, the working frequency of the resonance unit based on the feedback current such that the power is changed.

**[00151]** FIG. 14A and 14B are flow charts illustrating an embodiment of a method of light controlling. U2 is equivalent to LED control chip in FIG. 12. It can be a programmable single-chip MCU, and is used to control the LED array. If the circuit works normally, the LED array opens and closes periodically. The working cycle can be set when programming, and the maximum cycle should keep the LED array flicker free.

Working cycle refers to that the LED array works in a pulse mode, and the LED array is not always on, but on and off periodically, and the turn-off time is Toff. As long as the pulse frequency is high enough (> about 50Hz), there would be no flicker.

**[00152]** FIG. 14A shows a procedure of U2 after it is powered on and reset:

**[00153]** The method starts in block 1400, then, in block 1410, hardware of controller U2 is initialized, and then in block 1420, the process enters major control program, and tests LED string circularly in time division.

**[00154]** The method of determining the working temperature of the LED array in LED device comprises a fixed method and an automatic management method:

**[00155]** 1) manually fixed method

**[00156]** When the products are manufactured in a factory, different turn-off time Toff is selected according to the environmental temperature, so as to measure the working temperature when the LED array are stable, that is, Toff time of LED elements is determined according to the working temperature. Toff value can be programmed in chips.

**[00157]** 2) automatic management method

**[00158]** When the products are manufactured in a factory, they are equipped with a temperature sensor in the circuit, and the Toff value is automatically determined by the chip program according to the temperature of LED element feedback by the temperature sensor, so as to determine the overall temperature of the LED device.

**[00159]** Current detection for the LED array (each channel CH1 and CH2 or,...): controller U2 is connected to resistors R21, R22,... , which are respectively sampling resistors corresponding to the respective channels CH1, CH2,... , that is each analog-digital conversion channel ADC1, ADC2,... corresponding to U2. When U2 opens each channel CH1, CH2,... the current tested from each channel by U2 is treated as follows:

**[00160]** U2 compares the current obtained through corresponding analog-to-digital conversion ADC channel to the maximum pulse current (that is, the peak pulse current) of the LED string. The maximum current is the maximum pulse current value that

channels CH1 or CH2,... allow (which can be looked up in the LED element parameter table). The maximum pulse current value generally is three times the normal working current.

**[00161]** The measured current is compared with the maximum pulse currents of LED string. When the measured current is larger than the maximum pulse current value of the LED strings, the channel is closed, so as to prevent the LED strings from over current and electrical shorts.

**[00162]** When the LED string is on, the maximum current is three times the normal operating values (which can be looked up in the LED element information); and the minimum current value can be the normal working value. Software engineers can program to input in advance.

**[00163]** Alternatively, the LED string turn-on time and turn-off time value  $T_{off}$  can be an experimental value, which can be input with program by a software engineer in advance.

**[00164]** FIG. 14B shows a flow chart of an embodiment method of controlling the LED. In FIG. 14B, the method first determines, in block 1430, whether the LED string current is normal; by comparing measured current with maximum and minimum current values during programming. If the current is normal, the method turns on the corresponding LED string in block 1440, and supplies power to the gate of the corresponding LED string. Otherwise, the method turns off the corresponding LED string in block 1450; U2 sets the output of the corresponding CHANNEL (CHANNEL) to 0. After turning on the corresponding LED string, the method continues to perform ADC to test current in block 1460, and then it determines whether the turn-on time meets a predetermined condition in block 1470, such as whether the time reaches a predetermined duration, such as about 2ms. If the turn-on time meets the predetermined condition, then all LED strings are closed in block 1480, and then the method determines whether a turn-off time  $T_{off}$  meets a predetermined condition in block 1490, such as whether it reaches a predetermined duration, such as 3 ms. If the turn-off time meets the predetermined condition, then the method goes back to determine whether the LED string current is normal in block 1430. If the turn-off time



Toff does not meet the predetermined condition, the method continues to determine whether the closed time Toff meets the predetermined conditions in block 1490. If the turn-on time does not meet the predetermined condition, then the method returns to continue to determine whether the turn-on time meets the predetermined condition in block 1470.

**[00165]** Optionally, if the period for turn-on and turn-off is set, then the process of determining the turn-on time and turn-off time can be omitted.

**[00166]** Although the present invention has been described with reference to specific exemplary embodiments, the present invention is not limited to the embodiments described herein, and it can be implemented in form of modifications or alterations without deviating from the spirit and scope of the appended claims. Accordingly, the description and the drawings are to be considered in an illustrative rather than a restrictive sense.

**[00167]** From the foregoing, it will be appreciated that specific embodiments of the technology have been described herein for purposes of illustration; however various modifications can be made without deviating from the spirit and scope of the present invention. Accordingly, the present invention is not restricted except in the spirit of the appended claims.

**[00168]** Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims. In the claims the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. Even if particular features are recited in different dependent claims, the present invention also relates to the embodiments including all these features. Any reference signs in the claims should not be construed as limiting the scope.

**[00169]** Features and aspects of various embodiments may be integrated into other embodiments, and embodiments illustrated in this document may be implemented without all of the features or aspects illustrated or described. One skilled in the art will appreciate that although specific examples and embodiments of the system and

methods have been described for purposes of illustration, various modifications can be made without deviating from the spirit and scope of the present invention. Moreover, features of one embodiment may be incorporated into other embodiments, even where those features are not described together in a single embodiment within the present document. Accordingly, the invention is described by the appended claims.

## CLAIMS

### I/WE CLAIM:

1. A driving circuit comprising:
  - a transformer including a primary winding and a secondary winding, the secondary winding being located on a secondary side and configured to generate a power;
  - a first capacitor connected in series to the primary winding, wherein the first capacitor and the transformer are configured to form a resonance unit;
  - a first controller configured to obtain a feedback current from the secondary side, and change the working frequency of the resonance unit based on the feedback current so as to change the power.
2. The driving circuit of claim 1, further comprising a first MOSFET and a second MOSFET, wherein the first MOSFET and the second MOSFET are configured to be alternately on and to control the resonance unit to charge or discharge with the changed working frequency.
3. The driving circuit of claim 2, wherein a gate of the first MOSFET is connected to a first output port of the first controller, a gate of the second MOSFET is connected to a second output port of the first controller, a drain of the first MOSFET is connected to an input voltage, a source of the first MOSFET is connected to both a drain of the second MOSFET and the primary winding, a source of the second MOSFET is connected to ground, wherein the first output port and second output port of the first controller are configured to output a complementary square wave.
4. The driving circuit of claim 1, wherein the first controller is further configured to obtain a working current of the resonance unit, and change the working frequency of the resonance unit based on the feedback current and the working current.
5. The driving circuit of claim 4 wherein the first controller is further configured to obtain a change of input voltage, and change the working frequency of the

resonance unit based on the feedback current, the change of the input voltage and the working current.

6. The driving circuit of claim 1, further comprising a second capacitor connected between a connection point of the primary winding and the first capacitor and a first input port of the first controller, the second capacitor being configured to detect the working current.

7. The driving circuit of claim 1, wherein the secondary side further comprises a first rectifier connected to the secondary winding, and the first rectifier is configured to cut off the power when a voltage on the first rectifier is lower than a first voltage threshold, wherein the first rectifier comprises a Metal-Oxide-Semiconductor Field Effect Transistor.

8. The driving circuit of claim 7, wherein the secondary side further comprises a second controller; configured to turn on the first rectifier if the voltage during a duration is larger than a second voltage threshold, and the duration is larger than a time threshold.

9. The driving circuit of claim 8, wherein the second controller further comprises a timer, a RS trigger, a first comparator, a second comparator, a third comparator, and an amplifier, wherein

one input port of each of the first comparator, the second comparator and the third comparator is configured to receive an input voltage, the other input port of the first comparator, the second comparator and the third comparator is configured to obtain a third voltage threshold, a fourth voltage threshold, and a fifth voltage threshold respectively, wherein an output port of the first comparator is connected to a S port of the RS trigger, an output port of the second comparator is connected to a R port of the RS trigger, an output port of the third comparator is connected to a first input port of the amplifier, an input port of the timer is connected to a Q port of the RS trigger, a first

output port of the timer is connected to a control port of the RS trigger, a second output port of the timer is connected to a second input port of the amplifier.

10. The driving circuit of claim 7, wherein the secondary side further comprises a first diode, a third capacitor, wherein an anode of the first diode is connected to a first tap of the secondary winding, the third capacitor is connected between a cathode of the first diode and a second tap of the secondary winding, and the first rectifier is connected to a connection point of the second tap and the third capacitor.

11. The driving circuit of claim 7, wherein the secondary side further comprises a second rectifier connected to the secondary winding, wherein the first rectifier and the second rectifier are alternately on to perform a full wave rectification.

12. The driving circuit of claim 1, further comprising an optocoupler connected between the secondary side and the first controller, wherein the optocoupler is configured to provide the feedback current.

13. The driving circuit of claim 1, further comprising:  
a third rectifier configured to rectify an alternate input current to direct current;  
a power factor controller connected to the third rectifier and configured to adjust a power factor of the driving circuit.

14. A lighting device, comprising:  
a driving circuit comprising—  
a transformer including a primary winding and a secondary winding, the secondary winding being located in a secondary side and configured to generate a power;  
a first capacitor connected in series to the primary winding, wherein the first capacitor and the transformer are configured to form a resonance unit;

a first controller configured to obtain a feedback current from the secondary side, and change a working frequency of the resonance unit based on the feedback current; and wherein the resonance unit is configured to oscillate on the changed working frequency so as to output changed power;

a plurality of LED elements connected to the secondary side of the driving circuit, wherein the LED elements work in a range between about a normal working current and about a peak pulse current.

15. The lighting device of claim 14, wherein the normal working current comprises rated working current.

16. The lighting device of claim 14, wherein the LED elements work at about the peak pulse current.

17. The lighting device of claim 14, wherein the plurality of LED elements are arranged in columns, and the columns are connected in parallel.

18. The lighting device of claim 14, further comprises a second controller configured to control the columns of LED elements to light in turns.

19. The lighting device of claim 14, wherein the driving circuit further comprises a first MOSFET and a second MOSFET, wherein the first MOSFET and the second MOSFET are configured to be alternately on and to control the resonance unit to charge or discharge with the changed working frequency.

20. The lighting device of claim 19, wherein a gate of the first MOSFET is connected to a first output port of the first controller, a gate of the second MOSFET is connected to a second output port of the first controller, a drain of the first MOSFET is connected to an input voltage, a source of the first MOSFET is connected to both a

drain of the second MOSFET and the primary winding, a source of the second MOSFET is connected to ground, wherein the first output port and second output port of the first controller are configured to output complementary square wave.

21. The lighting device of claim 14, wherein the first controller is further configured to obtain a working current of the resonance unit, and change the working frequency of the resonance unit based on the feedback current and the working current.

22. The lighting device of claim 21, wherein the first controller is further configured to obtain a change of input voltage, and change the working frequency of the resonance unit based on the feedback current, the change of the input voltage and the working current.

23. The lighting device of claim 14, wherein the driving circuit further comprises a second capacitor connected between a connection point of the primary winding and the first capacitor and a first input port of the first controller, the second capacitor being configured to detect the working current.

24. The lighting device of claim 14, wherein the secondary side further comprises a first rectifier connected to the secondary winding, and the first rectifier is configured to cut off the power when a voltage on the first rectifier is lower than a first voltage threshold, wherein the first rectifier comprises a Metal-Oxide -Semiconductor Field Effect Transistor.

25. The lighting device of claim 24, wherein the secondary side further comprises a third controller, configured to turn on the first rectifier if the voltage during a duration is larger than a second voltage threshold, and the duration is larger than a time threshold.

26. The lighting device of claim 25, wherein the third controller further comprises a timer, a RS trigger, a first comparator, a second comparator, a third

comparator, and an amplifier, wherein

one input port of each of the first comparator, the second comparator and the third comparator is configured to receive an input voltage, the other input port of the first comparator, the second comparator and the third comparator is configured to obtain a third voltage threshold, a fourth voltage threshold, and a fifth voltage threshold respectively, wherein an output port of the first comparator is connected to a S port of the RS trigger, an output port of the second comparator is connected to a R port of the RS trigger, an output port of the third comparator is connected to a first input port of the amplifier, an input port of the timer is connected to a Q port of the RS trigger, a first output port of the timer is connected to a control port of the RS trigger, a second output port of the timer is connected to a second input port of the amplifier.

27. The lighting device of claim 24, wherein the secondary side further comprises a first diode, a third capacitor, wherein an anode of the first diode is connected to a first tap of the secondary winding, the third capacitor is connected between a cathode of the first diode and a second tap of the secondary winding, and the first rectifier is connected to a connection point of the second tap and the third capacitor.

28. The lighting device of claim 24, wherein the secondary side further comprises a second rectifier connected to the secondary winding, wherein the first rectifier and the second rectifier are alternately on to perform a full wave rectification.

29. The driving circuit of claim 1, wherein the driving circuit further comprises an optocoupler connected between the secondary side and the first controller, wherein the optocoupler is configured to provide the feedback current.

30. The lighting device of claim 14, wherein the driving circuit further comprises:

a third rectifier configured to rectify an alternate input current to direct current;



a power factor controller connected to the third rectifier and configured to adjust a power factor of the driving circuit.

31. A driving method, comprising:  
generating a power by a transformer including a primary winding and a secondary winding, the secondary winding being located in a secondary side;  
oscillating by a capacitor and the transformer at a working frequency;  
obtaining a feedback current from the secondary side,  
changing the working frequency based on the feedback current; and  
changing the power based on the changed working frequency.

32. The method of claim 31, further comprising:  
obtaining a working current of the resonance unit, and  
changing the working frequency of the resonance unit based on the feedback current and the working current.

33. The method of claim 33, further comprising:  
obtaining a change of input voltage, and  
changing the working frequency of the resonance unit based on the feedback current, the change of the input voltage and the working current.

34. A method of claim 31, further comprising:  
converting feedback voltage to the feedback current with optocoupler;  
obtaining working current with detection capacitor;  
determining whether the working current is larger than a current-limiting threshold;  
changing the working frequency of the resonance unit according to the feedback current if not larger than the current-limiting threshold;  
increasing the working frequency so as to reduce output voltage if larger than the current-limiting threshold.

35. A method of controlling LED device, comprising:  
detecting a temperature of the LED device;  
determining an off time in a cycle of the LED device based on the temperature;  
and  
switching the LED device on and off periodically, wherein the LED device is off for the determined off time in each cycle.

36. The method of claim 35, further comprising:  
supplying a voltage to the LED device, such that the LED device works in a range between about a normal working current and about a peak pulse current.

37. The method of claim 35, further comprising:  
supplying a voltage to the LED device, such that the LED device works at about the peak pulse current.

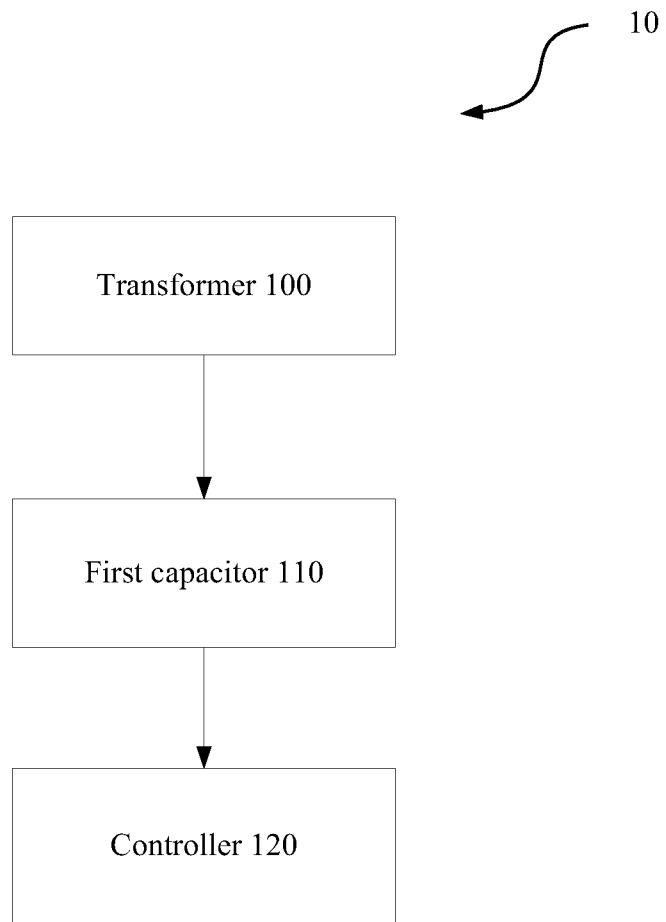


FIG. 1

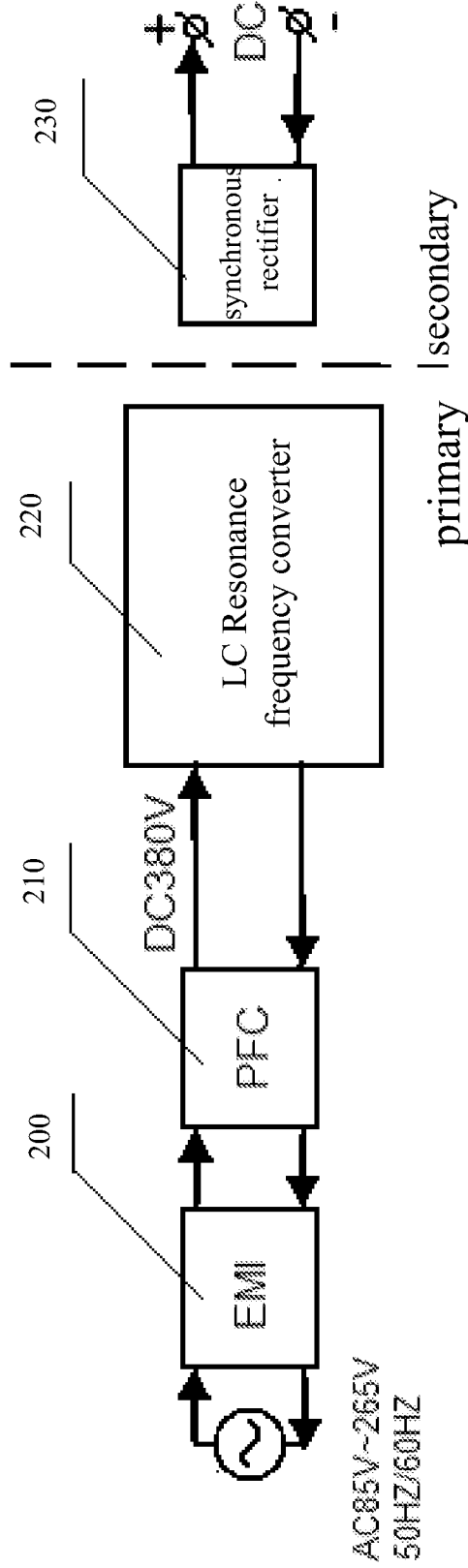


FIG. 2

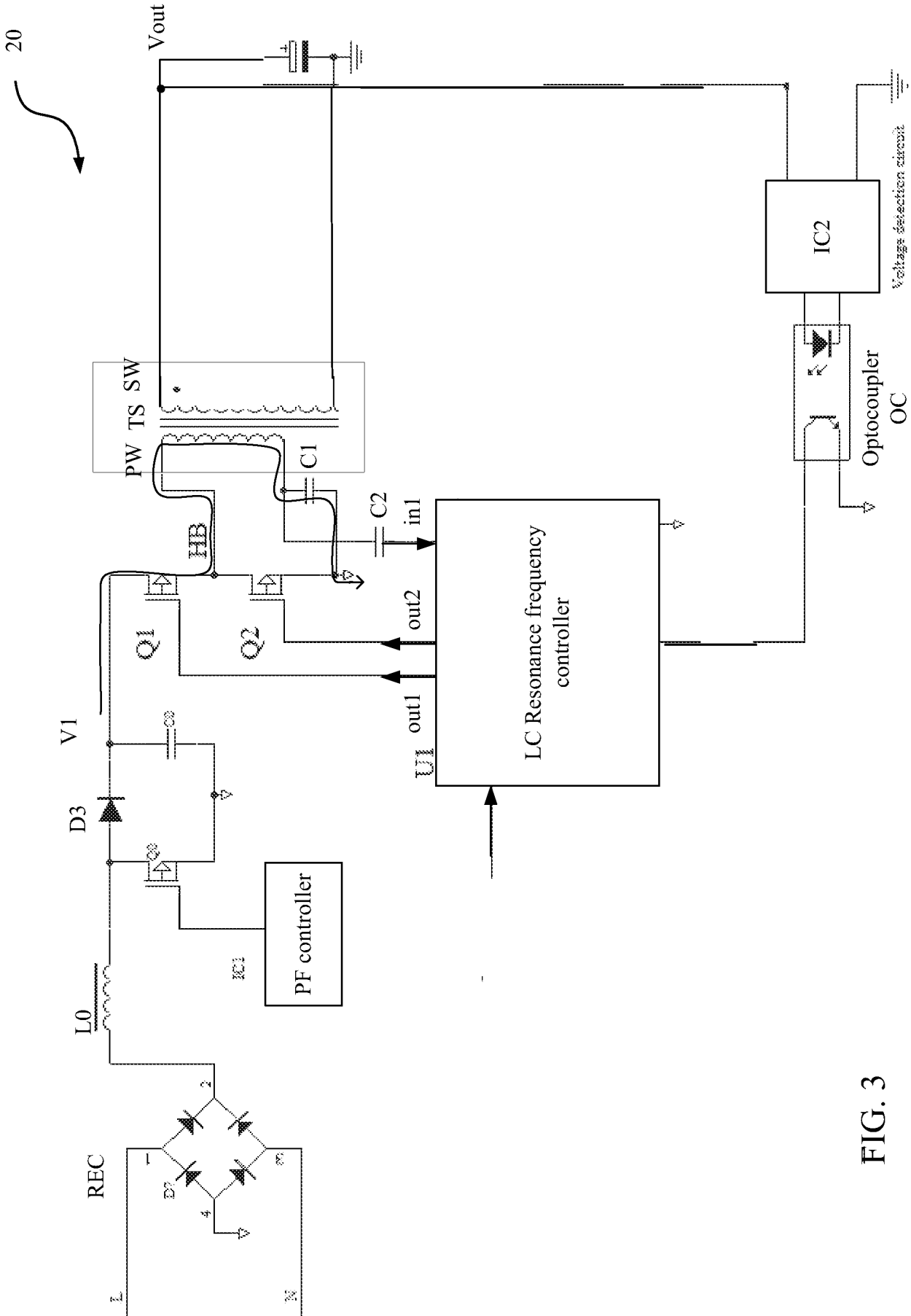


FIG. 3

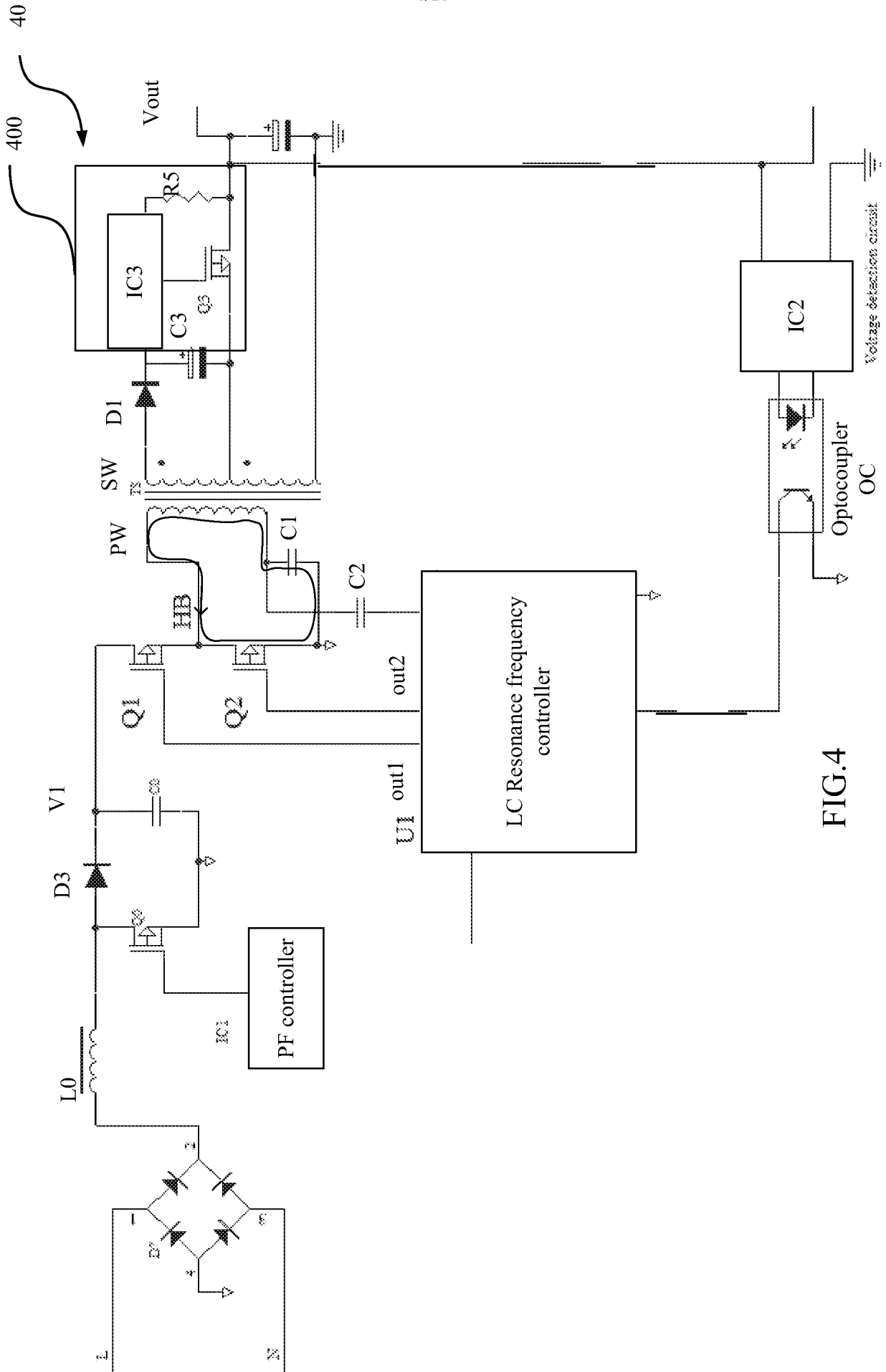


FIG.4

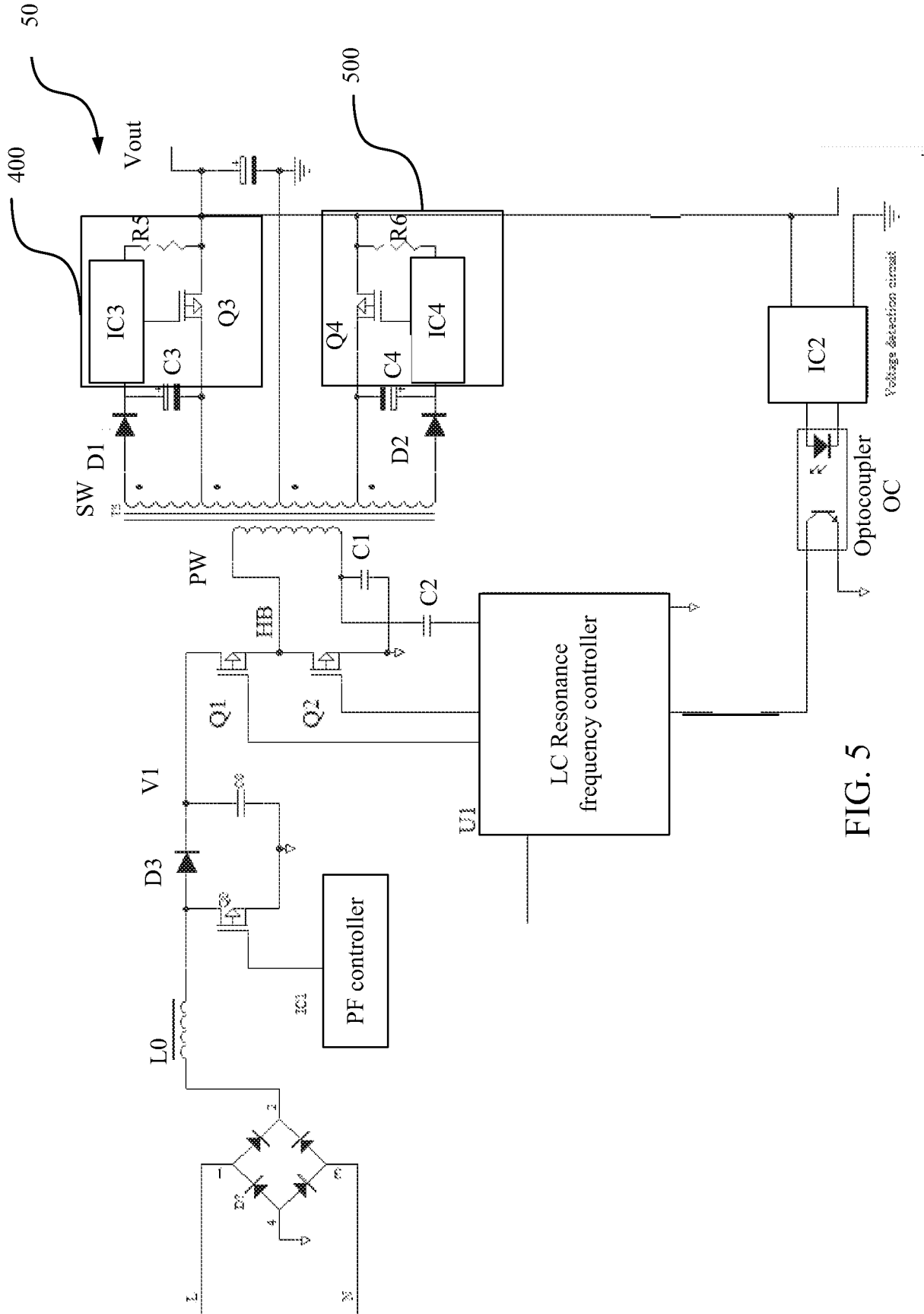


FIG. 5

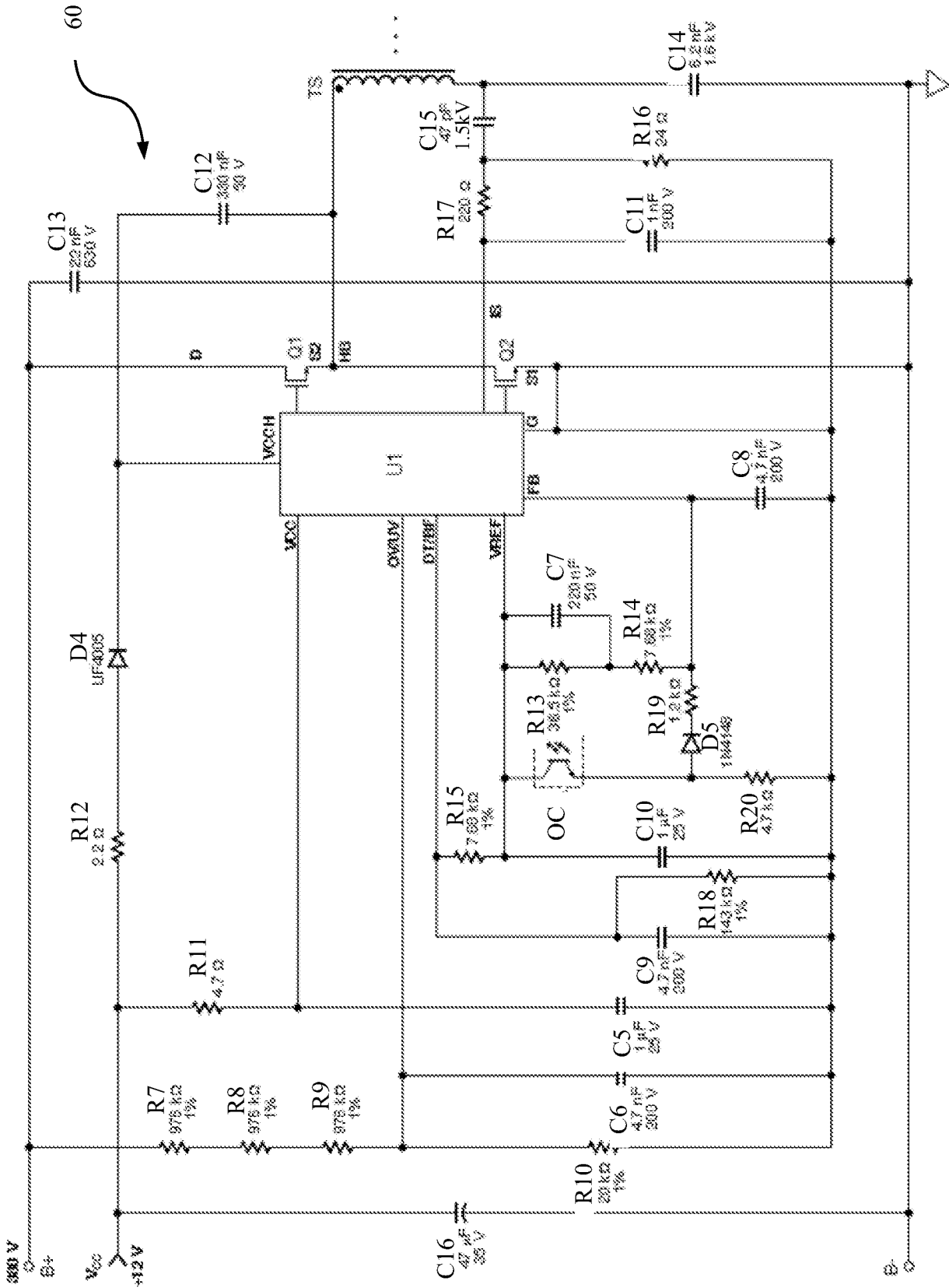
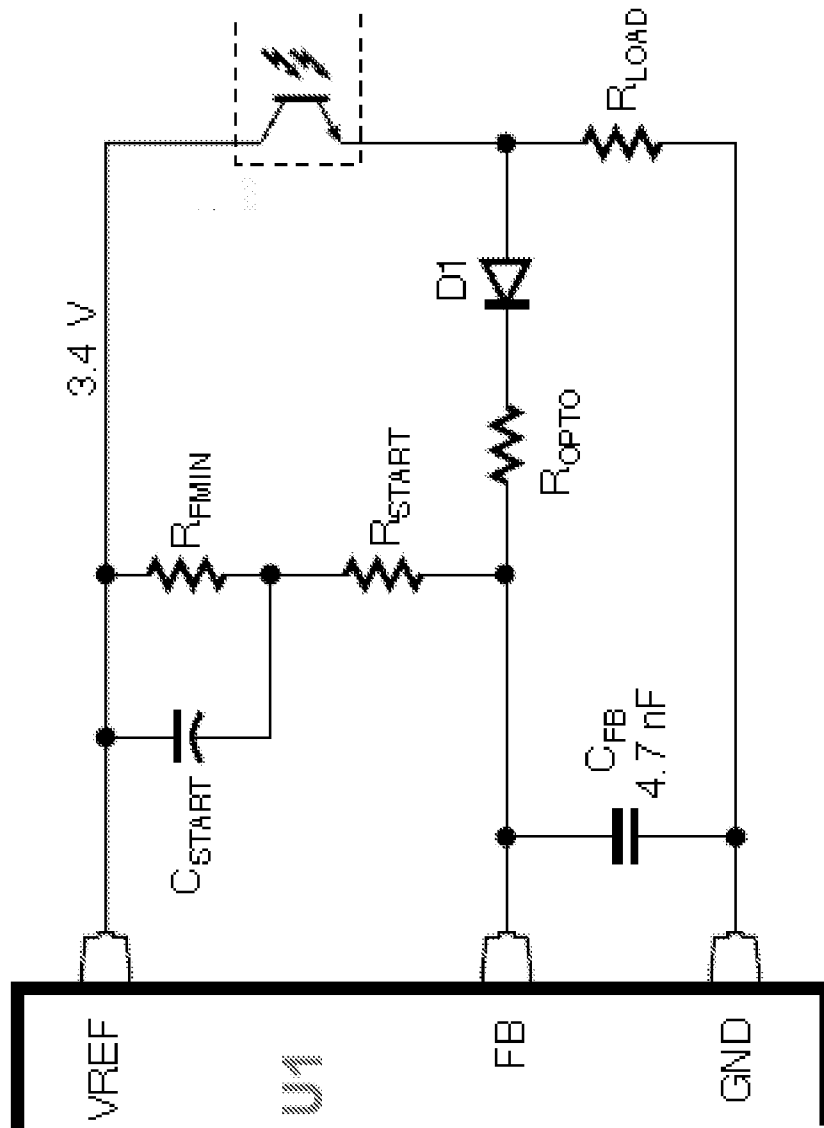
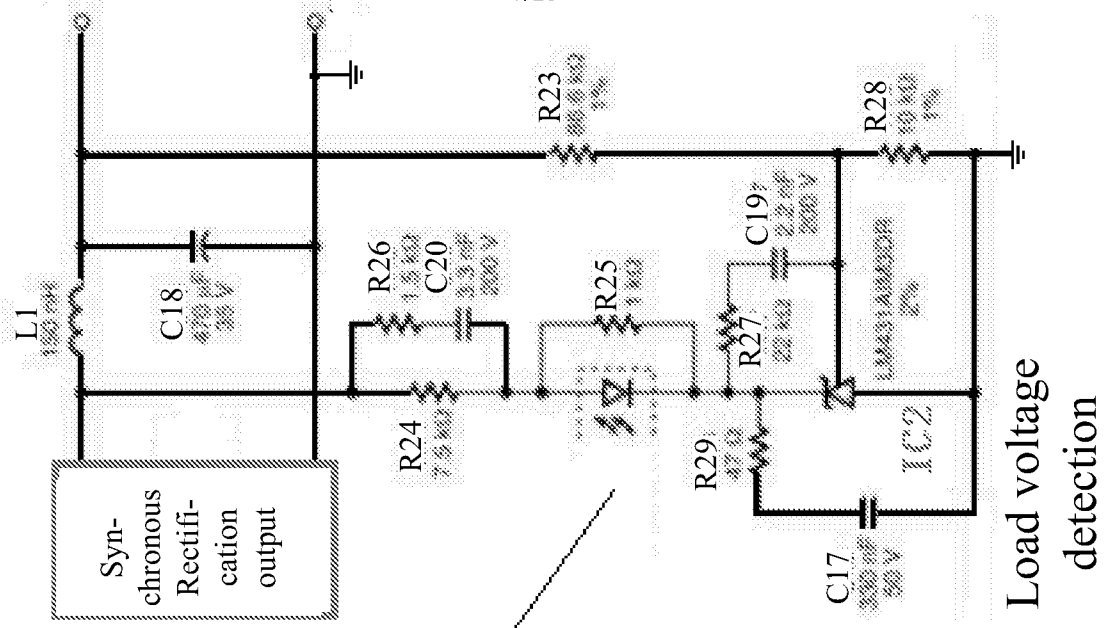


FIG. 6





load voltage feedback network

FIG. 7

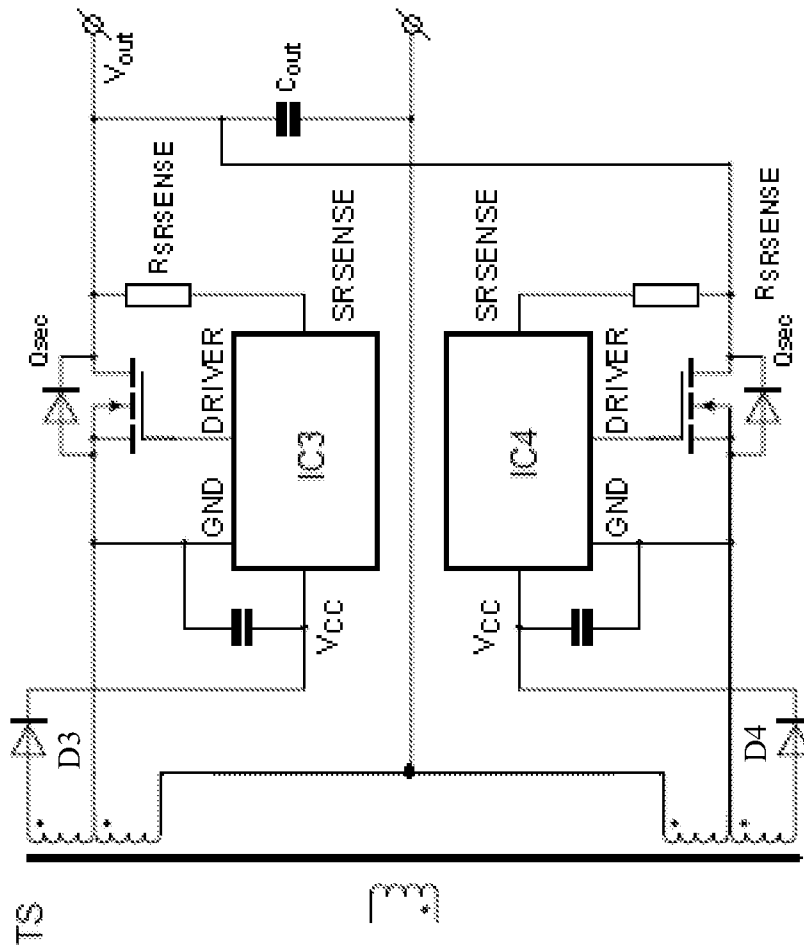


FIG. 8

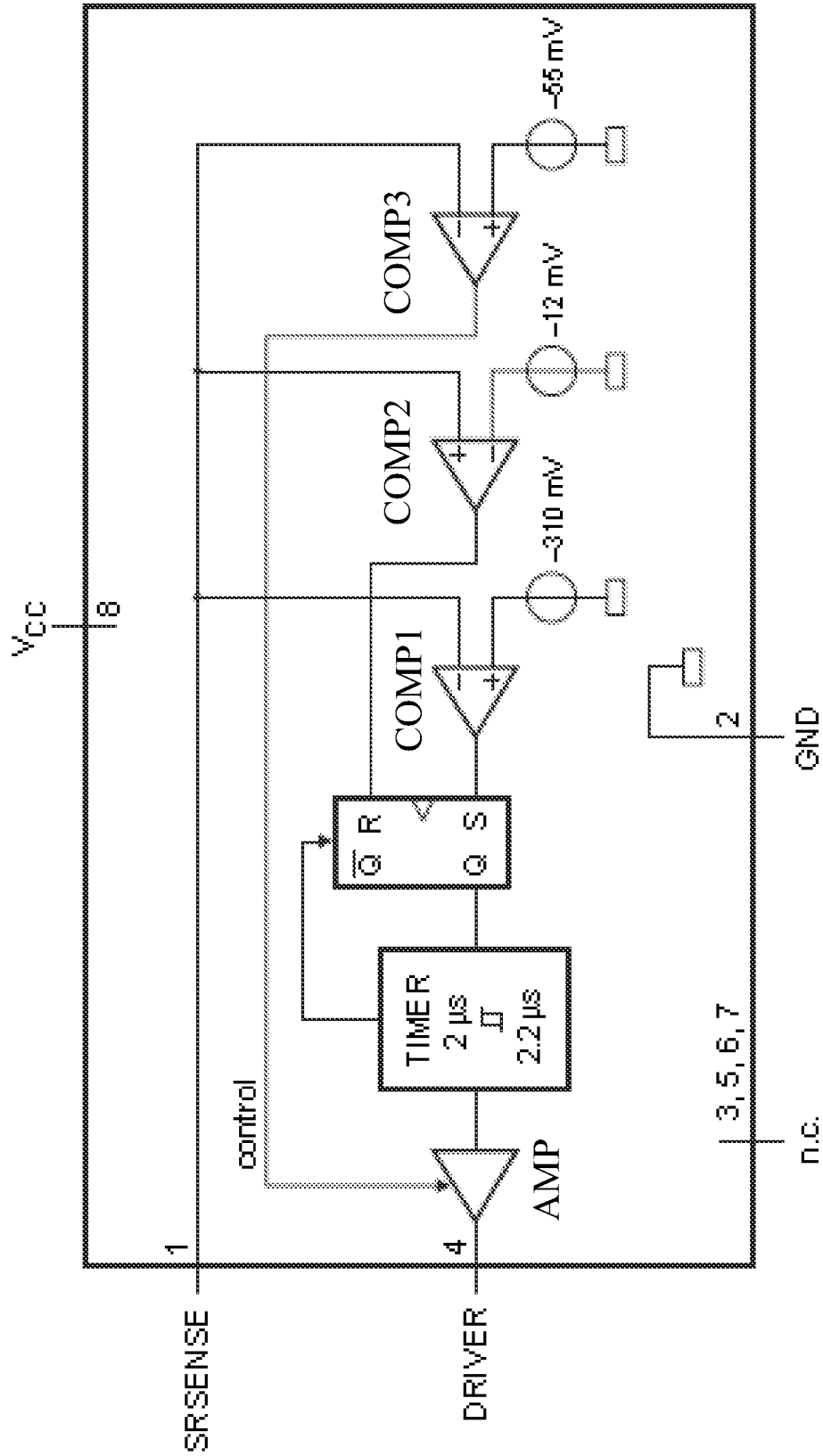


FIG. 9

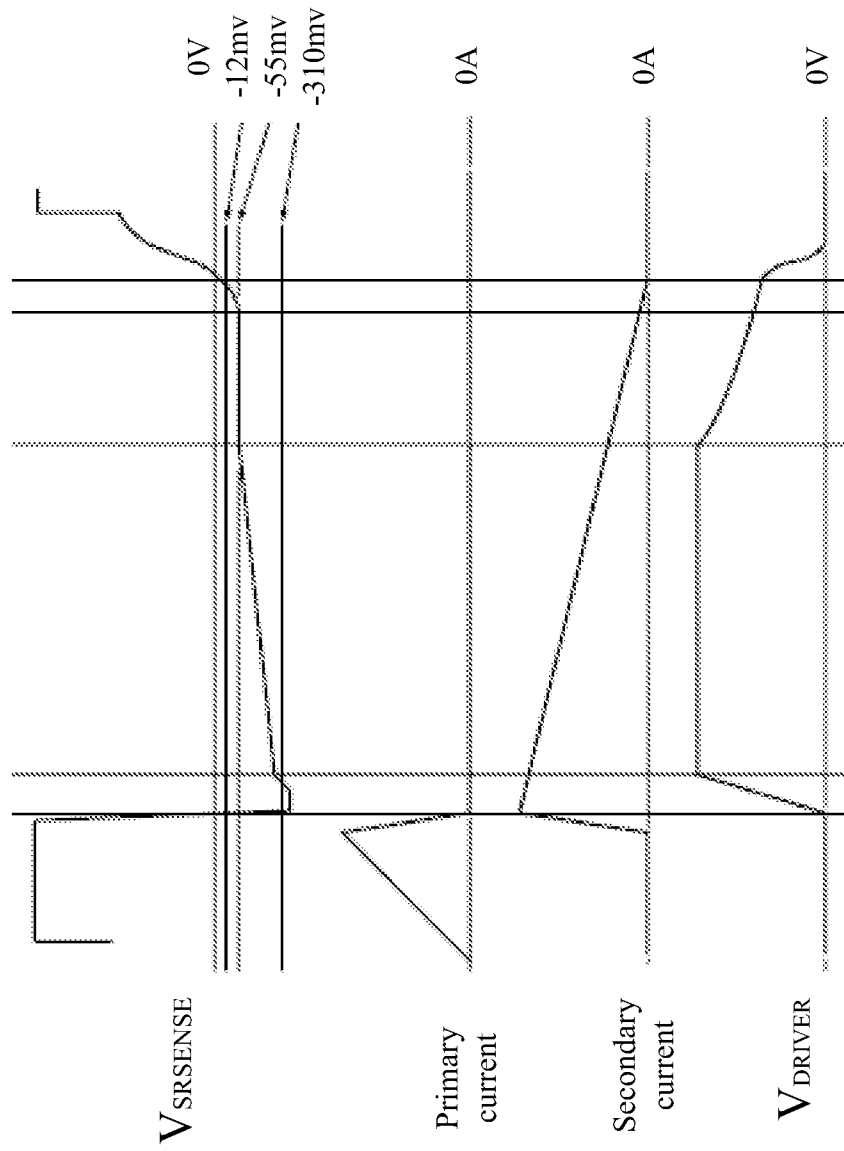


FIG. 10

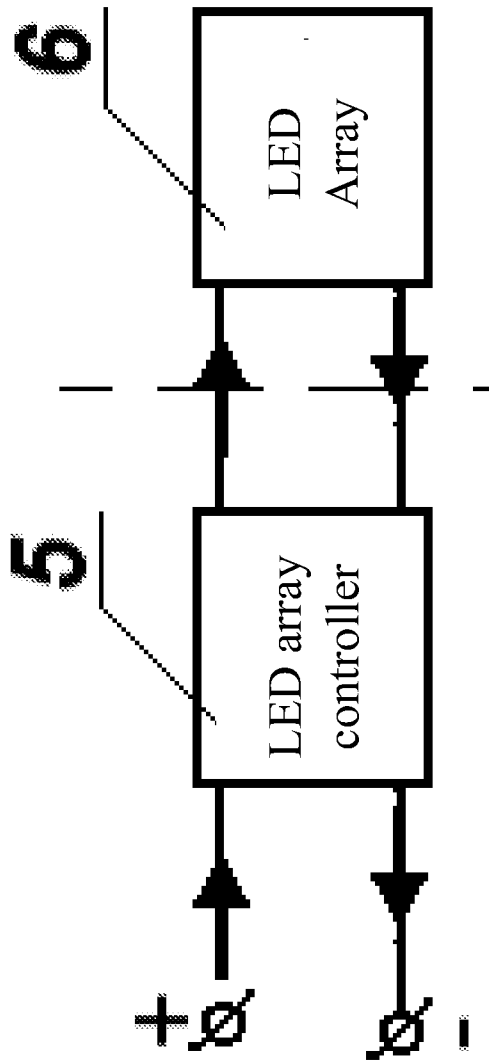


FIG. 11

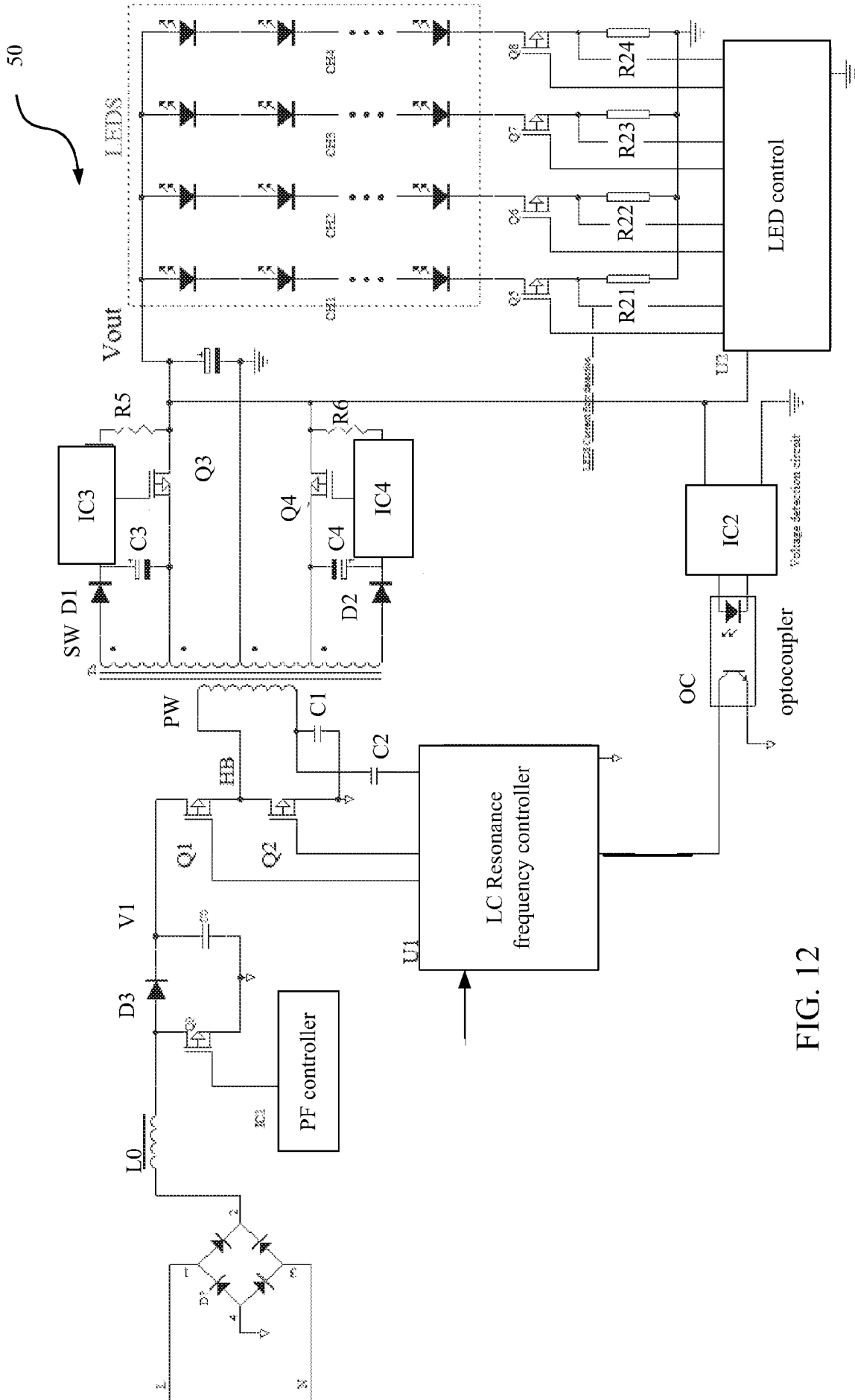


FIG. 12

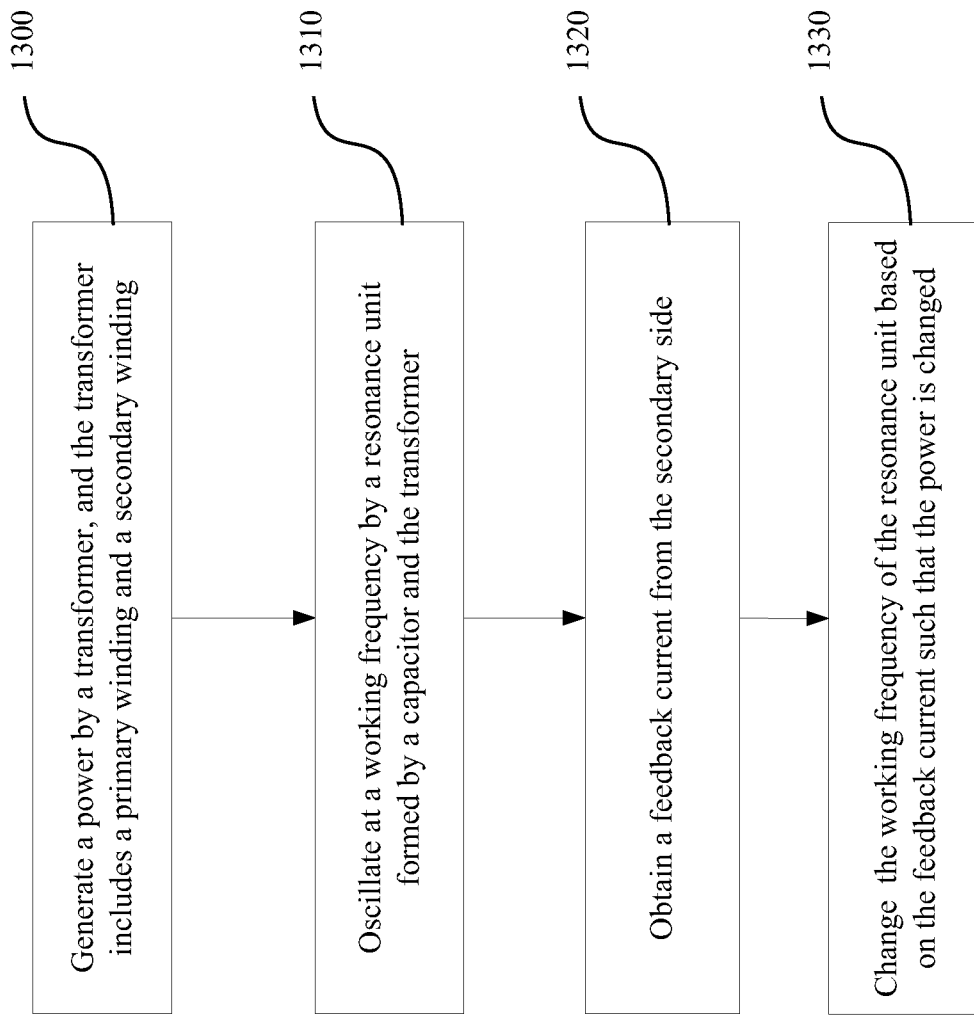


FIG. 13

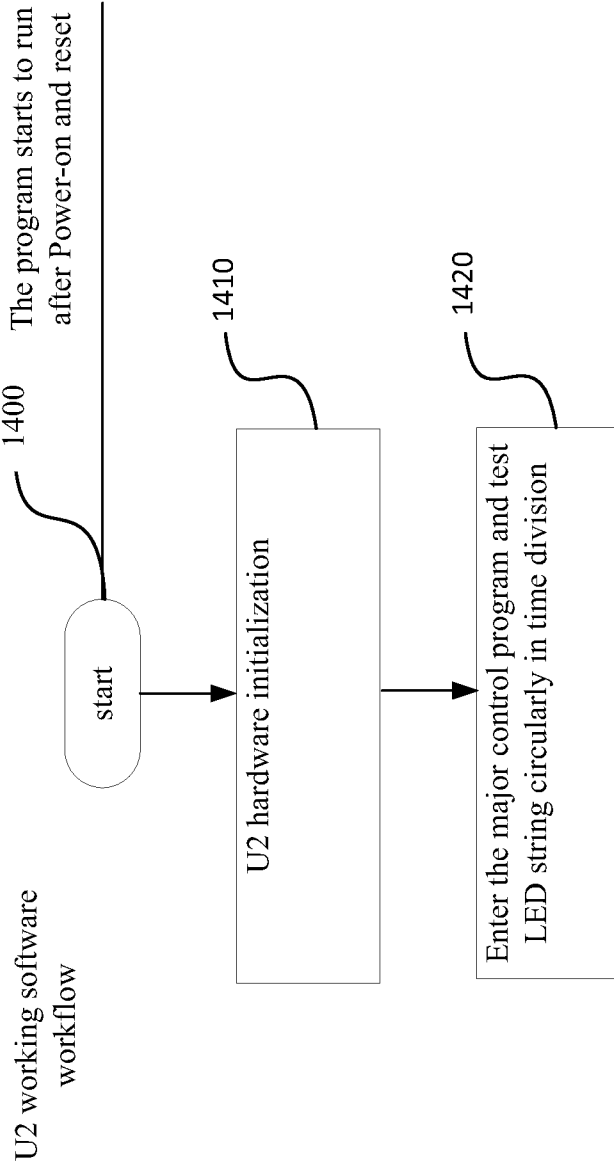


FIG. 14A



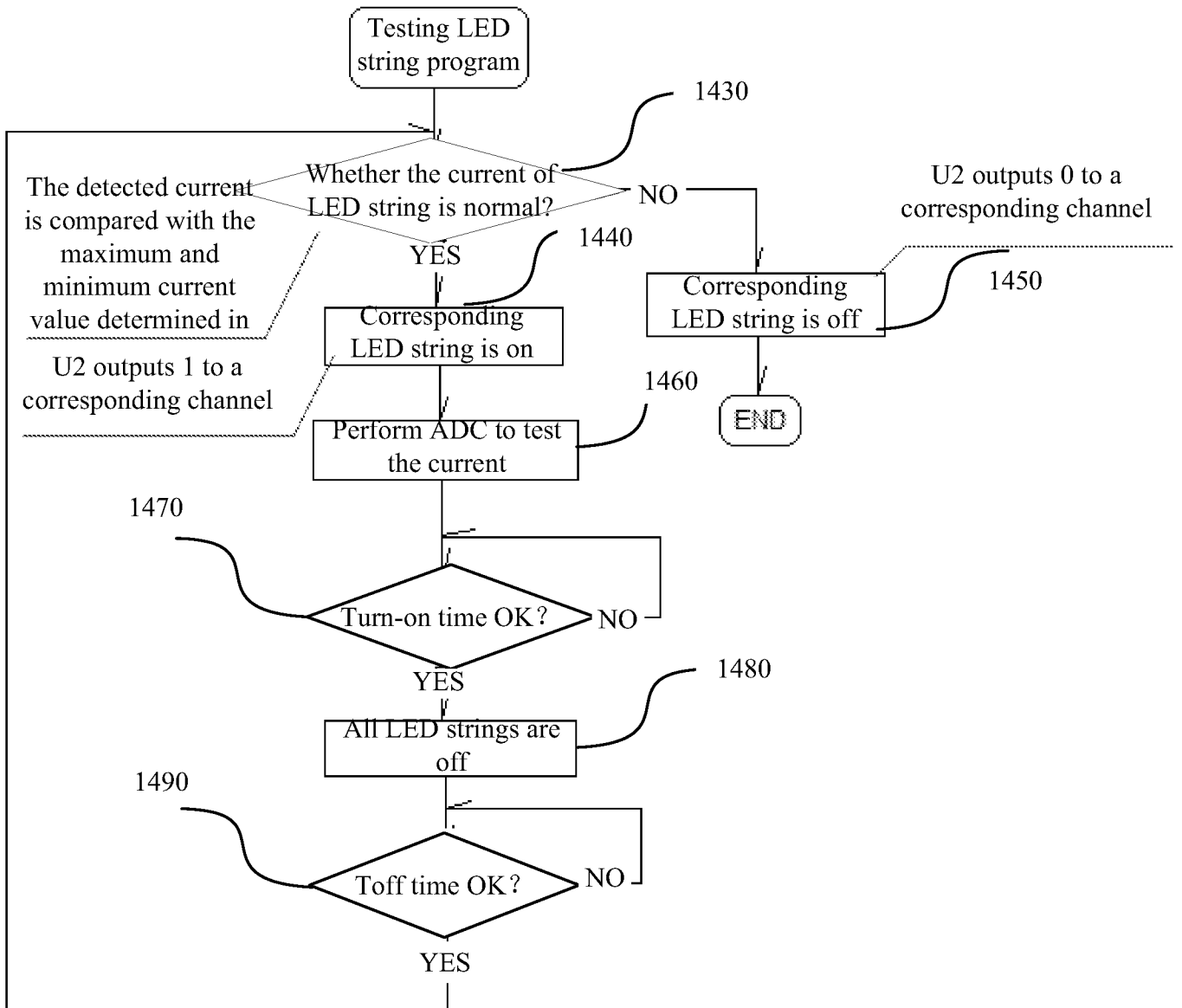


FIG. 14B

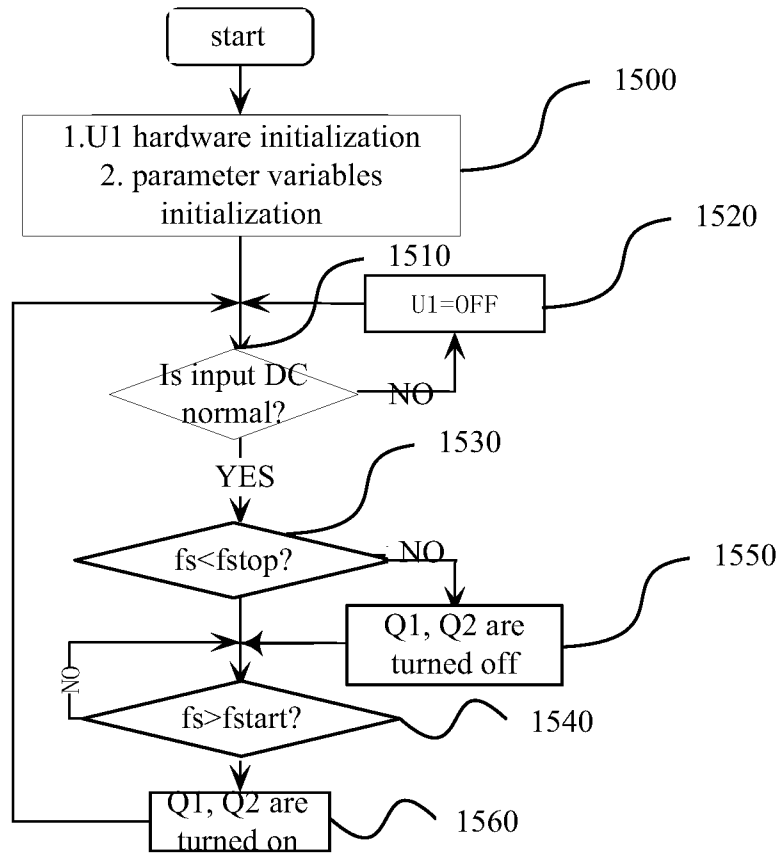


FIG. 15

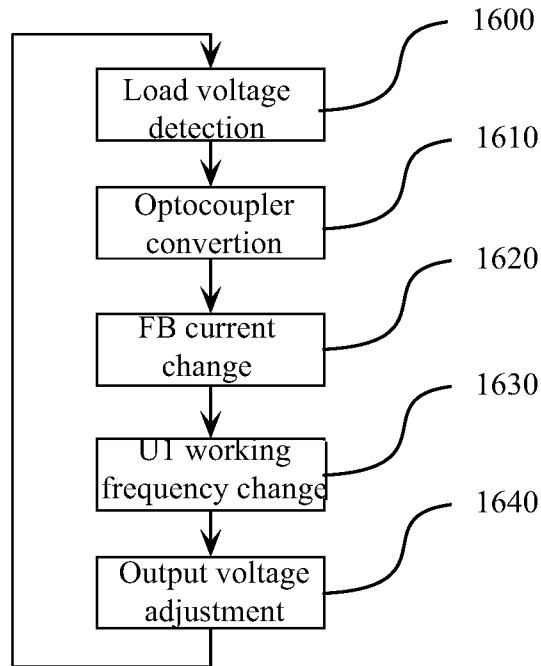


FIG. 16

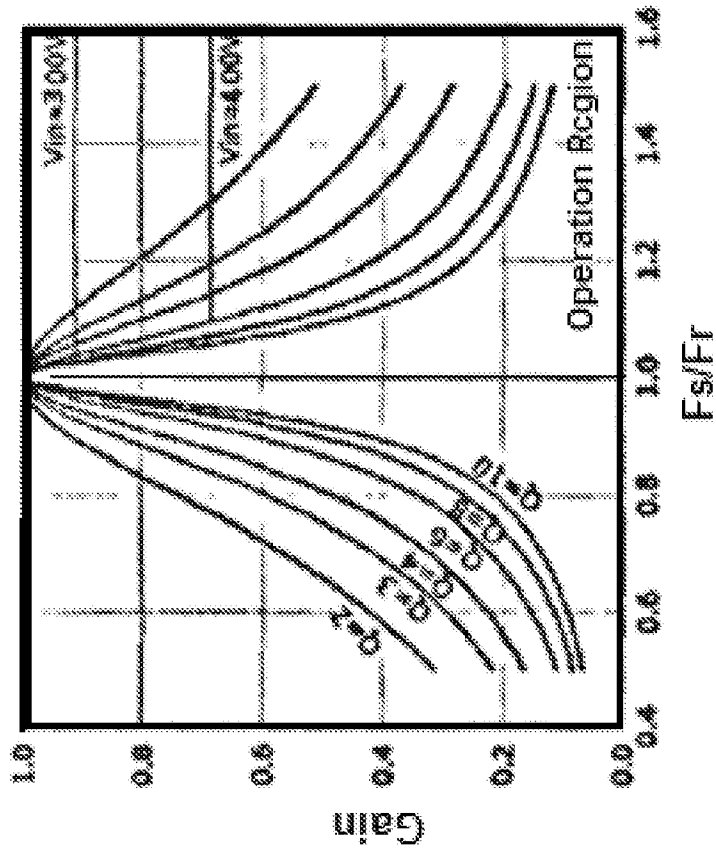


FIG. 17B

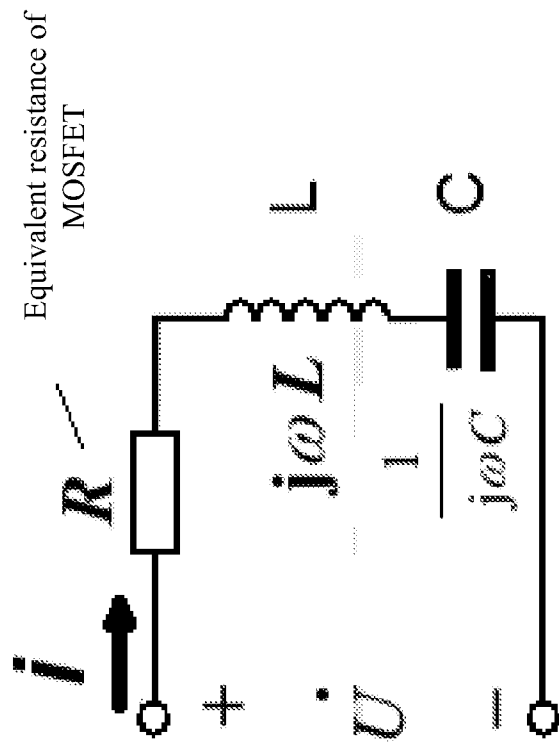


FIG. 17A

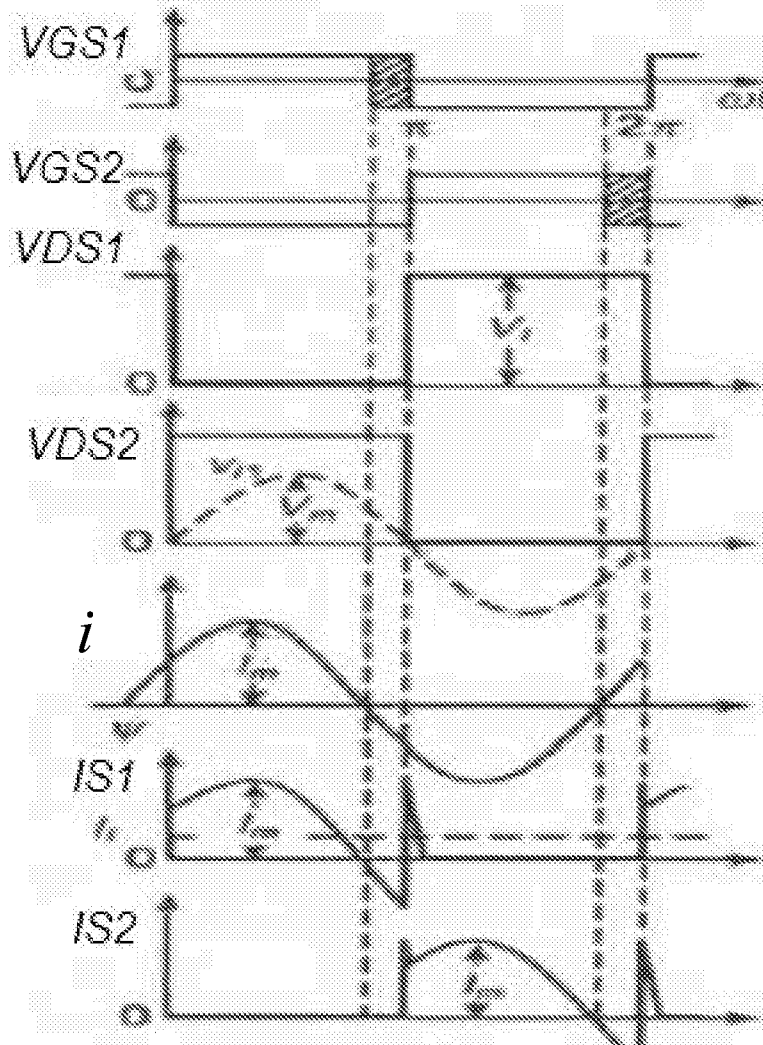


FIG. 18

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2014/084741

<b>A. CLASSIFICATION OF SUBJECT MATTER</b>		
H02M 3/325(2006.01)i; H05B 37/02(2006.01)j		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b>		
Minimum documentation searched (classification system followed by classification symbols) H02M3/-; H02M7/-; H05B37/-; G09G3/-		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) WPI, EPODOC, CNKI, CNPAT: power, convert+, transformer, halfbridge, resonan+, feedback+, current, voltage, capacit+, switch+, turn+, transistor?, FET?, temperature, heat+, thermal, detect+, sens+, LED?, light W emitting W diode		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011261592 A1 (CANON KABUSHIKI KAISHA) 27 October 2011 (2011-10-27) description, paragraphs [0023]-[0058], [0069], figures 1 and 2	1-6, 12-23, 29-34
X	CN 201278600 Y (FUGANG ELECTRONICSDONGGUAN CO., LTD. ET AL.) 22 July 2009 (2009-07-22) the abstract, description, page 4, line 10 - page 5, line 1, and figure 1	35-37
X	US 2010020578 A1 (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 28 January 2010 (2010-01-28) description, paragraphs [0028]-[0039], figures 2 and 3	1-4, 6, 12-21, 23, 29-32
X	CN 102067736 A (PANASONIC ELECTRIC WORKS CO., LTD.) 18 May 2011 (2011-05-18) description, paragraphs [0049]-[0056], [0082]-[0090], [0099]-[0110], and figures 4, 5, 7-10	1-5, 12-22, 29-33
X	CN 103797897 A (OSRAM SYLVANIA INC.) 14 May 2014 (2014-05-14) description, paragraphs [0023]-[0037], and figures 1-5, 6A, 6B	1-3, 12-20, 29-31
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search <b>23 April 2015</b>		Date of mailing of the international search report <b>21 May 2015</b>
Name and mailing address of the ISA/CN <b>STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA(ISA/CN) 6,Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China</b> Facsimile No. (86-10)62019451		Authorized officer <b>WANG,Shaowei</b> Telephone No. (86-10)82245658

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2014/084741

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 103051195 A (QINGDAO HISENSE ELECTRIC CO., LTD.) 17 April 2013 (2013-04-17) description, paragraphs [0026]-[0037], and figures 2-4	1-3, 12-20, 29-31
X	CN 102243850 A (QINGDAO HISENSE ELECTRIC CO., LTD.) 16 November 2011 (2011-11-16) description, paragraphs [0058]-[0100], and figure 2	1-3, 12-20, 29-31
X	CN 102097060 A (FUJIAN JIELIAN ELECTRONICS CO., LTD.) 15 June 2011 (2011-06-15) description, paragraphs [0021]-[0022], [0033], figures 1 and 2	1-3, 12-20, 29-31
X	CN 103813589 A (UNIVERSITY SOUTHEAST) 21 May 2014 (2014-05-21) description, paragraphs [0030]-[0032], [0051], figures 1 and 2	1-3, 12-20, 29-31
A	US 2011181205 A1 (AVERD LABS CO., LTD.) 28 July 2011 (2011-07-28) the whole document	1-34
A	CN 101340760 A (NEC LCD TECHNOLOGIES CO., LTD.) 07 January 2009 (2009-01-07) the whole document	35-37

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2014/084741

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

- [1] I: claims 1-13 direct to a driving circuit for generating and changing power, claims 14-30 direct to a lighting device comprising the driving circuit, and claims 31-34 direct to a driving method for generating and changing power.
- [2] II: claims 35-37 direct to a method of controlling LED device.
- [3] The inventions above do not include the same or corresponding special technical feature, hence, the application does not meet the requirements of unity of invention as defined in Rule 13.1 PCT.

- 1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
- 2.  As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
- 3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
- 4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

- Remark on Protest**
- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
  - The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
  - No protest accompanied the payment of additional search fees.

**INTERNATIONAL SEARCH REPORT**  
**Information on patent family members**

International application No.

**PCT/CN2014/084741**

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
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				US	8976545	B2	10 March 2015
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US	2010020578	A1	28 January 2010	US	8027174	B2	27 September 2011
				KR	20100011471	A	03 February 2010
				US	2012069603	A1	22 March 2012
				KR	100975925	B1	13 August 2010
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				EP	2302984	A1	30 March 2011
				CN	102067736	B	02 October 2013
				JP	2010021109	A	28 January 2010
				WO	2010007985	A1	21 January 2010
				US	8841863	B2	23 September 2014
				US	8841863	B2	23 September 2014
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				KR	20140051308	A	30 April 2014
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				JP	2014526229	A	02 October 2014
				US	8575849	B2	05 November 2013
				EP	2732676	A1	21 May 2014
				WO	2013012529	A1	24 January 2013
CN	103051195	A	17 April 2013	None			
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CN	102097060	A	15 June 2011	None			
CN	103813589	A	21 May 2014	None			
US	2011181205	A1	28 July 2011	US	8138688	B2	20 March 2012
CN	101340760	A	07 January 2009	US	2009015759	A1	15 January 2009
				JP	5024789	B2	12 September 2012
				JP	2009016280	A	22 January 2009
				CN	101340760	B	14 August 2013
				US	8896516	B2	25 November 2014