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An integrated circuit assembly incorporating protective caps

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Abstract

An integrated circuit assembly includes a substrate having an upper surface and a lower surface. A plurality of integrated circuit devices is positioned on the upper surface. A plurality of bond pads is positioned on the upper surface with a bond pad associated with each integrated circuit device. A plurality of protective caps is positioned on the upper surface of the substrate to enclose respective integrated circuit devices with each bond pad positioned outside the protective cap of its associated device. A plurality of protective members is positioned on the lower surface of the substrate such that each protective member is aligned with a respective protective cap. Each protective member is dimensioned to overlie the respective protective cap and associated bond pad to protect the integrated circuit devices and associated bond pads when the substrate is separated by a process applied to the lower surface of the substrate.

Figure 22

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AN INTEGRATED CIRCUIT ASSEMBLY INCORPORATING PROTECTIVE CAPS

Technical Field

This invention relates to the moulding and application of protective caps to microelectronic semiconductor chips on a wafer scale as opposed to application on an individual chip basis. More particularly the invention relates to the moulds used to form the protective caps.

Background Art

Semiconductor chips are normally packaged in a protective layer or layers to protect the chip and its wire bonds from atmospheric and mechanical damage. Existing packaging systems typically use epoxy moulding and thermal curing to create a solid protective layer around the chip. This is normally carried out on individually diced chips bonded to lead frames and so must be done many times for each wafer. Alternative methods of packaging include hermetically sealed metal or ceramic packages and array packages such as ball grid array (BGA) and pin grid array (PGA) packages. Recently wafer scale packaging (WSP) has started to be used. This is carried out at the wafer stage before the chips are separated. The use of moulding and curing techniques subjects the wafer to both mechanical and thermal stresses. In addition the protective cap so formed is a solid piece of material and so cannot be used for MEMS devices, since the MEMS device would be rendered inoperable by the polymer material. Existing packaging systems for MEMS devices include thematically sealed packages for individual devices, or use silicon or glass wafer scale packaging, both of which are relatively high cost operation.

Disclosure of the Invention

According to a first aspect of the invention, there is provided an integrated circuit assembly which includes

a substrate having an upper surface and a lower surface;

a plurality of integrated circuit devices positioned on the upper surface;

a plurality of bond pads positioned on the upper surface with a bond pad associated with each integrated circuit device;

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a plurality of protective caps positioned on the upper surface of the substrate to enclose respective integrated circuit devices with each bond pad positioned outside the protective cap of its associated device; and

a plurality of protective members positioned on the lower surface of the substrate such that each protective member is aligned with a respective protective cap, each protective member being dimensioned to overlie the respective protective cap and associated bond pad to protect the integrated circuit devices and associated bond pads when the substrate is separated by a process applied to the lower surface of the substrate.

The substrate may be a silicon wafer that is capable of being separated by etching, the protective member being of an etch-resistant material.

Each protective member may be a protective cap. The protective caps on the upper and lower surfaces of the wafer may be moulded of a thermoplastic material.

According to a second aspect of the invention, there is provided an integrated circuit assembly which includes

a substrate having an upper surface and a lower surface;

at least one integrated circuit device positioned on the upper surface;

a bond pad positioned on the upper surface to provide electrical communication with the integrated circuit device;

a protective cap positioned on the substrate to enclose the integrated circuit device with the bond pad positioned outside the protective cap; and

a protective member positioned on the lower surface of the substrate such that the protective member is aligned with the protective cap, the protective member being dimensioned to overlie the protective cap and bond pad to protect the integrated circuit device and bond pad when the substrate is separated by a process applied to the lower surface of the substrate.

In one broad form the invention provides pair of moulds formed substantially of silicon or silicon alloy for moulding a sheet of thermoplastic material into an array of microstructures, each of the moulds being a substantially planar wafer having a working face and rear face, the moulds each having one or more micro fabricated recesses in their working faces which, when the working faces are placed face to face, define at least one cavity between the two moulds, wherein the recesses on the moulds are configured such that the moulds only contact each other on the working faces, when the working faces are placed face to face.

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In plan view the first mould may have at least one first recess in the respective working face for each cavity and the second mould may have at least one first groove in the respective working face for each cavity, such that when the two moulds are in use, the at least one first recess defines a central portion of the cavity and the at least one groove defines a perimeter wall portion of the cavity extending from the edges of the central portion.

Preferably the at least one first recess is, in plan view, generally rectangular.

One of the moulds may have a recess therein having a base and one or more pillars of mould material extending from the base to the plane of the working face.

One of the moulds may have a recess therein having a base and wherein at least part of the base is concave or convex with respect to the respective mould's working face.

The other of the moulds may have a second recess therein having a second base and part of the second base may be concave or convex with respect to the respective mould's working face.

When two moulds are used with concave or convex portions, a lens shaped cavity may be defined.

The moulds are preferably formed of a semiconductor material, such as silicon.

The working surfaces of the moulds have preferably been prepared and the recesses have been formed using conventional lithography and deep silicon etching techniques.

In use, a spacer may be provided between the two moulds such that the working faces of the moulds do not contact each other.

Brief Description of the Drawings

Figure 1 shows a prior art method of forming protective caps on semiconductor chips.

Figure 2 shows a cross section of a prior art packaging made according to the figure 1 method.

Figure 3 shows a cross section of a prior art packaging of a MEMS device.

Figure 4 shows a cross section through a MEMS device packaged according to the invention.

Figure 5 shows a possible device for forming moulded caps;

Figure 6 shows method of applying caps formed using the device of figure 5a to a silicon wafer;

Figure 7 shows the wafer and caps of figure 6 bonded together

Figure 8 symbolically shows a method for applying moulded caps to a silicon wafer according to the invention;

Figure 9 shows the wafer and caps of figure 8 bonded together;

Figure 10 shows an exploded cross sectional view of a device for forming the protective caps.

Figure 11 shows an exploded perspective view of the device of figure 10.

Figure 12 shows a cross sectional view of the device of figure 10 at the commencement of moulding.

Figure 13 shows the device of figure 10 after moulding has finished and just before one side of the mould is released from the other side.

Figure 13a shows an expanded view of part of figure 13.

Figure 14 shows a perspective view of the figure 10 device corresponding to figure 13.

Figure 15 shows a cross sectional side view of the device after one of the moulds has been partially removed.

Figure 16 shows a cross sectional side view of the device after one of the moulds has been fully removed.

Figure 17 shows a cross sectional side view of the device undergoing an etch.

Figure 18 shows a cross sectional side view of the device after undergoing an etch.

Figure 19 shows a cross sectional side view of the device at the commencement of application to a wafer and removal of the second mould.

Figure 20 shows a cross sectional side view of a wafer after application of the caps.

Figure 21 shows a cross sectional side view of a series of chips after singulation of the wafer.

Figure 22 shows a cross sectional side view of a wafer with caps applied to both sides, before singulation of the wafer.

Best Mode of Carrying out the Invention

Referring to figures 1 and 2 there is show a prior art method of forming protective caps on semiconductor wafers on a wafer scale. A semiconductor wafer 10 is clamped against a mould 12 having cavities 14 formed therein and a liquid polymer material 16 is injected into the cavities 14. The polymer material sets to form solid protective caps 18.

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The wafer is then singulated using a wafer saw. This technique is not applicable to wafers having MEMS devices formed thereon as the liquid polymer material will surround the MEMS devices and stop them from working.

Figure 3 shows the present prior art technique for protecting MEMS devices. The MEMS chip 20 including the MEMS devices 24, shown symbolically, is bonded to a silicon wafer 26. This may be carried out at the individual chip stage or at the wafer stage. The wafer 26 is typically etched using a crystallographic anisotropic etch using an etchant such as KOH to form a series of recesses 28 which correspond to the locations of the MEMS devices. The wafers 26 are carefully aligned with the MEMS wafer 20 and bonded thereto. While this can be an effective means of packaging MEMS devices, it is expensive as it requires an extra silicon (or sometimes glass) wafer, which must be etched to form the cavities.

Figure 4 shows a MEMS wafer 30 having surface MEMS 32 formed thereon. A hollow protective cap 34 of thermoplastic material made and bonded to the wafer 30 according to the invention is provided so as to form a mechanical and atmospheric protective barrier for the MEMS devices. The cap 34 forms a cavity 36 with the wafer to allow the MEMS device(s) to operate.

The use of moulded thermoplastic hollow caps offers the possibility of providing inexpensive packaging. However, conventional techniques do not provide the required accuracy and thermal stability required for micro fabricated devices.

Figures 5 to 7 show a possible technique for packaging a semiconductor wafer 40 having a number of groups 42 of micro fabricated devices 44, shown symbolically, formed on or in an upper surface 46.

An array of caps 48 is formed using conventional injection moulding methods and steel mould tools 50 & 52. The caps are supported on a sprule 54 at the same nominal spacing as the groups 42. Using this method will almost invariably lead to misalignment with resulting destruction of MEMS devices, as shown in figure 20. In figure 20 the cap 48a has been aligned correctly with its group of MEMS devices 42a. However the spacing between the caps is greater than the spacing of the groups so that cap 48b is not aligned correctly, but does not destroy any of the MEMS devices of its respective group 42b. However, the caps 44c & d are sufficiently misaligned that the perimeter walls of the caps overlay one or more of the MEMS devices 44, destroying their functionality.

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This misalignment can be the result of a number of actors, including differential thermal expansion of the sprule material compared to the silicon wafer, non rigidity of the moulded components and the lack of machinery designed for accurate alignment and bonding of polymers to wafers using these techniques.

A solution is to use tools which have the same coefficient of thermal expansion as the wafer, such as silicon and figures 8 & 9 symbolically show a technique using a silicon tool 60 to hold an array of thermoplastics caps 60 as the caps are bonded to the silicon wafer 40. Since the tool 60 is formed of the same material as the wafer 40, changes in temperature will not result in changes in alignment; the spacing of the caps 60 will change by the same amount as the spacing of the groups 42 of MEMS devices 44. Thus, when bonded, all of the caps will be correctly aligned, as shown in figure 9. Additionally there is much experience in working silicon to the required accuracy.

Forming Caps

Figures 10 to 16 schematically show a first system for creating and applying hollow protective caps to wafers, preferably semiconductor wafers.

Figure 10 shows a moulding system 100 for forming the hollow protective caps shown in figure 4 which may be used with MEMS devices or any other micro fabricated device. The moulding system 100 includes two silicon wafers 102 & 104. The upper wafer 102 has been processed using conventional lithography and deep silicon etching techniques to have a series of recesses 106 in its lower surface 108. The lower wafer 104 has been similarly processed so that its upper surface 110 has a series of grooves 112 which align with edges of the recesses 106. The recesses 106 and grooves 112 are sized for the chip size of the wafer to be processed and repeat at centres corresponding to the repeat spacing on the wafer. In the embodiment shown the protective caps are designed for a MEMS inkjet printhead and so are very long relative to their width in plan view. The recesses are rectangular, although the ends of the recesses are not shown. The ends of the grooves 112 are not shown but it is to be understood that the grooves 112 at each side of each recess are in fact one groove which has a rectangular shape in plan view.

The grooves 112 for adjacent caps define a portion 114 of material which has not been etched. Similarly adjacent recesses 106 define a portion 116 of material which has not been etched. These portions of material 114 & 116 align with each other and when the two wafers are pressed together, the two wafers contact each other at these portions 114 & 116.

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The two surfaces have been etched so that the groove 112 for the perimeter of the cap is all in the lower wafer 104 and the recess 104 for the central portion is all in the upper wafer 102.

It is not essential that the mould wafers only contact on surfaces which have not been etched. Nor is it essential that the central portion is defined by a recess in only one mould or that the perimeter walls be defined by a groove or recess in only one mould. The effective split line between the moulds may be located at any position desired and need not be planar. However, planarity of the split line will typically simplify fabrication of the moulds.

The assembly 100 also includes an upper release or eject wafer 118 and a lower release or eject wafer 120. These upper and lower release wafers are silicon wafers which have been processed utilizing conventional lithography and deep silicon etching techniques to have a series of release pins 122 and 124 respectively. The upper and lower mould wafers 102 & 104 are formed with corresponding holes 126 & 128 respectively which receive the pins 122 & 124. The upper holes 126 are located generally toward the centre or axis of each recess 106 whilst the lower holes 128 are located in the grooves 112. However the location of the holes 126 and 128 is not especially critical and they may be placed as required for ejection of the moulded caps.

The release pins 122 & 124 have a length greater than the depth of the corresponding holes. When the free ends of the pins 122 align with the inner ends of the holes 126, there is a gap 130 between the upper mould wafer 102 and the upper release wafer 118. In this embodiment the length of the lower pins 124 is the same as the thickness of the lower mould wafer 104. However the length of the pins 124 may be greater than the thickness of the wafer or it may be less. When the length of the pins 124 is less than the maximum thickness of the lower wafer 104 it needs to be greater than the depth of the holes 128, i.e. at least the reduced thickness of the wafer 104 at the grooves 112. The lower wafers 104 and 120 are positioned with the pins 124 part way inserted in the holes 128 but not extending beyond the holes 128 into the grooves 112 and with a gap 132 between the two wafers. The pins 124 preferably extend to be flush with the ends of the holes so as to form a substantially planar base to the groove 112.

The thickness of the mould and release wafers is about 800 microns whilst the gaps 130 and 132 are of the order of 10 to 100 microns in thickness. However this is not critical.

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The mould tools are preferably etched using cryogenic deep silicon etching rather than Bosch etching as to produce a smoother etch. Bosch etching produces scalloping of etched side walls, such as the side walls of the pin and cap recesses. The scalloping makes the release of the moulds from the moulded material more difficult. In comparison, using a cryogenic etch results in much smother etched walls, with easier mould release.

A sheet 134 of thermoplastic material of about 200 to 500 microns in thickness is placed between the two wafers 102 & 104 and the assembly is placed in a conventional wafer bonding machine, such as an EV 501, available from Electronic Visions Group of Sharding, Austria.

The assembly is mechanically pressed together in the machine but it will be appreciated that the mould wafers may be urged toward each other to deform the thermoplastic sheet by applying an above ambient pressure to the gaps 130 & 132. Alternatively other means may be used.

The sheet 134 may be heated by conduction but is preferably heated by radiation and preferably by using infrared radiation, as indicated by arrows 136 in figure 12. A combination of conductive and radiant heating may be used. The mould and release wafers 102 &104 and 118 & 120 respectively are formed of silicon, which is substantially transparent to infrared light of a wavelength in the range of about 1000 nm to about 5000 nm. The material 134 chosen either intrinsically absorbs light within this wavelength range or is doped so as to absorb light within this wavelength range. If the material 134 does not intrinsically absorb within this range, a suitable dopant is "carbon black" (amorphous carbon particles) which absorbs light at these wavelengths. Other suitable dopants may be used.

The sheet 134 is placed between the two mould wafers and exposed to infrared light at a suitable wavelength, as indicated by arrows 136. The infrared radiation is preferably supplied from both sides of the wafers and the sheet 134 to provide symmetrical heating, but this is not essential and the infrared radiation may be supplied from only one side. Because the silicon wafers are transparent to the infrared radiation, the infrared radiation passes through the wafers and is absorbed by the sheet 134. After heating to a suitable temperature the mould wafers may then be urged together to deform the sheet 134. The wafers may be pressed together whilst the sheet 134 is being heated rather than waiting for the sheet 134 to be fully heated, particularly if conductive heating is being used. If a material other then silicon is used heating of the sheet 134 may be achieved using

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electromagnetic radiation at other wavelengths to which the material used is substantially transparent.

When processed in a wafer bonding machine the sheet 134 is moulded to the shape of the cavity defined by the recess 106 and the groove 112. The material is also substantially squeezed out of the gap between the two portions 114 & 116, as indicated by arrows 142 in figure 13a, to form a series of caps 138

As previously mentioned, the moulding wafers 102 & 102 are formed using conventional lithography and deep silicon etching techniques. The accuracy of this process is dependant on the lithography and the resist used. The etch selectivity of silicon versus resist is typically between about 40:1 and about 150:1, requiring a resist thickness for a 500 μm thick etch of between about 15 μm and 4 μm respectively. Using a contact or proximity mask, critical dimensions of around 2 μm can be achieved. Using steppers, electron beam or X-ray lithography the critical dimensions can be reduced to less than a micron. Thus the material 134 may be squeezed out totally from between the portions 114 & 116, totally separating the adjacent caps 136. Alternatively a thin layer 140 up to about 2 microns thick may be left between the portions 114 & 116 between adjacent caps 136 due to the variation in position of the relative surfaces due to manufacturing tolerances.

It is not essential that the mould wafers or the release wafers be made of semiconductor materials or that they are processed using conventional lithography and deep silicon etching methods. Other materials and methods may be used if desired. However, the use of similar materials to the semiconductor wafers provides better accuracy since temperature changes have less effect. Also lithography and deep silicon etching methods are well understood and provide the degree of accuracy required. In addition, the one fabrication plant may be used for production of both the semiconductor devices and the moulding apparatus.

It will be appreciated that the two mould wafers 102 & 104 will need to be shaped so that there is space for the material to move into as it is squeezed out from between the two wafers.

After forming of the protective caps 138 it is preferred to remove the lower mould and release wafers 104 & 120 whilst leaving the material 134 still attached to the upper mould wafer 102. A vacuum is applied to the gap 132 between the lower mould and release wafers. The release wafers 118 & 120 are mounted in the assembly so as to be immovable whilst the mould wafers 102 & 104 are movable perpendicular to the general plane of the

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wafers. Accordingly, the lower mould wafer 104 is drawn downwards to the release wafer 120. The pins 124 of the release wafer 120 firmly press against the material 134 and so retain the material 134 in position and prevent it moving downwards with the lower mould wafer 124. The configuration of the assembly 100 after this stage is shown in figure 15.

The lower release wafer 120 now only contacts the material 134 by pins 124 and so it is now relatively easy to remove the lower release wafer 120 from contact with the material 134 without dislodging the material from the upper mould wafer 102. This is done and the assembly is then in the configuration shown in figure 16, with the material 134 exposed for further processing and attachment to a wafer.

Whilst still attached to the upper mould, the sheet 134 is then subject to an etch, preferably an oxygen plasma etch, from below, to remove the thin layer 140 of material, as shown in figure 17. The etch has little effect on the rest of the material due to the significant greater in thickness of the rest of the material. The etched assembly is shown in figure 18.

The assembly is then placed over a wafer 144 having a number of chips formed on the wafer. Each chip has a plurality of MEMS devices 146. The components are aligned and then placed in a conventional wafer bonding machine, such as an EV 501 to bond the caps 138 to the wafer. The array of chips is positioned so that each cap overlays part or all of a chip. The devices are shown symbolically and may be MEMS devices, MOEMS devices, other micro fabricated devices, passive electronic elements or conventional semiconductor devices.

The assembly is removed from the wafer bonding machine and a vacuum is then applied to the upper gap 130 so as to draw the upper mould wafer 102 up toward the upper release wafer 118. Similar to the release of the lower mould wafer, the caps 138 are held in place by the pins 122 of the upper release wafer. Thus the chance of accidental detachment of any of the caps from the wafer due to the act of removing the upper mould wafer is reduced, if not totally prevented.

The wafer 144 is now in a state where each chip is protected by a discrete cap 138. The wafer can then be singulated into individual die. If the chips are arranged in a regular array, the conventional methods of wafer singulation – sawing or scribing may be used. However, if the separation lines between chips are not regular or if the chips are too fragile for sawing or scribing, deep reactive ion etching (DRIE) may be used to singulate the wafers. Although DRIE is much more expensive than wafer sawing, this is moot if the wafer already required through wafer deep etching, as is the case with an increasing number

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of MEMS devices. If etching is used, the wafer 144 is next subject to a deep silicon etch in an etching system, such as an Alcatel 601 E or a Surface Technology Systems Advanced Silicon Etch machine, to separate the wafer 144 into individual packages. This etch is carried out at a rate of about 2 to 5 microns per minute and may be applied from either the cap side of the wafer or the bottom side of the wafer. The etch is highly anisotropic (directional) so there is relatively little etching of silicon sideways of the direction of the etch. If the etch is applied from the caps side, the caps 138 act as masks and only the silicon material between the caps is etched. The etching continues until all the silicon material between individual chips is removed, thereby separating the chips 148 for subsequent processing. If the etch is applied from below, a separate mask will need to be applied to the bottom surface of the wafer.

Any silicon exposed to the direction of the deep etch at the separation stage will be etched away. Thus if the etch is from the top (cap) side any exposed silicon which needs to be retained, such as electrical bond pads, on the upper surface of the chip should be protected, such as by a resist, which must be removed prior to wire bonding. An alternative is to apply a mask to the lower surface of the wafer and to deep silicon etch from the rear. Alternatively second caps may be provided for the lower surface of the wafer, utilizing the same manufacturing methods as for the upper caps and using the lower caps as masks for the etch. By providing both upper and lower caps at the wafer stage, each chip is substantially completely packaged prior to singulation.

Figure 22 shows a technique for providing protective caps for both the upper and lower surfaces. The figure shows a wafer 150 upon which have been formed a series of MEMS device chips 153 on an upper surface 154. Each chip 153 includes one or more MEMS devices 152 and optionally other micro fabricated elements. A first set of protective caps 156 have been formed on the upper surface 154 as per the techniques of the invention previously described. The bond pads 158 of the individual chips 153 are on the upper surface 154 and are not covered by the protective caps 156. A second set of protective caps 160 have been formed on the lower surface 162 of the wafer as per the techniques of the invention previously described. The first and second sets of protective caps may be applied to the wafer sequentially or may be applied to the wafer simultaneously. The order of application is not important. The second set of caps 160 are located under each chip 153 but are larger than the first set 156 and extend under and beyond the bond pads 158.

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The wafer 150 is then subject to a deep silicon etch from the lower surface of the wafer as indicated by arrows 164, rather than from the upper surface, to separate the individual chips. The lower caps 160 thus act as a mask to the bond pads 158 and because the etching process is very directional, only silicon between the lower caps 160 of the individual chips is etched away. The bond pads 158 and other exposed parts on the upper surface within the outline of the lower caps are substantially unaffected by the etch and so the chips 152 will not be damaged by the etch.

It will be appreciated that the provision of the second set of caps is only a necessity where a hollow space is required; if a second set of caps is unnecessary or undesirable, a resist may be coated onto the lower surface with a grid pattern to leave areas between the chips exposed for deep etching.

Throughout the specification, reference is made to semiconductors and more particularly silicon semiconductors. It is to be understood that the invention is not limited to use on semiconductors or silicon based semiconductors and has application to non semiconductor devices and to non silicon based semiconductors, such as those based on gallium arsenide semiconductors.

Whilst the invention has been described with particular reference to MEMS devices, it is to be understood that the invention is not limited to MEMS or MOEMS devices and has application to any devices which are or may be bulk fabricated on a wafer.

It will be apparent to those skilled in the art that many obvious modifications and variations may be made to the embodiments described herein without departing from the spirit or scope of the invention.

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Claims:

1. An integrated circuit assembly which includes

a substrate having an upper surface and a lower surface;

a plurality of integrated circuit devices positioned on the upper surface;

a plurality of bond pads positioned on the upper surface with a bond pad associated with each integrated circuit device;

a plurality of protective caps positioned on the upper surface of the substrate to enclose respective integrated circuit devices with each bond pad positioned outside the protective cap of its associated device; and

a plurality of protective members positioned on the lower surface of the substrate such that each protective member is aligned with a respective protective cap, each protective member being dimensioned to overlie the respective protective cap and associated bond pad to protect the integrated circuit devices and associated bond pads when the substrate is separated by a process applied to the lower surface of the substrate.

2. An integrated circuit assembly as claimed in claim 1, in which the substrate is a silicon wafer that is capable of being separated by etching, the protective member being of an etch-resistant material.

3. An integrated circuit assembly as claimed in claim 1, in which each protective member is a protective cap.

4. An integrated circuit assembly as claimed in claim 3, in which the protective caps on the upper and lower surfaces of the wafer are moulded of a thermoplastic material.

5. An integrated circuit assembly which includes

a substrate having an upper surface and a lower surface;

at least one integrated circuit device positioned on the upper surface;

a bond pad positioned on the upper surface to provide electrical communication with the integrated circuit device;

a protective cap positioned on the substrate to enclose the integrated circuit device with the bond pad positioned outside the protective cap; and

a protective member positioned on the lower surface of the substrate such that the protective member is aligned with the protective cap, the protective member being dimensioned to overlie the protective cap and bond pad to protect the integrated circuit device and bond pad when the substrate is separated by a process applied to the lower surface of the substrate.

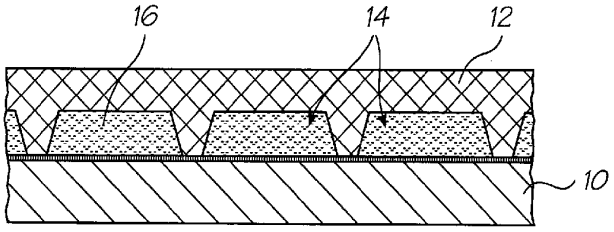

FIG. 1
(Prior Art)

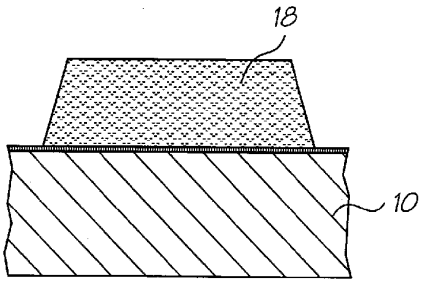

FIG. 2
(Prior Art)

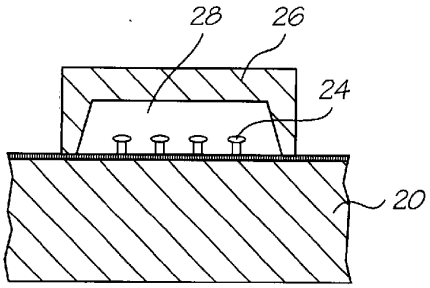

FIG. 3
(Prior Art)

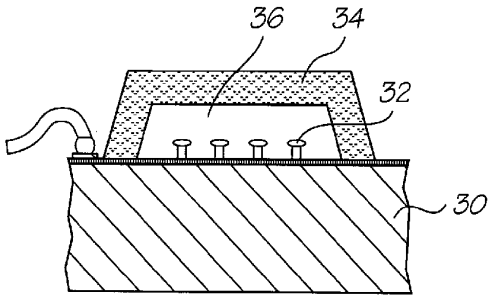

FIG. 4

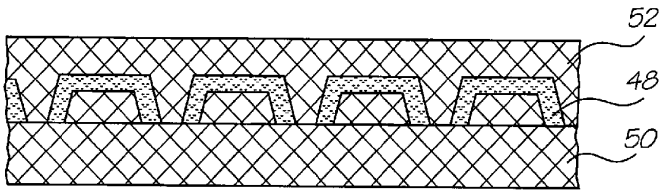

FIG. 5

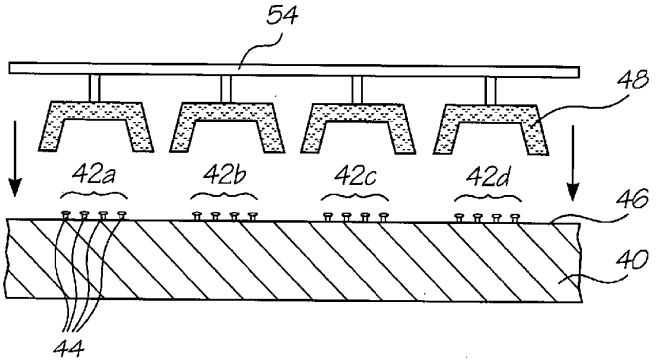

FIG. 6

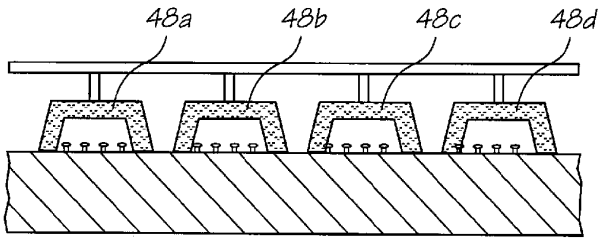

FIG. 7

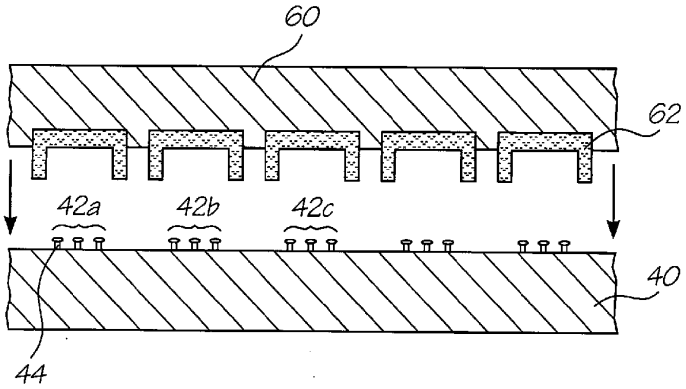

FIG. 8

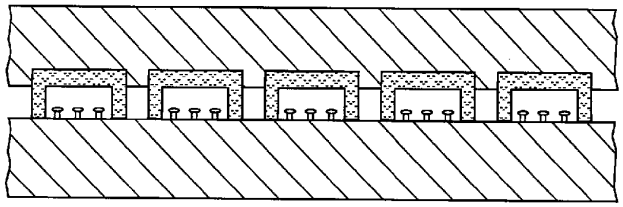

FIG. 9

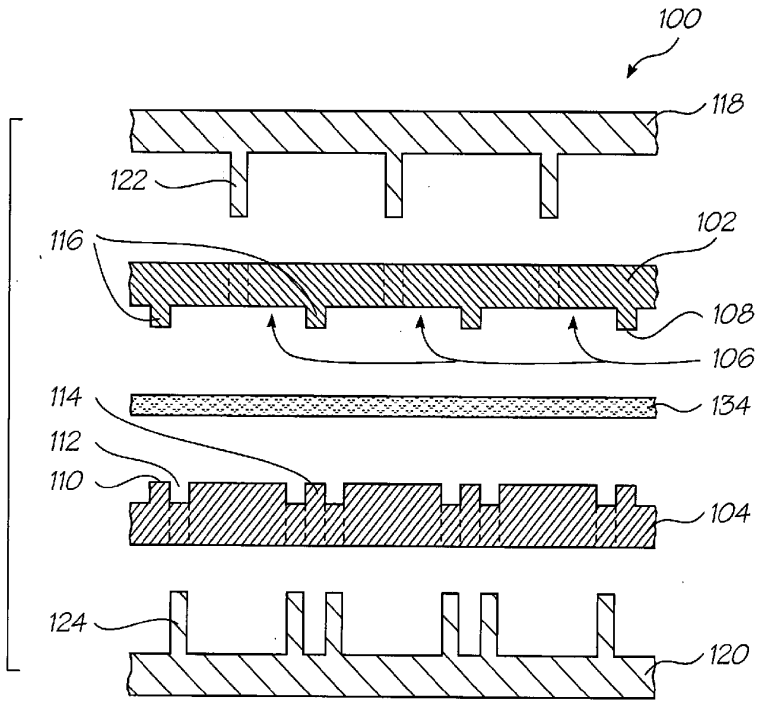

FIG. 10

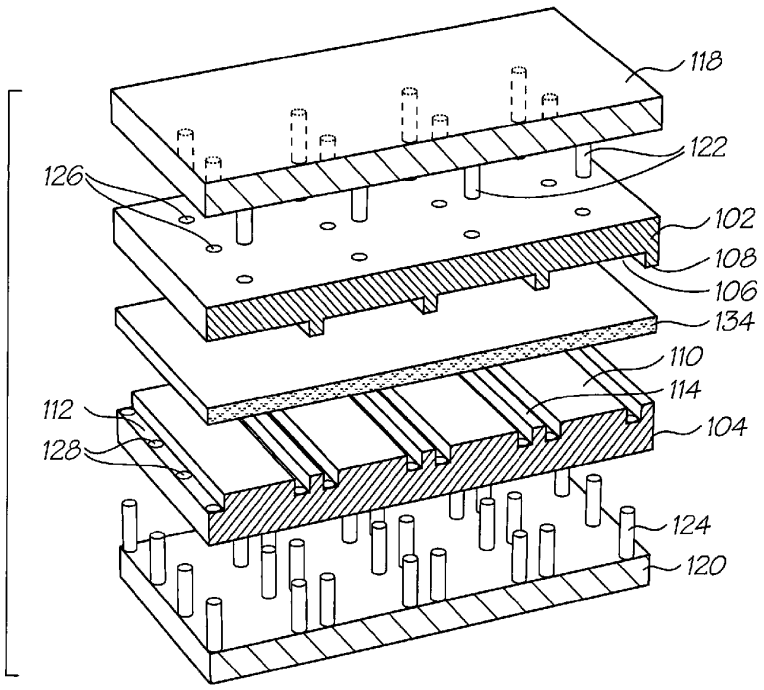

FIG. 11

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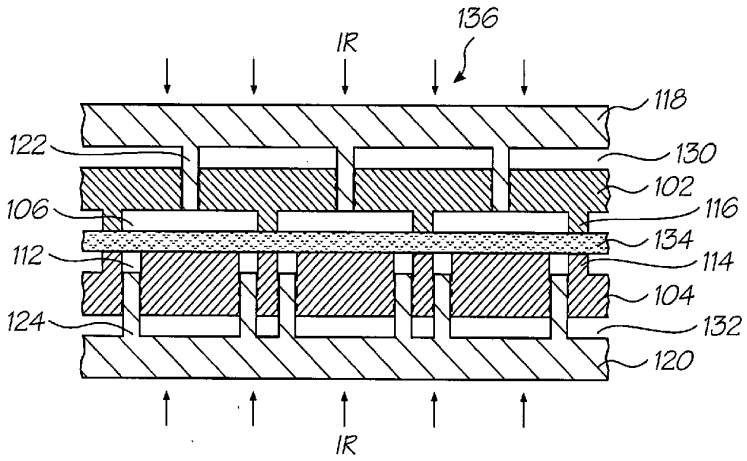

FIG. 12

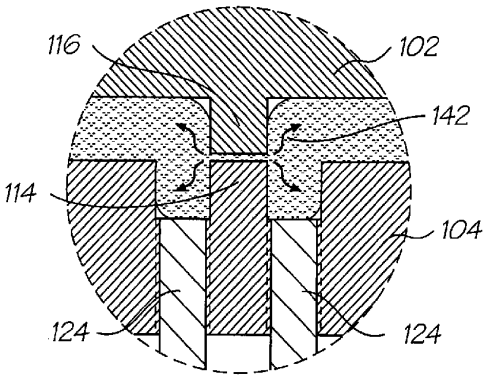

FIG. 13a

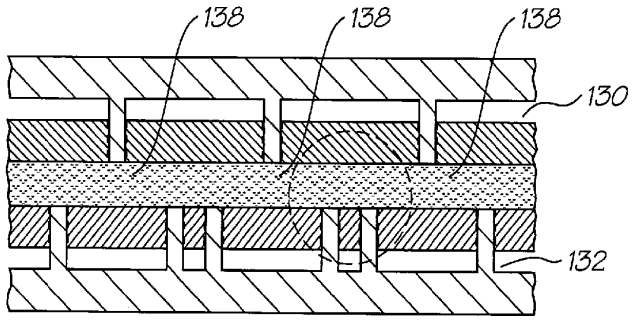

FIG. 13

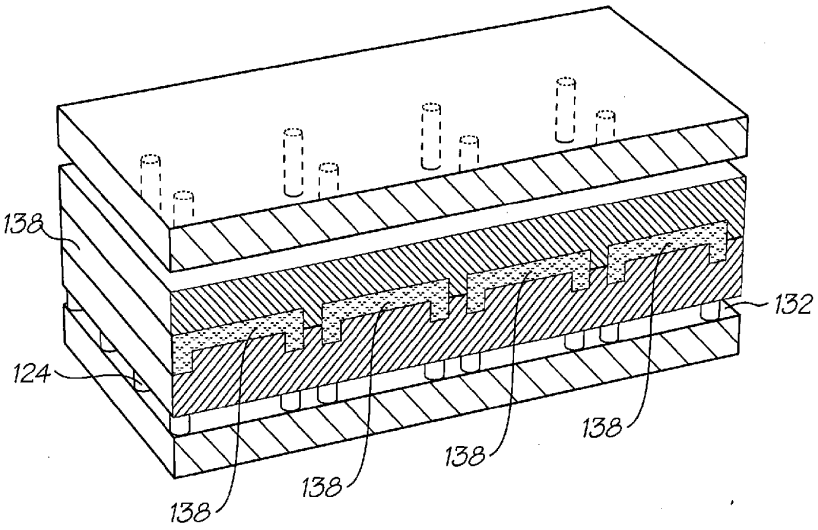

FIG. 14

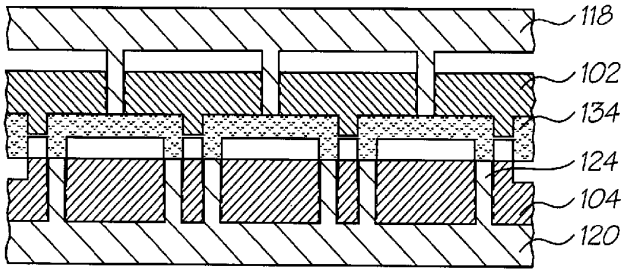

FIG. 15

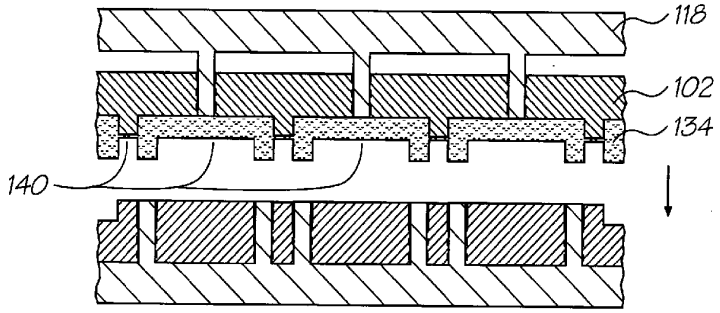

FIG. 16

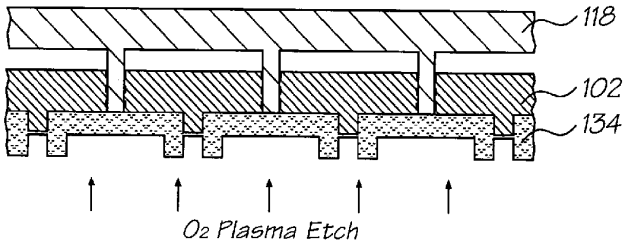

FIG. 17

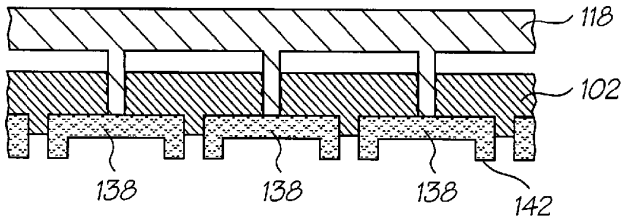

FIG. 18

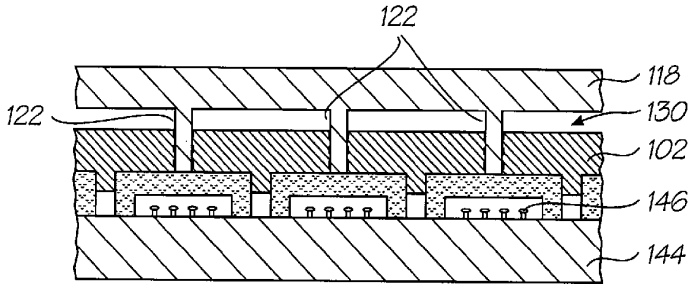

FIG. 19

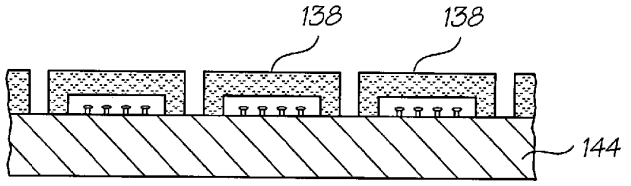

FIG. 20

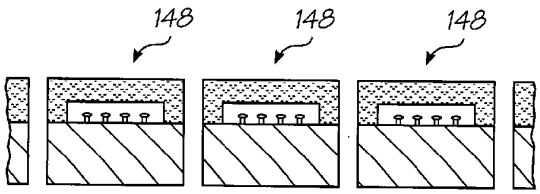

FIG. 21

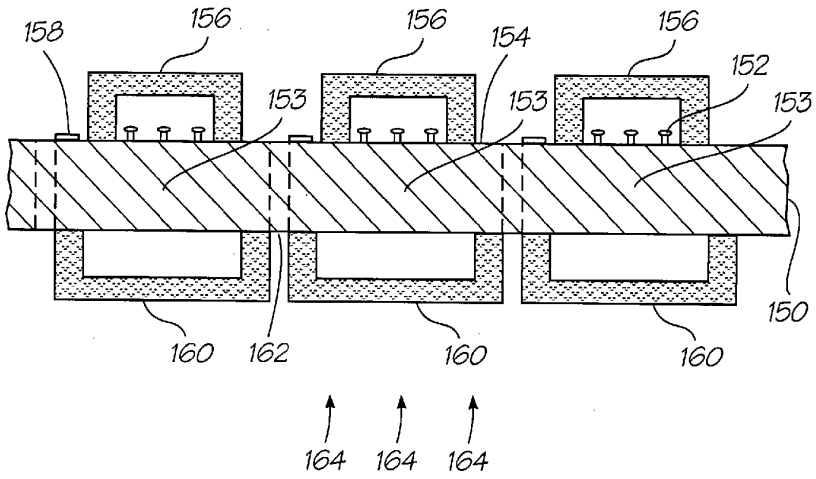
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FIG. 22