(12) UK Patent Application (19) GB (11) 2 309 336 (13) A

(43) Date of A Publication 23.07.1997

(21) Application No 9701204.1

(22) Date of Filing 21.01.1997

(30) Priority Data
(31) 08007935 (32) 22.01.1996 (33) JP

(71) Applicant(s)
Fuji Electric Co Ltd

(Incorporated in Japan)

1-1 Tanabeshinden, Kawasaki-ku, Kawasaki-shi, Kanagawa 210, Japan

(72) Inventor(s)
Tatsuhiko Fujihira

(74) Agent and/or Address for Service
Beresford & Co
2-5 Warwick Court, High Holborn, LONDON, WC1R 5DJ, United Kingdom

(51) INT CL^6
H01L 29/66 21/265 // H01L 29/73 29/74 29/778 29/78 29/861

(52) UK CL (Edition O)
H1K KKAX K1AA9 K1AB9 K1BC K1CA K1CB K1FX K2S1B K2S2P K2S20 K9D1 K9E K9N2 K9R2

(56) Documents Cited
EP 0164096 A2 **US 4963947 A**

(58) Field of Search
UK CL (Edition O) **H1K KCAD KCAV KKAX**
INT CL^6 **H01L**
ON LINE,W.P.I.

(54) **Drift regions in semiconductor devices**

(57) The semiconductor device has a drift region 190 which conducts a drift current when it is in the ON mode and is depleted when it is in the OFF mode. The drift region has a plurality of first conductivity type drift regions 1 and a plurality of second conductivity type regions 2 which are positioned in parallel between the drift regions to form p-n junctions jb. The device may be a lateral SOI MOSFET having a source 8, a drain 9 and a gate electrode 11. The structure enables a decrease in the on-resistance in addition to an increase in the breakdown voltage. The device may also be a diode, thyristor, IGBT, bipolar transistor or HEMT.

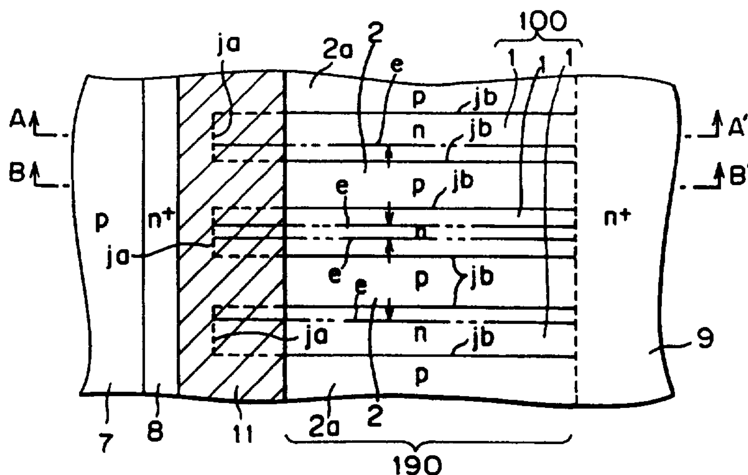


FIG.6A

GB 2 309 336 A

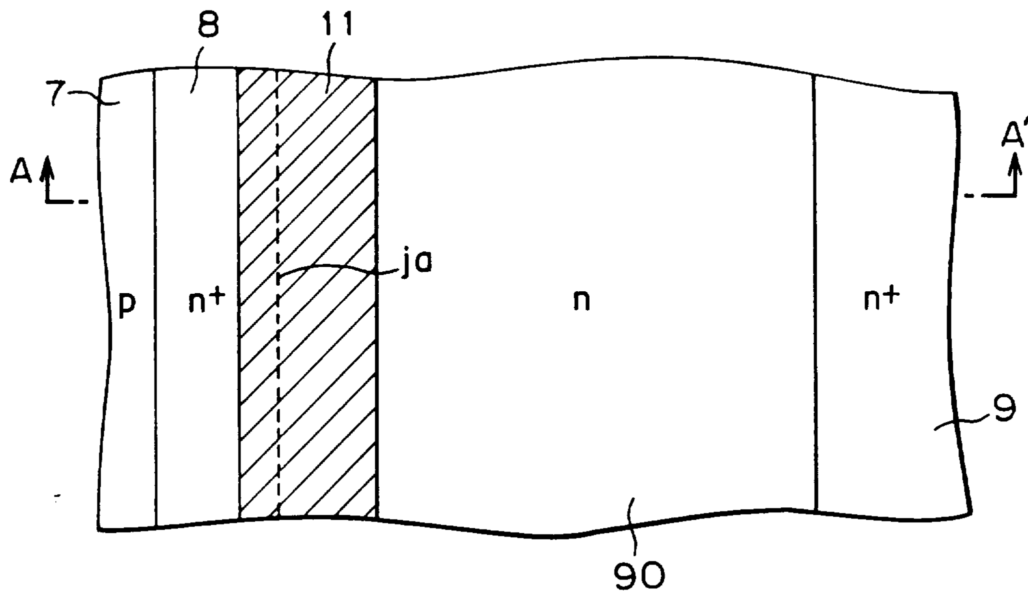


FIG.1A
(PRIOR ART)

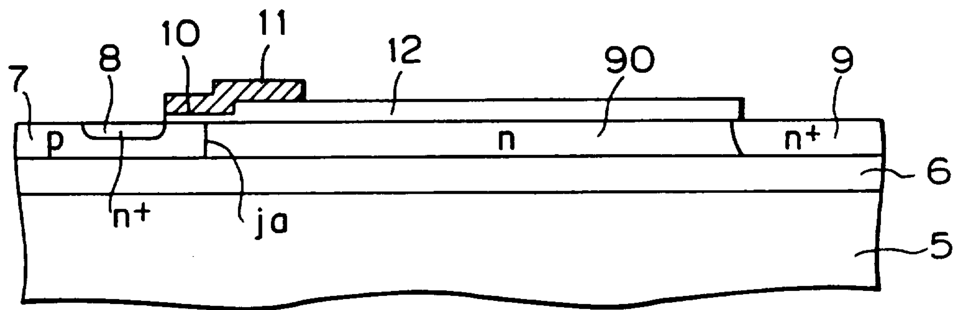


FIG.1B
(PRIOR ART)

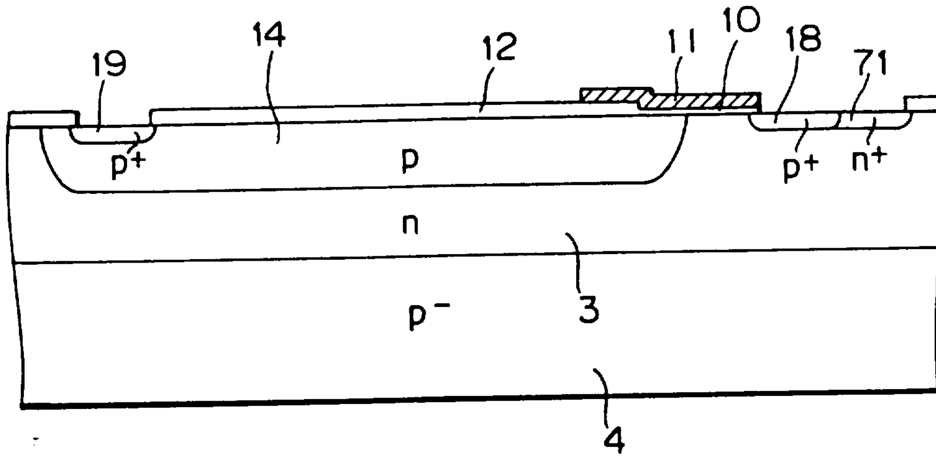


FIG.2A
(PRIOR ART)

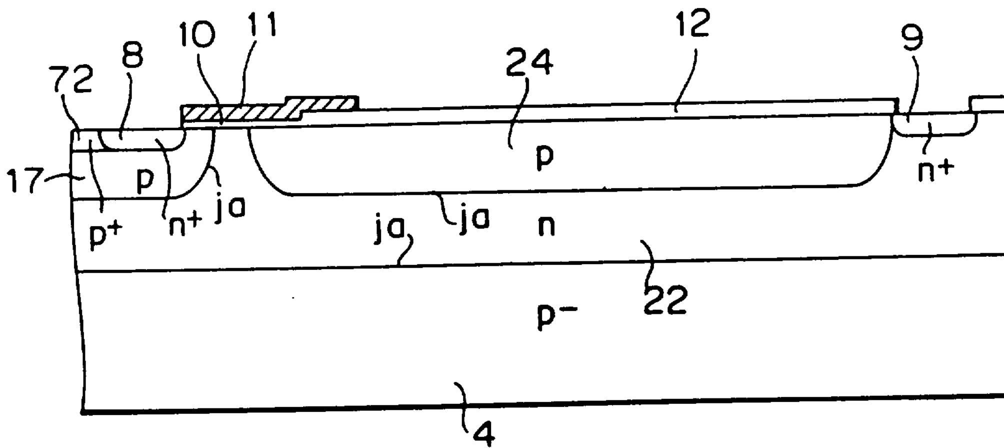


FIG.2B
(PRIOR ART)

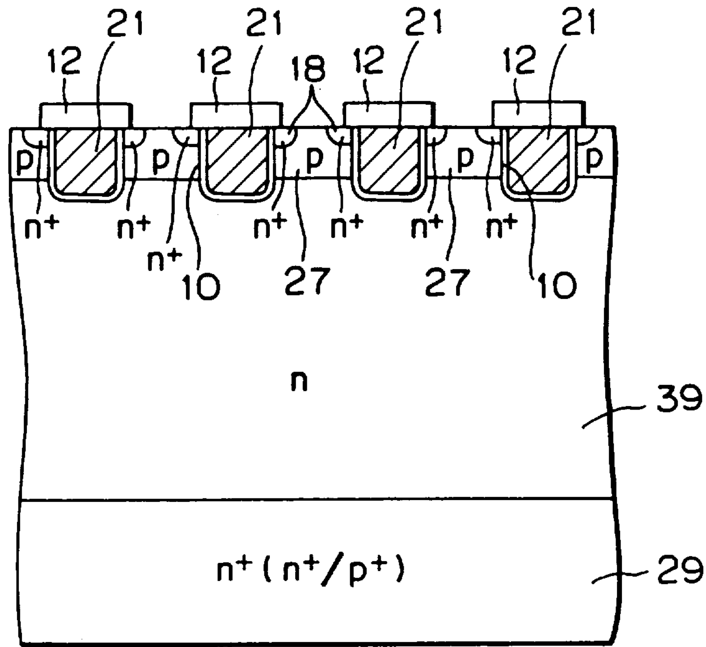


FIG.3
(PRIOR ART)

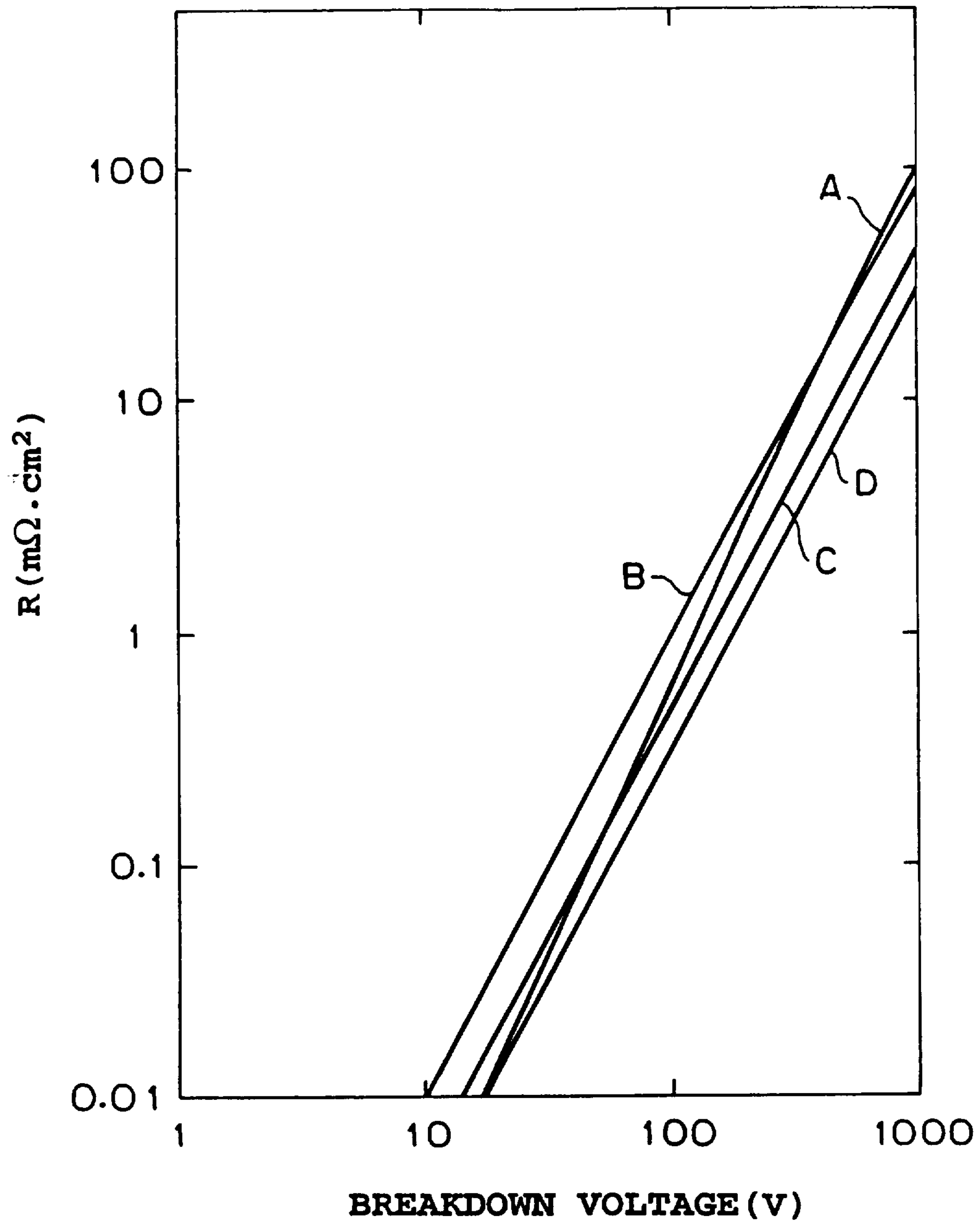


FIG.4

FIG.5A

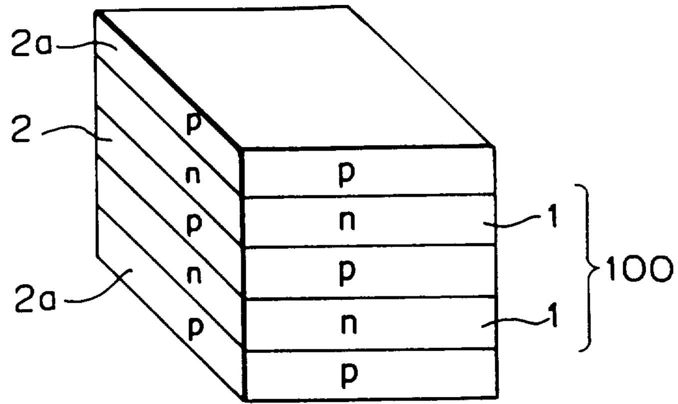


FIG.5B

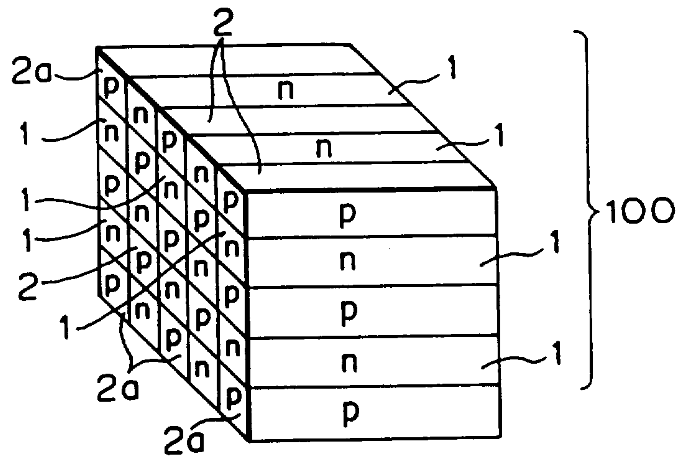
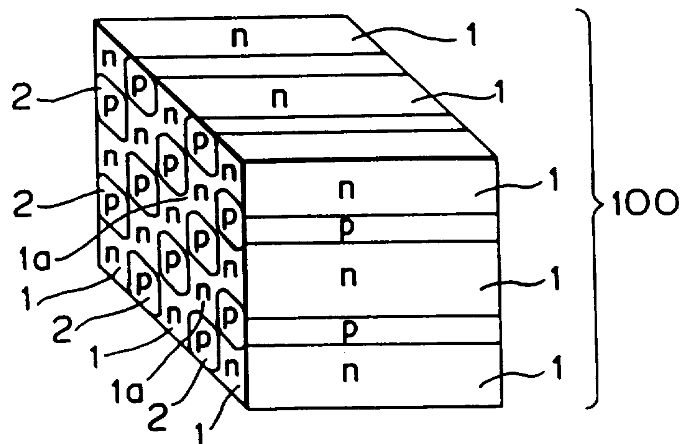


FIG.5C



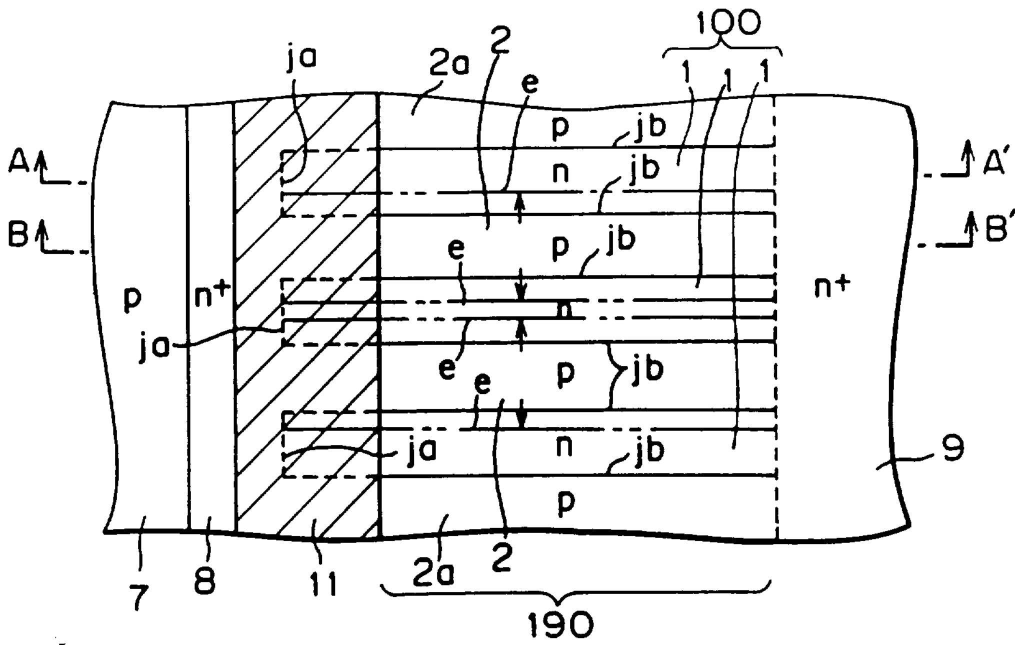


FIG.6A

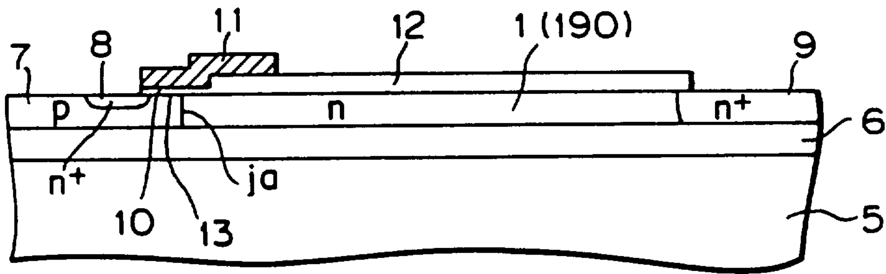


FIG.6B

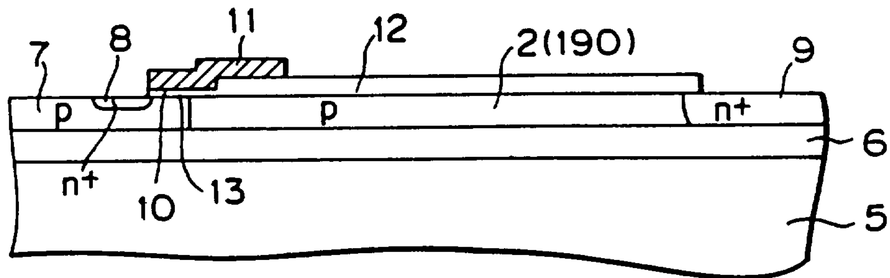


FIG.6C

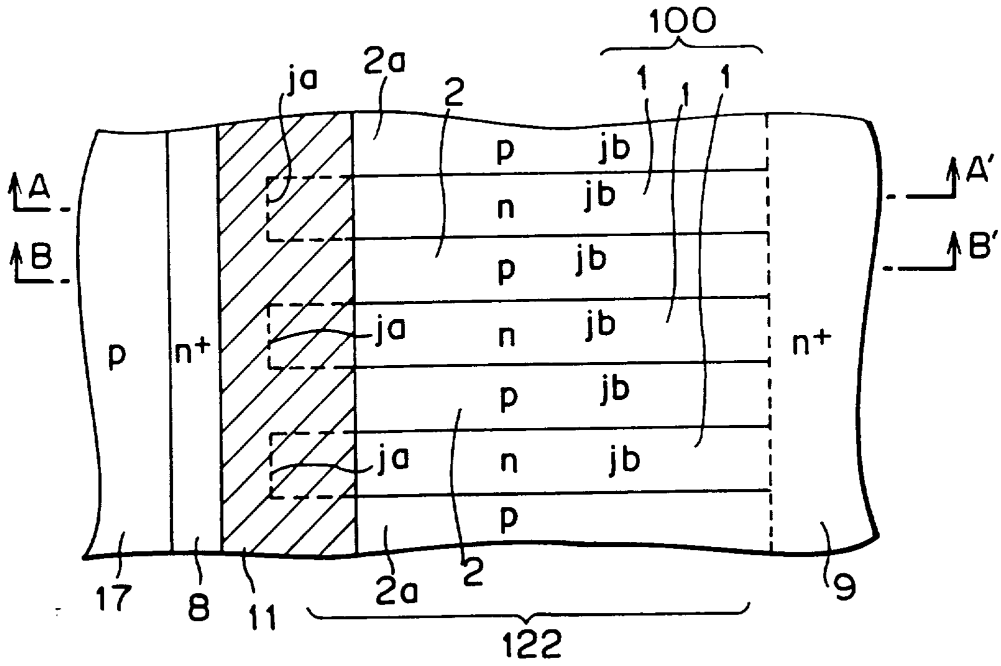


FIG.7A

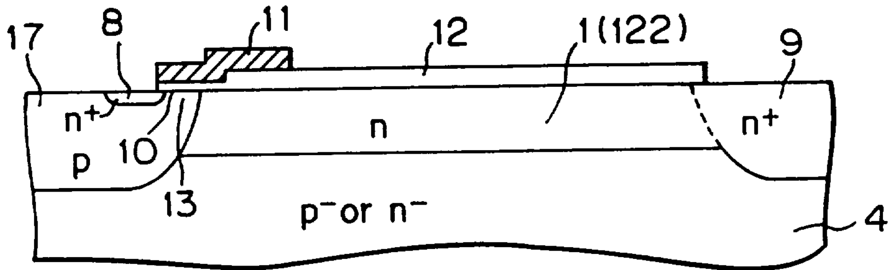


FIG.7B

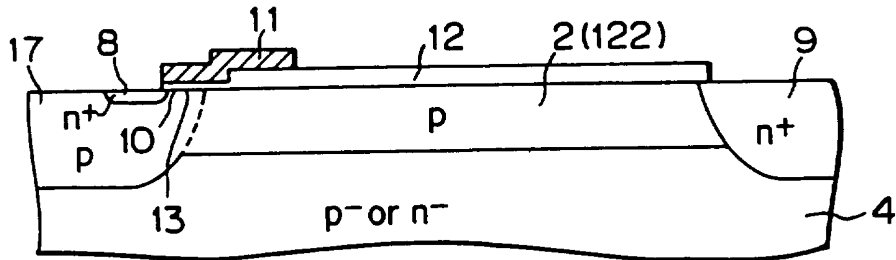


FIG.7C

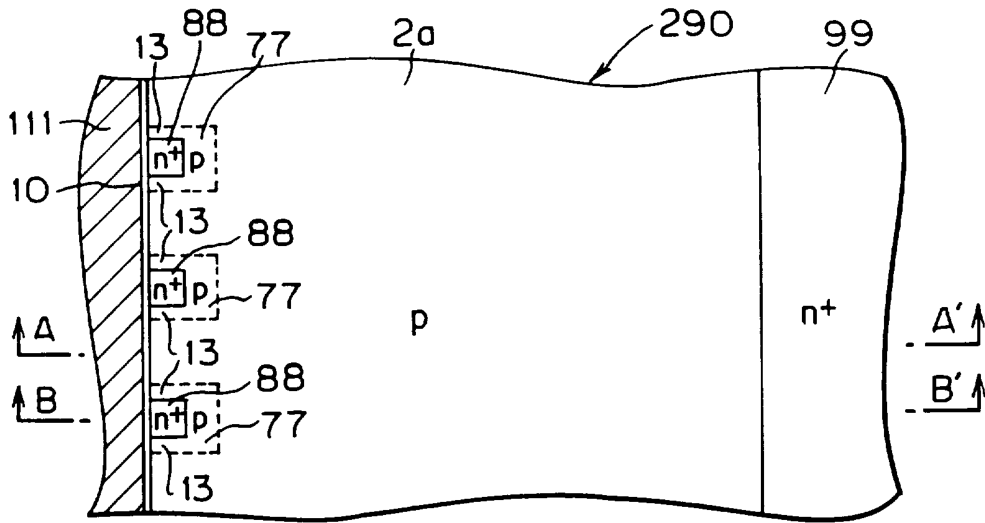


FIG. 8A

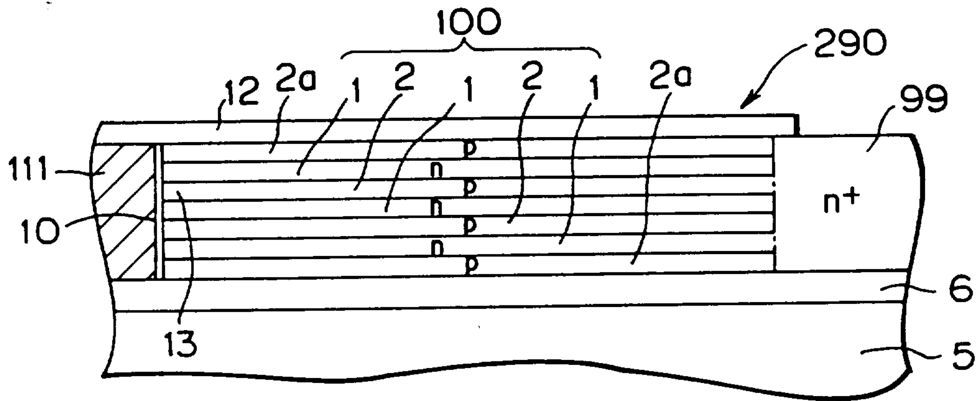


FIG. 8B

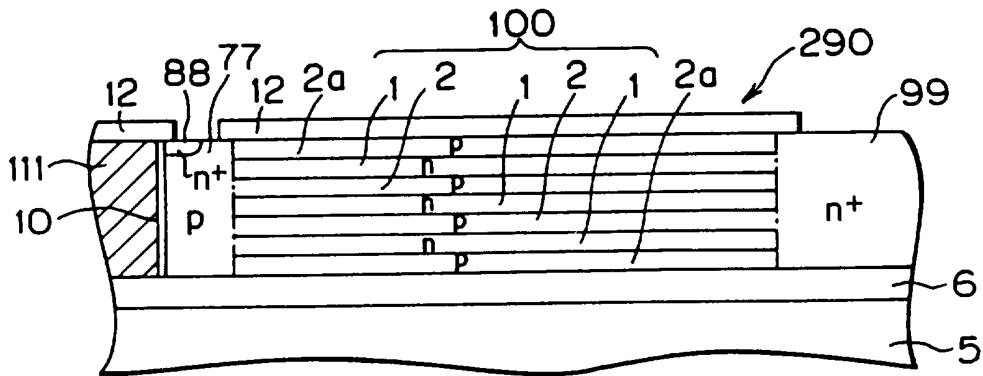


FIG. 8C

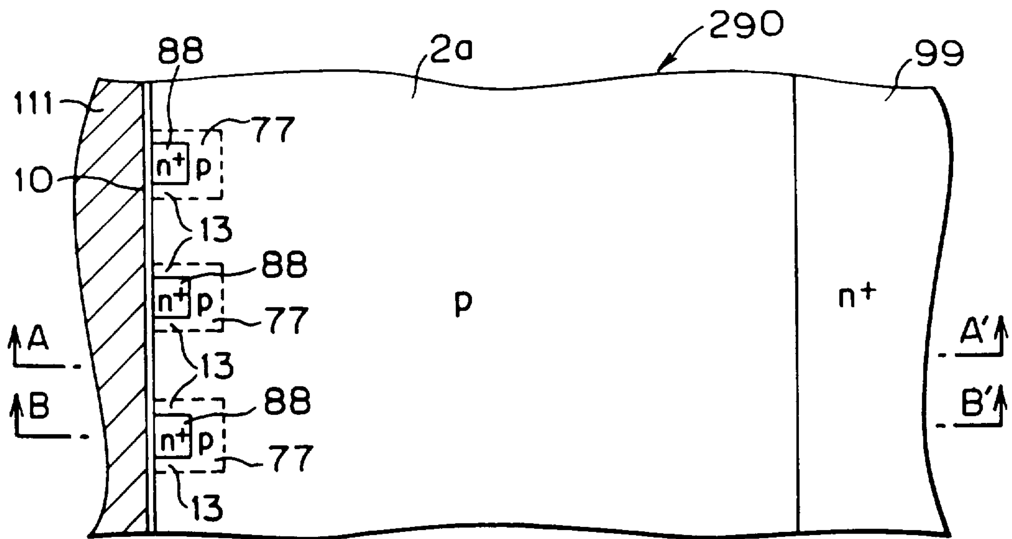


FIG.9A

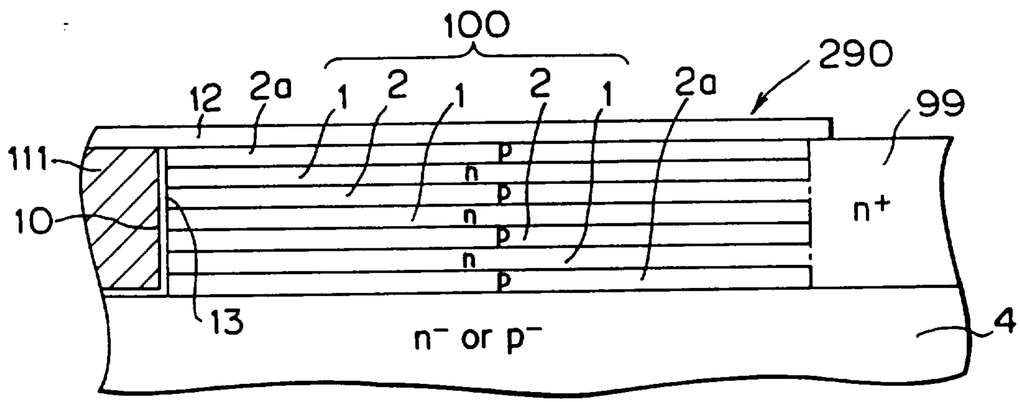


FIG.9B

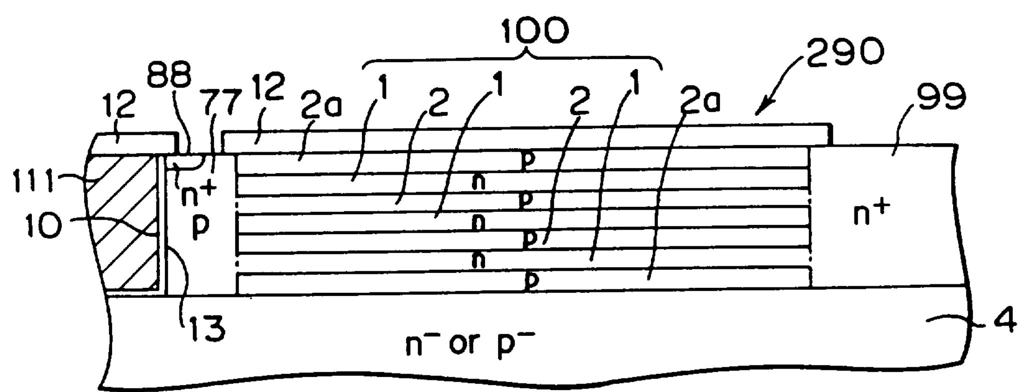


FIG.9C

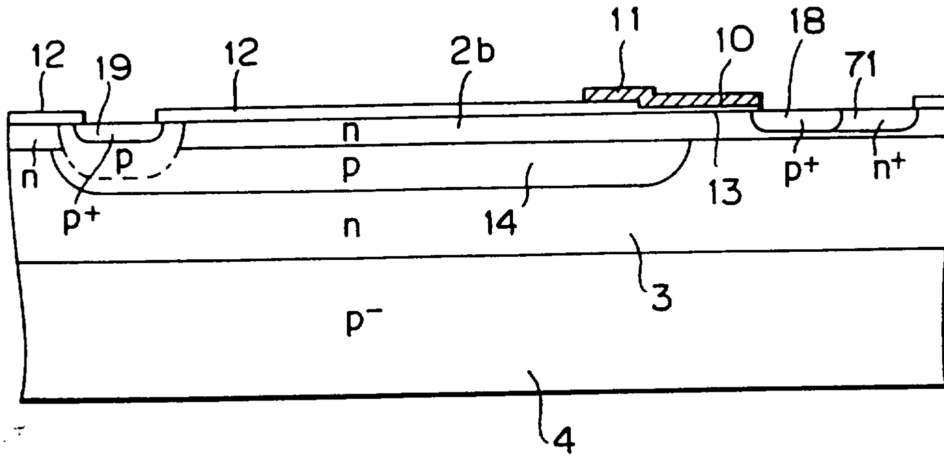


FIG.10

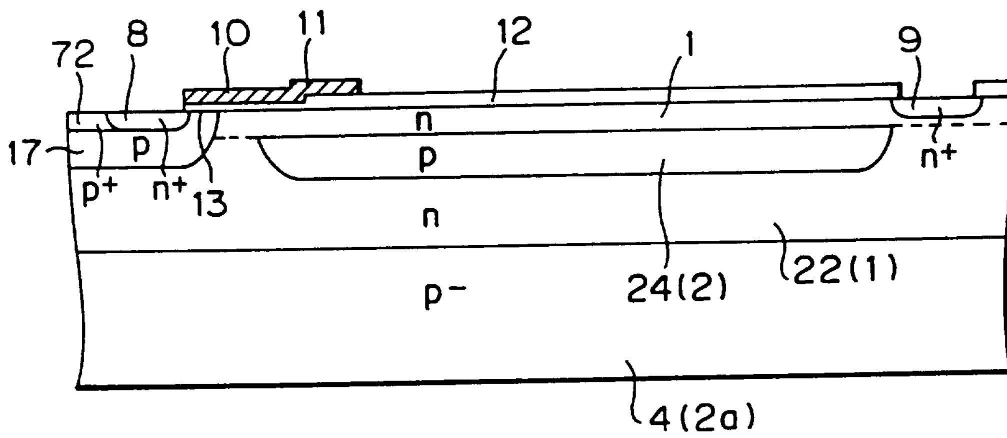


FIG.11

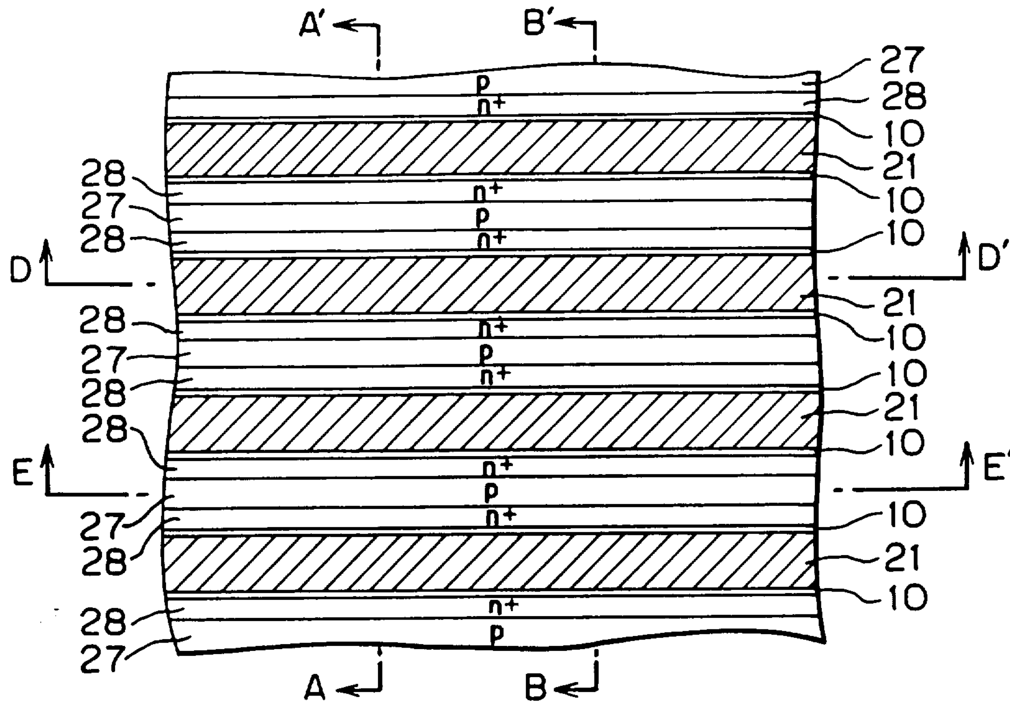


FIG.12A

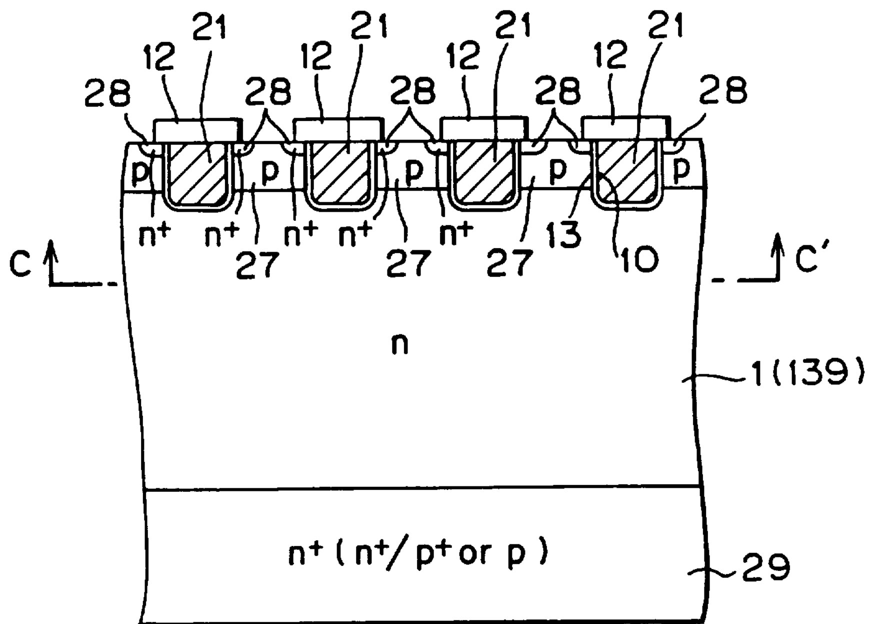


FIG.12B

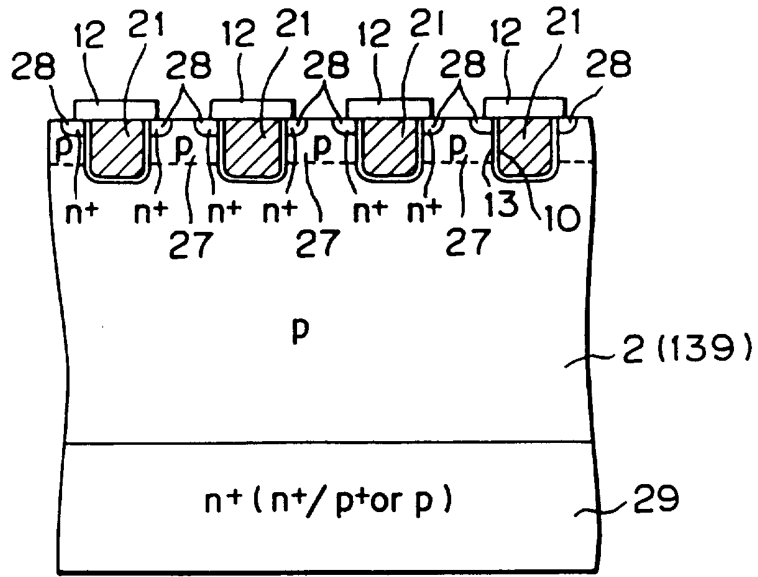


FIG.12C

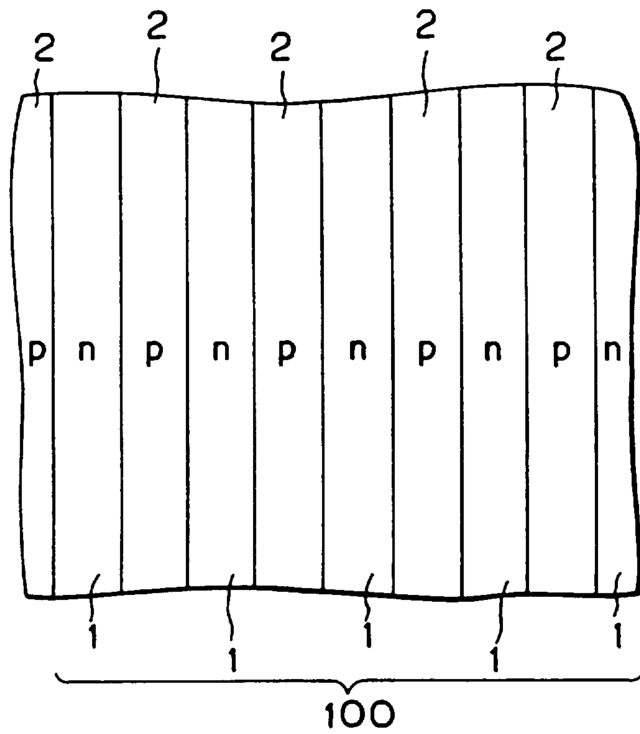


FIG.12D

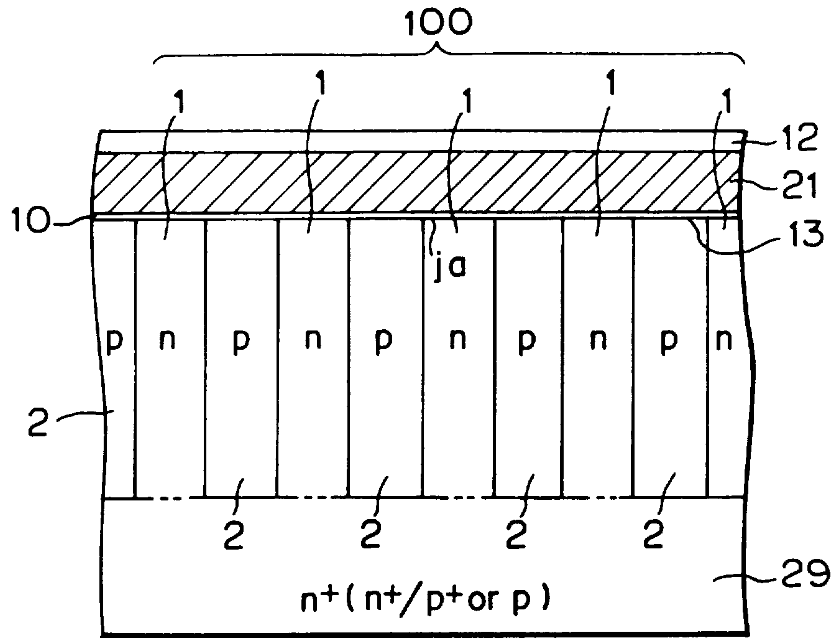


FIG.12E

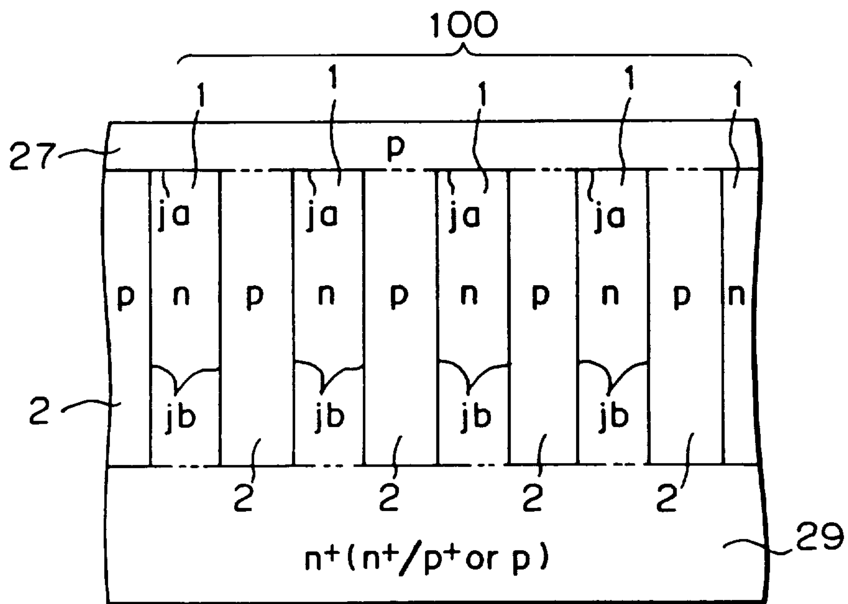


FIG.12F

2309336

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

5

The present invention relates to a semiconductor device with a large current capacity and a high breakdown voltage, such as a metal-oxide semiconductor field-effect transistor (MOSFET), an
10 IGBT, a bipolar transistor, and semiconductor diode, and also the present invention relates to a method for fabricating the semiconductor device mentioned above.

15 In general, structures of the semiconductor elements can be roughly grouped into two types: a lateral structure having an electric contact portion on one side thereof; and a vertical structure having electric contact portions on both sides thereof.

20 One of the example of the semiconductor element with the lateral structure is a SOI (silicon on insulator) -MOSFET (metal oxide silicon field effect transistor) shown in Fig. 1A and Fig. 1B, in which Fig. 1A is a plane view of the semiconductor element,
25 while Fig. 1B is a cross sectional view of the semiconductor along a line A-A' in Fig. 1A.

A structure of the SOI-MOSFET is based on an offset gate structure of n-channel MOSFET, in which a

p-type channel diffusion layer 7, an n^+-type low doped drain region (drain/drift region) 90, and an n^+-type drain region 9 are formed on a semiconductor base plate 5 via an insulation membrane 6 in that
5 order. In addition, an n^+-type source region 8 is formed on a part of a surface of the p-type channel diffusion layer, and also an insulation layer 12 is formed on a region extending from an end portion of the region 8 to an end of the n^+-type drain region 9.
10 Particularly, in close proximity to the above n^+-type source region, the insulating film 12 has a portion which is thinner than a remained potion 10 and is positioned on the boundary of the p-type channel diffusion layer 7 and the n^+-type low doped drain
15 region 90. An gate electrode 11 is formed so as to cover from the thin portion to the thick portion of the insulation film.

The above low doped drain region 90 can be operated as a drift region for transferring carriers
20 by an effect of electrical field if the MOSFET is in the ON mode. If the above low doped drain region 90 is in the OFF mode, on the other hand, it becomes a depletion region to reduce an electric field strength applied thereon, resulting in an increase in
25 breakdown voltage. It is possible to reduce its drift resistance by increasing the concentration of impurities in the low doped drain region 90 and by shortening a length of flowing electricity through

the region 90. As a result, a substantial ON resistance (drain-source resistance) of the MOSFET can be lowered. In this case, however, it will be difficult to extend the boundaries of the depletion
5 layer between the drain and the channel to be developed from a p-n junction between the p-type channel diffusion layer 7 and the n-type low doped drain region 90, so that the maximum permissible (critical) electric field strength of silicon reaches
10 at an earlier time, resulting in a reduction in the breakdown voltage (drain-source voltage). It means that there is a trade-off relationship between the ON resistance (current capacity) and the breakdown voltage. Similarly, it has been known that the
15 semiconductors such as IGBT, bipolar transistors, and semiconductor diodes make the above trade-off relationship.

Referring now to Figs. 2A and 2B, another example of the conventional MOSFETs having a lateral
20 structure will be described in detail, in which Fig. 2A is a cross sectional view of a p-channel MOSFET and Fig. 2B is a cross sectional view of a double diffusion type n-channel MOSFET.

The p-channel MOSFET shown in Fig. 2A comprises
25 a n-type channel diffusion layer 3 formed on a p-type semiconductor layer 4, a gate electrode 11 with a field plate formed on the diffusion layer 3 via a gate insulation film 10, a p^+-type source region 18

formed on a part of the diffusion layer 3 in close proximity to one end of the gate electrode 11, a p-type low doped drain region (drain/drift region) 14 formed as an well having an end immediately
5 underneath the other end of the gate electrode 11, an n^+-type contact region 71 adjacent to the p^+-type source region 18, a thick insulation film 12 formed on the p-type low doped drain region 14. In this structure, therefore, its ON resistance and breakdown
10 voltage can be defined as the trade-off relationship on the basis of a length of flowing electricity through the well-shaped p-type low doped drain region 14 and the concentration of its impurities.

The double diffusion type n-channel MOSFET
15 shown in Fig. 2B comprises a n-type low doped drain layer (drain/drift layer) 22 formed on a p-type semiconductor layer 4, a gate electrode 11 with a field plate formed on the low doped drain layer 22 via a gate insulation film, a p-type channel
20 diffusion region 17 formed on a part of the diffusion layer 22 in close proximity to one end of the gate electrode 11, an n^+-type source region 8 formed as an well in the p-type channel diffusion region 17, an n^+-type drain region 9 formed as an well positioned
25 at a distance from the n^+-type source region 8 and the gate electrode 11, an well-shaped p-type top layer 24 formed on a surface layer between the gate electrode 11 and the n^+-type drain region 9, a p^+-

type contact region 72 adjacent to the n^+-type source region 8, and a thick insulation film 12 formed on the p^+-type top layer 24. In this structure, therefore, its ON resistance and breakdown voltage can be defined as the trade-off relationship on the basis of a length of flowing electricity through the well-shaped n-type low doped drain region 22 and the concentration of its impurities.

In the structure of Fig. 2B, however, the n-type low doped drain layer 22 is sandwiched between the p-type semiconductor layer 4 and the p^+-type top layer 24, so that it can be provided as the structure with a high breakdown voltage if the MOSFET is in the OFF mode because the low doped drain layer 22 is depleted at an earlier time by widening a depletion layer not only from the p-n junctions Ja with the p-type channel diffusion region 18 but also from p-n junctions Jb of upper and lower sides of the n^+-type low doped drain layer 22 while the concentration of impurities in the low doped drain layer 22 can be increased.

Fig. 3 shows a trench gate type n-channel MOSFET as an example of the vertical semiconductor element. The n-channel MOSFET comprises a n-type low doped drain layer 39 formed on a n^+-type drain layer 29 electrically contacted with a back electrode (not shown), a trench gate electrode 21 imbedded in a trench formed on a surface of the low doped drain

layer 39 via a gate insulation film 10, a p-type
channel diffusion layer 27 formed on a surface of the
low doped drain layer 39 at a relatively shallow
depth compared with that of the trench gate electrode
5 21, a n^+-type source region 18 formed along an upper
edge of the trench gate electrode 21, and a thick
insulation film 12 as a sheathing of the gate
electrode 21. By the way, it is possible to make an
n-type IGBT structure using a double structure made
10 of an n^+-type upper layer and a p^+-type under layer
instead of the single layered n^+-drain layer 29. In
this kind of the vertical structure, therefore, the
low doped drain region 39 acts as a drift region for
flowing a drift current in the vertical direction if
15 the MOSFET is in the ON mode, while it is depleted to
increase its breakdown voltage if the MOSFET is in
the OFF mode. In this case, its ON resistance and
breakdown voltage can be defined as the trade-off
relationship on the basis of a thickness of the low
20 doped drain layer 39 and the concentration of its
impurities.

Fig. 4 is a graph that shows the relationship
between an ideal breakdown voltage and an ideal ON
resistance of the silicon n-channel MOSFET. In this
25 figure, it is based on the hypothesis that the
breakdown voltage cannot be lowered by an effect of
its form and the ideal ON resistance is very small
enough to ignore electrical resistance of the regions

except the low doped drain region.

In Fig. 4, the line A represents the relationship between an ideal breakdown voltage and an ideal ON resistance of the vertical structure type
5 n-channel MOSFET of Fig. 3; the line B represents the relationship between an ideal breakdown voltage and an ideal ON resistance of the n-channel type MOSFET which is prepared by replacing the channel type of the MOSFET of Fig. 2A; the line D represents the
10 relationship between an ideal breakdown voltage and an ideal ON resistance of the vertically structured double diffused n-channel MOSFET of Fig. 2B; and the line C represents the relationship between an ideal breakdown voltage and an ideal ON resistance of the
15 n-channel MOSFET of Fig. 11.

The vertical n-channel MOSFET is constructed so as to match the direction of flowing the drift current in the ON mode and the direction of expanding the depletion layer to be caused by a reverse bias in
20 the OFF mode. If we only take note of the low doped drain layer 39 of Fig. 3, the breakdown voltage BV at the time of the OFF mode, an approximate value of the BV can be obtained by the following equation.

$$BV = E_C^2 \varepsilon_0 \varepsilon_{si} \alpha (2-\alpha) / 2q N_D \qquad (1)$$

25 wherein

E_C is $E_C (N_D)$ which is the maximum electric field strength of silicon at the impurity concentration of N_D;

ε_0 is a dielectric constant of vacuum;

ε_{si} is a relative dielectric constant of silicon;

q is a unit charge;

N_D is the impurity concentration of the low doped

5 region; and

α is a factor ($0 < \alpha < 1$).

In addition, the ideal ON resistance per unit area in the ON mode can be obtained by the following equation, approximately.

10 $R \approx \alpha W / \mu q N_D$

wherein

μ is $\mu (N_D)$ which a mobility of electron at the impurity concentration of N_D ; and

W is equal to $E_C \varepsilon_0 \varepsilon_{si} / q N_D$.

15 Therefore, R can be represented by the following formula.

$$R = E_C \varepsilon_0 \varepsilon_{si} \alpha / \mu q^2 N_D^2 \qquad (2)$$

Thus, qN_D is erased from the formula (2) using the formula (1) and an optimum value such as 2/3 for a,

20 resulting in the following formula:

$$R = BV^2 \ (27/8 \ Ec^3 \varepsilon_0 \varepsilon_{si} \mu) \qquad (3)$$

In this formula, the ON resistance R seems to be proportional to the square of the breakdown voltage BV. In this case, however, the line A of Fig. 4 is

25 roughly proportional to BV raised to the 2.4th to 2.6th power.

In the case of the n-channel type MOSFET structure which is prepared by replacing the channel

type of the MOSFET of Fig. 2A, the drift current flows in the lateral direction if it is in the ON mode, while the depletion layer spreads upward (in the vertical direction) from the bottom of the well
5 substantially faster than spreading from one end of the well in the lateral direction. For obtaining a higher breakdown voltage in the depletion layer spreading out in the vertical direction, it should be depleted from a boundary surface of the p-n junction
10 (i.e., the bottom of the well) between the low doped drain region 14 and the channel diffusion layer 3 to a surface of the low doped drain region 14 (i.e., the surface of the well), so that the maximum value of the net doping amount in the low doped drain region
15 14 can be restricted by the following formula:

$$S_D = E_C \varepsilon_0 \varepsilon_{Si} / q \quad (4)$$

If the length of the low doped drain region 14 is defined as L, an ideal breakdown voltage BV is represented by the formula:

20 $$BV = E_C L \beta \quad (5)$$

wherein

β is a factor $(0 < \beta < 1)$.

In addition, the ideal ON resistance R per unit area in the ON mode can be obtained by the following
25 equation, approximately.

$$R = L^2 / \mu q S_D \quad (6)$$

wherein

μ is μ (S_D) which the mobility of electron at the

maximum impurity concentration of S_D.

Thus, L is erased from the formula (6) by substitution of the formulae (4) and (5), yielding the following formula:

5 $R = BV^2 / \beta^2 E_C^3 \varepsilon_0 \varepsilon_{Si} \mu$ (7)

In the case of the vertically structured double diffusion type n-channel MOSFET shown in Fig. 2B, it is constructed by forming a p-type top layer 24 on the MOSFET structure of Fig. 2A. Therefore, the

10 depletion layer spreads in the vertical direction, and thus the low doped drain layer 22 can be depleted quickly. As shown in the following formula (8), the net doping amount S_D in the low doped region 2 can be increased twice as much as that of Fig. 2A.

15 $S_D = 2 E_C \varepsilon_0 \varepsilon_{Si} / q$ (8)

In this case, the relationship between an ideal ON resistance R and an ideal breakdown voltage of the above structure is represented by the formula:

$R = BV^2 / 2\beta^2 E_C^3 \varepsilon_0 \varepsilon_{Si} \mu$ (9)

20 As is evident from a comparison between the above formula (7) and the above formula (9), the tread-off relationship (line B in Fig. 4) between the ON resistance and the breakdown voltage of the vertically structured n-channel type MOSFET of Fig.

25 2B is slightly improved more than the trade-off relationship (line C in Fig. 4) between the ON resistance and the breakdown voltage of the n-channel type MOSFET which is prepared by replacing the

channel type of the MOSFET of Fig. 2A is improved in some degree. In this case, however, the improvement only permit the doping concentration twice as much as before and it does not give us considerable
5 flexibility in a design criterion of the current capacity and the breakdown voltage of the semiconductor.

Accordingly, it is an object of the present invention to provide a semiconductor device which
10 relaxes the relationship between the ON resistance and the breakdown voltage to enable an increase in the current capacity by a reduction in the ON resistance under the high breakdown voltage.

It is another object of the present invention
15 to provide a manufacturing method for rolling out semiconductor devices.

In a first aspect of present invention, there is provided a semiconductor device having a drift region which flows a drift current if it is in an ON
20 mode and is depleted if it is in an OFF mode, wherein

the drift region is formed as a structure having a plurality of first conductive type divided drift path regions which are connected together in parallel to form a group of parallel drift paths and
25 a plurality of second conductive type side regions, in which each of the second conductive type side regions is positioned between adjacent the first conductive type divided drift path regions to form p-

n junctions.

Here, the semiconductor device may further comprise:

at least one additional second side region
5 which is connected to an outer side of a first conductive type divided drift path region positioned at an outer side of the group of parallel drift paths.

In a second aspect of present invention, there
10 is provided a semiconductor device having a drift region which flows a drift current if it is in an ON mode and is depleted if it is in an OFF mode, and the drift current flows in a lateral direction and the drift region is formed on a semiconductor or an
15 insulation film on the semiconductor, wherein

the drift region is formed as a parallel stripe structure in which a plurality of stripe-shaped first conductive divided drift path regions and a plurality of stripe-shaped second conductive type compartment
20 regions are alternatively arranged on a plane one by one in parallel.

In a third aspect of present invention, there is provided a semiconductor device having a drift region which flows a drift current if it is in an ON
25 mode and is depleted if it is in an OFF mode, and the drift current flows in a lateral direction and the drift region is formed on a semiconductor or an insulation film on the semiconductor, wherein

the drift region is formed as a parallel stacked structure in which a plurality of layer-shaped first conductive divided drift path regions and a plurality of layer-shaped second conductive
5 type compartment regions are alternatively stacked on a plane one by one in parallel.

In a fourth aspect of present invention, there is provided a semiconductor device having a drift region which flows a drift current if it is in an ON
10 mode and is depleted if it is in an OFF mode, and the drift current flows in a lateral direction and the drift region is formed on a second conductive type semiconductor, wherein

the drift region comprises:
15 a first conductive type divided drift region formed on the second conductive type semiconductor layer;

an well-shaped second conductive type compartment region formed on the first conductive
20 type divided drift path region; and

a secondary first conductive type divided drift path region formed on a surface layer of the well-shaped second conductive type compartment region and connected to the first conductive type divided drift
25 path region in parallel.

In a fifth aspect of present invention, there is provided a semiconductor device having a drift region which flows a drift current if it is in an ON

mode and is depleted if it is in an OFF mode, and the drift current flows in a vertical direction and the drift region is formed on a semiconductor, wherein

the drift region comprises a plurality of first conductive type divided drift regions in which each of them has a layer structure along the vertical direction and a plurality of first conductive type compartment regions in which each of them has a layer structure along the vertical direction, and

the plurality of first conductive type divided drift regions and the plurality of first conductive type compartment regions are stacked one by one in parallel in a direction perpendicular to the vertical direction to form a laterally stacked parallel structure.

In a sixth aspect of present invention, there is provided a method of manufacturing a semiconductor device having a drift region which flows a drift current if it is in an ON mode and is depleted if it is in an OFF mode, and the drift current flows in a lateral direction and the drift region is formed on a second conductive type semiconductor, where the drift region has: a first conductive type divided drift region formed on the second conductive type semiconductor layer; an well-shaped second conductive type compartment region formed on the first conductive type divided drift path region; and a secondary first conductive type divided drift path

region formed on a surface layer of the well-shaped second conductive type compartment region and connected to the first conductive type divided drift path region in parallel, comprising steps of:

5 forming a first conductive type divided drift path region on a second conductive type semiconductor layer made of silicon by a thermal diffusion after performing a phosphorus ion-implantation;

forming an well-shaped second conductive type

10 compartment region on the first conductive type divided drift region by a thermal diffusion after performing a selective boron ion-implantation; and

thermally oxidizing a structure obtained by the selective boron ion-implantation to form a secondary

15 first conductive type divided drift path region on a surface thereof through use of a concentration of phosphorus ions which are unevenly distributed on a surface of the silicon and a dilution of boron ions which are unevenly distributed into an oxidized film.

20

Fig. 1A is a plan view showing an example of the conventional SOI-MOSFET which is vertically structured;

Fig. 1B is a cross sectional view taken along

25 line A-A' in Fig. 1A;

Fig. 2A is a cross sectional view showing another example of the conventional MOSFET which is vertically structured;

Fig. 2B is a cross sectional view showing an example of the conventional n-channel MOSFET in the type of double diffusion;

Fig. 3 is a cross sectional view showing an
5 example of the conventional n-channel MOSFET in the type of trench gate;

Fig. 4 is a graph that illustrates the relationship between an ideal breakdown voltage and an ideal ON resistance of each silicon n-channel
10 MOSFET;

Fig. 5A is a perspective illustration of the first example of a drift region structure of a semiconductor device in accordance with the present invention;

15 Fig. 5B is a perspective illustration of the second example of the drift region structure of the semiconductor device in accordance with the present invention;

Fig. 5C is a perspective illustration of the
20 third example of the drift region structure of the semiconductor device in accordance with the present invention;

Fig. 6A is a plan view showing a SOI-MOSFET in the type of vertically structured as the first
25 preferred embodiment of the semiconductor device in accordance with the present invention;

Fig. 6B is a cross sectional view taken along line A-A' in Fig. 6A;

Fig. 6C is a cross sectional view taken along line B-B' in Fig. 6A;

Fig. 7A is a plan view showing a SOI-MOSFET in the type of double diffusion as the second preferred
5 embodiment of the semiconductor device in accordance with the present invention;

Fig. 7B is a cross sectional view taken along line A-A' in Fig. 7A;

Fig. 7C is a cross sectional view taken along
10 line B-B' in Fig. 7A;

Fig. 8A is a plan view showing a SOI-MOSFET in the type of vertically structured as the third preferred embodiment of the semiconductor device in accordance with the present invention;

15 Fig. 8B is a cross sectional view taken along line A-A' in Fig. 8A;

Fig. 8C is a cross sectional view taken along line B-B' in Fig. 8A;

Fig. 9A is a plan view showing a MOSFET in the
20 type of vertically structured as the fourth preferred embodiment of the semiconductor device in accordance with the present invention;

Fig. 9B is a cross sectional view taken along line A-A' in Fig. 9A;

25 Fig. 9C is a cross sectional view taken along line B-B' in Fig. 9A;

Fig. 10 is a cross sectional view showing a p-channel MOSFET in the type of vertically structured

as the fifth preferred embodiment of the semiconductor device in accordance with the present invention;

Fig. 11 is a cross sectional view showing an n-channel MOSFET in the type of vertically structured as the sixth preferred embodiment of the semiconductor device in accordance with the present invention;

Fig. 12A is a plan view showing a trench gate n-channel MOSFET in the type of vertically structured as the seventh preferred embodiment of the semiconductor device in accordance with the present invention;

Fig. 12B is a cross sectional view taken along line A-A' in Fig. 12A;

Fig. 12C is a cross sectional view taken along line B-B' in Fig. 12A;

Fig. 12D is a cross sectional view taken along line C-C' in Fig. 12A;

Fig. 12E is a cross sectional view taken along line D-D' in Fig. 12A; and

Fig. 12F is a cross sectional view taken along line E-E' in Fig. 12A.

According to the present invention, a semiconductor device has a drift region which flows a drift current in the ON mode and is depleted in the OFF mode. The drift region is formed as a structure

having a plurality of divided substructures (i.e., divided regions) in parallel, such as a layered structure, a fiber structure, or a honeycomb structure, as shown in Figs. 5A to 5C. In addition, 5 the drift region comprises a plurality of the first conductive type divided drift path regions 1 and a plurality of the second conductive type compartment regions 2 in which each of the regions 2 is positioned among the adjacent regions 1 to make p-n 10 junctions.

In Fig. 5A, for example, the drift region comprises a group of parallel drift path substructures (i.e., complex structure) 100 consisting of: at least two 1st type (e.g., n-type) 15 divided drift path regions 1 where each of them is in the shape of a plate connected to another plate in parallel at least at its one end; and at least one 2nd conductive type (e.g., p-type) compartment regions 2 being sandwiched between the divided drift 20 path regions 1, 1 so as to make p-n junctions. In this figure, a plurality of 2nd type compartment regions 2 is shown. These 2nd compartment regions are connected in parallel with each other by their end portions to say the least of it.

25 The drift region 1 shown in Fig. 5B is in the type of a multiple fiber structure. It comprises a plurality of the first conductive type (n-type) drift path regions 1 and a plurality of the second

conductive type (p-type) compartment. Each region 1 or 2 is in the shape of a fiber. In a bundle of fibers (i.e., drift regions) , the regions 1 and 2 are arranged so as to form a check pattern thereof in
5 cross section.

Furthermore, the drift region shown in Fig. 5C, the 1st conductive type (i.e., n-type) divided drift path region 1 has connecting portions 1a in the four corners in cross section.

10 Additional 2nd conductive side regions 2a may be provided on the outermost surfaces (i.e., top and bottom surfaces) of the complex structure 100 as shown in Fig. 5A or four corners of the complex structure 100 as shown in Fig. 5B.

15 If the semiconductor device is in the ON mode, a drift current flows through a plurality of the divided drift path regions 1, 1 arranged in parallel. If the semiconductor device is in the OFF mode, on the other hand, an extent of a depletion layer
20 spreads out from each p-n junction between the first conductive type divided drift region 1 and the second conductive type compartment region 2 into the region 1 to reduce the density of charge carriers therein. In this case, the depletion can be accelerated by
25 laterally extending the outermost ends of the depletion region (i.e., the region in which there are no charge carriers) from both longitudinal sides of the second conductive compartment region, and also

the second conductive compartment region 2 is simultaneously depleted. Consequently, a breakdown voltage of the semiconductor device becomes high, so that the impurity concentration of the n-type drift
5 path region 1 can be increased to reduce the ON resistance. Especially in the present invention, as described above, the depletion region can be widened from both longitudinal sides of the second conductive type compartment region 2 into the adjacent regions
10 1, 1, respectively. Elongating ends of the depletion region act effectively on the respective divided drift path regions 1, 1, so that the total width of the second conductive type compartment region 2 to be required for forming the depletion layer may be
15 reduced, while the cross-sectional area of the first conductive divided drift path region 1 may be increased by about the same extent, resulting in the drop in the ON resistance compared with the conventional device. Accordingly, it is preferable
20 that the second conductive type compartment region 2 is prepared so as to have a comparatively small width thereof as much as possible. It is also preferable that the impurity concentration of the second conductive type compartment region 2 is low as much
25 as possible. In addition, the trade-off relationship between the ON resistance and the breakdown voltage can be eased if the number of the first conductive type divided drift path regions 1 per unit area

(i.e., the number of divided regions per unit area) is increased.

In the present invention, an equation that represents the trade-off relationship between an
5 ideal ON resistance r and a breakdown voltage BV for each of the first conductive type divided drift path region 1 corresponds to the following formula (10) obtained by modifying the formula (9) on the assumption that the width of the second conductive
10 compartment region 2 is infinitely small, in which the ON resistance r is N times higher than the ideal ON resistance R.

$$r = NR = BV^2 / 2\beta^2 E_C^3 \varepsilon_0 \varepsilon_{Si} \mu \quad (10)$$

The relationship between an ideal ON resistance R and
15 an ideal breakdown voltage BV of the complex structure of drift path substructures arranged in parallel can be represented by the formula:

$$R = BV^2 / 2N \beta^2 E_C^3 \varepsilon_0 \varepsilon_{Si} \mu \quad (11)$$

Therefore, the possibility of manufacturing a
20 semiconductor device having a considerably low ON resistance can be increased in a direct proportional relationship with the number of the divided drift regions.

In much the same fashion as a lateral type
25 semiconductor device formed on a silicon-on-insulator (SOI) or a semiconductor layer, a lateral type semiconductor device having a drift region formed on a semiconductor layer or on an insulation film on the

semiconductor layer, in which the drift region flows a drift current in the lateral direction if it is in the ON mode and depletes mobile charges if it is in the OFF mode. The drift region can be fabricated as 5 a stripe structure by alternately arranging the respective first conductive type divided drift path regions in the shape of stripe and the respective second conductive type compartment regions in the shape of stripe on a plane. The stripe shaped p-n 10 junction repeated structure on the plane may be formed by performing a photolithography one time, resulting in a simple manufacturing process and a low production cost for the semiconductor device.

Another structure of the drift region to be 15 formed in the lateral type semiconductor device may be a superposed parallel structure by alternatively laminating the respective first conductive type divided drift path region in the shape of flat layer and the respective second conductive type compartment 20 region in the shape of flat layer. A thickness of each layer can be precisely decreased as much as possible using a metal organic chemical vapor deposition (MOCVD) or a molecular beam epitaxy (MBE), so that the trade-off relationship between the ON 25 resistance and the breakdown voltage can be substantially eased.

By the way, it may be possible to prepare the drift region as the superposed structure with the

striped parallel structure.

If N = 2 in the above formula (10) or (11), the complex structure of parallel drift paths is made of two stripe-shaped divided drift path regions. Thus
5 the most simple drift region of the lateral type semiconductor device comprises a first conductive type divided drift region formed on a second conductive type semiconductor layer, an well-shaped second conductive type compartment region formed on
10 the first conductive type divided drift path region, another first conductive type divided drift path second region formed on a surface layer of the second conductive type compartment region and connected to the first conductive type divided drift path region.
15 The ON resistance of the semiconductor device can be reduced because of connecting the another first conductive type divided drift path region with the first conductive type divided drift path region in parallel.

20 A method for fabricating the above simple lateral type semiconductor comprises the steps of: forming a first n-type divided drift path region formed on a p-type semiconductor layer on a silicon by a thermal diffusion after performing a phosphorus
25 ion-implantation; forming an well-shaped p-type compartment region on the first n-type divided drift region by a thermal diffusion after performing a selective boron ion-implantation; thermally oxidizing

the obtained layer structure to form a second n-type divided drift path region on a surface thereof through the use of concentrated phosphorus ions which are unevenly distributed on a surface of the silicon and of diluted boron ions which are unevenly distributed into the oxidized film.

There is no reverse conductive type layer adjacent to the top layer of the second n-type divided drift path region, so that it is enough to provide a thin layer to readily deplete the second n-type divided drift path region. The fabrication method of the present invention does not require the step of doping impurities and it provide the second n-type divided drift region only by the step of the thermal oxidation, contributing to reduced cost and a reduced number of the steps for providing a way for the practical mass production of semiconductor devices.

Furthermore, another semiconductor device according present invention has a drift region formed on a semiconductor layer, in which the drift region feeds a drift current in the vertical direction if the device is in the ON mode and the drift region is depleted if the device is in the OFF mode, such as vertical type semiconductor devices including a semiconductor using a trench gate or the like and IGBT. The drift region comprises a plurality of first conductive type divided drift regions and a

plurality of second conductive compartment regions, in which each region is in the shape of layer in the vertical direction. The respective first conductive type divided drift regions and the respective second conductive type compartment regions are alternatively laminated in parallel in the lateral direction. In the process for fabricating this structure, an etching step can be required for forming a deep groove. In this case, however, it is also possible to substantially ease the trade-off relationship between the ON resistance and the breakdown voltage of the vertical type semiconductor device.

Embodiment 1

Referring now to Figs. 6A to 6C, a silicon-on-insulator (SOI) metal oxide semiconductor field-effect transistor (MOSFET) in the type of a lateral structure (hereinafter, referred as a lateral SOI-MOSFET) will be described in detail as a first preferred embodiment of the present invention. In these figures, Fig. 6A is a plan view of the lateral SOI-MOSFET, Fig. 6B is a cross sectional view along a line A-A' in Fig. 6A, and Fig. 6C is a cross sectional view along a line B-B' in Fig. 6A.

The lateral SOI-MOSFET of the present embodiment has the same structure as the offset gate structure of the n-channel MOSFET shown in Figs. 1A and 1B except in the structure of drain/drift region.

A structure of the lateral SOI-MOSFET comprises a p-type channel diffusion layer 7 formed on an insulation film 6 on a semiconductor substrate 5, a gate electrode 7 with a field plate formed on the channel diffusion region 7 via an insulation film 10, an n^+-type source region 8 formed on a portion of the gate electrode 11 where the portion is on the side of one end of the gate electrode 11, an n^+-type drain region 9 formed on a position at a predetermined distance from the other end of the gate electrode 11, a drain/drift region 190 which is extended between the diffusion region 7 and the drain region 9, and a thick insulation film 12 formed on the drain/drift region 190.

The drain/drift region 190 of the present embodiment consists of a plurality of divided regions in the shape of a stripe: n-type drift path regions 1 and p-type compartment regions 2, which are alternately arranged in parallel on a plane to form a parallel stripe structure. One end of each n-type drift path region 1 is connected to the p-type channel diffusion region 7 to form a p-n junction, while the other end thereof is connected to the n^+-type drain region 9 . Thus the n-type path regions 1 arranged in parallel form a drift path group 100 branched off from the n^+-type drain region 9. In addition, as shown in the figure, there is a p-type semiconductor region 2a adjacent to a longitudinal

side of the drift region 1 positioned at each side of the drift path group, and also each of the drift regions 1 is sandwiched between p-type semiconductor regions 2 (2a). Furthermore, one end of each p-type
5 semiconductor is connected to the p-type channel diffusion region 7, while the other end thereof is connected to the n^+-type drain region 9 to form a p-n junction. Therefore, the respective p-type compartment regions 2 are branched off from the p-
10 type channel diffusion region 7 and form parallel connection with the respective n^+-type drain regions 9.

If the lateral SOI-MOSFET is in the ON mode, carriers (electrons) flow from the n^+-type source
15 region 8 into a plurality of the n-type drift path regions 1 through a channel inversion layer directly below the gate insulation film 10 to cause a drift current by an electric field generated by voltage placed between the drain and the source. If it is in
20 the OFF mode, on the other hand, the channel inversion layer 13 directly below the gate insulation film 10 is disappeared and a depletion layer is widened from the p-n junction Ja between the n-type drift path region 1 and the p-type channel diffusion
25 region 7 and the p-n junction Jb between the n-type drift path region 1 and the p-type compartment region 2 into the n-drift path region 1, resulting in a depletion of the n-drift path region 1. In this

case, one end of the depletion layer is widened from the p-n junction Ja along a path length in the n-type drift path region 1 and the other end thereof is widened from the p-n junction Jb along a path width
5 in the n-type drift path region 1. That is, the depletion layer is widened from its both sides to accelerate the depletion. Therefore, the electric field strength is weakened and the breakdown voltage becomes high, so that the concentration of impurities
10 in the respective n-type drift path regions 1 may be increased. In this embodiment, particularly, the ends of the depletion are extended from both of the longitudinal sides of the p-type compartment region 2 into the adjacent n-type drift path regions 1, 1,
15 respectively, and thus the total width of the p-type compartment regions 2 can be reduced in half, while the cross-sectional area of the n-type drift path region 1 can be increased. It results in the drop in the ON-resistance in comparison with that of he
20 conventional device. In addition, the trade-off relationship between the ON resistance and the breakdown voltage is extensively weakened as the number N of the n-type drift path region 1 per unit area is increased. It is preferable that the wide of
25 the p-type compartment regions 2 is as small as possible.

For the sake of clarity, the ON resistance R of the lateral SOI-MOSFET of the present embodiment will

be compared with that of the conventional one in a concretive manner, for example under the following condition: the ideal breakdown voltage BV =100 V; the concentration of impurities in the first n-drift path
5 region 1 $N_D = 3 \times 10^{15}$ (cm^{-3}); the maximum electric field strength of silicon $E_C = 3 \times 10^5$ (V/cm); the mobility of electron $\mu = 1{,}000$ ($cm^2/V\cdot sec$); the dielectric constant of vacuum $\varepsilon_0 = 8.8 \times 10^{-12}$ (C/Vm); the relative dielectric constant of silicon $\varepsilon_{Si} =$
10 12; and the unit charge $q = 1.6 \times 10^{-19}$ (C).

In the case of the lower doping drain region 90 of the conventional device shown in Fig. 10, the ideal ON resistance R is 9.1 ($m\cdot ohm\cdot cm^2$) using the equations described above if the region 90 is in the
15 length of 6.6 μm and the thickness of 1 μm. In the case of the present embodiment, on the other hand, the ideal ON resistance R is dramatically dropped when the width W of each of the n-type drift path region 1 and the p-type compartment region 2 is less
20 than 1 μm. That is, R = 7.9 ($m\cdot ohm\cdot cm^2$) when W = 10 μm; R = 0.8 ($m\cdot ohm\cdot cm^2$) when W= 1 μm; and R = 0.08 ($m\cdot ohm\cdot cm^2$) when W = 0.1 μm if the length thereof is 5 μm, and β is 2/3. If the width of the p-type compartment region 2 is slightly larger than that of
25 the n-type drift path region 1, a noticeable improvement in the ideal ON resistance R can be further obtained. For the mass-production of semiconductor devices, by the way, it is difficult to

obtain the width of each region 1 or 2 less than 0.5 μm by means of photolithography and ion-implantation at the present time. In the near future, however, further reduction in the ON resistance of the lateral
5 SOI-MOSFET of the present embodiment will be achieved by lessening the wide of each region 1 or 2 less than 0.5 μm as micro-machining technology progresses.

The structure of the drift region to be applied in the present embodiment is of having repeated p-n
10 junctions of stripes on a plane, so that the structure can be processed by a single step of photolithography for a simplification of the manufacturing process to provide chips at the lowest cost.

15

Embodiment 2

Referring now to Figs. 7A to 7C, a double diffused type n-channel MOSFET (hereinafter, also referred as a double diffused MOSFET) will be
20 described in detail as a first preferred embodiment of the present invention. In these figures, Fig. 7A is a plan view showing the double diffused MOSFET, Fig. 7B is a cross sectional view along a line A-A' in Fig. 7A, and Fig. 7C is a cross sectional view
25 along a line B-B' in Fig. 7A.

The double diffused MOSFET of the present embodiment has the same structure as the conventional double diffused MOSFET shown in Figs. 2A and 2B

except in the structure of drain/drift region. As shown in the figure, the double diffused MOSFET of the present embodiment comprises a drain/drift region 122 formed on a p- or n-type semiconductor layer 4, a gate electrode 11 with a filed plate formed on the drain/drift region 122 through a gate insulation film 10, a p-type channel diffusion region 17 in the shape of an well formed on a portion of the p-type channel diffusion region 17 where the portion is on the side of one end of the gate electrode 11, an n^+-type source region 8 in the shape of an well formed in the p-type channel diffusion region 17, an n^+-type drain region 9 formed on a position at a predetermined distance from the other end of the gate electrode 11, a drain/drift region 122 which is extended between the n-type diffusion region 17 and the n^+-type drain region 9, and a thick insulation film 12 formed on the drain/drift region 122.

The drain/drift region 122 of the present embodiment consists of a plurality of divided regions in the shape of a stripe as the same way as that of the first preferred embodiment shown in Figs. 6A to 6C: n-type drift path regions 1 and p-type compartment regions 2, which are alternately arranged in parallel on a plane to form a parallel stripe structure. One end of each n-type drift path region 1 is connected to the p-type channel diffusion region 7 to form a p-n junction, while the other end thereof

is connected to the n^+-type drain region 9. Thus the n-type path regions 1 arranged in parallel form a drift path group 100 branched off from the n^+-type drain region 9. In addition, as shown in the figure,
5 there is a p-type semiconductor region 2a adjacent to a longitudinal side of the drift region 1 positioned at each side of the drift path group, and also each of the drift regions 1 is sandwiched between p-type semiconductor regions 2 (2a). Furthermore, one end
10 of each p-type semiconductor is connected to the p-type channel diffusion region 7, while the other end thereof is connected to the n^+-type drain region 9 to form a p-n junction. Therefore, the respective p-type compartment regions 2 are branched off from the p-
15 type channel diffusion region 7 and form parallel connection with the respective n+-type drain regions 9.

If the double diffused MOSFET is in the OFF mode, as in the same way as that of the first
20 embodiment, the channel inversion layer 13 directly below the gate insulation film 10 is disappeared and a depletion layer is widened from the p-n junction Ja between the n-type drift path region 1 and the p-type channel diffusion region 7 and the p-n junction Jb
25 between the n-type drift path region 1 and the p-type compartment region 2 into the n-drift path region 1, resulting in a depletion of the n-drift path region 1. In this case, one end of the depletion layer is

widened from the p-n junction Ja along a path length in the n-type drift path region 1 and the other end thereof is widened from the p-n junction Jb along a path width in the n-type drift path region 1. That
5 is, the depletion layer is widened from its both sides to accelerate the depletion. Therefore, the breakdown voltage becomes high, so that the concentration of impurities in the respective n-type drift path regions 1 may be increased to the drop in
10 the ON resistance.

For the sake of clarity, the ON resistance R of the double diffused MOSFET of the present embodiment will be compared with that of the conventional one shown in Fig. 2B under the same conditions as that of
15 the first embodiment at the ideal breakdown voltage BV = 100 V. In the case of the conventional device shown in Fig. 2B, the ideal ON resistance R is about 0.5 ($m\cdot ohm\cdot cm^2$) . In the case of the present embodiment, on the other hand, the ideal ON
20 resistance R is 0.4 ($m\cdot ohm\cdot cm^2$), if each of the drift path region 1 and the compartment region 2 has a thickness of 1 mm and a width of 0.5 μm. It is possible to drop the ON resistance extensively by further narrowing a width of each region 1 or 2.
25 Alternatively, it is also possible to drop the ON resistance extensively by enlarging a resistance cross-section of the drift path region 1 by thickening the respective drift path regions 1 and

the respective p-type compartment region 2. For example, the ON resistance R can be 1/10 of the conventional one if a thickness of the region 1 or 2 is 10 μm and it can be 1/100 of the conventional one
5 if a thickness of the region 1 or 2 is 100 μm. For the doping into such a thickened region, an impurity ion-implantation with a plurality of energy levels (or successive energy levels) may be performed on the same portion of the thickened region.

10

Embodiment 3

Figs. 8A to 8C show a lateral SOI-MOSFET as a third preferred embodiment of the present invention. In these figures, Fig. 8A is a plan view of the
15 lateral SOI-MOSFET, Fig. 8B is a cross sectional view along a line A-A' in Fig. 8A, and Fig. 8C is a cross sectional view along a line B-B' in Fig. 8A.

The lateral SOI-MOSFET of the present embodiment comprises a p-type channel diffusion layer
20 77 formed on a semiconductor substrate 5 through an insulation layer 6, a trench gate electrode 111 formed on the p-type channel diffusion layer 77 through a gate insulation film 10, a plurality of n^+-type source regions 88 formed in the top side of the
25 p-type n-channel diffusion layer 77 and adjacent to an upper edge of the trench gate electrode 111, a n^+-type drain region 99 formed on a position at a predetermined distance from the gate electrode 111, a

drain/drift region 290 which is extended between the drain region and the gate electrode; and a thick insulation film 12 formed on the drain/drift region 290.

5 The drain/drift region 290 of the present embodiment, as distinct from that of the first embodiment, is provided as a stacked layer structure in which the respective n-type drift path regions 1 and the respective p-type compartment regions 2 are 10 alternatively stacked in parallel, repeatedly. In this case, each of these regions 1, 2 is in the shape of a plate. As shown in the figure, an additional p-type compartment region 2a as a bottom end region of the drain/drift region 290 is positioned at the side 15 of the bottom n-type drift region 1, and also another additional p-type compartment region 2a as a top end region of the drain/drift region 290 is positioned at the side of the top n-type drift region 1. A net doping concentration of each of the regions 2a is 20 less than $2 \times 10^{12}/cm^2$. One end of each of the respective n-type drift path region 1 is connected to the p-type channel diffusion layer 77 to form a p-n junction, while the other end thereof is connected to the n^+-type drain region 99. Thus the n^+-type path 25 regions 1 arranged in parallel form a drift path group 100 which is branched off from the n-type drain region 99. In addition, as shown in the figure, one end of each of the p-type compartment regions 2 is

connected to the p-type channel diffusion layer 77, while the other end thereof is connected to the n^+-type drain region 99 to form a p-n junction. Thus the p-type compartment regions 2 are branched off
5 from the p-type channel diffusion layer and arranged in a parallel connection.

In this embodiment, furthermore, an ideal ON resistance of the lateral SOI-MOSFET can be calculated by the formula (11) described above. In
10 this case, N is the number of the stacked n-type drift path regions. If the ideal breakdown voltage is 100V, the ideal ON resistance R is 0.5 (m·ohm·cm^2) for the conventional structure (N = 1) but 0.05 (m·ohm·cm^2) for the present structure (N = 10). It
15 means that the ON resistance R is substantially dropped in inverse proportion to the number N of divided regions 1.

As described above, basic technologies for fabricating the structures shown in Figs. 6A to 6C
20 and Figs. 7A to 7C are photolithography and ion implantation. In this embodiment shown in Figs. 8A to 8C, on the other hand, a crystal growth technique is used because the plate-shaped regions 1, 2 should be stacked in alternate order. A total thickness of
25 the whole regions 1, 2 and a period of performing the crystal growth are increased in proportionate to the number of the regions 1, 2 to be stacked. Thus an unequal distribution of the impurities cannot be

ignored because the impurities tends to diffuse in the respective thicken regions. Preferably, a thickness of each regions 1, 2 should be reduced as much as possible to perform the crystal growth at a low temperature enough to ignore the unequal distribution. Comparing with an epitaxial growth heavily used in the conventional silicon-processing technologies, it is preferable to use a metal organic chemical vapor deposition (MOCVD) and a molecular beam epitaxy (MBE), which are generally applied in the fabrication of compound semiconductors such as a gallium arsenide semiconductor, in the present embodiment. These techniques can be provided as micro-machining techniques which contribute to reduce the ON resistance by an effect of thinning the plate-shaped n-type drift path regions 1 and the plate-shaped p-type compartment regions 2.

In this embodiment, by the way, the difficulty of forming a channel inversion layer 13 is increased if the concentration of impurities is increased by thinning those regions 1, 2. Consequently, it is difficult to drop the ON resistance because of the difficulty of lowering the channel resistance. To solve this problem, it is preferable to make a low concentrated area on a part of the region where the gate insulation membrane 10 touches one of the n-type drift regions 1 and the p-type compartment regions 2.

Embodiment 4

Referring now to Figs. 9A to 9C, a lateral MOSFET will be described in detail as a preferred embodiment of the present invention. In these 5 figures, Fig. 9A is a plan view showing the lateral MOSFET, Fig. 9B is a cross sectional view along a line A-A' in Fig. 9A, and Fig. 9C is a cross sectional view along a line B-B' in Fig. 7A.

The lateral MOSFET of the present embodiment 10 comprises a p-type channel diffusion layer 77 formed on a p^-- or n^--type semiconductor substrate 7, a trench gate electrode 111 formed on side wall of the p-type channel diffusion layer 77 through a gate insulation film 10, a plurality of n^+-type source 15 regions 88 formed in the top end of the p-type n-channel diffusion layer 77 and adjacent to an upper edge of the trench gate electrode 111, a n^+-type drain region 99 formed on a position at a predetermined distance from the gate electrode 111, a 20 drain/drift region 290 which is extended between the drain region and the gate electrode; and a thick insulation film 12 formed on the drain/drift region 290.

The drain/drift region 290 of the present 25 embodiment, as the same as that of the third embodiment, is provided as a stacked layer structure in which the respective n-type drift path regions 1 and the respective p-type compartment regions 2 are

alternatively stacked in parallel, repeatedly. In this case, each of these regions 1, 2 is in the shape of a plate. As shown in the figure, an additional p-type compartment region 2a as a bottom end region of the drain/drift region 290 is positioned at the side of the bottom n-type drift region 1, and also another additional p-type compartment region 2a as a top end region of the drain/drift region 290 is positioned at the side of the top n-type drift region 1. A net doping concentration of each of the regions 2a is less than 2 x $10^{12}/cm^2$. One end of each of the respective n-type drift path region 1 is connected to the p-type channel diffusion layer 77 to form a p-n junction, while the other end thereof is connected to the n^+-type drain region 99. Thus the n^+-type path regions 1 arranged in parallel form a drift path group 100 which is branched off from the n-type drain region 99. In addition, as shown in the figure, one end of each of the p-type compartment regions 2 is connected to the p-type channel diffusion layer 77, while the other end thereof is connected to the n^+-type drain region 99 to form a p-n junction. Thus the p-type compartment regions 2 are branched off from the p-type channel diffusion layer and arranged in a parallel connection.

In this embodiment, as in the case of the third embodiment, it is possible to reduce the ON resistance and to increase the breakdown voltage.

The relationship between the structure of the present embodiment and that of the third embodiment shown in Figs. 8A to 8C corresponds to the relationship between the second embodiment shown in Figs. 7A to 7C
5 and the first embodiment shown in Figs. 6A to 6C. That is, the structure of the present invention is not of SOI, so that it is possible to fabricate the semiconductor device at a low cost.

10 Embodiment 5

Fig. 10 is a cross sectional view of a lateral p-channel MOSFET as a fifth preferred embodiment of the present invention, corresponding to that of Fig. 2A except for the drain/drift region.

15 The lateral p-channel MOSFET of the present embodiment comprises a n-type channel diffusion layer 3 formed on a p^--type semiconductor layer 4,, a gate electrode 11 with a filed plate formed on the n-type channel diffusion layer through a gate insulation
20 film 10, a p^+-type source region 28 in the shape of an well formed on a portion of the n-type channel diffusion region 3 where the portion is on the side of one end of the gate electrode 11, a p-type drain/drift region 14 in the shape of an well formed
25 in the n-type channel diffusion region 3 where the portion is directly below the other end of the gate electrode 11, a n-type compartment region 2a as a top side region formed on a surface of the p-type

drain/drift region 14, a p^+-type drain region 19 formed on a position at a predetermined distance from the other end of the gate electrode 11, an n^+-type contact region 71 adjacent to the p^+-type source region 18, and a thick insulation film 12 formed on the p-type drain/drift region 14. In this embodiment, the number of divided drain regions N is one (1), so that the p-type drain/drift region 14 corresponds to a stripe of the drain path region 1 in the cross sectional view. A thickness of the n-type top side region 2b on the p-type drain/drift region 14 is formed as a thin film for the purpose of expediting the depletion. Comparing with the structure of Fig. 2A, the n-type top side region 2b is provided in the present structure for accelerating the depletion by providing a depletion layer from the channel diffusion layer 3 under the p-type drain/drift region 14 and another depletion layer from the n-type top side region 2a above the p-type drain/drift region 14. The net doping concentration of the drain/drift region 14 of the conventional structure shown in Fig. 2A is approximately 1×10^{12} / cm^2, while the structure of the present invention has the net doping concentration of approximately 2×10^{12} / cm^2 which is more than twice as much as that of the conventional one. According to the present embodiment, therefore, it is possible to reduce the ON resistance as a result of increasing the

concentration of impurities in the drain/drift region in addition to increase the breakdown voltage.

Embodiment 6

5 Fig. 11 is a cross sectional view showing a double diffused n-channel MOSFET in the type of a lateral structure (hereinafter, simply referred as a double diffused MOSFET) as a sixth preferred embodiment of the present invention, corresponding to 10 that of Fig. 2B except for the drain/drift region.

The double diffused MOSFET comprises a drain/drift region 22 (i.e., a first n-type drift region 1) formed on a p-type semiconductor layer 4 (i.e., a p-type bottom side region 2a), a gate 15 electrode 11 with a field plate formed on the drain/drift region 22 through a gate insulation film 10, a p-type channel diffusion region 17 in the shape of an well formed on a portion of the drain/drift region 22 where the portion is positioned at the side 20 of one end of the gate electrode 11, an n^+-type source region 8 in the shape of an well formed in the p-type channel diffusion region 17, a p-type top layer 24 (i.e., a p-type compartment region 2) formed on a surface layer between the gate electrode 11 and 25 the n+-type drain region 9 positioned at a predetermined distance from the gate electrode 11, a second drift path region 1 formed on a surface of the p-type compartment region 2, a p^+-type contact region

72 adjacent to the n^+-type source region 8, and a thick insulation layer 12 formed on a p-type compartment region 2.

The drain/drift region 22 as a lower layer and the drift path region 1 as an upper layer are contacted together in parallel through the p-type compartment region 2. In the present embodiment, comparing with the structure of Fig. 2B, the drift region 1 is additionally provided on the p-type compartment region 2. As described above, it is possible to increase the breakdown voltage as a result of widening the depletion layers from the p-type compartment region 2 to the drain/drift region 22 as the under layer thereof and to the drift path region 1 as the upper layer thereof, respectively, resulting in the drop in the ON resistance. The net doping concentration of the drift region 22 of the structure shown in Fig. 2B is approximately 2×10^{12} / cm^2, while the structure of the present invention has the net doping concentration (i.e., the sum of doping concentration of the under layered drain/drift region 22 and the upper layered drift path region 1) of approximately 3×10^{12} / cm^2 which is 1.5-fold concentration of the conventional one. According to the present embodiment, therefore, it is possible to obtain the trade-off relationship between the ideal breakdown voltage and the ideal ON resistance represented by the line D in Fig. 4. As is evident

from the above description, it is revealed that the above trade-off relationship can be eased by the present structure compared with the conventional one.

A method for fabricating the structure of each of the fifth and sixth embodiments includes the steps of: forming a n-type semiconductor layer 3 (32) by implanting phosphorus ions into a p-type semiconductor and subjecting to a heat treatment (i.e., thermal dispersion); forming a p-type region 14 (24) on a surface of the n-type semiconductor layer 3 (22) by selectively implanting boron ions and subjecting to a heat treatment (i.e., thermal dispersion), and subjecting the obtained intermediate structure to a thermal oxidization to form a thin n-type top side region 2b (i.e., a n-type drift path region 1) on a surface layer through the use of concentrated phosphorus ions which are unevenly distributed on a surface of the silicon and diluted boron ions which are unevenly distributed into the oxidized film. In this case, there is no reverse conductive type layer adjacent to the upper layer of the n-type drift path region 1 or the n-type top side region 2b, so that it is enough to provide a thin layer to readily deplete the second n-type drift path region. The fabrication method of the present embodiment does not require the step of doping impurities and it provide the n-type top side region 2b (n-type drift path region 1) only by the step of

the thermal oxidation, contributing a way for reducing the total number of steps and the practical mass production of semiconductor devices.

In the fifth preferred embodiment, the gate insulation film 10 and the drain/drift region 14 are separated by the n-type top side region 2b because the n-type top side region 2b is unwillingly formed on a substantially whole surface of the silicon surface layer using the above fabrication method. In this case, however, there is no problem occurred. The drain/drift region 14 can be electrically conducted by a channel inversion layer formed directly underneath the gate 10 if the n-type top side region 2b is formed as a thin film.

Embodiment 7

Figs. 12A to Figs. 12F show a trench gate n-channel MOSFET in the type of a vertical structure (hereinafter, referred as a vertical MOSFET) as a seventh embodiment of the present invention. In these figures, Fig. 12A is a plan view showing the vertical MOSFET; Fig. 12B is a cross sectional view along a line A-A' in Fig. 12A; Fig. 12C is a cross sectional view along a line B-B' in Fig. 12A; Fig. 12D is a cross sectional view along a line C-C' in Fig. 12A; Fig. 12E is a cross sectional view along a line D-D' in Fig. 12A; and Fig. 12F is a cross sectional view along a line E-E' in Fig. 12A.

The vertical MOSFET comprises an n^+-type drain layer 29 electrically contacted to a back electrode (not shown), a drain/drift region 139 formed on the n^+-type drain layer 29, a trench gate electrode 21
5 imbedded in a trench formed on a surface of the drain/drift region 139 via a gate insulation film 10, a p-type channel diffusion layer 27 formed on a surface of the drain/drift region 139 at a relatively shallow depth compared with that of the trench gate
10 electrode 21, a n^+-type source region 18 formed along an upper edge of the trench gate electrode 21, and a thick insulation film 12 as a sheathing of the gate electrode 21. By the way, it is possible to make a n type IGBT structure using a p-type layer or a double
15 layered structure made of an n^+-type upper layer and a p^+-type under layer instead of the single layered n^+-type drain layer 29.

According to the present embodiment, as shown in Figs. 12D and 12E, the drain/drift region 139
20 comprises a plurality of plate-shaped divided regions in the vertical direction, in which n-type drift path regions 1 and p-type compartment regions, which are alternately arranged in parallel in the vertical direction to form a parallel stripe structure. An
25 upper end of each n-type drift path region 1 is connected to the p-type channel diffusion layer 27 to form a p-n junction, while a lower end thereof is connected to a n^+-type drain layer 29 . Thus the n-

type drift path region 1 arranged in parallel form a drift path group 100 branched off from the n^+-type drain layer 29. In addition, not shown in the figure, there is a p-type semiconductor side region
5 adjacent to a longitudinal side of the drift region 1 positioned at each side of the drift path group, and also each of the drift regions 1 is sandwiched between p-type semiconductor side regions or p-type compartment regions. Furthermore, the upper end of
10 each of the p-type compartment regions 2 is connected to the p-type channel diffusion layer 27, while the lower end thereof is connected to the n^+-type drain layer 29 to form a p-n junction. Therefore, the respective p-type compartment regions 2 are branched
15 off from the p-type channel diffusion region 27 and form parallel connection with the respective n^+-type drain regions 29.

If the vertical MOSFET is in the OFF mode, the channel inversion layer 13 directly below the gate
20 insulation film 10 is disappeared. By an effect of the potential between the drain and the source, in addition, depletion layers are widened from the p-n junction Ja between the n-type drift path region 1 and the p-type channel diffusion region 27 and the p-
25 n junction Jb between the n-type drift path region 1 and the p-type compartment region 2 into the n-drift path region 1, resulting in a depletion of the n-drift path region 1. In this case, one end of the

depletion layer is widened from the p-n junction Ja along a path length in the n-type drift path region 1 and the other end thereof is widened from the p-n junction Jb along a path width in the n-type drift path region 1. That is, the depletion layer is widened from its both sides to accelerate the depletion, and at the same time the p-type compartment region 2 is also depleted. Especially in the present invention, as described above, the depletion region can be extended from both longitudinal sides of the second conductive type compartment region 2 into the adjacent regions 1, 1, respectively. Elongating ends of the depletion region act effectively on the respective divided drift path regions 1, 1, so that the total width of the second conductive type compartment region 2 to be required for forming the depletion layer may be reduced, while the cross-sectional area of the first conductive divided drift path region 1 may be increased by about the same extent, resulting in a drop in the ON resistance compared with the conventional device. In addition, the trade-off relationship between the ON resistance and the breakdown voltage can be relaxed roughly proportional to increase the number of the n-type divided drift path regions 1 per unit area (i.e., the number of divided regions per unit area).

For the sake of clarity, the ON resistance R of

the vertical MOSFET of the present embodiment will be compared with that of the conventional n-channel MOSFET of Fig. 3 with the ideal breakdown voltage BV =100 V.

In the case of the conventional one, the ideal ON resistance R is approximately 0.6 (m·ohm·cm^2) according to the line A in Fig. 4. In the case of the present embodiment, on the other hand, the ideal ON resistance R is 1.6 (m·ohm·cm^2) when W = 10 μm; 0.16 (m·ohm·cm^2) when W= 1 μm; and 0.016 (m·ohm·cm^2) when W = 0.1 μm if a depth (path length) of each of the n-type drift path region 1 and the p-type compartment region 2 is 5 μm and β is 2/3. Therefore, a noticeable reduction of the ideal ON resistance R can be further obtained. If the width of the p-type compartment region 2 is slightly larger than that of the n-type drift path region 1, a further noticeable improvement in the ideal ON resistance R can be obtained. For the mass-production of semiconductor devices, by the way, it is difficult to obtain the width of each region 1 or 2 less than 0.5 μm by means of photolithography and ion-implantation at the present time. In the near future, however, further reduction in the ON resistance of the vertical MOSFET of the present embodiment will be achieved by lessening the wide of each region 1 or 2 less than 0.5 μm as micro-machining technology progresses.

Comparing with the lateral semiconductor structure, the vertical semiconductor structure having the repeat of n-type divided drift regions 1 and p-type divided compartment regions 2 arranged in 5 the vertical direction may be difficult to fabricate. However, it may be possible to fabricate the vertical semiconductor structure by the process including the steps of: forming a n-type layer on a drain region 29 by means of epitaxial growth; removing the 10 predetermined portions of the n-type layer by means of etching to form a plurality of grooves in the shape of stripes at established spacing; and molding the etched grooves by means of p-type epitaxial growth and removing undesired portions, or by the 15 process including the steps of selectively implanting neutrons or high energy particles having long ranges and performing a nuclear transformation of the implanted particles to selectively form a deep reverse conductive region.

20 The invention has been described in detail with respect to various embodiments. The structure associated with the present invention is not limited to the drain/drift region of MOSFET described above. It is also possible to use a semiconductor region 25 which becomes a depletion region if the device is in the OFF mode and also becomes a drift region if the device is in the ON mode, and furthermore most of the semiconductor elements such as an IGBT, a bipolar

transistor, a semiconductor diode, a JFET, a thyristor, a MESFET, and a HEMT. According to the present invention, the conductive type can be changed to a reversed conductive type in case of necessity. 5 In Figs. 5A to 5C, there are the structures having a plurality of divided substructures in parallel, such as a layered structure, a fiber structure, and a honeycomb structure, respectively, but not limited to these shapes. It is also possible to use other 10 shapes.

As described above, the present invention has the features including: a set of first conductive type drift regions as a parallel divided structure, in which each of the divided drift region flows a 15 drift current if it is in the ON mode while it is depleted if it is in the OFF mode; and a second conductive type compartment region placed in an interface of the side surfaces of the adjacent drift regions to form a p-n junction.

20 Accordingly, the present invention produces at least the following effects.

(1) The depletion region can be widened from both longitudinal sides of the second conductive type compartment region into the adjacent regions, 25 respectively. Widening ends of the depletion region act effectively on the respective divided drift path regions, so that the total width of the second conductive type compartment region to be required for

forming the depletion layer may be reduced, while the cross-sectional area of the first conductive divided drift path region may be increased by about the same extent, resulting in the drop in the ON resistance compared with the conventional device. Accordingly, the trade-off relationship between the ON resistance and the breakdown voltage can be eased if the number of the first conductive type divided drift path regions per unit area (i.e., the number of divided regions per unit area) is increased.

(2) The drift region can be fabricated as a stripe structure by alternately arranging the respective first conductive type divided drift path regions in the shape of stripe and the respective second conductive type compartment regions in the shape of stripe on a plane. The stripe shaped p-n junction repeated structure on the plane may be formed by performing a photolithography one time, resulting in a simple manufacturing process and a low production cost for the semiconductor device.

(3) The drift region to be provided in the lateral type semiconductor device may be a superposed parallel structure by alternatively laminating the respective first conductive type divided drift path region in the shape of flat layer and the respective second conductive type compartment region in the shape of flat layer. A thickness of each layer can be precisely decreased as much as possible using a

metal organic chemical vapor deposition (MOCVD) or a molecular beam epitaxy (MBE), so that the trade-off relationship between the ON resistance and the breakdown voltage can be substantially eased.

5 (4) The most simple drift region of the lateral type semiconductor device comprises a first conductive type divided drift region formed on a second conductive type semiconductor layer, an well-shaped second conductive type compartment region formed on 10 the first conductive type divided drift path region, another first conductive type divided drift path second region formed on a surface layer of the second conductive type compartment region and connected to the first conductive type divided drift path region. 15 The ON resistance of the semiconductor device can be reduced because of connecting the another first conductive type divided drift path region with the first conductive type divided drift path region in parallel. In this structure, there is no reverse 20 conductive type layer adjacent to the upper layer of the secondary first conductive type divided drift path region, so that the depletion can be easily obtained with the decrease in a thickness of the layer.

25 (5) The fabrication method of the present invention does not require the step of doping impurities and it provide the second n-type divided drift region only by the step of the thermal oxidation, contributing to

reduced cost and a reduced number of the steps for providing a way for the practical mass production of semiconductor devices.

(6) The drift region of the vertical type semiconductor device comprises a plurality of first conductive type divided drift regions and a plurality of second conductive compartment regions, in which each region is in the shape of layer in the vertical direction. The respective first conductive type divided drift regions and the respective second conductive type compartment regions are alternatively stacked in parallel in the lateral direction. In the process for fabricating this structure, an etching step can be required for forming a deep groove. In this case, however, it is also possible to substantially ease the trade-off relationship between the ON resistance and the breakdown voltage of the vertical type semiconductor device.

CLAIMS:

1. A semiconductor device having a drift region which flows a drift current if it is in an ON mode
5 and is depleted if it is in an OFF mode, characterized in that

the drift region is formed as a structure having a plurality of first conductive type divided drift path regions which are connected together in
10 parallel to form a group of parallel drift paths and a plurality of second conductive type side regions, in which each of the second conductive type side regions is positioned between adjacent the first conductive type divided drift path regions to form p-
15 n junctions.

2. A semiconductor device as claimed in claim 1, further characterized by comprising:

at least one additional second side region
20 which is connected to an outer side of a first conductive type divided drift path region positioned at an outer side of the group of parallel drift paths.

25 3. A semiconductor device having a drift region which flows a drift current if it is in an ON mode and is depleted if it is in an OFF mode, and the drift current flows in a lateral direction and the

drift region is formed on a semiconductor or an insulation film on the semiconductor, characterized in that

the drift region is formed as a parallel stripe
5 structure in which a plurality of stripe-shaped first conductive divided drift path regions and a plurality of stripe-shaped second conductive type compartment regions are alternatively arranged on a plane one by one in parallel.

10

4. A semiconductor device having a drift region which flows a drift current if it is in an ON mode and is depleted if it is in an OFF mode, and the drift current flows in a lateral direction and the
15 drift region is formed on a semiconductor or an insulation film on the semiconductor, characterized in that

the drift region is formed as a parallel stacked structure in which a plurality of layer-
20 shaped first conductive divided drift path regions and a plurality of layer-shaped second conductive type compartment regions are alternatively stacked on a plane one by one in parallel.

25 5. A semiconductor device having a drift region which flows a drift current if it is in an ON mode and is depleted if it is in an OFF mode, and the drift current flows in a lateral direction and the

drift region is formed on a second conductive type semiconductor, characterized in that

the drift region comprises:

a first conductive type divided drift region formed on the second conductive type semiconductor layer;

an well-shaped second conductive type compartment region formed on the first conductive type divided drift path region; and

a secondary first conductive type divided drift path region formed on a surface layer of the well-shaped second conductive type compartment region and connected to the first conductive type divided drift path region in parallel.

6. A semiconductor device having a drift region which flows a drift current if it is in an ON mode and is depleted if it is in an OFF mode, and the drift current flows in a vertical direction and the drift region is formed on a semiconductor, characterized in that

the drift region comprises a plurality of first conductive type divided drift regions in which each of them has a layer structure along the vertical direction and a plurality of first conductive type compartment regions in which each of them has a layer structure along the vertical direction, and

the plurality of first conductive type divided

drift regions and the plurality of first conductive type compartment regions are stacked one by one in parallel in a direction perpendicular to the vertical direction to form a laterally stacked parallel
5 structure.

7. A method of manufacturing a semiconductor device having a drift region which flows a drift current if it is in an ON mode and is depleted if it is in an
10 OFF mode, and the drift current flows in a lateral direction and the drift region is formed on a second conductive type semiconductor, where the drift region has: a first conductive type divided drift region formed on the second conductive type semiconductor
15 layer; an well-shaped second conductive type compartment region formed on the first conductive type divided drift path region; and a secondary first conductive type divided drift path region formed on a surface layer of the well-shaped second conductive
20 type compartment region and connected to the first conductive type divided drift path region in parallel, characterized by comprising steps of:

forming a first conductive type divided drift path region on a second conductive type semiconductor
25 layer made of silicon by a thermal diffusion after performing a phosphorus ion-implantation;

forming an well-shaped second conductive type compartment region on the first conductive type

divided drift region by a thermal diffusion after performing a selective boron ion-implantation; and

thermally oxidizing a structure obtained by the selective boron ion-implantation to form a secondary
5 first conductive type divided drift path region on a surface thereof through use of a concentration of phosphorus ions which are unevenly distributed on a surface of the silicon and a dilution of boron ions which are unevenly distributed into an oxidized film.

8. A semiconductor device constructed, adapted and arranged to operate substantially as described hereinbefore with reference to and as shown in any of figures 5 to 12 of the accompanying drawings.

The Patent Office

61

Application No: GB 9701204.1
Claims searched: All

Examiner: C.D.Stone
Date of search: 3 April 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K(KKAX,KCAD,KCAV)

Int Cl (Ed.6): H01L

Other: ON LINE,W.P.I.

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	EP 0164096 A2 EATON	
X	US 4963947 TELEFUNKEN	3,4

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
		E	Patent document published on or after, but with priority date earlier than, the filing date of this application.
&	Member of the same patent family		