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(54) **Title:** MIRROR ARRAY DEVICE

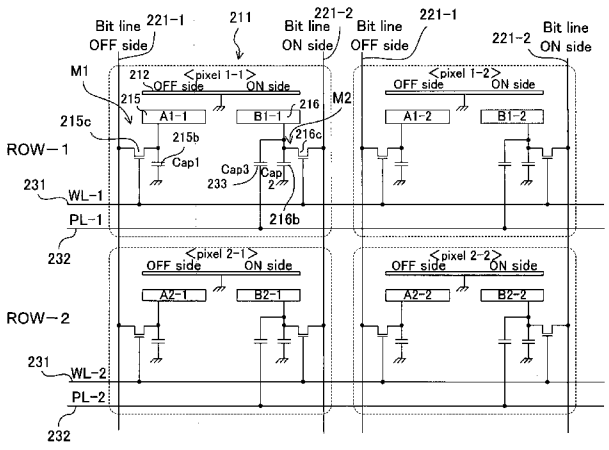

Fig. 10A

(57) **Abstract:** The present invention provides a mirror array device, comprising: a plurality of mirror elements each comprising a hinge and a deflectable mirror supported by the hinge; a memory cell for controlling the mirror element; a bit line for transmitting a data signal to the memory cell; a word line for controlling a connection between the bit line and the memory cell; a plate line for controlling the memory cell. Each of the mirror elements further comprises a first address electrode controlled by the word line to connect to the memory cell. Each of the mirror elements further comprises a second address electrode electrically connected to the plate line.

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MIRROR ARRAY DEVICE

Cross Reference to Related Applications

This application is a Non-provisional Application claiming a Priority date of November 16, 2007 based on a previously filed Provisional Application 61/003,372 and a Non-provisional Patent Application 11/121,543 filed on May 3, 2005 issued into Patent 7,268,932. The Application 11/121,543 is a Continuation In Part (CIP) Application of three previously filed Applications. These three Applications are 10/698,620 filed on November 1, 2003, 10/699,140 filed on November 1, 2003 now issued into Patent 6,862,127, and 10/699,143 filed on November 1, 2003 now issued into Patent 6,903,860 by the Applicant of this Patent Applications. The disclosures made in these Patent Applications are hereby incorporated by reference in this Patent Application.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to systems and methods to configure a projection apparatus comprising a spatial light modulator. More particularly this invention relates to systems and methods for implementing a new and improved spatial light modulator in a projection apparatus to achieve a higher quality of image display.

Description of the Related Art

After the dominance of CRT technology in the display industry for over 100 years, Flat Panel Display (FPD) and Projection Display have gained popularity because of their space efficiency and larger screen size. Projection displays using micro-display technology are gaining popularity among consumers because of their high picture quality and lower cost. There are two types of micro-displays used for projection displays in the market. One is micro-LCD (Liquid Crystal Display) and the other is micro-mirror technology. Because a micro-mirror device uses un-polarized light, it produces better brightness than micro-LCD, which uses polarized light.

Although significant advances have been made in technologies of implementing electromechanical micro-mirror devices as spatial light modulators, there are still limitations in their high quality images display. Specifically, when display images are digitally controlled, image quality is adversely due to an insufficient number of gray scales.

Electromechanical micro-mirror devices have drawn considerable interest because of their application as spatial light modulators (SLMs). A spatial light modulator requires an array of a relatively large number of micro-mirror devices. In general, the number of required devices ranges from 60,000 to several million for each SLM. Referring to Fig. 1A, an image display system 1 including a screen 2 is disclosed in a relevant US Patent 5,214,420. A light source 10 is used to generate light beams to project illumination for the display images on the display screen 2. The light 9 projected from the light source is further concentrated and directed toward lens 12 by

way of mirror 11. Lenses 12, 13 and 14 form a beam columnator operative to columnate the light 9 into a column of light 8. A spatial light modulator 15 is controlled by a computer through data transmitted over data cable 18 to selectively redirect a portion of the light from path 7 toward lens 5 to display on screen 2. Fig. 1B shows a SLM 15 that has a surface 16 that includes an array of switchable reflective elements 17, 27, 37, and 47, each of these reflective elements is attached to a hinge 30. When the element 17 is in an ON position, a portion of the light from path 7 is reflected and redirected along path 6 to lens 5 where it is enlarged or spread along path 4 to impinge on the display screen 2 to form an illuminated pixel 3. When the element 17 is in an OFF position, the light is reflected away from the display screen 2 and, hence, pixel 3 is dark.

The on-and-off states of the micromirror control scheme, as that implemented in the Patent 5,214,420 and in most conventional display systems, impose a limitation on the quality of the display. Specifically, applying the conventional configuration of a control circuit limits the gray scale gradations produced in a conventional system (PWM between ON and OFF states), limited by the LSB (least significant bit, or the least pulse width). Due to the ON-OFF states implemented in the conventional systems, there is no way of providing a shorter pulse width than the duration represented by the LSB. The least quantity of light, which determines the gray scale, is the light reflected during the least pulse width. The limited levels of gray scale lead to a degradation of the display image.

Specifically, Fig. 1C exemplifies, as related disclosures, a circuit diagram for controlling a micromirror according to US Patent 5,285,407. The control circuit includes memory cell 32. Various transistors are referred to as "M*" where "*" designates a transistor number and each transistor is an insulated gate field effect transistor. Transistors M5, and M7 are p-channel transistors; transistors, M6, M8, and M9 are n-channel transistors. The capacitances, C1 and C2, represent the capacitive loads in the memory cell 32. The memory cell 32 includes an access switch transistor M9 and a latch 32a based on a Static Random Access switch Memory (SRAM) design. All access transistors M9 on a Row line receive a DATA signal from a different Bit-line 31a. The particular memory cell 32 is accessed for writing a bit to the cell by turning on the appropriate row select transistor M9, using the ROW signal functioning as a Word-line. Latch 32a consists of two cross-coupled inverters, M5/M6 and M7/M8, which permit two stable states that include a state 1 when is Node A high and Node B low, and a state 2 when Node A is low and Node B is high.

The control circuit positions the micro-mirrors to be at either an ON or an OFF angular orientation, as that shown in Fig. 1A. The brightness, i.e., the number of gray scales of display for a digitally control image system, is determined by the length of time the micro-mirror stays at an ON position. The length of time a micromirror is in an ON position is controlled by a multiple bit word. Fig. 1D shows the "binary time intervals" when controlling micromirrors with a four-bit word. As shown in Fig. 1D, the time durations have relative values of 1, 2, 4, 8, which in turn

define the relative brightness for each of the four bits where "1" is the least significant bit and "8" is the most significant bit. According to the control mechanism as shown, the minimum controllable differences between gray scales for showing different levels of brightness is a represented by the "least significant bit" that maintains the micromirror at an ON position.

For example, assuming n bits of gray scales, one time frame is divided into $2^n - 1$ equal time periods. For a 16.7-millisecond frame period and n-bit intensity values, the time period is $16.7/(2^n - 1)$ milliseconds.

Having established these times for each pixel of each frame, pixel intensities are quantified such that black is a 0 time period, the intensity level represented by the LSB is 1 time period, and the maximum brightness is $2^n - 1$ time periods. Each pixel's quantified intensity determines its ON-time during a time frame. Thus, during a time frame, each pixel with a quantified value of more than 0 is ON for the number of time periods that correspond to its intensity. The viewer's eye integrates the pixel brightness so that the image appears the same as if it were generated with analog levels of light.

For controlling deflectable mirror devices, the PWM applies data to be formatted into "bit-planes", with each bit-plane corresponding to a bit weight of the intensity of light. Thus, if the brightness of each pixel is represented by an n-bit value, each frame of data has the n-bit-planes. Then, each bit-plane has a 0 or 1 value for each mirror element. According to the PWM control scheme described in the preceding paragraphs, each bit-plane is independently loaded and the mirror elements are controlled according to bit-plane values corresponding to the value of each bit during one frame. Specifically, the bit-plane according to the LSB of each pixel is displayed for 1 time period.

Meanwhile, higher levels of resolution and higher grades of gray scales required for better quality display images are in demand for projection apparatuses, especially in recent years due to the increased availability of video images, such as that provided by high definition television (HDTV) broadcasting.

However, in the gray scale control by the pulse width modulation (PWM), as shown in Fig. 1D, the expressible gray scale is limited by the length of the time period determined by the LSB. An attempt to add a new control structure to a memory cell of the above described SRAM structure in order to overcome the aforementioned limitation creates another problem, that is, the structure of a complex memory cell, with a larger number of transistors than, for example, the memory cell of a DRAM structure, increases the size of the mechanism.

That is, in order to obtain a higher definition display image, a large number of mirror elements are required. Each of these mirror elements, comprising an SRAM-structured memory cell, must be reduced in size to fit in the space of a certain mounting size (e.g., a predefined package size or chip size). However, the addition of a new control structure to an SRAM-structured

memory cell in order to attain a higher level gray scale display image increases the size of the memory cell, thereby inhibiting a higher level display image.

Furthermore, the conventional method drives a micromirror device by first reading a drive signal on the bit line into memory and drives the mirror by using a signal input to the word line as trigger.

Since the voltage applied to the electrode is constant, such drive method only allows flexibility of adjusting the timing of voltage application. , For example, the timing of applying the voltage is applied to adjust the amplitude for controlling the oscillation of the micromirror. However, this method induces another technical problem that the minimum length of controllable time due to the read-in time of a control signal is limited. Therefore, a timely control cannot be carried out. This technical problem will be more pronounced when the drive voltage is reduced and the natural frequency of the mirror is lower.

Meanwhile, the reference US Patent 7,012,592 has disclosed a technique using "charge pump line" and attempting to enable the application of a drive voltage that is higher than the withstanding voltage of a transistor to a memory cell. The technique put forth by the US Patent 7,012,592 however, is faced with a technical problem that the drive voltage is determined on the basis of the signal condition of the bit line and therefore the speed of control is limited by the read-in time of a bit line signal.

Meanwhile, the US Patent 4,878,122 has disclosed a division of an address electrode, but there is no disclosure about controlling a drive voltage.

SUMMARY OF THE INVENTION

Therefore, an aspect of the present invention is to provide a new and improved image projection system implemented with new spatial light modulator to achieve both a high resolution and a high grade of gray scale of a projection image in a projection technique using a spatial light modulator.

Another purpose of the present invention is to provide a new and improved spatial light modulator by implementing a high degree of operation control for a mirror by applying a sufficient drive voltage to pixel units of a spatial light modulator and by controlling a high speed application timing of the aforementioned drive voltage.

A first exemplary embodiment of the present invention provides a mirror array device, comprising: a plurality of mirror elements each comprising a hinge and a deflectable mirror supported by the hinge; a memory cell for controlling the mirror element; a bit line for transmitting a data signal to the memory cell; a word line for controlling a connection between the bit line and the memory cell; a plate line for controlling the memory cell; each of said mirror elements further comprises a first address electrode controlled by the word line to connect to the memory cell; and each of said mirror elements further includes a second address electrode electrically connected to

the plate line.

A second exemplary embodiment of the present invention provides the mirror array device according to the first aspect, wherein the first and second address electrodes disposed on a surface of a device substrate having different cross sectional shapes and/or heights.

A third exemplary embodiment of the present invention provides the mirror array device according to the second aspect, wherein one of the first and second address electrodes is disposed near a deflection axis of the mirror element and the other address electrode is disposed at a greater distance from the deflection axis.

A fourth exemplary embodiment of the present invention provides the mirror array device according to the third aspect, wherein the address electrode disposed near the deflection axis further comprises a stopper for regulating a rang of angular deflection of the deflectable mirror.

A fifth exemplary embodiment of the present invention provides the mirror array device according to the second aspect, wherein a borderline dividing the first and second address electrodes is placed on the device substrate in a direction approximately perpendicular to the deflection axis of the deflectable mirror.

A sixth exemplary embodiment of the present invention provides the mirror array device according to the second aspect, wherein a borderline dividing the first and second address electrodes is disposed on a location on the device substrate to locate in adjacent to at least sides of the first and second address electrodes.

A seventh exemplary embodiment of the present invention provides the mirror array device according to the second aspect, wherein a borderline dividing the first and second address electrodes is disposed on a location on the device substrate to locate in adjacent to at least sides of the first and second address electrodes.

An eighth exemplary embodiment of the present invention provides the mirror array device according to the first aspect, wherein the first and second address electrodes are configured and controlled for application of different voltages thereon.

A ninth exemplary embodiment of the present invention provides the mirror array device according to the first aspect, wherein the first and second address electrodes are address electrodes are configured and controlled for applying a same range of voltages thereon.

A tenth exemplary embodiment of the present invention provides a mirror array device, comprising: a plurality of mirror elements each comprising a hinge and a deflectable mirror supported by the hinge; a memory cell for controlling the mirror element; a bit line for transmitting a data signal to the memory cell; a word line for controlling a connection between the bit line and the memory cell; a plate line for controlling the memory cell; and each of the mirror elements further comprises an address electrode connected to the word line and the plate line to apply an adjustable drive voltage to the address electrode.

An eleventh exemplary embodiment of the present invention provides the mirror array

device according to the tenth aspect, wherein each of the mirror elements comprises at least one address electrode.

A twelfth exemplary embodiment of the present invention provides the mirror array device according to the tenth aspect, wherein each of the mirror elements comprises two address electrodes.

A thirteenth exemplary embodiment of the present invention provides the mirror array device according to the tenth aspect, wherein the address electrodes are disposed at locations for applying a voltage to draw the mirror element to an ON angular direction and an OFF angular directions and the address electrodes are further configured and controlled for applying adjustable drive voltages thereon.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is described in detail below with reference to the following Figures.

Fig. 1A illustrates the basic principle of a projection display using a micromirror device.

Fig. 1B illustrates the basic principle of a micromirror device used for projection display.

Fig. 1C shows an exemplary driving circuit of a related art.

Fig. 1D shows the scheme of Binary Pulse Width Modulation (Binary PWM) of conventional digital micromirrors for generating grayscale.

Fig. 2 is a functional block diagram for illustrating the configuration of a display system according to a preferred embodiment of the present invention.

Fig. 3 is a block diagram illustrating the configuration of a spatial light modulator constituting a display system according to a preferred embodiment of the present invention.

Fig. 4 is a cross-sectional outline diagram of one mirror element on the line II-II of the spatial light modulator shown in Fig. 5.

Fig. 5 is a diagonal view diagram showing a part of the configuration of a spatial light modulator constituting a display system according to a preferred embodiment of the present invention.

Fig. 6 is a chart illustrating a mirror control profile used in a display system according to a preferred embodiment of the present invention.

Fig. 7A is a cross-sectional diagram showing the ON state of a micromirror.

Fig. 7B is a chart showing the quantity of light projected in the ON state of a micromirror.

Fig. 7C is a cross-sectional diagram showing the OFF state of a micromirror.

Fig. 7D is a chart showing the quantity of light projected in the OFF state of a micromirror.

Fig. 7E is a cross-sectional diagram showing the oscillation state of a micromirror.

Fig. 7F is a chart showing the quantity of light projected in the oscillation state of a micromirror.

Fig. 8A is a cross-sectional diagram illustrating the specific configuration of a pixel unit in

a display system according to a preferred embodiment of the present invention.

Fig. 8B is a plain view diagram of the surface of the pixel unit of Fig. 8A.

Fig. 8C is a plain view diagram of Fig. 8A with the mirror removed from the pixel unit.

Fig. 8D is a cross-sectional diagram of the mirror element shown in Fig. 8A deflected in an ON state.

Fig. 8E is a cross-sectional diagram of the mirror element shown in Fig. 8A deflected in an OFF state.

Fig. 9A is a conceptual diagram illustrating the action of a pixel unit of the configuration shown in Figs. 8A through 8E.

Fig. 9B is a conceptual diagram illustrating the action of a pixel unit of the configuration shown in Figs. 8A through 8E.

Fig. 9C is a conceptual diagram illustrating the action of a pixel unit of the configuration shown in Figs. 8A through 8E.

Fig. 9D is a conceptual diagram illustrating the action of a pixel unit of the configuration shown in Figs. 8A through 8E.

Fig. 10A is a conceptual diagram illustrating an example of a configuration of a pixel unit comprised in a display system according to a preferred embodiment of the present invention.

Fig. 10B is a conceptual diagram illustrating an example of a modification of a pixel unit comprised in a display system according to a preferred embodiment of the present invention.

Fig. 10C is a plain view diagram illustrating the layout of a capacitor used in a possible modification of a pixel unit comprised in a display system according to a preferred embodiment of the present invention.

Fig. 10D is a conceptual diagram illustrating another modification of a pixel unit comprised in a display system according to a preferred embodiment of the present invention.

Fig. 10E is a conceptual diagram illustrating a possible modification of a pixel array comprised in a display system according to a preferred embodiment of the present invention.

Fig. 11A is a conceptual diagram illustrating the action of a pixel unit comprised in a display system according to a preferred embodiment of the present invention.

Fig. 11B is a conceptual diagram illustrating the action of a pixel unit comprised in a display system according to a preferred embodiment of the present invention.

Fig. 11C is a conceptual diagram illustrating the action of a pixel unit comprised in a display system according to a preferred embodiment of the present invention.

Fig. 11D is a conceptual diagram showing in greater detail the equalization circuit of Fig. 11B.

Fig. 11E is a conceptual diagram showing in greater detail the equalization circuit of Fig. 11C.

Fig. 12A is a conceptual diagram illustrating the placement of the peripheral circuit of a

pixel array comprised in a display system according to a preferred embodiment of the present invention.

Fig. 12B is a conceptual diagram illustrating the internal configuration of a plate line driver (PL Driver) shown in Fig. 12A;

Fig. 12C is a conceptual diagram illustrating the internal configuration of a plate line address decoder (PL Address Decoder-a) shown in Fig. 12A.

Fig. 12D is a conceptual diagram showing a possible modification configured by adding a function to the plate line address decoder (PL Address Decoder-a) shown in Fig. 12C.

Fig. 12E is a diagram illustrating the internal configuration of a bit line driver unit (Bitline Driver) shown in Fig. 12A.

Fig. 12F is a truth table for regulating the operation of the bit line driver unit (Bitline Driver) shown in Fig. 12E.

Fig. 13 is a timing chart illustrating the operation of a pixel array of the configuration shown in Fig. 10A.

Fig. 14 is a timing chart of the address decoder for the ROW lines shown in Fig. 12A.

Fig. 15 is a conceptual diagram showing another possible modification of the pixel unit shown in Fig. 10A.

Fig. 15A is a cross-sectional diagram of a pixel unit in an ON state comprising two electrodes, i.e., an ON electrode and a second ON electrode, on the ON side shown in Fig. 15.

Fig. 15B is a cross-sectional diagram of a pixel unit in an OFF state comprising two electrodes, i.e., an ON electrode and a second ON electrode, on the ON side shown in Fig. 15.

Fig. 15C is a plain view diagram showing a possible layout of the second ON electrode that is added to the pixel unit shown in Fig. 15.

Fig. 15D is a plain view diagram showing another possible layout of the second ON electrode that is added to the pixel unit shown in Fig. 15.

Fig. 15E is a plain view diagram showing another possible layout of the second ON electrode that is added to the pixel unit shown in Fig. 15.

Fig. 15F is a plain view diagram showing another possible layout of the second ON electrode that is added to the pixel unit shown in Fig. 15.

Fig. 15G is a conceptual diagram showing a modification of the memory cell on the ON side of the pixel unit shown in Fig. 15.

Fig. 15H is a conceptual diagram showing a modification of the connection between the memory cell on the ON side, a word line, and a plate line at the pixel unit shown in Fig. 15.

Fig. 16 is a timing chart showing the action of the pixel unit shown in Fig. 15.

Fig. 17A is a chart illustrating the setup of a mirror control profile.

Fig. 17B is a chart illustrating the setup of a mirror control profile.

Fig. 17C is a chart illustrating the setup of a mirror control profile.

Fig. 17D is a chart illustrating the setup of a mirror control profile.

Fig. 17E is a chart illustrating the setup of a mirror control profile.

Fig. 17F is a chart illustrating the setup of a mirror control profile.

Fig. 17G is a chart illustrating the setup of a mirror control profile.

Fig. 18 is a conceptual diagram showing another possible modification of the pixel unit shown in Fig. 10A.

Fig. 19 is a timing chart showing the action of another possible modification of the pixel unit shown in Fig. 18.

Fig. 20 is a conceptual diagram illustrating the layout of a peripheral circuit performing the action of the pixel unit shown in Fig. 18.

Fig. 21 is a conceptual diagram showing another possible modification of the pixel unit shown in Fig. 10A.

Fig. 22A is a conceptual diagram showing a possible modification of the placement of the peripheral circuit for a pixel array according to a preferred embodiment of the present invention.

Fig. 22B is a conceptual diagram showing a possible modification of the placement of the peripheral circuit for a pixel array according to a preferred embodiment of the present invention.

Fig. 22C is a conceptual diagram showing a possible modification of the placement of the peripheral circuit for a pixel array according to a preferred embodiment of the present invention.

Fig. 22D is a conceptual diagram showing a possible modification of the configuration of placing the peripheral circuit for a pixel array according to a preferred embodiment of the present invention.

Fig. 23A is a cross-sectional diagram for showing an exemplary modification of the configuration of a pixel unit (i.e., a mirror element) comprising a mirror implemented with a cantilever structure according to a preferred embodiment of the present invention.

Fig. 23B is a cross sectional schematic diagram showing an exemplary configuration of the drive circuit shown in Fig. 23A.

Fig. 24 is a circuit diagram illustrating in detail a part of the layout of the pixel unit comprising a mirror (shown in Fig. 23A) that is structured as a cantilever.

Fig. 25 is a timing chart illustrating the action of a pixel unit (i.e., a mirror element) comprising a mirror (shown in Fig. 23A) that is structured as a cantilever.

Fig. 26A is a plain view diagram illustrating the packaging structure of a package accommodating a spatial light modulator according to a preferred embodiment of the present invention.

Fig. 26B is a cross-sectional diagram of Fig. 26A.

Fig. 27 is a conceptual diagram showing the configuration of a projection apparatus according to a preferred embodiment of the present invention.

Fig. 28 is a block diagram illustrating the configuration of a control unit comprised in the

projection apparatus shown in Fig. 27.

Fig. 29 is a conceptual diagram showing another possible modification of a multi-panel projection apparatus according to a preferred embodiment of the present invention.

Fig. 30 is a block diagram showing a possible configuration of the control unit of a multi-panel projection apparatus according to a preferred embodiment of the present invention.

Fig. 31 is a conceptual diagram showing a possible modification of a multi-panel projection apparatus according to another preferred embodiment of the present invention.

Fig. 32 is a block diagram showing a possible configuration of a control unit comprised in the projection apparatus shown in Fig. 31.

Fig. 33 is a chart showing the waveform of a control signal of the projection apparatus shown in Fig. 31.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following is a description, in detail, of the preferred embodiment of the present invention with reference to the accompanying drawings.

Fig. 2 is a conceptual diagram for illustrating the configuration of a display system according to a preferred embodiment of the present invention. Fig. 3 is a block diagram illustrating the configuration of a spatial light modulator constituting a display system according to a preferred embodiment of the present invention. Fig. 4 is a cross sectional view showing a schematic diagram for illustrating the configuration of a pixel unit 211 implemented in a spatial light modulator shown according to the present embodiment.

The following description first describes a configuration of a projection apparatus 100 according to the present embodiment, which serves as a premise for the individual embodiments, whose descriptions are also included.

The projection apparatus 100 according to the present embodiment comprises a spatial light modulator 200, a control apparatus 300, a light source 510, and a projection optical system 520.

Fig. 5 is a diagram for showing a perspective view along a diagonal direction of a spatial light modulator in which multiple mirror elements (i.e., pixel units) for modulating the reflecting direction of incident light by deflecting mirrors are formed as a two-dimensional array on a device substrate.

As shown in Fig. 5, the spatial light modulator 200 is configured with the pixel units 211 arranged as a two-dimensional array on a substrate 214. Each pixel unit comprises an address electrode (not shown in the drawing here), an elastic hinge (not shown in the drawing here), and a mirror 212 supported by the elastic hinge. According to the configuration shown in Fig. 5, pixel units 211 having square mirrors 212 arranged in a two-dimensional array on substrate 214. Voltages applied to an address electrode formed on the substrate 214 control the mirror 212 in each pixel

unit 211 to move to different deflection angles.

Meanwhile, in consideration of the number of pixels required by a super high definition television, the pitch, i.e., the interval between adjacent mirrors 212, is set between 4μm and 14μm, or, preferably, between 5μm and 10μm, to achieve the resolution of a full HD TV, e.g., 2048 by 4096, or a non-full TD TV, and of the size of mirror devices. More specifically, the pitch is defined as the distance between the deflection axes of adjacent mirrors 212. In an exemplary embodiment, the area of a mirror 212 may be between 16 μm^2 and 196μm^2, or, preferably, between 25μm^2 and 100μm^2. Note that the shape mirror 212 or the pitch between the mirrors 212 may be flexibly adjusted according to specific requirements of display resolution.

The drawing also shows a dotted line as a deflection axis 212a of the mirror 212 . Specifically, when the light emitted from a light source 510 is a coherent light, the angle of incident to mirror 212 is configured along a orthogonal or diagonal direction relative to deflection axis 212a. The light source 510 emits a coherent light when the light source is implemented as a laser light source.

The following description further explains the control processes and the operation of the pixel unit 211 with reference to the cross-sectional diagram across the line II – II over a pixel unit of the spatial light modulator 200 shown in Fig. 5. Specifically, Fig. 4 is a cross-sectional outline diagram for showing a cross-section of one mirror element of the spatial light modulator on the line II – II in Fig. 5.

As illustrated in Figs. 3 and 4, a spatial light modulator 200 according to the present embodiment comprises a pixel array 210, a bit line driver part 220, and a word line driver unit 230.

In pixel array 210, multiple pixel units 211 are arrayed on a grid at each of the positions where bit lines 221 extending vertically from the bit line driver part 220 cross word lines 231 extending horizontally from the word line driver unit 230.

As illustrated in Fig. 4, each pixel unit 211 comprises a mirror 212 that freely tilts and is supported on the substrate 214 by a hinge 213.

An OFF electrode 215 and an OFF stopper 215a are placed symmetrically across hinge 213 that comprises a hinge electrode 213a on the substrate 214, and likewise an ON electrode 216 and an ON stopper 216a are placed thereon.

A predetermined voltage applied to the OFF electrode 215 draws mirror 212 with a Coulomb force to tilt to an angular position abutting the OFF stopper 215a. The mirror 212 thus reflects the incident light 511 to the light path along an OFF direction away from the optical axis of a projection optical system 130.

A predetermined voltage applied to the ON electrode 216draws the mirror 212 with a Coulomb force to tilt to an angular position abutting the ON stopper 216a. The mirror 212 reflects the incident light 311 to the light path along an ON direction coincident with the optical axis of the projection optical system 130.

Fig. 4 shows an OFF capacitor 215b is connected to the OFF electrode 215 and to the bit line 221-1 by way of a gate transistor 215c that is implemented as a field effect transistor (FET). An ON capacitor 216b is connected to the ON electrode 216, and to the bit line 221-2 by way of a gate transistor 216c that is implemented as a field effect transistor (FET).

The signal on the wordline 231 controls the turning ON and OFF of the gate transistor 215c.

Specifically, a select signal on a word line 231 simultaneously selects all the pixel units 211 connected to the horizontal word line 231. The signals on the bitlines 221-1 and 221-2 control the charging and discharging of the OFF capacitor 215b and ON capacitor 216b. Therefore, the micromirror 212 in each pixel unit 211 along a horizontal row is controlled to turn ON and OFF.

A memory cell M1 configured with a DRAM structure includes an OFF capacitor 215b and gate transistor 215c on the side of the OFF electrode 215. Likewise, the memory cell M2 also configured with a DRAM structure includes an ON capacitor 216b and gate transistor 216c on the side of the ON electrode 216. With this configuration, the tilting operation of the mirror 212 is controlled in accordance with the presence and absence data written to the respective memory cells of the OFF electrode 215 and ON electrode 216.

The light source 510 emits an incident light 511 to illuminate the spatial light modulator 200. The individual micromirrors 212 then reflects the incident light 511 as the reflection light 512. Reflection light 512 on the light path passes through a projection optical system 520 and is projected onto a screen (not shown in a drawing herein) or the like, as projection light 513.

The descriptions below explain the operation of a control apparatus 300 according to the present embodiment. The control apparatus controls the spatial light modulator 200 to operate in the ON/OFF states (i.e., an ON/OFF modulation) and oscillation state (i.e., an oscillation modulation) of mirror 212 of the spatial light modulator 200 to achieve a higher level of gray scales by operating with an intermediate gray scale.

A non-binary block 320 generates non-binary data 430 used for controlling mirror 212 by converting, into non-binary data, a binary video image signal 400 that is externally input binary data. In this event, the LSB is different for the period of ON/OFF states of the mirror 212 and the period of intermediate oscillation state.

A timing control unit 330 generates a drive timing 420 for the non-binary block 320, a PWM drive timing 440, and an OSC drive timing 441 for the mirror 212 on the basis of an input synchronous signal 410 (Sync).

As illustrated in Fig. 6, the present embodiment is configured such that a desired number of bits of the upper bits 401 of the binary video image signal 400 is assigned to the ON/OFF control for the mirror and the remaining lower number of bits 402 is assigned to the oscillation control. The control is such that the ON/OFF (positioning) state is controlled by the PWM drive timing 440 from the timing control unit 330 and the non-binary data 430, while the oscillation state is

controlled by the PWM drive timing 440 and OSC drive timing 441 from the timing control unit 330 and the non-binary data 430.

The following is a description of the basic control of a micromirror 212 of a spatial light modulator 200 according to the present embodiment.

Note that "Va (1, 0)" indicates an application of a predetermined voltage Va to the OFF electrode 215 and no application of voltage to the ON electrode 216 in the following description.

Also, "Va (0, 1)" indicates no application of voltage to the OFF electrode 215 and an application of a voltage Va to the ON electrode 216.

Also, "Va (1, 1) indicates the application of a voltage Va to both the OFF electrode 215 and ON electrode 216.

Figs. 7A, 7B, 7C, 7D, 7E and 7F show the configuration of a pixel unit 211 comprising a mirror 212, a hinge 213, OFF electrode 215, and ON electrode 216, and a basic example of how a mirror 212 is controlled under an ON/OFF state and under an oscillating state.

Fig. 7A shows the mirror 212 having been tilted from the neutral state by being attracted by the ON electrode 216, thus tilting to an ON state, as a result of applying a predetermined voltage (i.e., Va (0, 1)) to only the ON electrode 216. In the ON state of micromirror 212, reflection light 512 by way of mirror 212 is captured by projection optical system 520 and projected as projection light 513. Fig. 7B shows the quantity of light projected in the ON state.

Fig. 7C shows the mirror 212 having been tilted from the neutral state by being attracted by the OFF electrode 215, thus tilting to an OFF state, as a result of applying a predetermined voltage (i.e., Va (1, 0)) to only the OFF electrode 215. In the OFF state of micromirror 212, reflection light 512 is deflected away from projection optical system 520, and therefore does not transmit light along the optical path of the projection light 513. The right side of Fig. 7B shows the quantity of light projected in the OFF state. Fig. 7D shows the quantity of light projected in the OFF state.

Fig. 7E illustrates mirror 212 performing a free oscillation in the maximum amplitude of A0 between a tilted position (i.e., a Full ON), contacting with the ON electrode 216, and another tilted position (i.e., a Full OFF), contacting with the OFF electrode 215 (at Va (0, 0)).

Incident light 511 is projected onto the micromirror 212 at a prescribed angle, and the quantity of light resulting from incident light 511 reflecting in the ON direction. A portion of the quantity of light (i.e. the quantity of light of the reflection light 512) reflecting in a direction that is between the ON direction and OFF direction are incident to projection optical system 520 so as to be projected as the brightness of the image (i.e., the projection light 513). Fig. 7F shows the quantity of light projected in an oscillation state.

That is, in the ON state of mirror 212 shown in Fig. 7A, the flux of light of reflection light 512 proceeds to the ON direction so as to be captured almost entirely by projection optical system 520 and projected as projection light 513.

In the OFF state of mirror 212, shown in Fig. 7C, reflection light 512 proceeds to an OFF direction shifted from projection optical system 520, and thus a light projected as projection light 513 does not exist.

In the oscillating state of mirror 212, shown in Fig. 7E, a portion of the light flux of reflection light 512, diffraction light, diffusion light, and the like are captured by projection optical system 520 and projected as projection light 513.

Note that the examples shown in Figs. 7A, 7B, 7C, 7D, 7E and 7F described above have been described for in the case of applying the voltage Va represented by a binary value of "0" or "1" to OFF electrode 215 and ON electrode 216. However, a more precise control of the tilting angle of mirror 212 is possible by increasing the steps of Coulomb force generated between mirror 212 and OFF electrode 215 or ON electrode 216 by increasing the step of the voltage value Va to multiple values.

Also note that the examples shown in Figs. 7A, 7B, 7C, 7D, 7E and 7F described above presume that mirror 212 (i.e., the hinge electrode 213a) is set at the ground potential. However, a more precise control of the tilting angle of the mirror 212 is possible by applying an offset voltage thereto.

The present embodiment is configured to apply the voltages, i.e., Va (0, 1), Va (1, 0) and Va (0, 0), at the appropriate times during the tilting of the mirror 212 between the ON and OFF states as described below so as to generate a free oscillation in an amplitude that is smaller than the maximum amplitude between the ON and OFF states, thereby producing a more refined gray scale.

The following describes a method for displaying a video image using the projection apparatus according to the present embodiment.

Non-binary data 430, a PWM drive timing 440, and an OSC drive timing 441 are generated when a binary video image signal 400 and a synchronous signal 410 are input to a control apparatus 300.

Non-binary block 320 and timing control unit 330 calculate the period of time for controlling mirror 212 under an ON state. That is, they calculate the time for controlling the mirror 212 under an oscillation state, or the number of times for oscillating the mirror 212 for each mirror 212 of spatial light modulator 200, which displays the pixels of a video image in accordance with binary video image signal 400 and drive timing 420. Drive timing 420 is generated by timing control unit 330 from synchronous signal 410, and it generates non-binary data 430, a PWM drive timing 440, and an OSC drive timing 441.

Here, non-binary block 320 and timing control unit 330, that are comprised in control apparatus 300, use the ratio of the quantity of light of a projection light 513, obtained by oscillating a predetermined mirror 212 in an oscillation time T, to the quantity of light of a projection light 513, obtained by controlling mirror 212 under an ON state during the oscillation time T. This ratio is used to calculate the period of time for controlling mirror 212 under an ON state, the period of time

for controlling the mirror 212 under the oscillation state, or the number of oscillations of mirror 212.

Non-binary data 430, PWM drive timing 440, and OSC drive timing 441 are generated on the basis of the calculated value of the time or the number of oscillations used to perform the ON/OFF control and oscillation control for each of the mirrors 212 constituting one frame of video image.

Fig. 8A is a cross-sectional diagram illustrating the specific configuration of a pixel unit 211 in the above described spatial light modulator 200.

The mirror element shown in Fig. 8A comprises wirings 1) 906a, 906b, and 906c of a drive circuit used for driving and controlling a mirror 913, 2) first Vias 907a, 907b, 907c, 907d, 907d, and 907e, all of which are connected to the wirings 906a, 906b, and 906c of the drive circuit, and 3) a first insulation layer 902, which is on a substrate 901. Wiring 906a on the left side is implemented with two first Vias 907a and 907e, and with first insulation layer 902 separating the two Vias. Likewise, wiring 906b on the right side is also implemented with two first Vias 907b and 907d, and with first insulation layer 902 separating the two Vias. Wiring 906c in the center is implemented with only one first via 907a. In summary, the present embodiment is implemented with five first Vias each has an insulation layer.

The present embodiment is also implemented with the wirings on the left and right sides with two first Vias. The number of first Vias may be different between the left and right sides. The number of first Vias may also be greater or fewer than in the present embodiment.

Furthermore, on the first Vias 907a, 907b, 907c, 907d, 907d, and 907e are formed second Vias 915a, 915b, and 915c and surface electrodes 908a and 908b, all of which are formed on the right and left sides the second Vias, respectively.

The second via 915a is formed on the first via 907a, which has been formed on wiring 906c at the center. The second Vias 915b and 915c are formed on first Vias 907b and 907c, respectively, both of which are formed on the wirings 906a and 906b on the left and right sides, respectively. Surface electrodes 908a and 908b are formed on first Vias 907d and 907e, respectively, whereas second Vias 915a, 915b, or 915c is not formed on wirings 906a and 906b.

Furthermore, a first protective layer 903 is laid on the first insulation layer 902, and a second protective layer 904 is laid on the first protective layer 903.

Substrate 901 is preferably a silicon substrate.

Wirings 906a, 906b, and 906c of the drive circuit are preferably aluminum wirings.

First Vias 907a, 907b, 907c, 907d, 907d, and 907e and second Vias 915a, 915b, and 915c are preferably made of a metallic material containing tungsten and/or cupper.

Surface electrodes 908a and 908b may be made of a material similar to that of first Vias 907a, 907b, 907c, 907d, 907d, and 907e and second Vias 915a, 915b, and 915c (e.g., tungsten), or of a material with high electrical conductivity, such as aluminum. The form of the surface

electrodes 908a and 908b is arbitrary. Fig. 8 illustrates an example of placing the surface electrodes 908a and 908b on first Vias 907d and 907e, respectively. They may alternatively be placed directly on wirings 906a and 906b.

First insulation layer 902, first protective layer 903, and second protective layer 904 are preferably layers containing silicon such as silicon carbide (SiC), amorphous silicon, or silicon dioxide (SiO_2).

If aluminum is used for surface electrodes 908a and 908b, a direct contact between the amorphous silicon and aluminum electrode corrodes the aluminum surface electrodes 908a and 908b, and therefore a silicon carbide (SiC) layer between the amorphous silicon and aluminum surface electrodes 908a and 908b is recommended. Alternatively, an electrode may be formed by mixing aluminum with an impurity, such as silicon; alternatively, a barrier layer may be provided by using a material other than a SiC layer. Such a barrier layer may comprise two layers or more.

For example, first insulation layer 902 of Fig. 8A is a layer made of silicon carbide (SiC). First insulation layer 902 may be made of another material such as titanium nitride (TiN), or the like, which takes into consideration the etching of a dispensable layer with hydrogen fluoride (HF), which is employed for producing a mirror element; this also takes into consideration the stiction of between a mirror element and electrode 909a or 909b when the former deflects and abuts onto the latter.

The mirror element, according to the present embodiment, is equips electrodes 909a, 909b, and 914 so as to a secure electrical connection to second Vias 915a, 915b, and 915c, respectively.

Electrodes 909a, 909b, and 914 may preferably use a high electrically conductive material such as aluminum.

Electrode 914, shown in Fig. 8A, (constituting a hinge electrode later) is an electrode equipped with an elastic hinge 911 and is configured to be the same height as electrodes 909a and 909b on the left and right. Configuring individual electrodes 909a, 909b, and 914 to be the same height as the center, left, and right makes it possible to form the three electrodes 909a, 909b and 914 in the same production process. Furthermore, a barrier layer 910 made of tantrum, titanium, or such is placed on electrode 914 at the center. Barrier layer 910 may comprise two layers or more.

Furthermore, an appropriate modification of the height of the electrode at the center makes it possible to determine the height for placing an elastic hinge 911 at the center described below. The height of the placement of elastic hinge 911 may be determined by adjusting the height of barrier layer 910.

Elastic hinge 911 is placed on electrode 914 at the center, on which barrier layer 910 has been laid, so as to be connected to barrier layer 910.

Elastic hinge 911 is made of a material such as amorphous silicon. The thickness of elastic hinge 911 (in the left and right direction of the drawing of Fig. 8A) is preferably between

approximately 150 and 400 angstroms.

Multiple elastic hinges may be provided for one mirror and the mirror may be supported by such elastic hinges that are reduced in width. For example, two elastic hinges narrower than the conventional configuration may be used one mirror at either end of the mirror.

Elastic hinge 911 is preferably applied with In-Situ doping (such as arsenic and phosphorus), an ion implanting, a diffusion of metallic silicide, such as nickel silicide (NiSi), titanium silicide (TiSi), so as to possess electric conductivity.

Furthermore, the mirror element according to the present embodiment provides a second insulation layer 905 on the surface of the substrate where electrodes 909a, 909b, and 914 have been placed.

Second insulation layer 905 is preferably a layer containing silicon, such as silicon carbide (SiC), amorphous silicon, or silicon dioxide (SiO_2). This layer is provided to prevent corrosion by hydrogen fluoride (HF) if the electrodes 908a, 908b, 909a, 909b, and 914 are made of aluminum as described above.

The upper surface of elastic hinge 911 may be provided with a joinder layer, which can be configured to be the same form and size as mirror 913 described below. The present embodiment is configured so that the joinder layer is the smallest possible size. Such a configuration makes it possible to prevent mirror 913 from being deformed or warped by the difference in thermal expansion coefficients between mirror 913 and the joinder layer.

Furthermore, a metallic layer 912 is laid on the joinder layer of elastic hinge 911 in order to provide electric conductivity between elastic hinge 911 and mirror 913, while eliminating a variation in heights between individual mirror elements.

Metallic layer 912 is made of a material containing tungsten or titanium; a material containing another metal may also be used.

If mirror 913 is made of aluminum and elastic hinge 911 is made with a silicon material, then a barrier layer (not shown in a drawing herein) may further be laid on and under metallic layer 912 in order to prevent mirror 913 from touching elastic hinge 911. Such a barrier layer may comprise two layers or more.

The barrier layer is made of a material containing tantrum, or titanium, et cetera.

Furthermore, the mirror element according to the present embodiment is configured by placing a mirror 913 on metallic layer 912 of elastic hinge 911.

Mirror 913 is preferably made of a material with high light reflectivity, such as aluminum.

Mirror 913 is also preferably has an approximately square shape, with one side measuring between 4.5 and 11μm. The gap between individual mirrors 913 is preferably between 0.15 and 0.55μm. The aperture ratio of each individual mirror element is preferably about 90%.

Such is the configuration of the mirror element according to the present embodiment shown in Fig. 8A.

Fig. 8B is a plain view diagram of the surface of the substrate of the mirror device according to the present embodiment.

Note that surface electrodes 909a and 909b on the left and right, and the hinge electrode 914, at the center, which are formed on mirror 913 and the second Vias 915a, 915b, and 915c are delineated by the dotted lines. Also, the deflection axis of mirror 913 is indicated by chain lines.

As shown in Fig. 8B, second Vias 915a, 915b, and 915c for electric conduction to electrodes 909a, 909b, and 914 are placed under electrodes 909a, 909b, and 914. Surface electrodes 908a and 908b, placed so as to increase a Coulomb force for deflecting the mirror 913, are placed under the mirror 913.

Fig. 8C is a plain view diagram with mirror 913 of the mirror element, according to the present embodiment, is removed. The position of mirror 913 is indicated by dotted lines.

As shown in Fig. 8C, the respective apexes of electrodes 909a and 909b at both end of mirror 913 are formed as protrusions. This design ensures that the deflection angle of mirror 913 is at a prescribed angle as a result of mirror 913 hitting the protrusions of electrodes 909a and 909b when mirror 913 is deflected.

Note than the tips of electrodes 909a and 909b are preferably designed so as to make the deflection angle of mirror 913 between 12 and 14 degrees. Such a deflection angle of mirror 913 is preferably designed in compliance to the design of the light source and optical system of a projection apparatus. Furthermore, the length of elastic hinge 911 of each mirror element is preferably no larger than 2μm, and mirror 913 is preferably an approximate square, with the length of one side being 10μm or smaller.

The surface of the substrate is formed with the electrodes 909a and 909b and hinge electrode 914 such that the substrate has convex and concave surfaces.

Fig. 8D is a cross-sectional diagram the mirror element shown in Fig. 8A deflected in an ON state.

The present embodiment presumes a configuration in which the light emitted from a light source is an ON light when mirror 913, shown in Fig. 8A, is deflected to the right side, while the light emitted from a light source is an OFF light when the mirror 913 is deflected to the left side.

When a voltage is not applied to individual surface electrodes 908a or 908b on the left and right, or to the individual surface electrodes 909a or 909b, the elastic hinge 911 is not deformed and the mirror 913 is therefore maintained in a horizontal position.

When a voltage to surface electrode 909b on the right side and to surface electrode 908a on the right side is applied, a Coulomb force determined by the following expression is generated:

[top surface area size of electrode]*[voltage applied to electrode]*[the second power of the distance between aluminum and mirror].

This Coulomb force is generated between the right surface electrode 909b and mirror 913 and between the right surface electrode 908a and mirror 913. Mirror 913 is deflected by the total

Coulomb force generated between the right surface electrode 909b and mirror 913 and between the right side surface electrode 908a and mirror 913.

In this event, the distance between mirror 913 and right surface electrode 908a is longer than that between mirror 913 and right surface electrode 909b, and the area of right surface electrode 908a is smaller than that of the right surface electrode 909b. Therefore, the generated Coulomb force is also smaller than that generated between the right surface electrode 909b and mirror 913.

Furthermore, when mirror 913 is attracted to right surface electrode 908a as the mirror is deflected as a result, mirror 913 is deflected to an angle between 12 and 14 degrees, and there is a strong reactive force of the elastic hinge due to its resilience. The Coulomb force attracts the tip of mirror 913 to the right surface electrode 908a placed on the substrate surface so that mirror 913 can be attracted by a smaller Coulomb force due to the type of movement characteristic of a rigid body. As a result, the right surface electrode 908a is capable of retaining the deflection of mirror 913 in a state for a low voltage to be applied thereto.

When mirror 913 is deflected to the right side, the surface electrode 908b on the other side (that is, the left side) and the left side surface electrode 909a are put in the same potential and are grounded.

Fig. 8E is a cross-sectional diagram of the mirror element shown in Fig. 8A deflected to an OFF state.

In Fig. 8E, the application of a voltage to left side surface electrode 909a and left side surface electrode 908b makes it possible to deflect mirror 913 to the left side, like to the process described for Fig. 8D.

The principles in operation and the action of the Coulomb force in this case are similar to those noted for Fig. 8D and therefore further descriptions are not provided here.

Incidentally, if the forms of mirror 913 and elastic hinge 911 are changed between the right and left sides of the mirror element, and if the resilience of elastic hinge 911 is different for the right and left sides of the mirror element, and if the deflection control for mirror 913 is different for the right and left sides of the mirror element, then the area, height, and placement of the respective surface electrodes 908a and 908b, or the respective surface electrodes 909a, 909b, and 914, on the right and left sides of the mirror element may be changed so as to apply the appropriate voltage to thereby control the deflection of mirror 913.

Furthermore, an alternative control may also be performed so that voltages are applied in multiple steps to the respective surface electrodes 908a and 908b and respective surface electrodes 909a and 909b on the right and left sides of the mirror element.

Furthermore, the circuits and voltages for driving surface electrode 908a (or 908b) and surface electrode 909a (or 909b) on either one side of surface electrode 908a (and surface electrode 909b) on the right side of the mirror element and the surface electrode 908b (and surface electrode

909a) on the left side of the mirror element may be appropriately changed. In other words, surface electrodes 908a and 909b are driven together, or surface electrodes 908b and 909a are driven together.

Furthermore, both or either one of surface electrode 908a (or 908b) and 909a (or 909b) of surface electrodes 908a and 909b on the right side of the mirror element or surface electrode 908b and electrode 909a on the left side of the mirror element may protrude from the surface of the substrate.

Furthermore, both or either one of surface electrode 908a (or 908b) and electrode 909a (or 909b) of surface electrodes 908a and 909b on the right side of the mirror element or surface electrode 908b and electrode 909a on the left side of the mirror element may be placed on the surface of the substrate.

As such, mirror 913 of the mirror element according to the present embodiment is deflected, and thus the reflecting direction of the illumination light can appropriately be changed.

The following is a description of the benefits of placing surface electrode 909b and surface electrode 909a on the ON side apart from each other in the present embodiment, with reference to Figs. 9A, 9B, 9C, and 9D.

Fig. 9A is a conceptual diagram illustrating the advantage of the structure of pixel unit 211, also illustrated in the above described Fig. 8A, et cetera.

Fig. 9A shows 1) the use of surface electrode 909a (i.e., the electrode A) as a stopper located near elastic hinge 911, which supports mirror 913, and 2) the use of surface electrode 909b of the surface electrode 909b (i.e., the electrode B) and surface electrode 908a (i.e., the electrode B') as stoppers also. In this case, electrode A is placed on substrate 901, while electrode B' is placed under the surface of substrate 901.

If the position of each stopper (i.e., electrode A and B) is at a short distance (i.e., a distance d) from elastic hinge 911, the deflection angle of mirror 913 is determined by h/d. Where "h" is the height of the base of elastic hinge 911, this calculation is less accurate than when "h" is the height of the electrodes A and B, in which case the accuracy of the calculation is good.

Furthermore, the position of each stopper (i.e., the electrode A or B) is close to elastic hinge 911 and therefore the spring force (i.e., the rigidity) of elastic hinge 911 may be decreased to counter stiction (i.e., the force attributable to an intermolecular attraction) between mirror 913 and each stopper. This makes possible the advantageous decrease in size of the mirror element.

Fig. 9B illustrates a stopper placed far from elastic hinge 911 of electrodes B and B'.

In this case, if the position of each stopper (i.e., the electrode A or B) is at a far distance (i.e., a distance d') from elastic hinge 911, the deflection angle of mirror 913 is achieved with greater accuracy.

In order to detach mirror 913 from a stopper 920 by a spring force that is larger than the stiction between mirror 913 and stopper 920, however, a stronger spring force is required than in

the configuration shown in the above described Fig. 9A.

At the same time, a stronger spring force of elastic hinge 911 will be needed to increase the voltage applied to electrodes B and B' to control mirror 913.

Figs. 9C and 9D illustrate the placing of electrodes B and B' on substrate 901.

Fig. 9C illustrates the edge (at a distance d1 from elastic hinge 911) of the electrode B functioning as a stopper, while Fig. 9D illustrates electrode B' functioning as stopper.

In Fig. 9C, the distance d2 of the edge of electrode B' from elastic hinge 911 is set at a value in order to prevent electrode B' from touching mirror 913.

In contrast, in of Fig. 9D, the distance d1' of the edge of electrode B from elastic hinge 911 is set at a value smaller than the above described distance d1, and the distance d2' of the edge of electrode B' from elastic hinge 911 is set at a value larger than the above described distance d2 so that the edge of electrode B' functions as a stopper for mirror 913.

In this case, electrodes B and B' exist on the substrate 901 and therefore the voltage applied to electrodes B and B' decreases as the distance between mirror 913 and electrodes B/B' decreases, when the area of electrodes B and B' is the same as in the above described Figs. 9A and 9B.

In Figs. 9C and 9D, if the length of elastic hinge 911 is the same, the configuration illustrated in Fig. 9C makes it possible to enlarge the area of electrode B.

In contrast, the area of electrode B' can therefore be enlarged in the configuration shown in Fig. 9D.

As described above, the placement of electrodes on the ON side separately according to the present embodiment optimizes the area of the electrode, the distance between mirror 913 and electrode B (and B'), and the distance of between electrode B (and B') and elastic hinge 911. This is achieved by using multiple electrodes B and B', thereby providing a layout to reduce the drive voltage.

With the above described configuration serving as a premise, the following is a description of an exemplary configuration, with reference to Fig. 10A, of a pixel unit 211 implemented in a pixel array 210 of a spatial light modulator 200 according to the present embodiment,.

In contrast to the configuration of pixel unit 211, as illustrated in Fig. 4, described above, in which one pixel is implemented with a mirror, two electrodes, and two DRAM-structured memory cells, the present embodiment 1 is configured with the addition of plate lines 232 (PL-n; where "n" represents the number of ROW lines) to respective ROW lines and interconnect the plate line 232 (PL) and ON electrode 216 by way of a second ON capacitor 233 (Cap 3).

This configuration enables the control of ON electrodes 216 (i.e., B1-1, B1-2 and so on) of the same ROW line even with lines other than bit line (bit line 221-1 and bit line 221-2) and word line 231 (WL-1).

The present embodiment is configured such that the memory cell used for controlling

mirror 212 is a simple DRAM structure requiring only one transistor in individual pixel unit 211 constituting the pixel array. Therefore the size of the structure of the memory cell can be kept at a minimum, even if plate line 232 and the second ON capacitor 233 are added. Therefore, a high resolution is easily achieved through an arrangement of a larger number of pixel units 211 within a pixel array of a certain size.

Furthermore, the addition of plate line 232 and second ON capacitor 233 makes it possible to greatly expand the gray scale expression through a combination of the ON/OFF control and oscillation control of mirror 212. This achieves a greater gray scale expression than that achieved through a simple PWM control, as described below.

In other words, it is possible to attain both higher definition and a higher level of gray scale for a projection image by using a spatial light modulator such as spatial light modulator 200.

The following is a description of an operation of pixel unit 211, configured as shown in Fig. 10A.

On the word line 231 (WL) and plate line 232 (PL), both of which are placed on the same ROW line, plate line 232 (PL) is made active when word line 231 (WL) is not selected (L) and when ON electrode 216 is discharged (e.g., 0 volts).

With this, ON electrode 216 is charged. The charge voltage is determined by the ratio of the capacitance of ON capacitor 216b (Cap 2) to that of the second ON capacitor 233 (Cap 3). The charge voltage of ON electrode 216 is no less than twice the voltage of plate line 232 (PL) when the capacitance ratio is set at Cap 3>Cap 2.

When word line 231 (WL) is in a selected state (H level), plate line 232 (PL) is discharged (e.g., 0 volts).

Fig. 10B is a diagram showing a possible modification of the configuration of pixel unit 211 according to the present embodiment.

The configuration shown in Fig. 10B eliminates the ON capacitor 216b (Cap 2) connected to ON electrode 216 from the configuration illustrated in the above described Fig. 10A.

However, gate transistor 216c has a floating capacitance Cf at the source terminal that is connected to ON electrode 216, and the floating capacitance Cf produces an effect similar to the effect produced by the eliminated Cap 2.

In this case, the capacitance of the second ON capacitor 233 is set at approximately the same capacitance as that of OFF capacitor 215b (i.e., Cap 3= Cap 1). The floating capacitance Cf is usually very small, making Cap 3>>Cf and, thus, the charge of ON electrode 216 becomes close to the voltage of plate line 232 (PL).

Fig. 10C is a plain view diagram of an example layout within pixel unit 211, of 1) OFF capacitor 215b in the configuration illustrated in Fig. 10B and of 2) second ON capacitor 233 connected to the line 232, with the same delineations used in Figs. 8A through 8C.

Fig. 10C is a diagram with a perspective from the top surface of mirror 212 (or mirror 913),

showing a layer on which upper plate 233a of second ON capacitor 233 (and OFF capacitor 215b) are placed.

The upper plate 233a and lower plate 233b, which includes the present second ON capacitor 233 are of the same size, with lower plate 233b placed right under upper plate 233a.

Furthermore, the size of upper plate 233a and lower plate 233b is smaller than that of mirror 212 (or the mirror 913). This configuration prevents the size of the mirror device from increasing due to the area of the second ON capacitor 233 jutting out of the contour of mirror 212.

Fig. 10D is a description diagram showing another possible modification of the configuration of pixel unit 211 shown in the above described Fig. 10A.

The modification shown in Fig. 10D is configured with a second OFF capacitor 234 between plate line 232 and OFF electrode 215, in addition to adding the second ON capacitor 233.

This configuration enables a control of the electric potential on the side of the OFF electrode 215 by way of plate line 232 (PL), thus enabling a diverse control of the mirror 212.

Fig. 10E shows an example configuration in which a second word line 231-2 and a second plate line 232-2 are added to the pixel array 210 (i.e., the pixel unit 211) illustrated in the above described Fig. 10A.

The configuration of Fig. 10E is such that, in each of multiple pixel units 211 belonging to the same ROW line (ROW-n), a gate transistor 215c is connected to a word line 231, and a gate transistor 216c is connected to a second word line 231-2.

Furthermore, in each of the multiple pixel units 211 belonging to the same ROW line (ROW-n), the second ON capacitor 233 is connected to plate line 232 or second plate line 232-2, respectively. For example, in pixel unit 1-1, the second ON capacitor 233 is connected to plate line 232, while in next pixel unit 1-2, the second ON capacitor 233 is connected to second plate line 232-2.

The following is a description of the area around the ON electrode 216 of one pixel <pixel 1-1> shown in the above described Fig. 10A, and the operations of word line 231 (WL-1) and plate line 232 (PL-1) with reference to Figs. 11A, 11B, 11C, 11D, and 11E.

Referring to Fig. 11A, plate line 232 (PL-1) is at L level (0 volts), and "0" volts of bit line 221-2 (Bitline) is applied to ON electrode 216 by means of the H level (5 volts) of word line 231 (WL-1).

In the transition between the states shown in shifting of the state of Fig. 11A to that of Fig. 11B, in which word line 231 (WL-1) is shifted to L level (e.g., 0 volts), the gate transistor 216c is shifted to OFF and ON electrode 216 is separated from bit line 221-2 (Bitline), shifting plate line 232 (PL-1) to H level (e.g., 20 volts), and thereby a 10-volt is applied to ON electrode 216 on the basis of the ratio of the capacitance (e.g., 1: 1) of the second ON capacitor 233 (Cap 3) to that of ON capacitor 216b (Cap 2).

Fig. 11D shows an equivalent circuit in the state illustrated in Fig. 11B.

Referring to Fig. 11B, while word line 231 (WL-1) remains at L level (0 volts), the shifting of plate line 232 (PL-1) to L (0 volts) changes the potential of ON electrode 216 to 10 volts.

Fig. 11E shows an equivalent circuit in the state illustrated in Fig. 11C.

The above description has illustrated one case of Cap 2= 15 femto farad (fF) and Cap 3= 15 fF; if Cap 2 is only the floating capacitance Cf of gate transistor 216c, a voltage close to the potential of plate line 232 (PL-1) will be applied to ON electrode 216.

Fig. 12A illustrates a configuration placing the control circuit of pixel array 210 that arranges pixel units 211 as shown in the above described Fig. 10A.

In order to control plate line 232, which is added to the configuration of pixel array 210, as illustrated in the above described Fig. 3, a plate line driver unit 250 is added.

That is, the present embodiment is configured so that a plate line driver unit 250 is added to the area near pixel array 210, in addition to the provision of bit line driver part 220 and word line driver unit 230.

Word line driver unit 230 comprises a first address decoder 230a and a word line driver 230b, which are used for selecting word lines 231 (WL).

Plate line driver unit 250 comprises a plate line driver 251, and plate line address decoders 252-1 and 252-2, all of which are used for selecting plate lines 232 (PL).

Each pixel unit 211 is connected to bit lines 221-1 and 221-2 of the bit line driver unit 220 (bit line driver) so that data is written to pixel units 211, which belongs to the ROW line selected by a word line 231 (WL).

For a word line 231 (WL), externally input serial data WL_ADDR1 is made parallel to the first address decoder 230a (WL Address Decoder) and is changed to a required voltage by word line driver 230b (WL Driver).

ON electrode 216 of an individual pixel unit 211 is controlled by plate line 232 (PL) separately from word line 231 (WL-1), and, for plate line 232 (PL), externally input serial data PL_ADDRa and PL_ADDRb are made parallel to plate line address decoders 252-1 (PL Address Decoder-a) and 252-2 (PL Address Decoder-b), respectively, so that either value is converted by plate line driver 251 (PL Driver) to the required voltage.

Here, the number of ROM lines comprising multiple pixel units 211 on one horizontal line can be, for example, 720 lines or more.

In such a case, each data signal input to memory cells M1 and M2 from the bit line 221-1 and 221-2, respectively, is transmitted to individual pieces of memory on one ROW line at the speed of 23 nanoseconds (nsec.) or slower.

That is, in order to process 720 ROW lines by dividing and assigning a display period into four colors (red (R), green (G), blue (B) and white (W)) at the rate of 60 frames per second, with each color in 256-bit gray scale, the transmission speed is as follows:

1/60 [sec] / 4 [divisions] / 256 [bit gray scale] / 720 [lines] = 22.6 nsec.

Furthermore, in order to process 1080 ROW lines by dividing and assigning a display period into three colors(R, G and B) at the rate of 60 frames per second, with each color in 256-bit gray scale, the transmission speed is as follows:

1/60/3/256/1080= 20 nsec.

Fig. 12B is a conceptual diagram illustrating the internal configuration of plate line driver 251 (PL Driver) shown in the above described Fig. 12A.

The internal configuration of plate line driver 251 (PL Driver) comprises circuits provided to correspond to plate lines 232 (PL).

In plate line driver 251, an OR circuit 251a is equipped at the initial stage so as to enable either plate line address decoder 252-1 (PL Address Decoder-a) or plate line address decoder 252-2 (PL Address Decoder-b) to select a plate line 232 (PL).

The output of OR circuit 251a is input to flip-flop 251b (Flip-Flop) and the output value is retained therein.

Then, the output value is latched at latch 251c (Latch) with a WL-CLK in order to synchronize with bit line driver part 220 (bit line driver). It is then converted by level shift circuit 251d (Level shift) into the required voltage for applying to ON electrode 216.

Fig. 12C illustrates the internal configuration of the plate line address decoder 252-1 (PL Address Decoder-a) shown in the above described Fig. 12A.

Plate line address decoder 252-1 comprises 1) a serial-parallel conversion circuit 252a for the serial-to-parallel conversion of an external serially input address signal (PL_ADDRa) into the number of bits of plate lines 232, and 2) an address detection unit includes EXOR circuits 252b and NOR circuits 252c, all of which are implemented for the number of bits of PL_ADDRa.

An externally input address signal (PL_ADDRa) is serial-to-parallel converted by serial-parallel conversion circuit 252a and is inputted in parallel to the respective EXOR circuits 252b.

If a plate line (PL) is the same as a plate line 232 (PL) selected by the parallel-converted value, the present PL is selected by the address detection unit (i.e., the EXOR circuit 252b and NOR circuit 252c) corresponding to individual plate line 232.

Although not specifically shown in a drawing, the internal configurations of plate line address decoder 252-2 (PL Address Decoder-b) and the first address decoder 230a (WL Address Decoder) can be similar to that of the above described plate line address decoder 252-1.

Fig. 12D is a diagram showing an exemplary modification configured by adding a function to the address decoder shown Fig. 12C as described above.

If the number of plate lines 232 (PL) is, for example, 1080, the bit width required for the serial input of the PL_ADDRa is 11 bits. In this case, there is a surplus of 967 (= 2047 (i.e., 11 bits) – 1080).

Then, if there is an address input (PL_ADDRa) of 1080 or more, those addresses are

detected and all plate lines 232 (PL) are selected in this case, and thereby reset operations of pixel unit 211 can be performed.

For this purpose, Fig. 12D shows a circuit that further includes an OR circuit 252d for taking the logic sum of the outputs of all address detection units, in addition to being equipped with the address detection units (i.e., the EXOR circuits 252b and NOR circuits 252c) corresponding to surplus address values.

This circuit as shown can detect surplus address(es) if there is an input of 1080 addresses or more and to select all plate lines 232 (PL) at the OR circuit 252d, thereby enabling a reset operation of pixel unit 211.

Fig. 12E is a diagram illustrating the internal configuration of bit line driver unit 220 (Bitline Driver) shown in the above described Fig. 12A.

Bit line driver unit 220, according to the present embodiment, comprises a first stage latch 220a, a second stage latch 220b, a level shift circuit 220c, a third stage latch 220d, an inverter 110e, and a mode changeover switch 220f.

The inverter 110e and mode changeover switch 220f function as a column decoder for controlling bit lines 221-1 and 221-2.

That is, inverter 220e logically inverts the output (latch out) from third stage latch 220d to branch out as a bit line 221-1, while mode changeover switch 220f turns ON/OFF the latch out output to the pre-branched bit line 221-2.

If one ROW is, for example, 1920 bits, bit line driver part 220 receives an external input that is 15 times 128-bit pixel data.

Bit line driver part 220 latches this volume of data in three stages as follows:

First stage: 128 latches (at the first stage latch 220a)

↓

Second stage: 640 latches (at the second stage latch 220b)

↓

Voltage conversion (level shift) (at the level shift circuit 220c)

↓

Third stage: 1920 latches (at the third stage latch 220d)

As such, after performing 1920 latches at the third stage latch 220d, and when the data is sent to the ON side (i.e., the bit line 221-2) and OFF side (i.e., the bit line 221-1) of the bit line, the respective logic states of bit line 221-1 and bit line 221-2 are determined by a judgment logic on the basis of the truth table shown in Fig. 12F.

Fig. 13 is a timing chart depicting the relationship between (i) and (ii), where (i) is the operation timing of the <pixel 1-1> (i.e., pixel unit 211) and <pixel 1-2> (i.e., pixel unit 211) belonging to the same ROW line, and (ii) is the behavior of mirror 212 in pixel array 210 shown in the above described Fig. 10A.

In this case, the respective display states of the two pixel units 211 are a gray display for the < pixel 1-1> and a black display for the <pixel 1-2>.

The <pixel 1-1> and <pixel 1-2> belong to the same ROW line and therefore the mode changeover signal 221-3 (Intermediate), word line 231 (WL-1), and plate line 232 (PL-1) are common signals.

In the example shown in Fig. 13, the signal (WL) on a word line 231 operates during a predetermined interval (i.e., one cycle of an interval between a control timing t1 and a control timing t4 in this case) in order to carry out the selection control of bit line 221-1 and bit line 221-2.

In contrast, the signal (PL) on plate line 232 operates during an interval (i.e., control timing t1 and control timing t2) that is shorter than one cycle of the signal (WL) on a word line 231.

For example, the signal (PL) operates at two consecutive times (refer to the changes in the potentials 232a that is turned ON with the pulse of plate line address decoder 252-1 and turned OFF with the pulse of plate line address decoder 252-2) within the period of one cycle of word line 231 in the example shown in Fig. 13.

Therefore, the transmission speed (i.e., the frequency) of a signal on plate line 232 is faster than the transmission speed (i.e., the frequency) of a signal on word line 231.

Until control time t1, the mirror 212 of the < pixel 1-1> is stationarily deflected to the side of ON electrode 216 if the Latch OUT (i.e., the output of the third stage latch 220d) is "1" and to the side of OFF electrode 215 if the Latch OUT is "0". That is, until control time t1, the operation of mirror 212 is controlled by means of a pulse width modulation (PWM) in accordance with a PWM control profile 451.

Immediately prior to control time t1, mirror 212 is stationarily deflected to the side of ON electrode 216; then, at control time t1, the mode changeover signal 221-3 (Intermediate) is turned to be "H", and (although the latch OUT is "1") OFF electrode 215 and ON electrode 216 are turned to be "0" volts, prompting mirror 212 to start a free oscillation.

At control time t2, plate line 232 (PL-1) is selected by plate line address decoder 252-1 (PL Address Decoder-a) and PL-1 is turned to be an H level potential 232a (i.e., a potential higher than the H level potential 221a of bit line 221 (bit line).

At control time t3, plate line 232 (PL-1) is selected by plate line address decoder 252-2 (PL Address Decoder-b) and plate line 232 is turned to be L level.

During the period between control time t2 and t3, mirror 212 is drawn back to the side of ON electrode 216 and starts an intermediate oscillation (OSC) as shown by an intermediate oscillation control profile 452.

Then, at control time t5, after control time t4, an "H" is set by bit line 221-1 (Bitline) at the side of OFF electrode 215, and mirror 212 is drawn to OFF electrode 215 to be stationary in the OFF state.

Meanwhile, the mirror 212 of the <pixel 1-2> must be continuously stationary on the side of OFF electrode 215, in order to display black.

Plate line 232 (PL-1) is common to the <pixel 1-2> and < pixel 1-1>, and therefore during the period between control time t2 and t3, a voltage (i.e., potential 221a) is generated at ON electrode 216. However, mirror 212 is stationary on the OFF side and the distance between ON electrode 216 and mirror 212 is far, and therefore the Coulomb force applied to the mirror 212 is weak and the position thereof will not be changed.

Note that the interval between control time t1 and t2 (i.e., a predetermined delay time) can be set to be the same (i.e., constant) within one frame.

Furthermore, the above described predetermined delay time can be determined by the intensity of illumination light or the quantity of reflection light of mirror 212 of a pixel unit 211.

Note that, in Fig. 13, the intermediate oscillation starts at a PWM ON. If it starts at OFF, the method comprises 1) connecting plate line (232) to the memory on the OFF side, 2) connecting the capacitor of the ON side memory to the ground, 3) setting the potential of the electrode A1-1 at "H" and the potential of the electrode B1-1 at "L" at the timing t1, and 4) applying a voltage to the electrode A1-1 from the plate line (232) at control time t2 and t3.

Fig. 14 is a timing chart of the ROW lines and address decoder which are shown in Fig. 12A.

In Fig. 14, control times t1, t2, t3, and t4 correspond to times t1 through t4 as shown in Fig. 13.

On ROW 1, at control time t1, word line 231 (WL-1) carries out data loading and then first address decoder 230a (WL_ADDR1) selects ROW 2, 3, 4 through 1080 sequentially to carry out data loading.

At control time t2, plate line address decoder 252-1 (PL_ADDRa) selects plate line 232 (PL-1).

Plate line address decoder 252-1 (PL_ADDRa) selects PL-2, 2-3, 2-4 through 2-1080 sequentially.

At control time t3, plate line address decoder 252-2 (PL_ADDRb) selects plate line 232 (PL-1).

Plate line address decoder 252-2 (PL_ADDRb) selects PL-2, 2-3, 2-4 through 2-1080 sequentially.

As such, the control of the intermediate oscillation of all ROW lines is enabled in the minimum interval (i.e., during the period between control time t1 and t4) of data loading performed by word line 231 (WL).

Fig. 15 is a conceptual diagram showing another possible modification of pixel unit 211. Fig. 15 shows a second ON electrode 235 (i.e., an electrode C) connected directly to plate line 232, in addition to comprising the ON electrode 216 (i.e., the electrode B).

That is, in contrast to the configuration of controlling ON electrode 216 by means of plate line 232 (PL), as shown in the above described Fig. 12A (in which two electrodes, that is, OFF electrode 215 and ON electrode 216, are equipped for one pixel) pixel unit 211, as shown in Fig. 15, has a second ON electrode 235 (i.e., an electrode C) and connects plate line 232 (PL) directly to the electrode C without the intervention of a circuit element.

The drive circuit for pixel unit 211 shown in Fig. 15 is the same as that shown in Fig. 12A.

Figs. 15A and 15B are cross-sectional diagrams of a pixel unit 211, in an ON state and an OFF state, respectively, comprising two electrodes, i.e., an ON electrode 216 and a second ON electrode 235, on the ON side illustrated in Fig. 15.

Note that the delineation symbols used in Figs. 15A and 15B are the same as those described in Fig. 8A.

Figs. 15C and 15D are plain view diagrams showing possible layouts of the added second ON electrode.

The configuration of Fig. 15D shows surface electrodes 909b and 908a, which includes the ON electrode 216 in the configuration shown in the above described Fig. 8B, electrically mutually independent and connected to plate line 232 (PL), and thereby the function of the second ON electrode 235 (i.e., the electrode C) is achieved.

Furthermore, Fig. 15D shows a configuration in which surface electrode 908a, of surface electrodes 909b and 908a of above described Fig. 8C, is eliminated and the area of surface electrode 909b is enlarged and divided into two parts. Thereby the function of ON electrode 216 (i.e., the electrode B) and second ON electrode 235 (i.e., the electrode C) are achieved.

Fig. 15E is a plain view diagram showing another possible layout of electrode B connected to word line 231 and electrode C connected to plate line 232. Fig. 15F is a cross-sectional diagram.

Electrode C (i.e., surface electrode 908a), which is connected to plate line 232, is placed near elastic hinge 911 in a rectangular-shaped character "C" so as to surround elastic hinge 911. Additionally, electrode B, which is connected to word line 231, is placed so as to surround three sides of electrode C.

Fig. 15G is configured, in pixel unit 211 shown in the above described Fig. 15, with the additional of a second ON capacitor 217b and a second ON gate transistor 217c, both of which are used to control second ON electrode 235. A second plate line 232-2 is also added.

Additionally, the second ON capacitor 217b is connected to plate line 232, and the second ON capacitor 217b is also connected to the newly added second plate line 232-2.

Fig. 15H differs from Fig. 15G in that the configuration of Fig. 15H is equipped with a second word line 231-2 instead of second plate line 232-2.

Furthermore, the gate of the second ON gate transistor 217 of the second ON electrode 235 is connected to, and controlled by, the second word line 231-2.

Fig. 16 is a timing chart showing 1) the operation timings of the < pixel 1-1> and < pixel

1-2>, both of which belong to the same ROW line, and 2) the operation of mirror 212 in pixel unit 211, which is equipped with the second ON electrode 235 shown in the above described Fig. 15.

Additionally, the < pixel 1-1> displays gray, while the < pixel 1-2> displays black.

Since the two belong to the same ROW line, the mode changeover signal 221-3 (Intermediate), word line 231 (WL-1), and plate line 232 (PL-1) are common signals to the < pixel 1-1> and < pixel 1-2>.

In contrast to the timing chart shown in the above described Fig. 13, the chart shown in Fig. 16 are the waveforms of ON electrode 216 (i.e., the electrode B) and second ON electrode 235 (i.e., the electrode C) when attracting mirror 212 from the ON state to the oscillation state.

That is, in Fig. 16, mirror 212 is attracted to the oscillation state by changing the potential of second ON electrode 235 (i.e., the electrode C) to a potential 232a by plate line 232, instead of changing the potential of ON electrode 216.

As such, in this configuration the second ON electrode 235 is equipped in addition to ON electrode 216, and the potential of the second ON electrode 235 is controlled by plate line 232 as shown in Fig. 15, et cetera. This makes it possible to apply a voltage to the second ON electrode 235 independent from the signals from bit lines 221-1 and 221-2, thus enabling a more accurate control of operations than the control by means of only word line 231 or the like.

Furthermore, control by plate line 232 makes it possible to have multiple voltages applied to the address electrodes, such as the second ON electrode 235 and ON electrode 216, thereby attaining a more complex operation control.

This configuration enables a sufficient level of drive voltage for memory cell M2 and control of the high-speed timing for applying the voltage, thereby attaining a high-speed operation control for mirror 212.

Incidentally, bit data is ignored in the example configuration shown in Fig. 15, and, therefore, the drive voltage is increased for each line of plate lines 232. In this case, such a lump control for each line of plate lines 232 does not create a problem because it is an amplitude adjustment in the oscillation control for mirror 212.

Figs. 17A, 17B, 17C, 17D, and 17E are timing diagrams for showing various exemplary PWM control profile 451 (PWM) (i.e., a PWM drive timing 440) and an intermediate oscillation control profile 452 (OSC) (i.e., an OSC drive timing 441) in mirror control profile 450 for one frame period of a mirror.

The mirror control profile shown in Fig. 17A illustrates the generation of a PWM control profile 451 and an intermediate oscillation control profile 452 sequentially, in the latter part of one frame.

Fig. 17B illustrates the generation of PWM control profile 451 at the beginning of one frame and generation of intermediate oscillation control profile 452 toward the end of one frame.

Fig. 17C illustrates the case of generation intermediate oscillation control profile 452

during the first half of one frame and then the generation of PWM control profile 451.

Fig. 17D illustrates the case of generation intermediate oscillation control profile 452 at the start of one frame and the generation of PWM control profile 451 at the end of the frame.

Fig. 17E illustrates the aligning of the ON position of PWM control profile 451 with the beginning of one frame and the aligning of the end of intermediate oscillation control profile 452 with the end of one frame.

The pattern (i.e., the intermediate oscillation control profile 452) of mirror 212 of the pixel displaying gray (i.e., < pixel 1-1>) shown in the above described Figs. 13 and 16 corresponds to the above described Fig. 17A.

Note that the present embodiment is also configured to be capable of changing oscillation states in the midst of an intermediate oscillation (i.e., the intermediate oscillation control profile 452).

Figs. 17F and 17G show the operation of mirror 212 when a voltage is re-applied, from plate line 232 (PL), to ON electrode 216 (i.e., the electrode B) in the midst of an intermediate oscillation, for example, under the control shown in Fig. 13.

Referring to Figs. 17F and 17G, a re-application voltage is generated at ON electrode 216 at control time t6, so that the waveforms of the intermediate oscillation are changed by the timing of the application, the period of time of the application, and the voltage of the re-application.

In Fig. 17F, the period of application time of the re-application voltage 221b is relatively small and therefore the center of the oscillation of mirror 212 does not change and only the amplitude becomes smaller.

In contrast, Fig. 17G shows that the period of application time of the re-application voltage 221b is relatively large and therefore the center of the oscillation of mirror 212 is biased to the ON side instead of the center.

Fig. 18 illustrates the placing of a diode 236 in place of the second ON capacitor 233 in the configuration of pixel unit 211 as shown in the above described Fig. 10A.

The drive circuit for pixel unit 211 in this case is the same as Fig. 12A. The drive timing, however, uses bit line 221-1(bit line) at the end of returning the mirror 212 as described below.

Fig. 19 is a timing chart illustrating the operation of mirror 212 and the operation timing of the < pixel 1-1> and < pixel 1-2> that belong to the same ROW line of the pixel array 210 as shown in Fig. 18.

Also, in this case, of the two pixel units 211 in focus, the < pixel 1-1> displays gray, while the < pixel 1-2> displays black.

Since the two belong to the same ROW line, the mode changeover signal 221-3 (Intermediate), word line 231 (WL-1), and plate line 232 (PL-1) are common signals to the < pixel 1-1> and < pixel 1-2>.

The example control shown in Fig. 19 differs from the example control shown in the

above described Fig. 13 since the former discharges ON electrode 216 at control time t3 with bit line 221-1 (bit line) and word line 231 (WL) (refer to the waveform at control time t3 in word line 231).

Therefore, only one PL Address Decoder (i.e., plate line address decoder 252-1 and plate line address decoder 252-2) is required.

Fig. 20 illustrates the connection between the address decoder and bit line driver part 220 (bit line driver) that are used for selecting word line 231 (WL) and plate line 232 (PL) of pixel array 210.

As shown in Fig. 20, this is a simple configuration connecting one plate line address decoder 252 to plate line driver 251, in place of connecting two plate line address decoders 252-1 and 252-2 thereto.

Fig. 21 shows another possible modification of the configuration of pixel unit 211 according to the present embodiment.

The configuration shown in Fig. 21 places a field effect transistor 237 (FET) in place of second ON capacitor 233 in the configuration of pixel unit 211 shown in the above described Fig. 10A.

That is, plate line 232 is connected to the gate electrode of field effect transistor 237, and the applied voltage from plate line 232 controls whether or not a power source voltage Vcc (to which the drain of field effect transistor 237 is connected is) is applied to ON capacitor 216b.

The drive circuit for pixel unit 211 according to the example modification shown in Fig. 21 is the same as that of the above described Fig. 12A.

The drive time of pixel unit 211, comprising field effect transistor 237, is controlled in the same manner as that of the circuit shown in Fig. 12A, where the setup voltage from plate line 232 (PL) to ON electrode 216 is determined by the power source voltage Vcc, to which the drain of the FET is connected, instead of being determined by the voltage of plate line 232 (PL).

Fig. 22A is a conceptual diagram showing an example modification of the configuration of pixel array 210 according to the present embodiment.

The configuration illustrated in Fig. 22A divides multiple ROW lines (ROW-1 through ROW-1080) into upper and lower groups (i.e., an upper row line area 210a and a lower row line area 210b, each comprising an upper bit line driver part 220-1 and a lower bit line driver part 220-2 (bit line Driver), a first address decoder 230a, a word line driver 230b (WL Address Decoder_up and WL Driver_up, WL Driver_down and WL Driver_down), a plate line driver 251-1, a plate line address decoder 252-1, and a plate line address decoder 252-2 (PL Address Decoder-a_up and PL Driver_up, PL Address Decoder-a_down, b_down and PL Driver_up, down)).

Specifically, multiple row lines are divided into the upper row line area 210a including row lines ROW-1 through ROW-540, and the lower row line area 210b that includes row lines ROW-541 through ROW-1080.

In this case, the level change (i.e., the potential 232a) of plate line 232 is accomplished by plate line address decoder 252-1 changing it to H level and plate line address decoder 252-2 changing it to L level.

Fig. 22B shows an example configuration in which plate line driver 251-1 (PL Driver_up) and plate line driver 251-2 (PL Driver_down) that are equipped for the upper and lower ROW line groups, each equipped with one plate line address decoder 252 (PL Address Decoder_up) and one plate line address decoder 252 (PL Address Decoder_down) in the comprisal of pixel array 210 as shown in the above described Fig. 22A.

In this case, the level change (i.e., the potential 232a) of plate line 232 (PL) is carried out by plate line 232 (PL).

Fig. 22C illustrates the configuration in which a first address decoder 230a and a word line driver 230b, a plate line driver 251 and a plate line address decoder 252-1, and a plate line address decoder 252-2 are equipped commonly for each group in the configuration in which multiple ROW lines of a pixel array 210 is divided into the upper and lower groups. Each of the upper and lower ROW line groups is equipped with upper bit line driver part 220-1 and lower bit line driver part 220-2.

In this case, the ROW lines (both upper and lower) applicable to the same address are driven simultaneously. The combination of the respective ROW lines in the upper and lower groups to be simultaneously driven is determined by wirings.

For example, the ROW lines applicable to the same address (in the example of Fig. 22C, the first ROW-1 in the upper group and the first ROW-541 in the lower group) are simultaneously driven.

Fig. 22D shows an example configuration in which plate line driver 251 commonly equipped in the upper and lower groups is separated into a plate line driver 251-1 (PL Driver_up) corresponding to the upper group and a plate line driver 251-2 (PL Driver_down) corresponding to the lower group. The divided drivers are placed correspondingly at the respective groups, according to the configuration of pixel array 210 shown in Fig. 22C.

In this case, the ROW lines belonging to the upper and lower groups are individually driven, unlike the configuration shown in the above described Fig. 22C.

Fig. 23A is a cross-sectional diagram showing an example modification of the configuration of a pixel unit 211 (i.e., a mirror element 4011) according to the present embodiment. Fig. 23B is a conceptual diagram showing an example configuration of the drive circuit for the pixel unit.

Mirror element 4011 (i.e., pixel unit 211) according to the present embodiment comprises a hinge electrode 4009 and an address electrode 4013, both of which are placed on a device substrate 4004 and covered with an insulation layer 4006.

A mirror 4003 is supported on insulation layer 4006 of hinge electrode 4009 by way of an

elastic hinge 4007. In this case, mirror 4003 is supported as a cantilever against elastic hinge 4007, with the entirety of the mirror 4003 protruding over an address electrode 4013.

Furthermore, a stopper 4002 is placed on the other side of the address electrode 4013 across from the elastic hinge 4007, with the lower edge of the stopper 4002 fixed onto the device substrate 4004.

Furthermore, mirror 4003 is tilted to close to address electrode 4013 by a Coulomb force resulting from an application of a voltage V1 to address electrode 4013. Mirror 4003 is stopped at a position abutting on insulation layer 4006 covering address electrode 4013 (which is called an ON state).

Furthermore, when the application of voltage V1 to address electrode 4013 is cut off, mirror 4003 is restored by the elasticity of elastic hinge 4007 to its horizontal position, abutted by the stopper 4002 so that it does not move beyond this state (which is called an OFF state).

The following is a description of a control circuit for mirror element 4011, as illustrated in Fig. 23B. In this case, mirror element 4011 is supported by elastic hinge 4007 in a cantilever and therefore is a configuration equipped with bit line 221-2, gate transistor 216c, ON capacitor 216b, and word line 231, which are the circuit elements of memory cell M2 on the ON side, included in the circuit configuration shown in the above described Fig. 10A.

Furthermore, as shown in Fig.10A, the present embodiment is equipped with plate line 232, in addition to word line 231, and connects plate line 232 to address electrode 4013 by way of the second ON capacitor 233.

Further, with the control using word line 231, plate line 232 and bit line 221-2, the OFF state, ON state, and the intermediate oscillation state that is between the ON state and OFF state, are achieved as described below.

The following is a description of an example method for controlling pixel array 210 comprising the cantilever-structured mirror 4003 as shown in the above described Fig. 23A and 23B.

Note that the control system can use the configuration, as is, as shown in Fig. 12A.

Fig. 24 is a circuit diagram illustrating in detail a part of the layout of pixel array 210 comprising a mirror 4003 (shown in the above described Fig. 23B) that is structured as a cantilever.

Fig. 25 is a timing chart depicting the operation of the mirror and the operation timings of the <pixel 1-1> and <pixel 1-2> belonging to the same ROW line as that of Fig. 24.

The example shown in Figs. 24 and 25 presupposes that the <pixel 1-1> displays gray, while the <pixel 1-2> displays black.

In this case, since the <pixel 1-1> and <pixel 1-2> belong to the same ROW line, the mode changeover signal 221-3 (Intermediate), word line 231 (WL-1), and plate line 232 (PL-1) are common signals to the two of them.

Until control time t1, mirror 4003 of the <pixel 1-1> is in PWM operation and a voltage

V1 in accordance with bit line 221 (bitline) is applied to the electrode.

Specifically, if the voltage at bit line 221 (bitline) is at the H level, mirror 4003 is drawn to address electrode 4013 so as to abut onto insulation layer 4006 of address electrode 4013 and is stationary. This is an ON state.

If the potential at bit line 221 (bitline) is L level, mirror 4003 separates from address electrode 4013, abuts on stopper 4002 and stops thereat. This is an OFF state.

Just prior to control time t1, mirror 4003 is stationary in the ON state, that is, abutting on address electrode 4013., At control time t1, address electrode 4013 is changed by bit line 221 (bitline) to be "0" volts (i.e., discharged), and mirror 4003 starts to separate from address electrode 4013 by means of the elasticity of elastic hinge 4007.

At control time t2, that is, before mirror 4003 is far from address electrode 4013, plate line address decoder 252-1 (PL Address Decoder-a) selects plate line 232 (PL-1), and plate line 232 (PL-1) is changed to H level (i.e., a potential 232b,which is lower than the H level of bit line 221). A voltage is generated at the electrode by the potential 232b so that mirror 4003 is attracted by address electrode 4013 and is stationary thereat.

At control time t3, the plate line address decoder 252-2 (PL Address Decoder-b) selects plate line 232 (PL-1) and, if it is L level, mirror 4003 starts to separate from address electrode 4013 again.

At control time t4, that is before mirror 4003 is far from address electrode 4013, as at t2, the plate line address decoder 252-2 (PL Address Decoder-a) selects plate line 232 (PL-1) and is changed to H level (i.e., the potential 232b) and mirror 4003 is re-attracted to address electrode 4013 and is stationary thereat.

At control time t5, the plate line address decoder 252-2 (PL Address Decoder-b) selects plate line 232 (PL-1), and the PL-1 is changed to L level so that mirror 4003 is re-attracted by address electrode 4013 to be stationary thereat. Simultaneously, or a little thereafter, a memory cell is selected by word line 231, and "0" volts is set by bit line 221.

With this series of operation, mirror 4003 able 1) to generate a smaller quantity of light than the quantity during the minimum data-loading period in accordance with a PWM control with word line 231 (WL) and 2) to express an intermediate gray scale.

In this case, the mirror of the <pixel 1-2> adjacent to the <pixel 1-1> displays black and therefore the mirror needs to be continuously stationary on the side of stopper 4002 (i.e., the OFF side).

Plate line 232 (PL-1) is common to the <pixel 1-1> and <pixel 1-2> and therefore, between control times t2 and t5, a voltage is generated at address electrode 4013. However, mirror 4003 is stationary on the OFF side and the distance between address electrode 4013 and mirror 4003 is far, and, therefore, a Coulomb force applied to mirror 4003 is small, causing no change to the position of mirror 4003.

That is, the control is such as to maintain the following relationship in order not to change the position of mirror 4003:

[H level (V1) of the bit line 221 (Bitline)] > [H level (V2) of the PL]

As such, spatial light modulator 200 comprising mirror element 4011, configured as shown in Figs. 23A and 23B, is configured to control mirror element 4011 with one memory cell M2, thereby making it possible to make the size of the mirror element 4011 more compact and express various gray scale by means of the intermediate oscillation of mirror 4003, in addition to the ON and OFF states, using plate line 232.

In a projection technique using spatial light modulator 200, a reduction in the size of mirror element 4011 makes it possible to obtain both a higher level of definition of the projection image by arraying a larger number of mirror elements 4011 and a higher grade of gray scale with the intermediate oscillation of mirror 4003 using plate line 232.

Fig. 26A is a plain view diagram illustrating the packaging structure of a package accommodating the spatial light modulator shown in the above described Figs. 22A through 22D, et cetera. Fig. 26B is its cross-sectional diagram.

The spatial light modulator 200 according to the present embodiment places the upper bit line driver part 220-1 and lower bit line driver part 220-2 along the upper and lower sides, respectively, which are parallel to the ROW line in the surrounding area of pixel array 210, and places word line driver unit 230 and plate line driver unit 250 along the left and right sides, respectively, which cross the aforementioned upper and lower sides.

The spatial light modulator 200 is accommodated in the concave part 201a of package 201.

Multiple bonding pads 202 are placed in the surrounding area of the concave part 201a of package 201.

Bit lines and address lines placed in the upper bit line driver part 220-1, lower bit line driver part 220-2, word line driver unit 230, and plate line driver unit 250 are connected, by way of bonding wires, to bonding pads 202 provided in the surrounding area, and are further connected electrically, by way of external connection electrodes (which are not shown in a drawing here) that are placed on the bottom part of the package 201, to the wiring board or the like of a projection apparatus (which is described below) incorporating package 201.

The following is a description of an example configuration of a projection apparatus comprising spatial light modulator 200 equipped with the above described plate line 232. Note that the constituent component corresponding to the previously described constituent component is noted in the drawing with a corresponding sign in parenthesis as appropriate.

Fig. 27 is a conceptual diagram showing the configuration of a projection apparatus according to a preferred embodiment of the present invention.

As shown in Fig. 27, a projection apparatus 5010 according to the present embodiment comprises a single spatial light modulator (SLM) 5100 (i.e., the spatial light modulator 200), a

control unit 5500 (i.e., the control apparatus 300), a Total Internal Reflection (TIR) prism 5300, a projection optical system 5400, and a light source optical system 5200.

The spatial light modulator 5100 is implemented according to the above-described spatial light modulator 200 comprising plate line 232.

The projection apparatus 5010 is generally referred to as a single-panel projection apparatus 5010 implemented with a single spatial light modulator 5100.

The projection optical system 5400 is equipped with spatial light modulator 5100 and TIR prism 5300 in the optical axis of projection optical system 5400, and the light source optical system 5200 is equipped in such a manner that the optical axis thereof matches that of projection optical system 5400.

The TIR prism 5300 causes 1) an illumination light 5600 from light source optical system 5200, which is placed onto the side, to enter spatial light modulator 5100 at a prescribed inclination angle relative thereto as incident light 5601 and 2) a reflection light 5602 reflected by spatial light modulator 5100 so as to reach projection optical system 5400.

The projection optical system 5400 projects reflection light 5602, as projection light 5603, by way of spatial light modulator 5100 and TIR prism 5300 to a screen 5900 or the like.

The light source optical system 5200 comprises an adjustable light source 5210 for generating illumination light 5600, a condenser lens 5220 for focusing illumination light 5600, a rod type condenser body 5230, and a condenser lens 5240.

The adjustable light source 5210, condenser lens 5220, rod type condenser body 5230, and condenser lens 5240 are sequentially placed in the aforementioned order on the optical axis of illumination light 5600 emitted from adjustable light source 5210 and incident to the side face of TIR prism 5300.

The projection apparatus 5010 employs a single spatial light modulator 5100 for implementing a color display on the screen 5900 by means of a sequential color display method.

That is, adjustable light source 5210, comprising a red laser light source 5211, a green laser light source 5212, and a blue laser light source 5213 (which are not shown in a drawing here), which allows independent controls for the light emission states, performs the operation of dividing one frame of display data into multiple sub-fields (i.e., three sub-fields, that is, red (R), green (G) and blue (B) in the present case) and causes the red laser light source 5211, green laser light source 5212, and blue laser light source 5213 to emit each respective light in at the time frame corresponding to the sub-field of each color as described below.

Fig. 28 is a block diagram showing an example configuration of control unit 5500 comprised in the above described single-panel projection apparatus 5010. Control unit 5500 comprises a frame memory 5520, an SLM controller 5530, a sequencer 5540, a video image analysis unit 5550, a light source control unit 5560, and a light source drive circuit 5570.

The sequencer 5540 implements a microprocessor and the like, controls the operation

timing and the like of the entirety of control unit 5500 and spatial light modulator 5100.

The frame memory 5520 retains, for example, the equivalent to one frame, input digital video data 5700 (i.e., a binary video image signal 400) from an external device (not shown in a drawing herein) that is connected to a video signal input unit 5510. The input digital video data 5700 is updated, moment-by-moment, every time the display of one frame is completed.

The SLM controller 5530 processes the input digital video data 5700 read from the frame memory 5520 as described below, separating the read data into multiple sub-fields, and outputs them to the spatial light modulators 5100 as control data used for implementing the ON/OFF control and oscillation control (which are described below) of a mirror 5112 of spatial light modulator 5100.

The sequencer 5540 outputs a timing signal to the spatial light modulators 5100 synchronously with the generation of data at the SLM controller 5530.

The video image analysis unit 5550 outputs a video image analysis signal 6800 used for generating various light source pulse patterns on the basis of the input digital video data 5700 inputted from the video signal input unit 5510.

The light source control unit 5560 controls, by way of the light source drive circuit 5570, the operation of adjustable light source 5210 emitting illumination light 5600 on the basis of the video image analysis signal 6800 obtained from the video image analysis unit 5550 by way of the sequencer 5540.

The light source drive circuit 5570 drives the red laser light source 5211, green laser light source 5212, and blue laser light source 5213 of adjustable light source 5210 to emit light on the basis of an instruction from the light source control unit 5560.

Fig. 29 is a conceptual diagram showing another exemplary modification of a multi-panel projection apparatus according to the present embodiment.

The projection apparatus 5040 is configured so that multiple to place spatial light modulators 5100 (i.e., the spatial light modulator 200) corresponding to the three respective colors R, G and B, so as to be adjacent to one another in the same plane on one side of a light separation/synthesis optical system 5330.

This configuration makes it possible consolidate spatial light modulators 5100 into the same packaging unit, for example, a package 201 or the like, and thereby save space.

The light separation/synthesis optical system 5330 comprises a TIR prism 5331, a TIR prism 5332, and a TIR prism 5333.

TIR prism 5331 has guides to spatial light modulators 5100 illumination light 5600, incident in the lateral direction of the optical axis of projection optical system 5400, as incident light 5601.

TIR prism 5332 separates a red color light from the incident light 5601 and guides it to the red color-use spatial light modulator 5100, and also captures reflection light 5602 of the separated

incident light and guides it to projection optical system 5400.

Likewise, TIR prism 5333 separates the incident lights of green and blue colors from incident light 5601, makes them incident to the individual spatial light modulators 5100, equipped correspondently to their respective colors, and captures reflection lights 5602 of the respective colors and guides them to projection optical system 5400.

Fig. 30 is a block diagram showing an example configuration of the control unit of a multi-panel projection apparatus according to the present embodiment.

Control unit 5502 comprises SLM controllers 5531, 5532, and 5533, which are used for controlling each of the spatial light modulators 5100 equipped for the colors R, G and B. The comprisal of the controllers is different from the above described control unit 5500, which is otherwise similar.

That is, SLM controller 5531, SLM controller 5532, and SLM controller 5533 correspond to their respective color-use spatial light modulators 5100, which are formed on the same substrates as those of their respective spatial light modulators 5100 (i.e., the spatial light modulators 200). This configuration makes it possible to place the individual spatial light modulators 5100 and the respectively corresponding SLM controller 5531, SLM controller 5532, and SLM controller 5533 close to each other, thereby enabling a high speed data transfer rate.

Furthermore, a system bus 5580 is formed to connect to the frame memory 5520, light source control unit 5560, sequencer 5540, and SLM controllers 5531 through 5533, in order to speed up and simplify the connection path of each connecting element.

Fig. 31 is a functional block diagram for showing an exemplary modification of a multi-panel projection apparatus according to another preferred embodiment of the present invention.

The projection apparatus 5020 shown in Fig. 31 is implemented with two spatial light modulators 5100 (i.e., the spatial light modulators 200), each of which comprises the above described plate line 232, wherein one spatial light modulator 200 modulates the green light while the other spatial light modulator 200 modulates the red and blue lights.

Specifically, projection apparatus 5020 comprises a dichroic mirror 5320 as a light separation/synthesis optical system.

Dichroic mirror 5320 separates the wavelength component of a green light and the wavelength components of red and blue lights from incidence light 5601, which is incident from light source optical system 5200, causing them to branch into two spatial light modulators 200, respectively, synthesizing reflection light 5602 of the green light reflected (i.e., modulated) by the corresponding spatial light modulator 200 with the reflection light of the red and blue light reflected (i.e., modulated) by the corresponding spatial light modulator 200 to guide the synthesized light to the optical axis of projection optical system 5400, and projecting the synthesized light onto a screen 5900 as projection light 5603.

Fig. 32 is a block diagram for showing an example configuration of a control unit 5506 provided in projection apparatus 5020 comprising the above-described two spatial light modulators 200. In this case, SLM controller 5530 controls two spatial light modulators 5100 (i.e., the spatial light modulators 200), which is the only difference from the configuration shown in Fig. 28.

Fig. 33 is a timing diagram for showing the waveform of a control signal of the projection apparatus according to the present embodiment.

A drive signal (i.e., a mirror control profile 450 shown in Fig. 33) generated by SLM controller 5530 drives multiple spatial light modulators 5100.

The light source control unit 5560 generates a light source profile control signal 5800 corresponding to mirror control profile 450, which is a signal for driving individual spatial light modulators 5100 for inputting the signal generated to light source drive circuit 5570, which then adjusts the intensity of the laser light (i.e., the illumination light 5600) emitted from the red laser light source 5211, the green laser light source 5212, and the blue laser light source 5213.

The control unit 5506 comprised in the projection apparatus 5020 is configured such that a single SLM controller 5530 drives the spatial light modulators 5100, thereby enabling the irradiation of illumination light 5600 on the respective spatial light modulators 5100 with the optimal quantity of light, without a requirement to configure the light source control unit 5560 or light source drive circuit 5570 for each spatial light modulator 5100. This configuration simplifies the circuit configuration of the control unit 5506.

As shown in Fig. 33, the light source control unit 5560 and light source drive circuit 5570 drives the red laser light source 5211, green laser light source 5212, and blue laser light source 5213 so as to adjust the intensities of individual lasers (i.e., illumination light 5600) of the colors R, G, and B synchronously with the irrespective SLM drive signals (i.e., the mirror control profile 450) generated by the SLM controller 5530.

In this case, two colors, R and B, share one spatial light modulator 5100, and therefore the control is a color sequential method.

That is, one frame includes multiple subfields, that include subfields 6701, 6702, and 6703, and the same light source pulse pattern 6815 is repeated in each subfield in one spatial light modulator 5100 corresponding to green (G).

Meanwhile, the pulse emission of the red laser light source 5211 and blue laser light source 5213 for the red (R) and blue (B) lights that share one spatial light modulator 5100are separately controlled. Therefore, the subfields that include subfields 6701 through 6703 are alternately applied in a time series as the light source pulse pattern 6816 and light source pulse pattern 6817.

Furthermore, with the light source as described, the emission pulse intervals ti and emission pulse widths tp can be changed in the light source pulse pattern 6815 of the green laser, the light source pulse pattern 6816 of the red laser, and the light source pulse pattern 6817 of the

blue laser.

Therefore, the present embodiment can improve the levels of the gray scale for each of the R, G, and B colors.

According to above descriptions, the present invention discloses a system configuration and method for increasing the definition of the projection image while improving the levels of the gray scale for an image projection system implemented with a spatial light modulator.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alternations and modifications will no doubt become apparent to those skilled in the art after reading the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alternations and modifications as fall within the true spirit and scope of the invention.

The present invention makes it possible to provide a technique enabling both a high definition and a high degree of gradation of a projection image in a projection technique using a spatial light modulator.

The present invention also makes it possible to provide a technique enabling the implementation of a high degree of operation control for a mirror by applying a sufficient drive voltage to pixel units constituting a spatial light modulator and by controlling a high speed application timing of the aforementioned drive voltage.

CLAIMS

What is claimed is:

1. A mirror array device, comprising:
a plurality of mirror elements each comprising a hinge and a deflectable mirror supported by the hinge; a memory cell for controlling the mirror element; a bit line for transmitting a data signal to the memory cell; a word line for controlling a connection between the bit line and the memory cell; a plate line for controlling the memory cell; each of said mirror elements further comprises a first address electrode controlled by the word line to connect to the memory cell; and each of said mirror elements further includes a second address electrode electrically connected to the plate line.

2. The mirror array device according to claim 1, wherein:
the first and second address electrodes disposed on a surface of a device substrate having different cross sectional shapes and/or heights.

3. The mirror array device according to claim 2, wherein:
one of the first and second address electrodes is disposed near a deflection axis of the mirror element and the other address electrode is disposed at a greater distance from the deflection axis.

4. The mirror array device according to claim 3, wherein:
the address electrode disposed near the deflection axis further comprises a stopper for regulating a range of angular deflection of the deflectable mirror.

5. The mirror array device according to claim 2, wherein:
a borderline dividing the first and second address electrodes is placed on the device substrate in a direction approximately perpendicular to the deflection axis of the deflectable mirror.

6. The mirror array device according to claim 2, wherein:
a borderline dividing the first and second address electrodes is disposed on a location on the device substrate to locate in adjacent to at least sides of the first and second address electrodes.

7. The mirror array device according to claim 2, wherein:
the first address electrode has a different cross sectional area from the second address electrode.

8. The mirror array device according to claim 1, wherein:
the first and second address electrodes are configured and controlled for application of different voltages thereon.

9. The mirror array device according to claim 1, wherein:
the first and second address electrodes are address electrodes are configured and controlled for applying a same range of voltages thereon.

10. A mirror array device, comprising:
a plurality of mirror elements each comprising a hinge and a deflectable mirror supported by the hinge; a memory cell for controlling the mirror element; a bit line for transmitting a data signal to the memory cell; a word line for controlling a connection between the bit line and the memory cell; a plate line for controlling the memory cell; and each of the mirror elements further comprises an address electrode connected to the word line and the plate line to apply an adjustable drive voltage to the address electrode.

11. The mirror array device according to claim 10, wherein:
each of the mirror elements comprises at least one address electrode.

12. The mirror array device according to claim 10, wherein:
each of the mirror elements comprises two address electrodes.

13. The mirror array device according to claim 10, wherein:
the address electrodes are disposed at locations for applying a voltage to draw the mirror element to an ON angular direction and an OFF angular directions and the address electrodes are further configured and controlled for applying adjustable drive voltages thereon.

Fig. 1A (Prior Art)

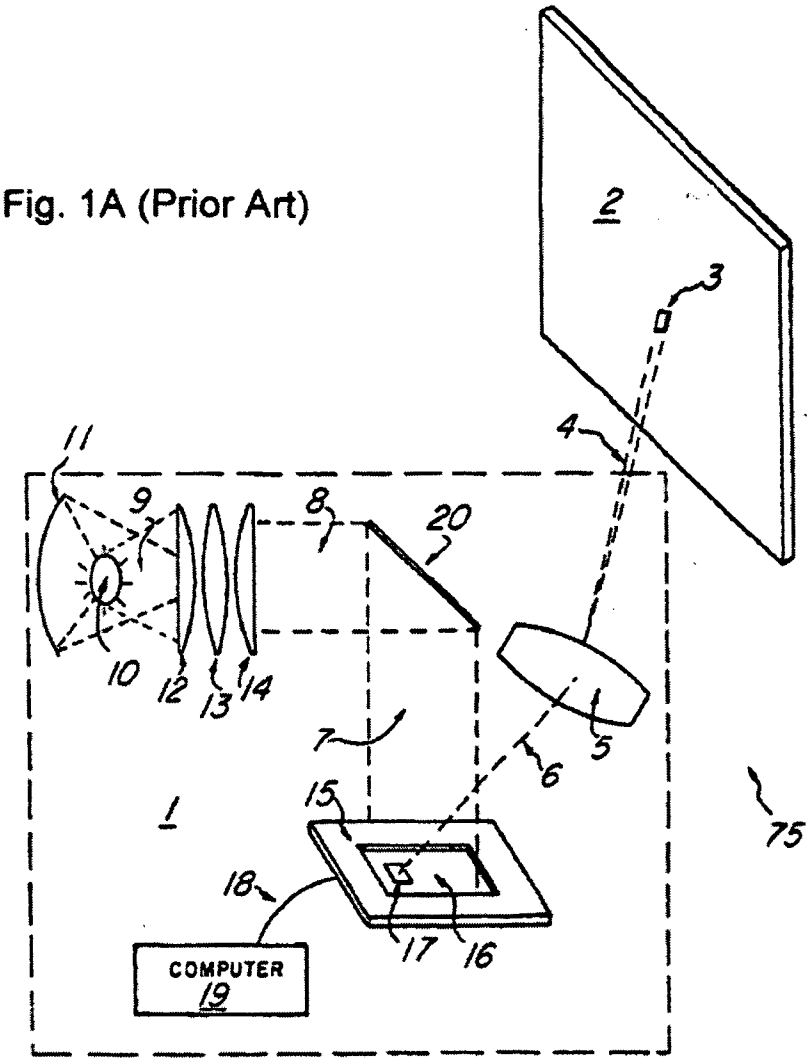
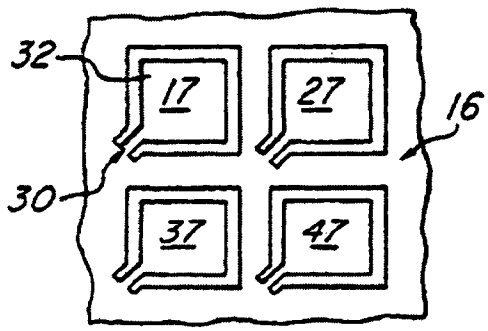


Fig. 1B(Prior Art)



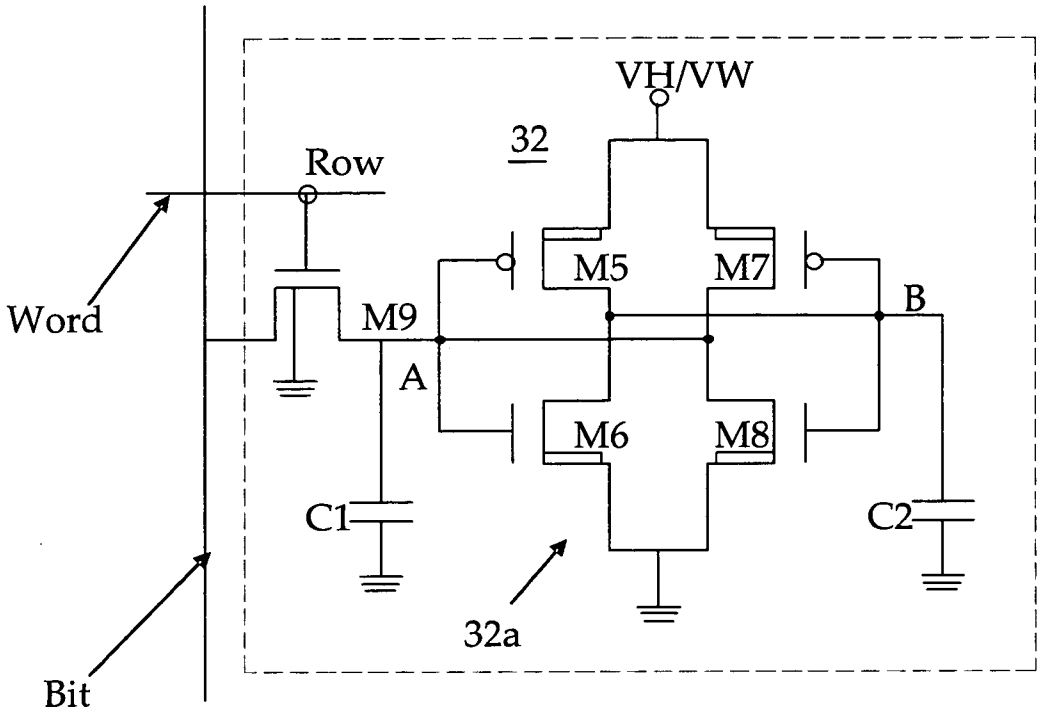


Fig.1C (Prior Art)

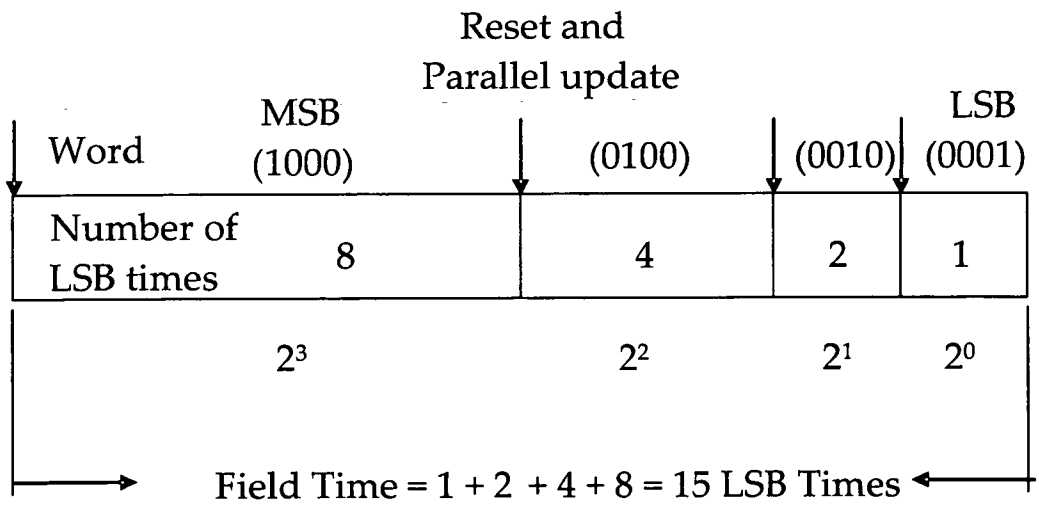


Fig. 1D (Prior Art)

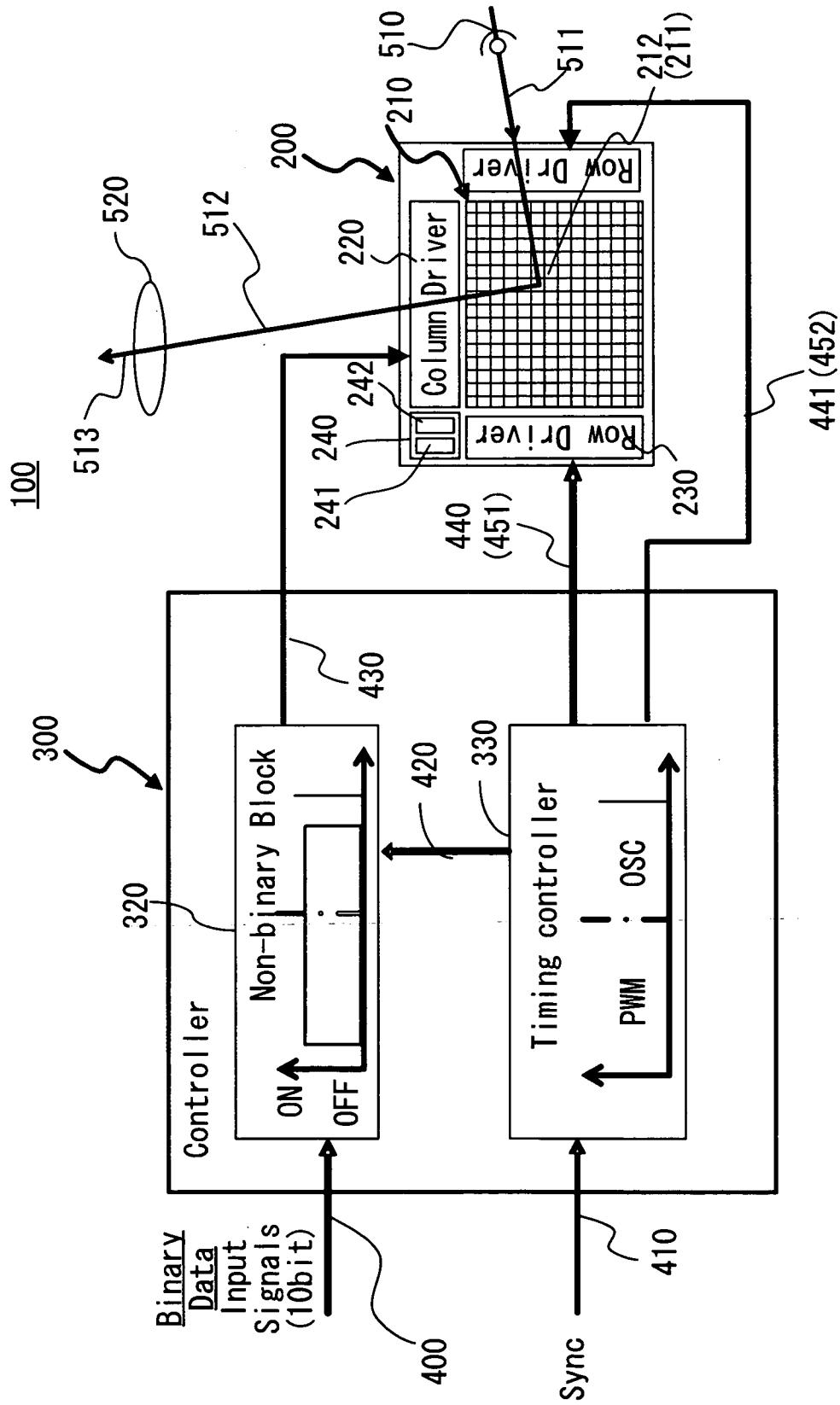

100
200
210
212 (211)
220
230
240
241
242
300
320
330
400
410
420
430
440 (451)
441 (452)
510
511
512
513
520
Row Driver
Column Driver
Row Driver
Controller
Non-binary Block
ON
OFF
Timing controller
PWM
OSC
Binary Data Input Signals (10bit)
Sync

FIG. 2

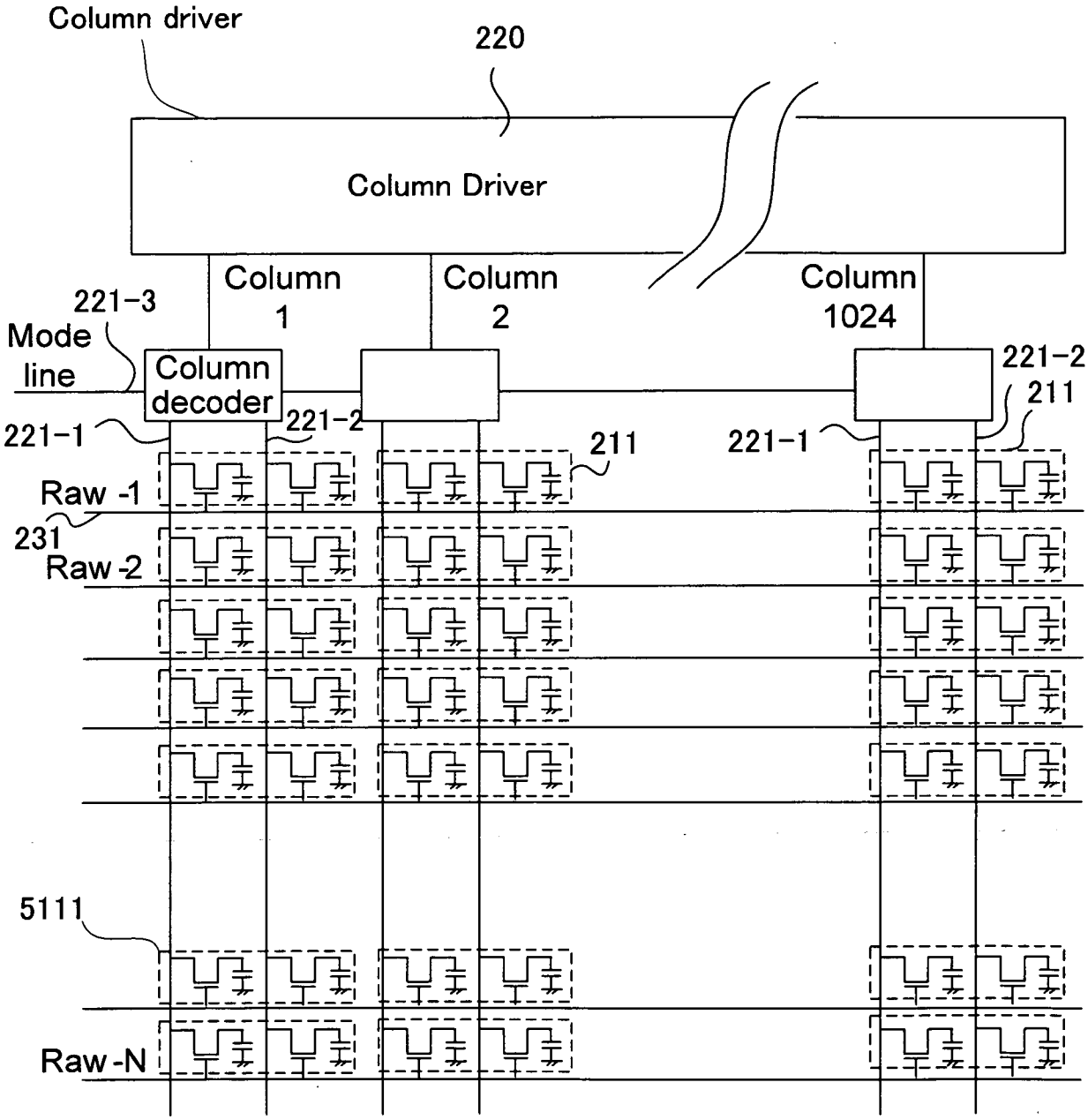


FIG. 3 **Transistor array**

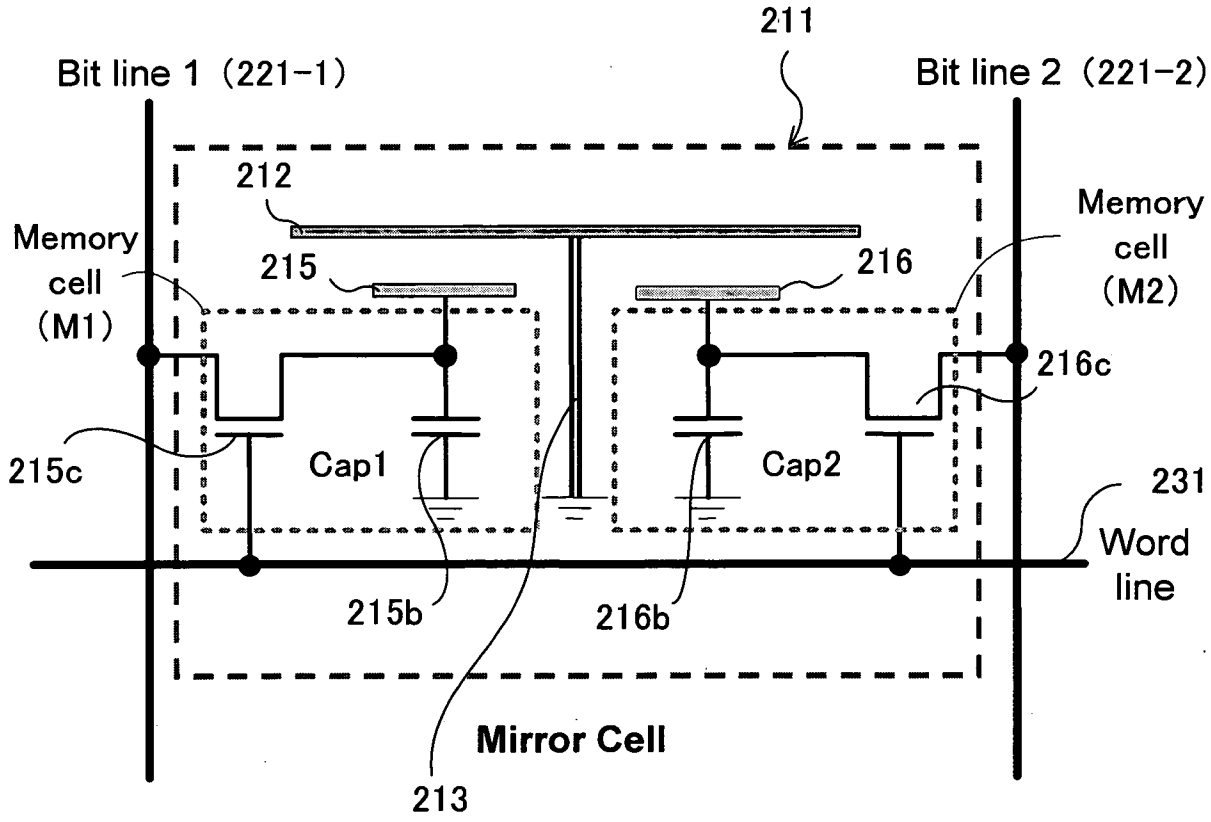


FIG. 4 **Mirror Cell structure**

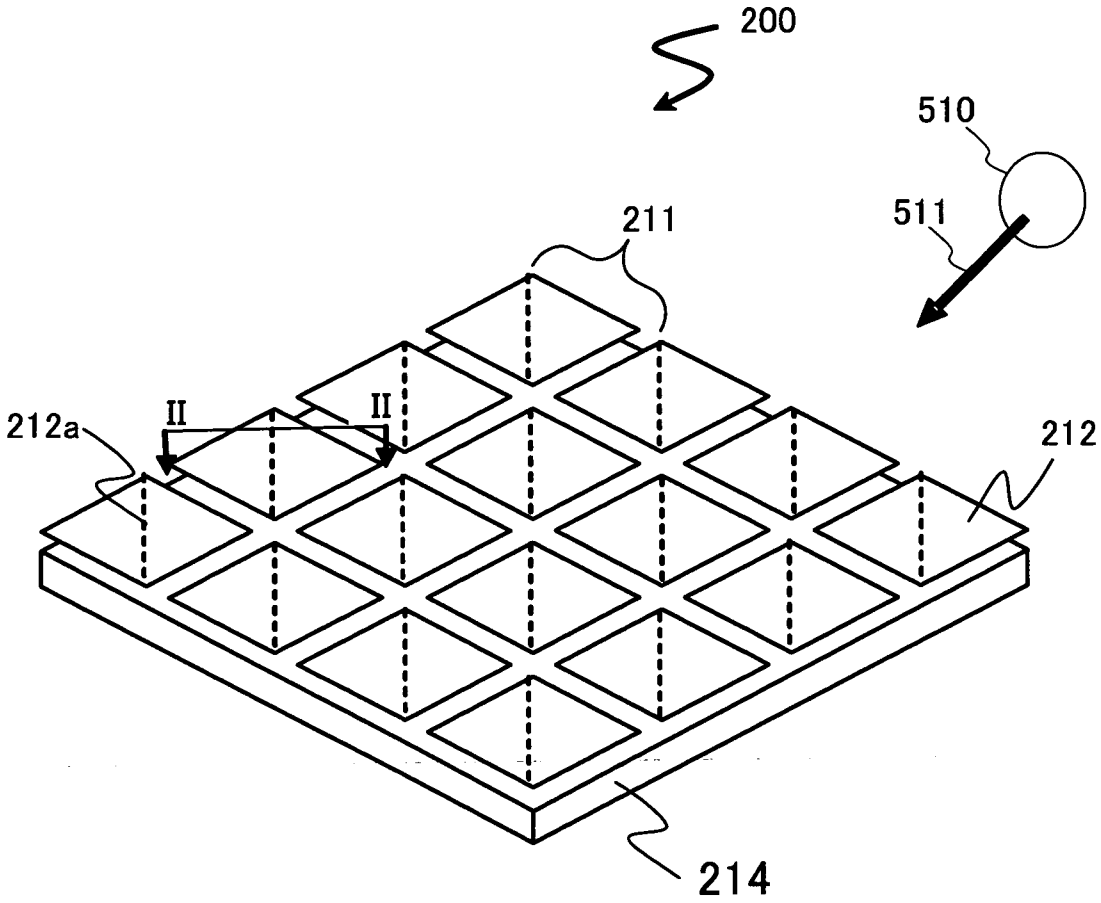


Fig. 5

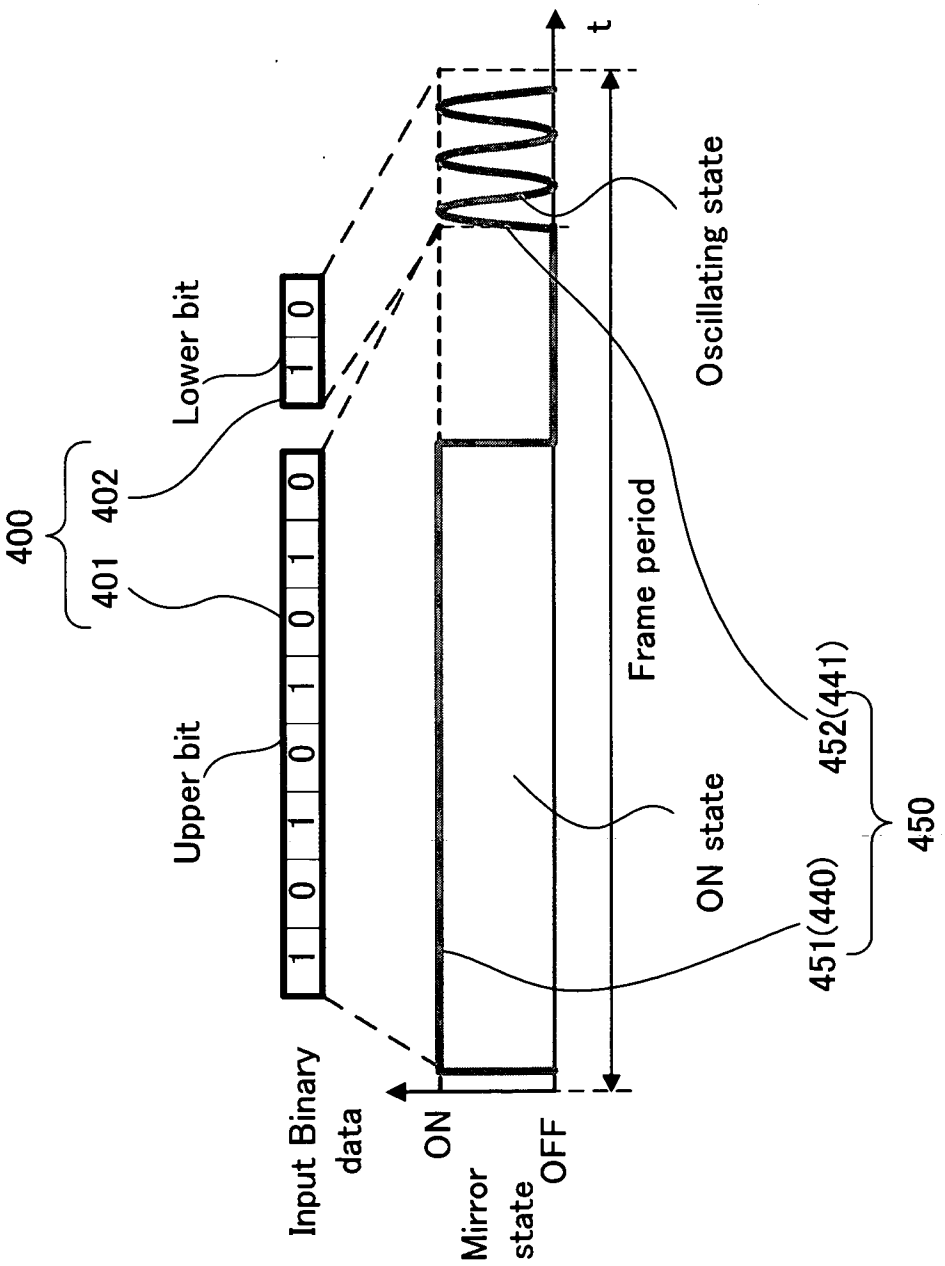

400
401
402
Lower bit
Upper bit
1 0 1 0 1 0 1 0
1 0
Input Binary data
ON
OFF
Mirror state
t
Frame period
Oscillating state
ON state
452(441)
451(440)
450

Fig.6

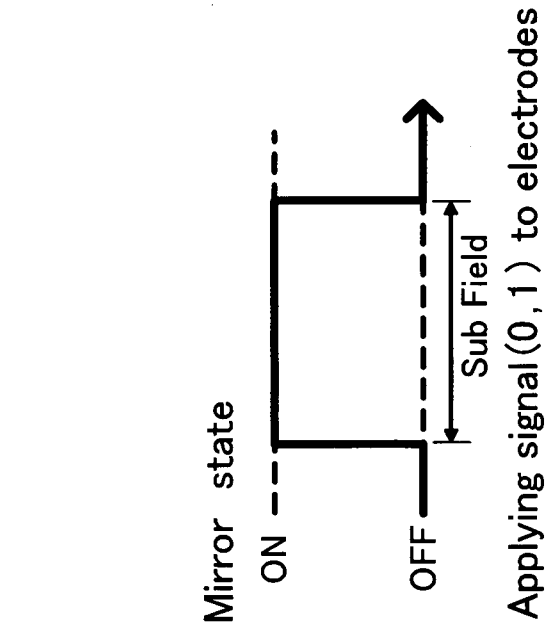

Mirror state
ON
OFF
Sub Field
Applying signal(0,1) to electrodes

Fig.7B

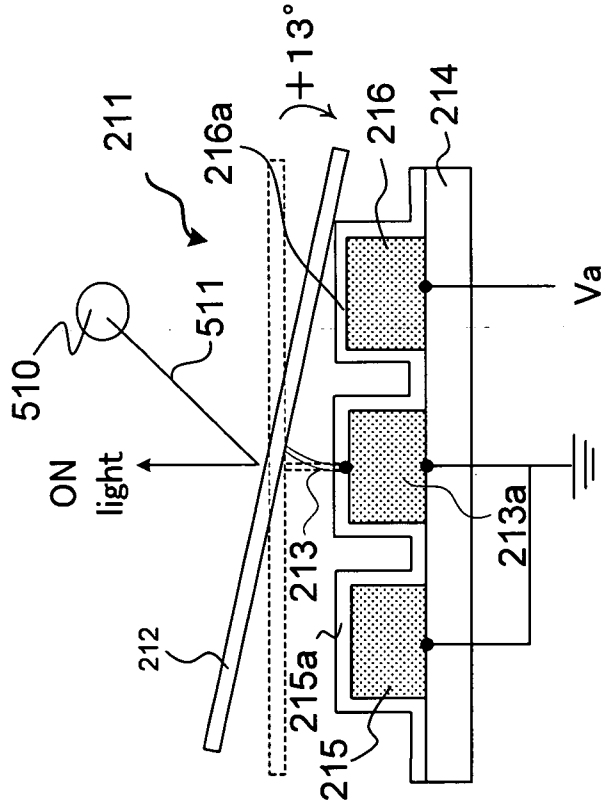

211
216a
+13°
216
214
510
511
ON
light
Va
213
213a
212
215a
215

Fig.7A

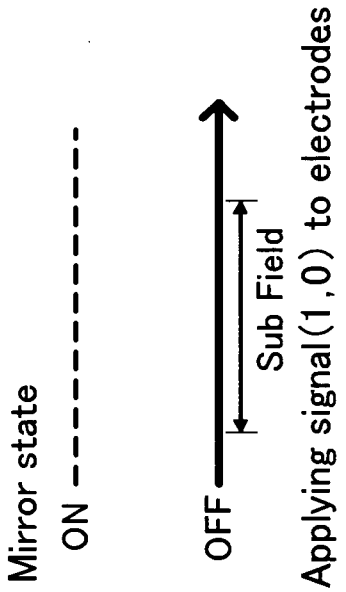

Mirror state
ON
OFF
Sub Field
Applying signal(1,0) to electrodes

Fig.7D

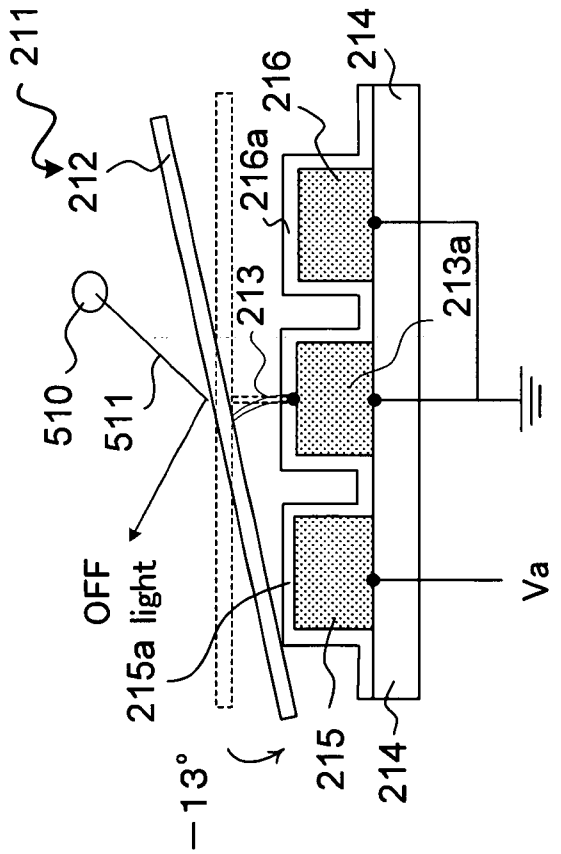

211
212
216
214
216a
213
213a
510
511
OFF
215a light
Va
215
214
−13°

Fig.7C

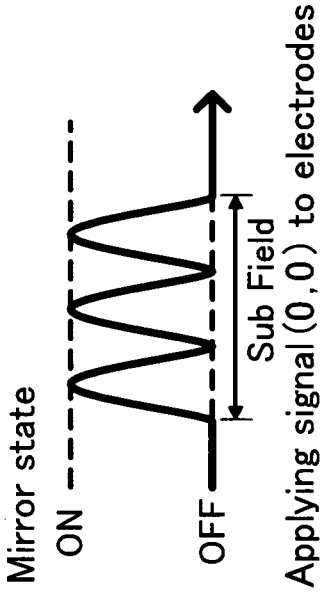

Mirror state
ON
OFF
Sub Field
Applying signal (0, 0) to electrodes

Fig.7F

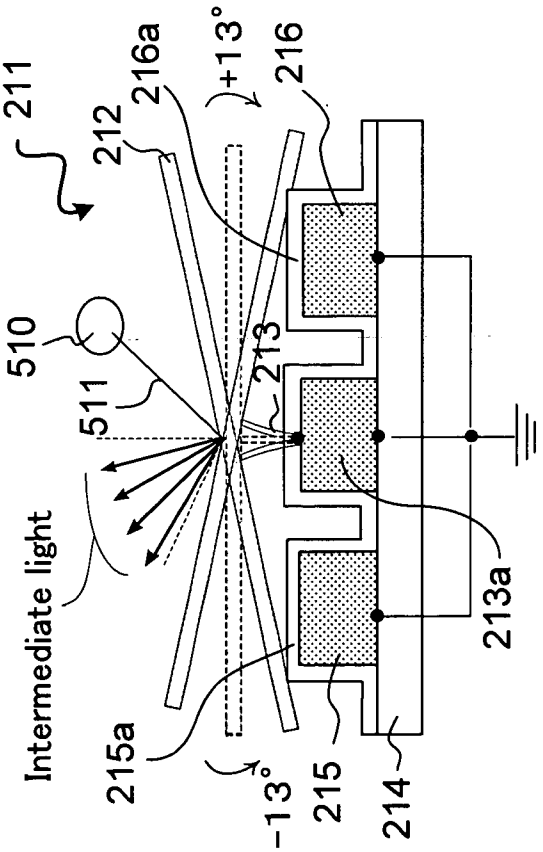

211
212
216a
+13°
216
510
511
213
Intermediate light
215a
-13°
215
214
213a

Fig.7E

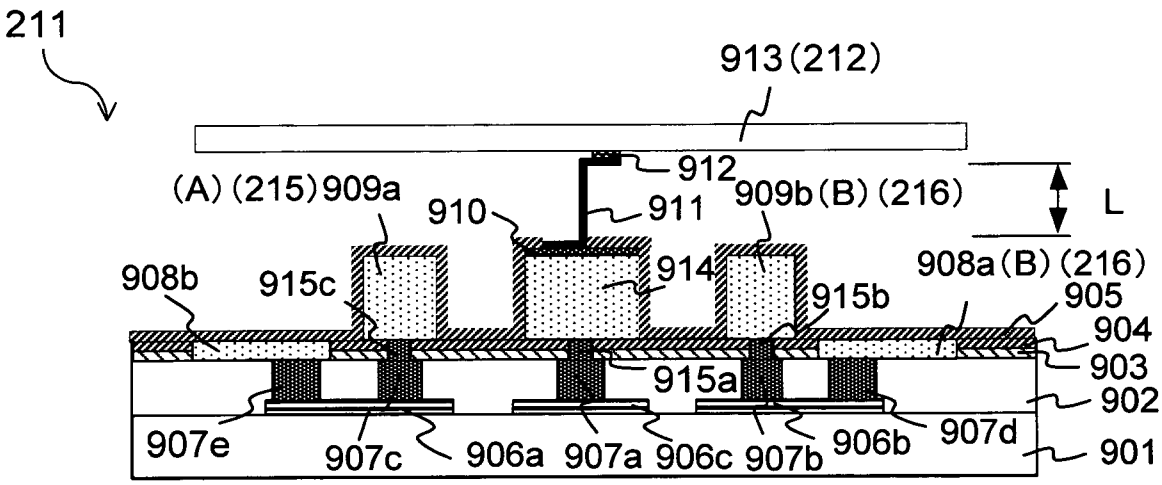

211
913(212)
912
(A)(215)909a
910
911
909b(B)(216)
L
908b
915c
914
915b
908a(B)(216)
905
904
903
915a
902
907e
907c
906a
907a
906c
907b
906b
907d
901

Fig. 8A

Fig. 8B

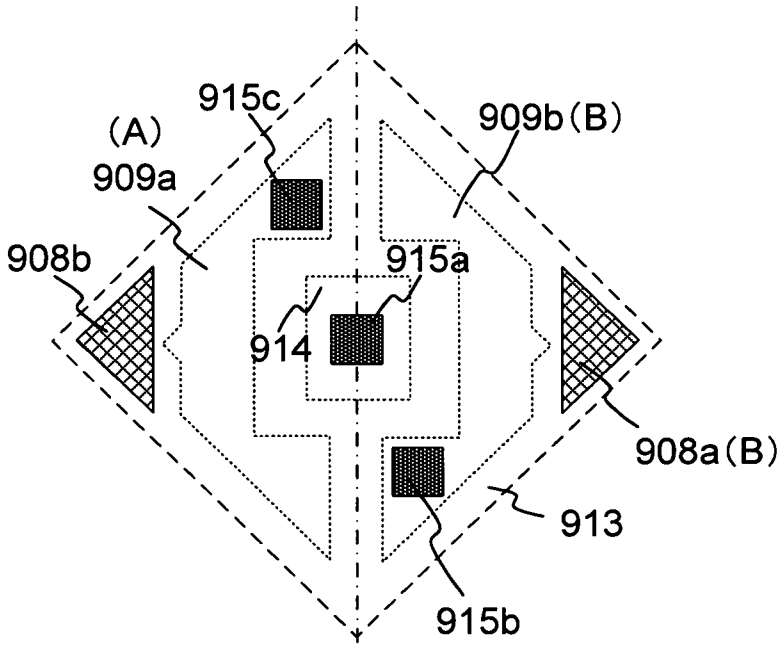
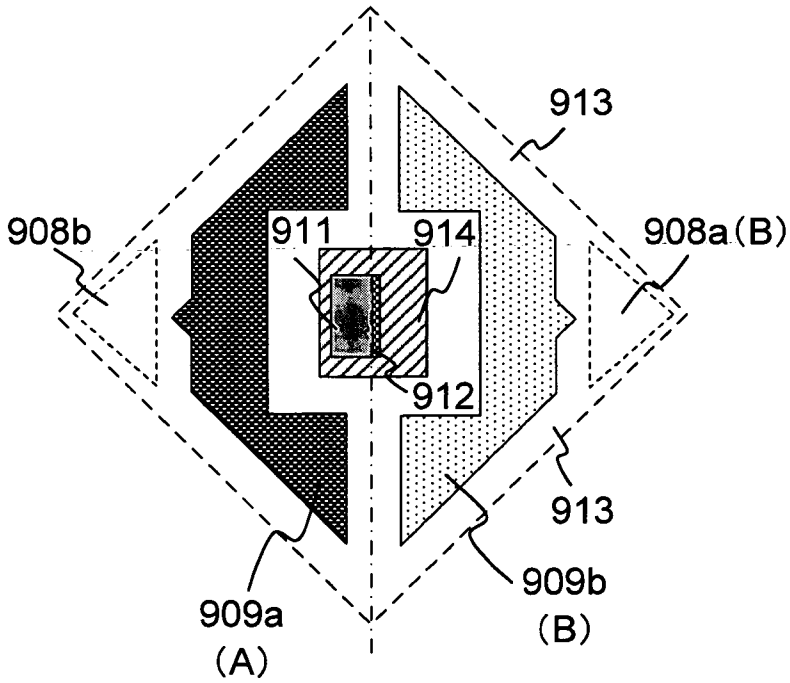

915c
(A)
909a
909b(B)
908b
915a
914
908a(B)
913
915b

Fig. 8C


913
908b
911
914
908a(B)
912
913
909b
(B)
909a
(A)

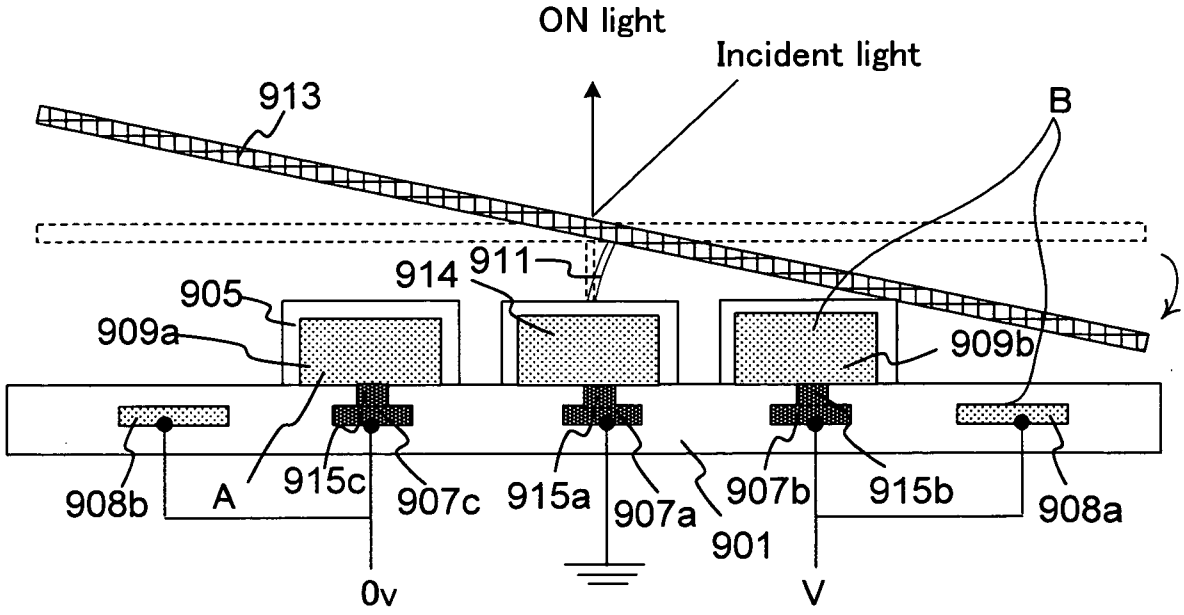

ON light
Incident light
913
B
914
911
905
909a
909b
908b
A
915c
907c
915a
907a
907b
915b
908a
901
0v
V

Fig. 8D

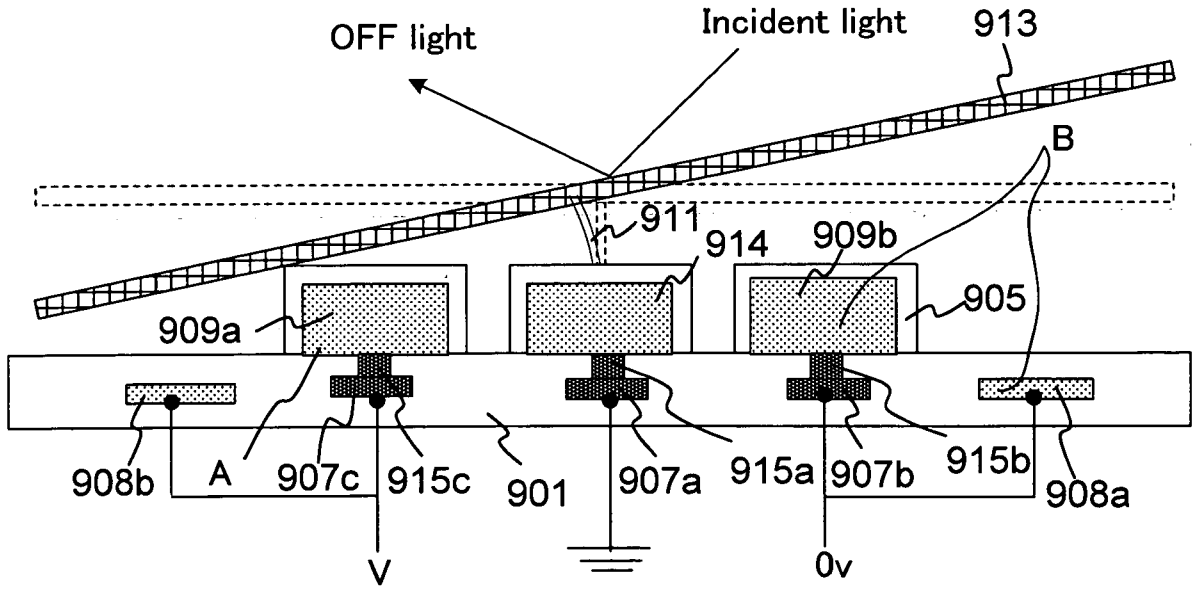

OFF light
Incident light
913
B
911
914
909b
905
909a
908b
A
907c
915c
901
907a
915a
907b
915b
908a
V
0v

Fig. 8E

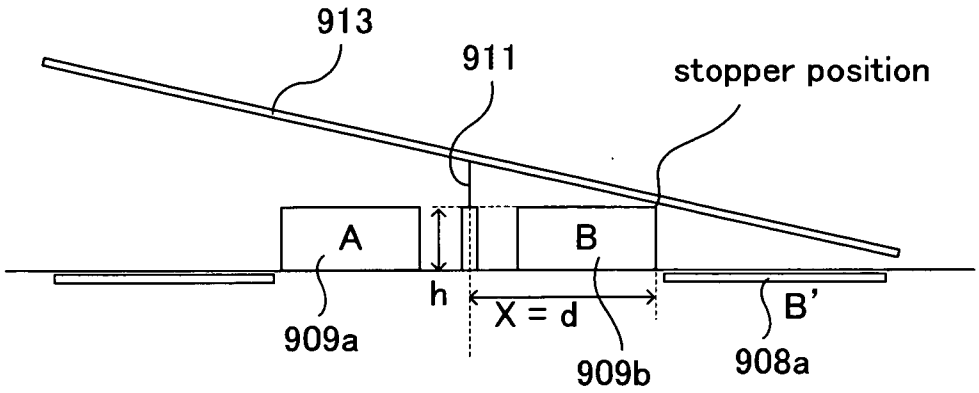

913
911
stopper position
A
B
h
X = d
909a
909b
908a
B'

Fig. 9A

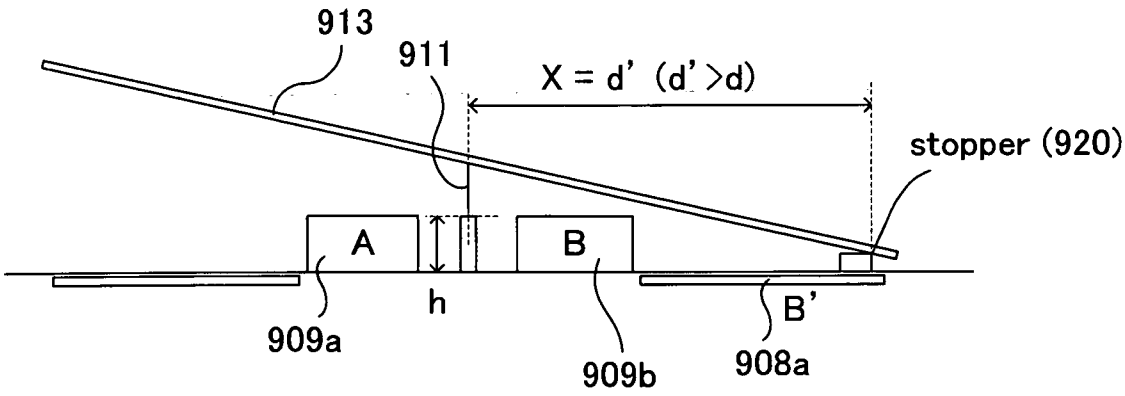

913
911
X = d' (d'>d)
stopper (920)
A
B
h
909a
909b
908a
B'

Fig. 9B

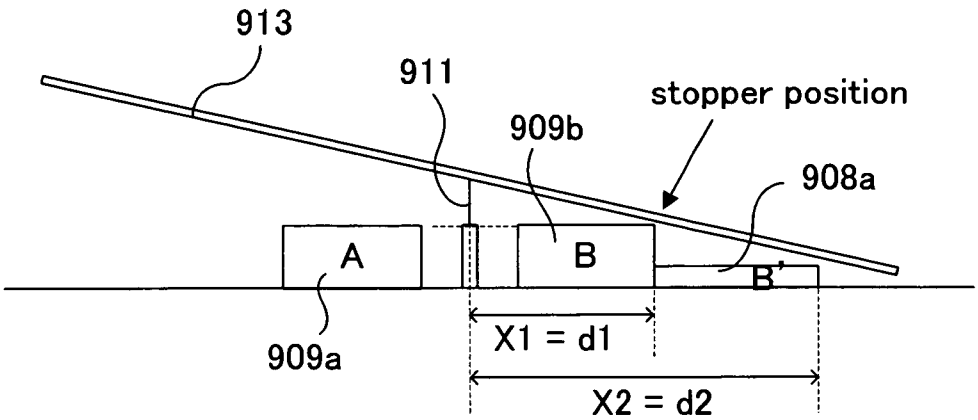

913
911
909b
stopper position
908a
A
B
B'
909a
X1 = d1
X2 = d2

Fig. 9C

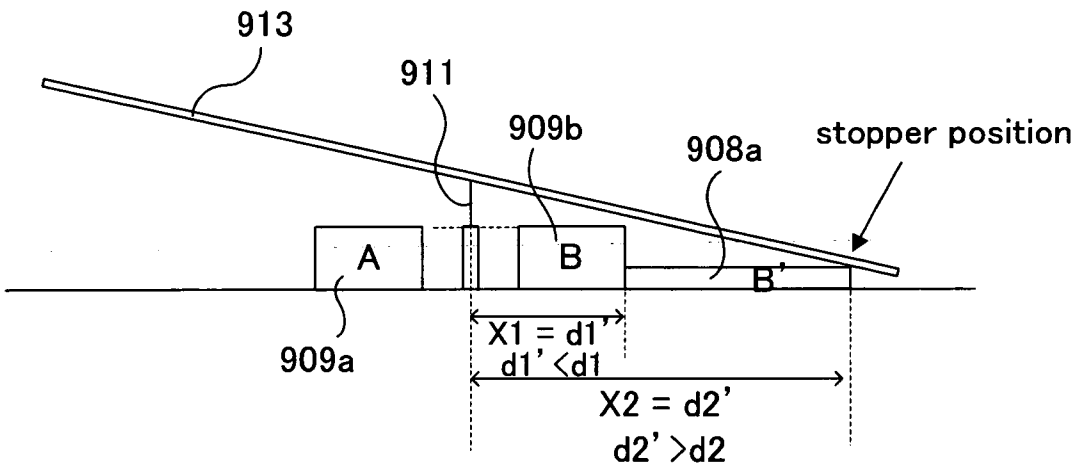

913
911
909b
908a
stopper position
A
B
B'
909a
X1 = d1''
d1' <d1
X2 = d2'
d2' >d2

Fig. 9D

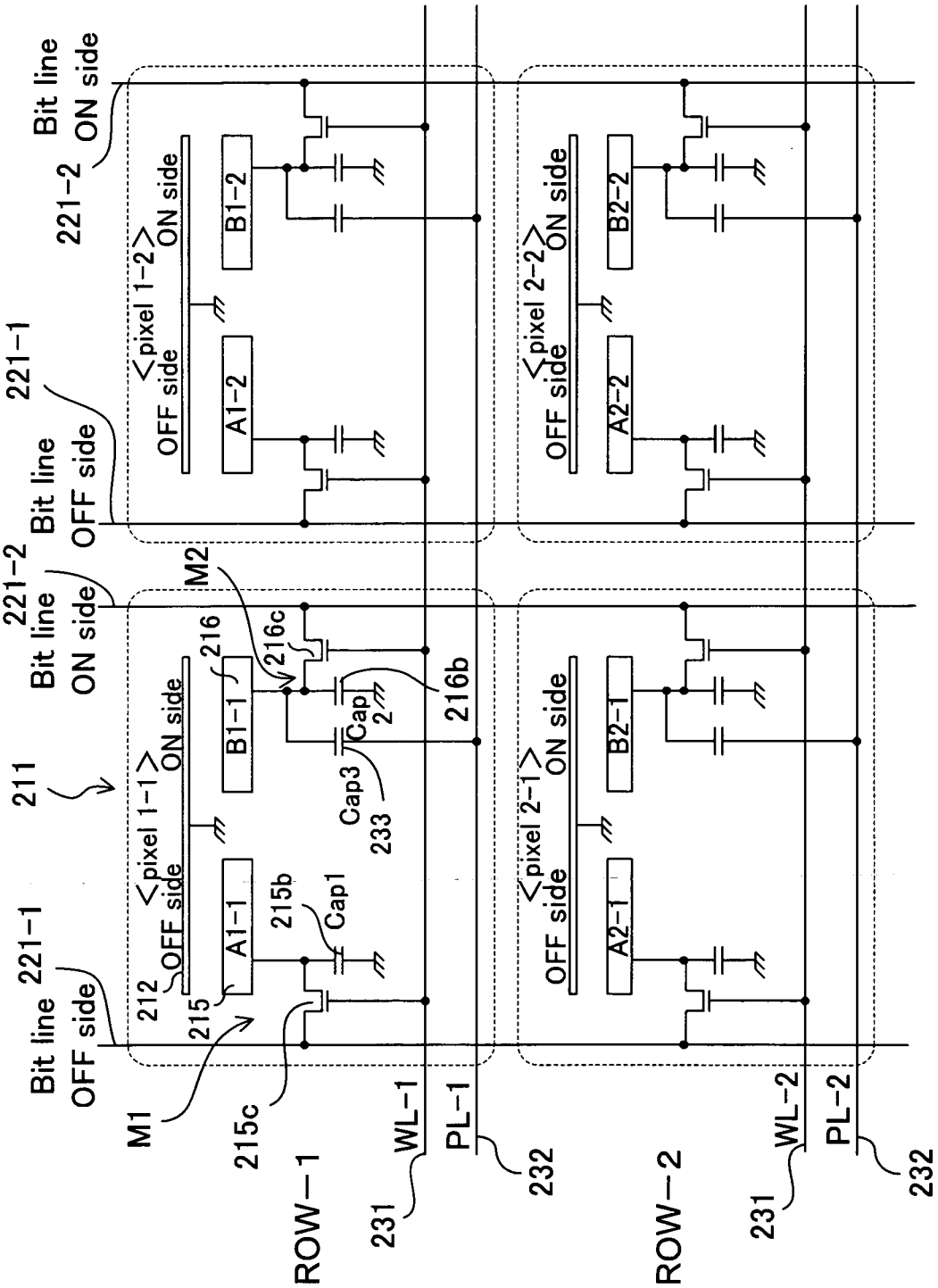

Bit line OFF side
221-1
Bit line ON side
221-2
211
<pixel 1-1>
OFF side
ON side
A1-1
B1-1
<pixel 1-2>
A1-2
B1-2
<pixel 2-1>
A2-1
B2-1
<pixel 2-2>
A2-2
B2-2
212
215
215b
215c
216
216b
216c
M1
M2
Cap1
Cap2
Cap3
233
ROW-1
ROW-2
231
WL-1
WL-2
PL-1
PL-2
232

Fig. 10A

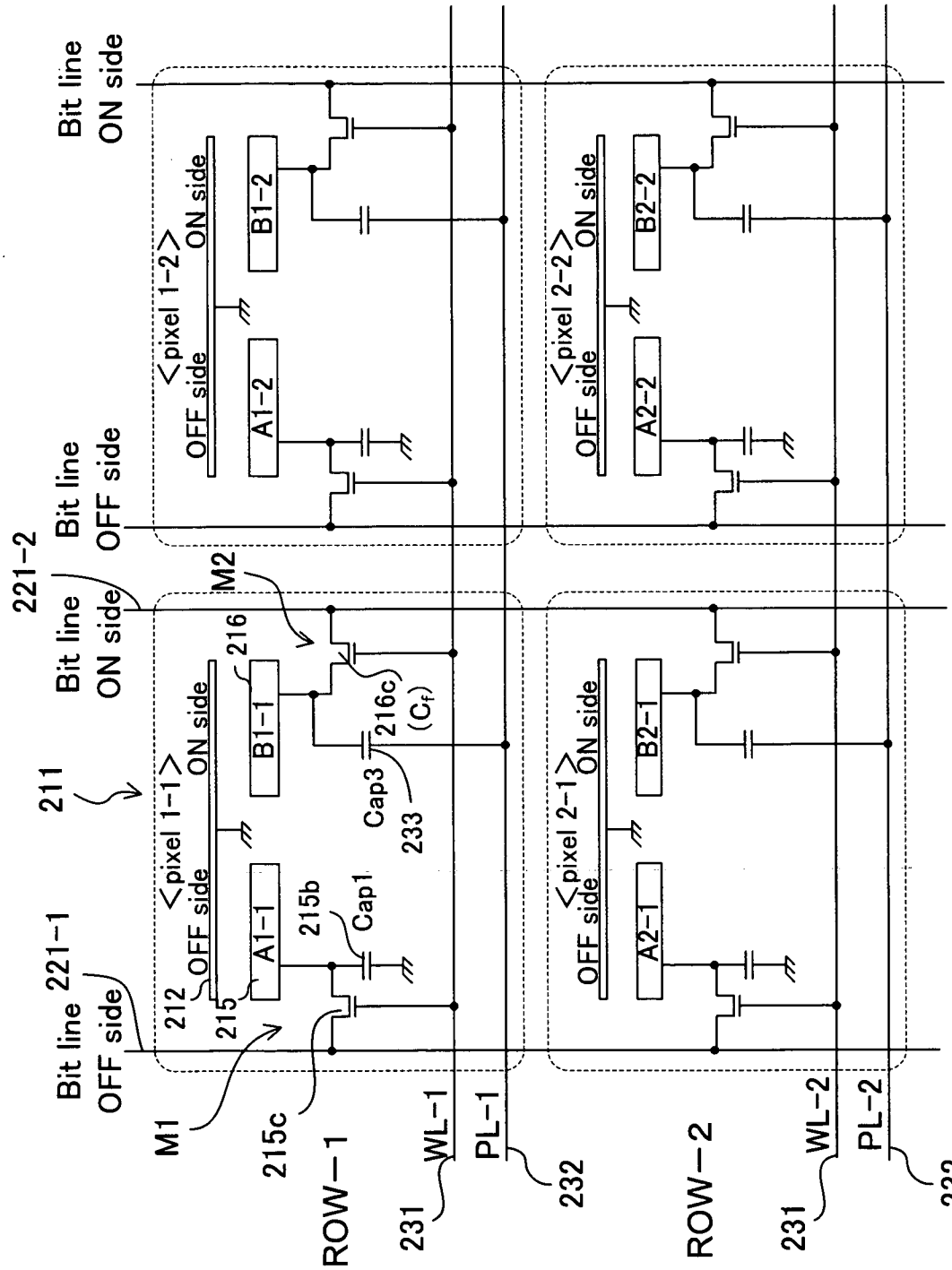

Bit line
OFF side
221-1
Bit line
ON side
221-2
211
<pixel 1-1>
OFF side
ON side
<pixel 1-2>
<pixel 2-1>
<pixel 2-2>
A1-1
A1-2
A2-1
A2-2
B1-1
B1-2
B2-1
B2-2
212
215
215b
215c
216
216c
Cap1
Cap3
233
M1
M2
ROW-1
ROW-2
WL-1
WL-2
PL-1
PL-2
231
232

Fig. 10B

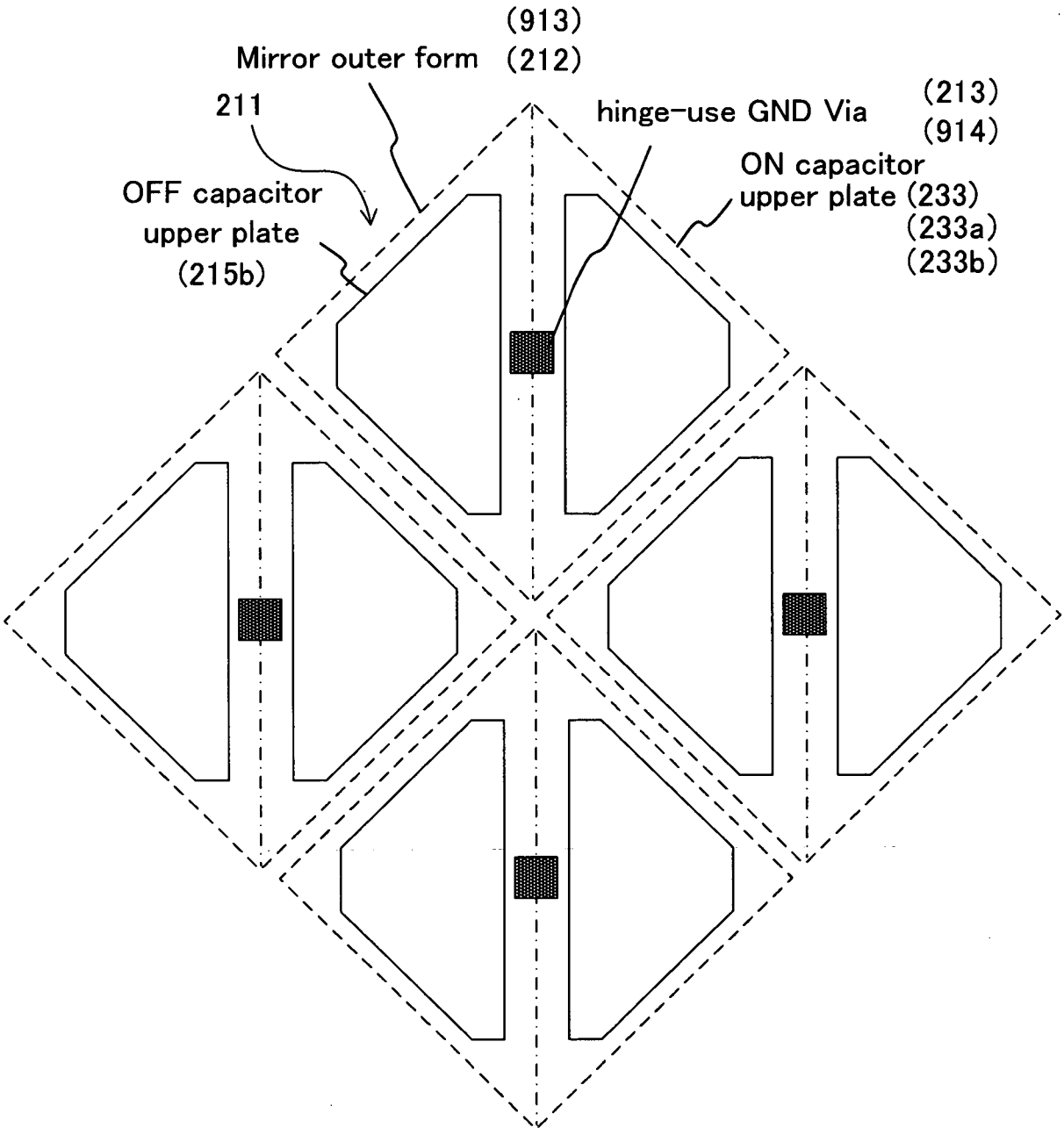

(913)
Mirror outer form (212)
211
hinge-use GND Via
(213)
(914)
ON capacitor
upper plate (233)
(233a)
(233b)
OFF capacitor
upper plate
(215b)

Fig. 10C

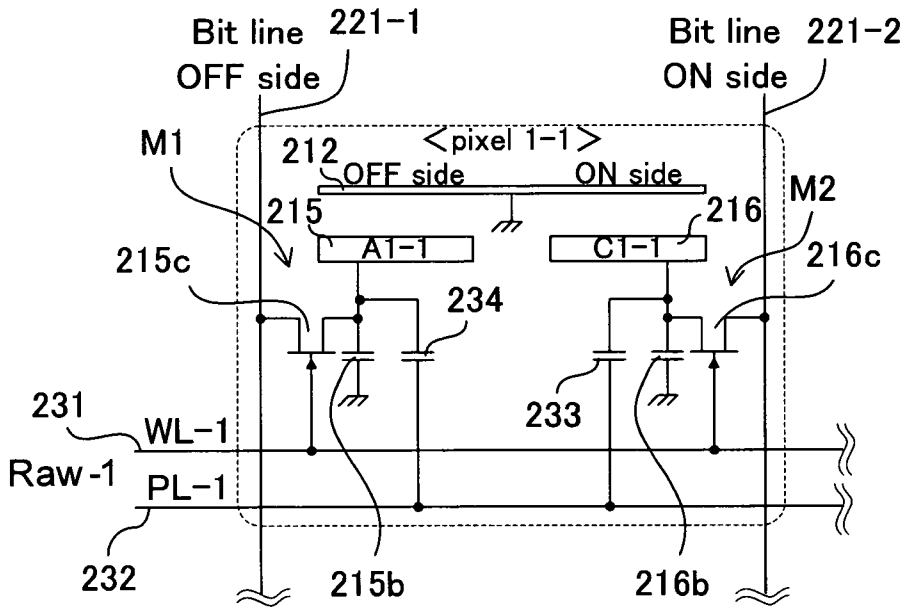

Bit line 221-1
OFF side
Bit line 221-2
ON side
M1
212
<pixel 1-1>
OFF side
ON side
M2
215
216
A1-1
C1-1
215c
216c
234
231
WL-1
233
Raw-1
PL-1
232
215b
216b

Fig. 10D

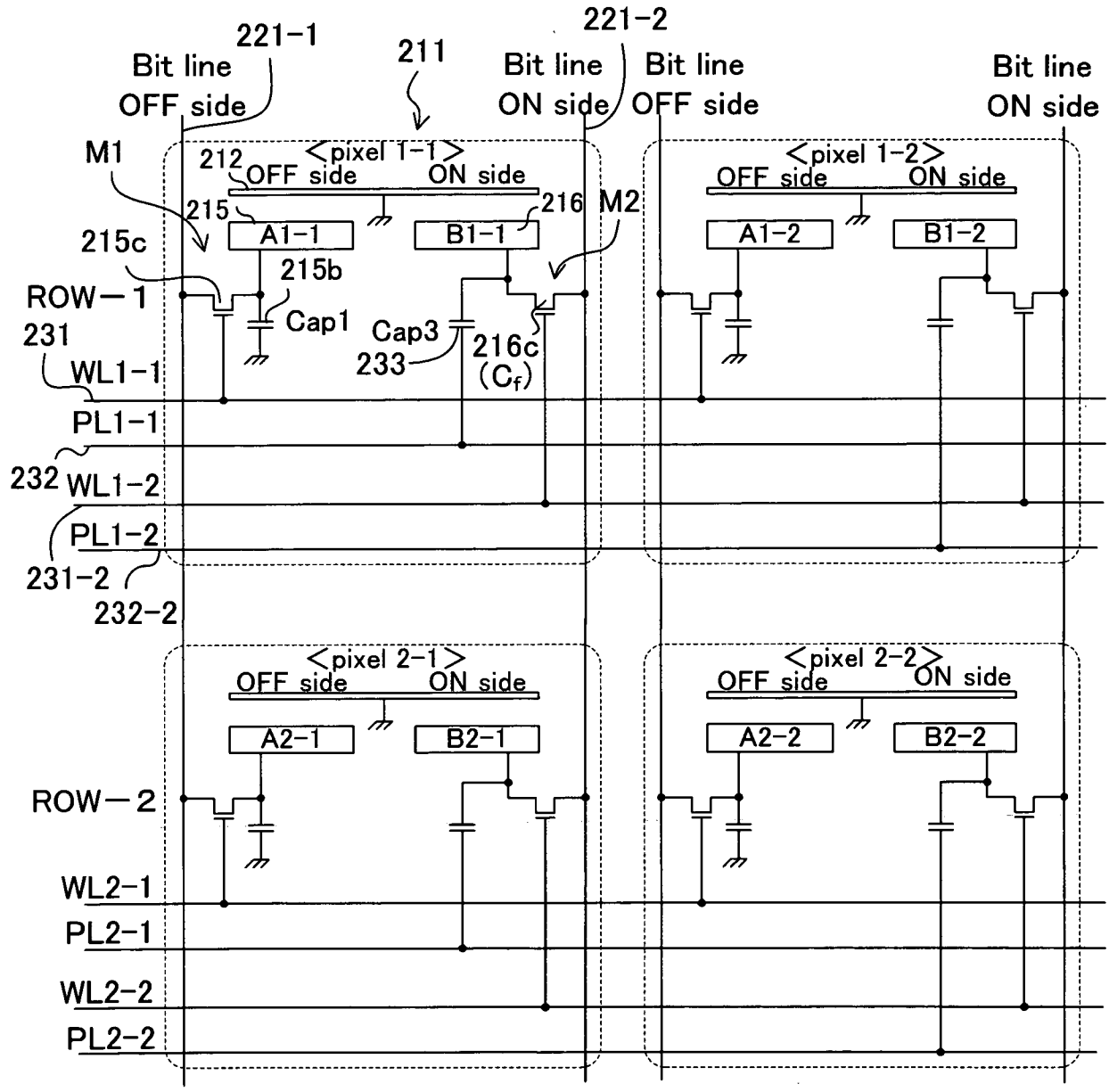


Fig. 10E **Mirror Cell structure**

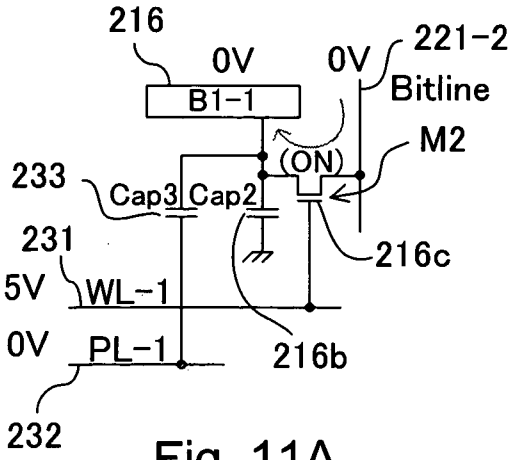


Fig. 11A

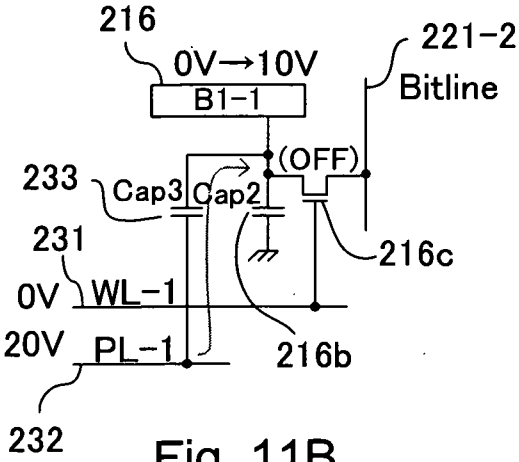


Fig. 11B

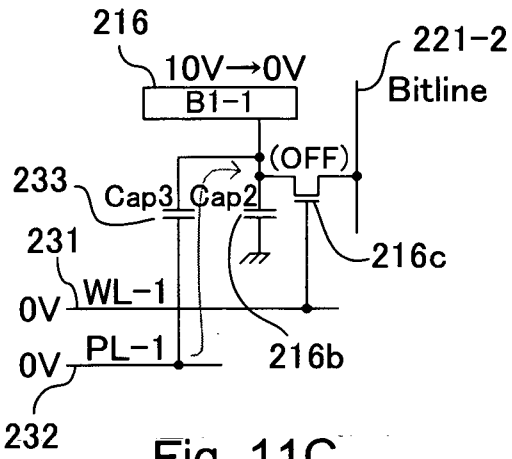


Fig. 11C

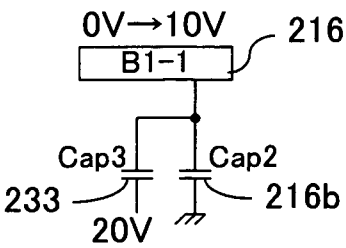


Fig. 11D

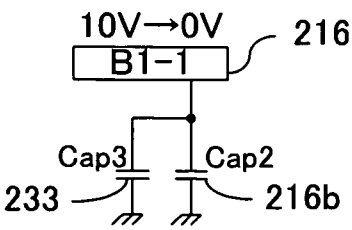


Fig. 11E

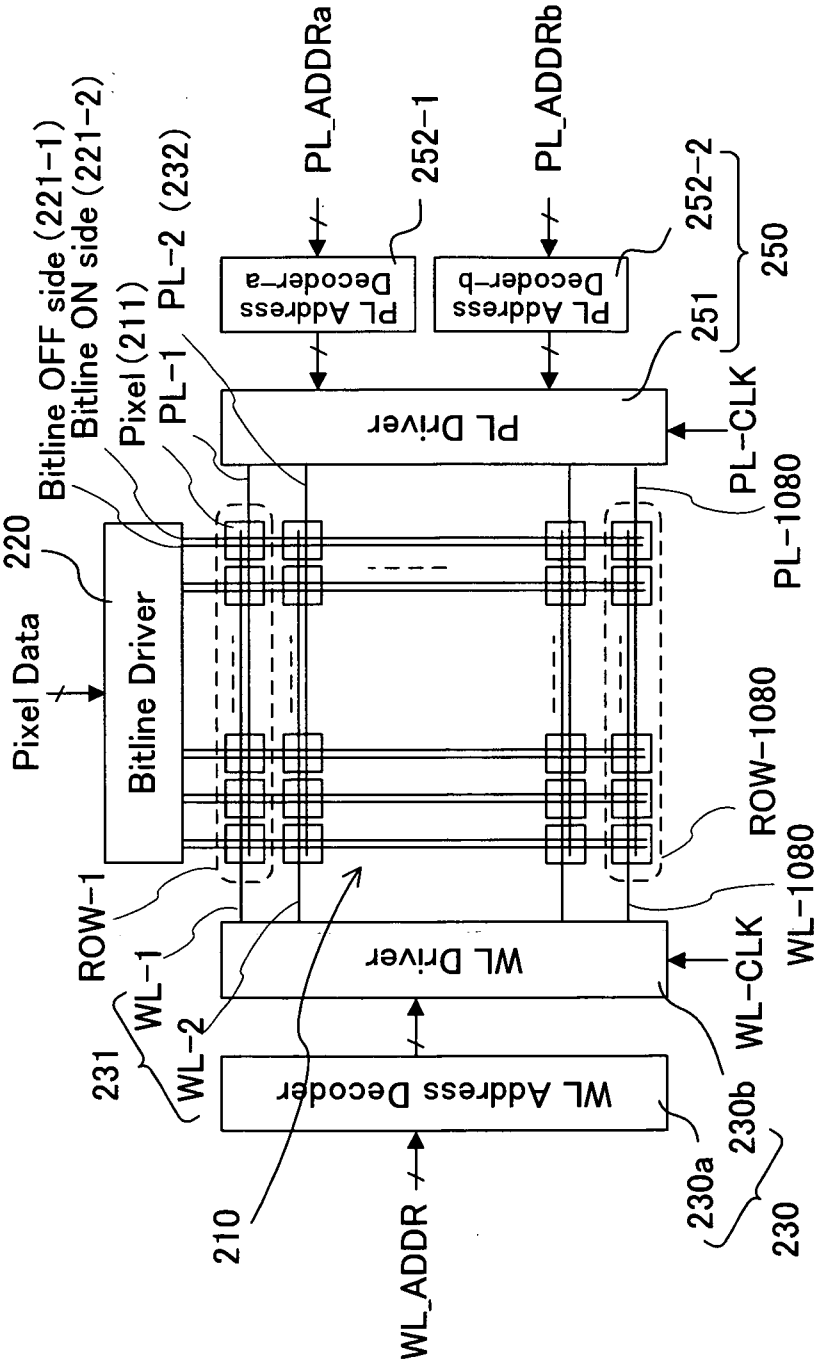

PL_ADDRa
PL_ADDRb
252-1
252-2
250
PL Address Decoder-a
PL Address Decoder-b
251
PL Driver
PL-CLK
PL-1080
Bitline OFF side (221-1)
Bitline ON side (221-2)
Pixel (211)
PL-1
PL-2 (232)
220
Pixel Data
Bitline Driver
ROW-1
ROW-1080
WL-1
WL-2
WL-1080
WL Driver
WL-CLK
231
WL Address Decoder
230b
230a
230
210
WL_ADDR

Fig. 12A

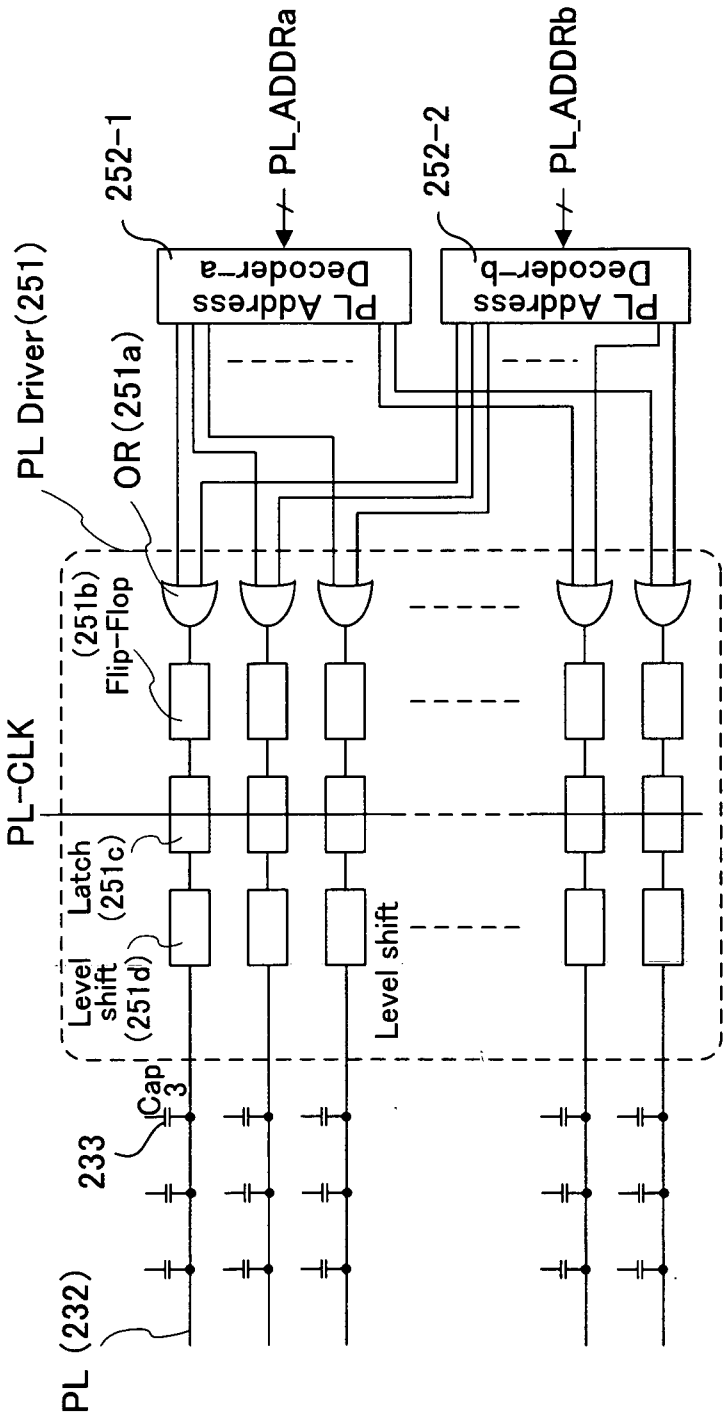

PL_ADDRa
PL_ADDRb
252-1
252-2
PL Address Decoder-a
PL Address Decoder-b
PL Driver(251)
OR (251a)
(251b) Flip-Flop
PL-CLK
Latch (251c)
Level shift (251d)
Level shift
Cap 3
233
PL (232)

Fig. 12B

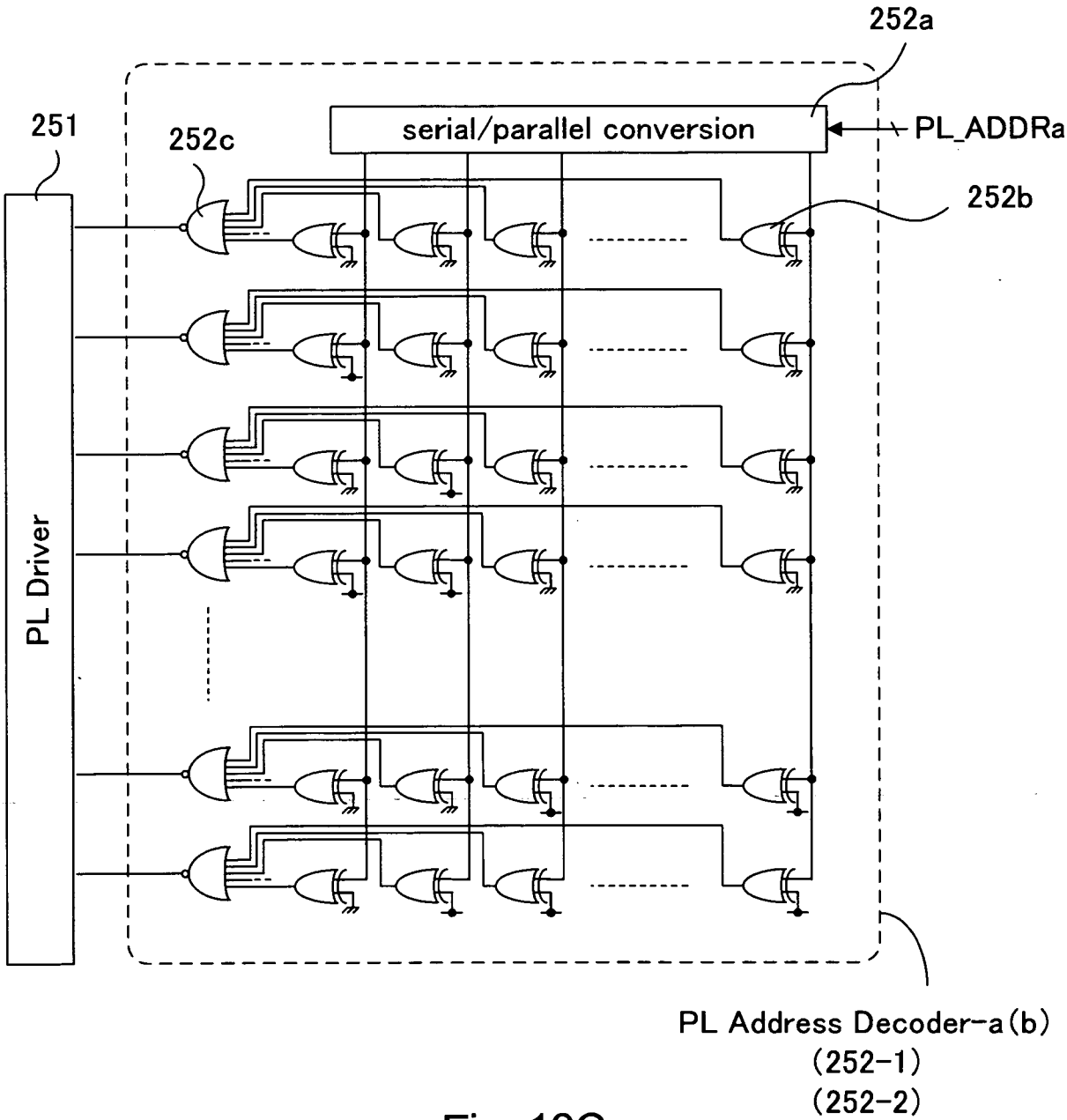

252a
251
252c
serial/parallel conversion
PL_ADDRa
252b
PL Driver
PL Address Decoder-a(b)
(252-1)
(252-2)

Fig. 12C

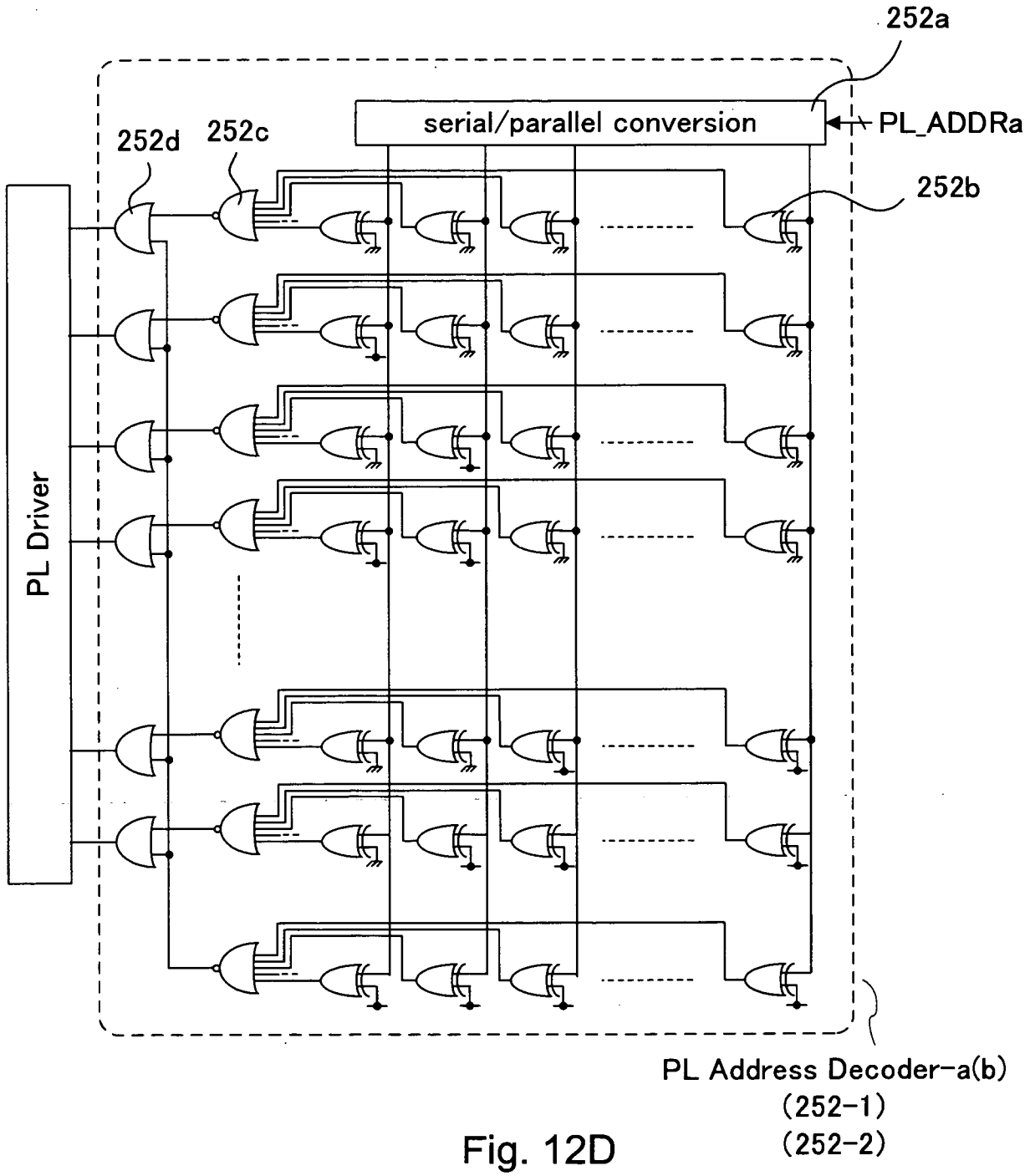

252a
serial/parallel conversion
PL_ADDRa
252d
252c
252b
PL Driver
PL Address Decoder-a(b)
(252-1)
(252-2)

Fig. 12D

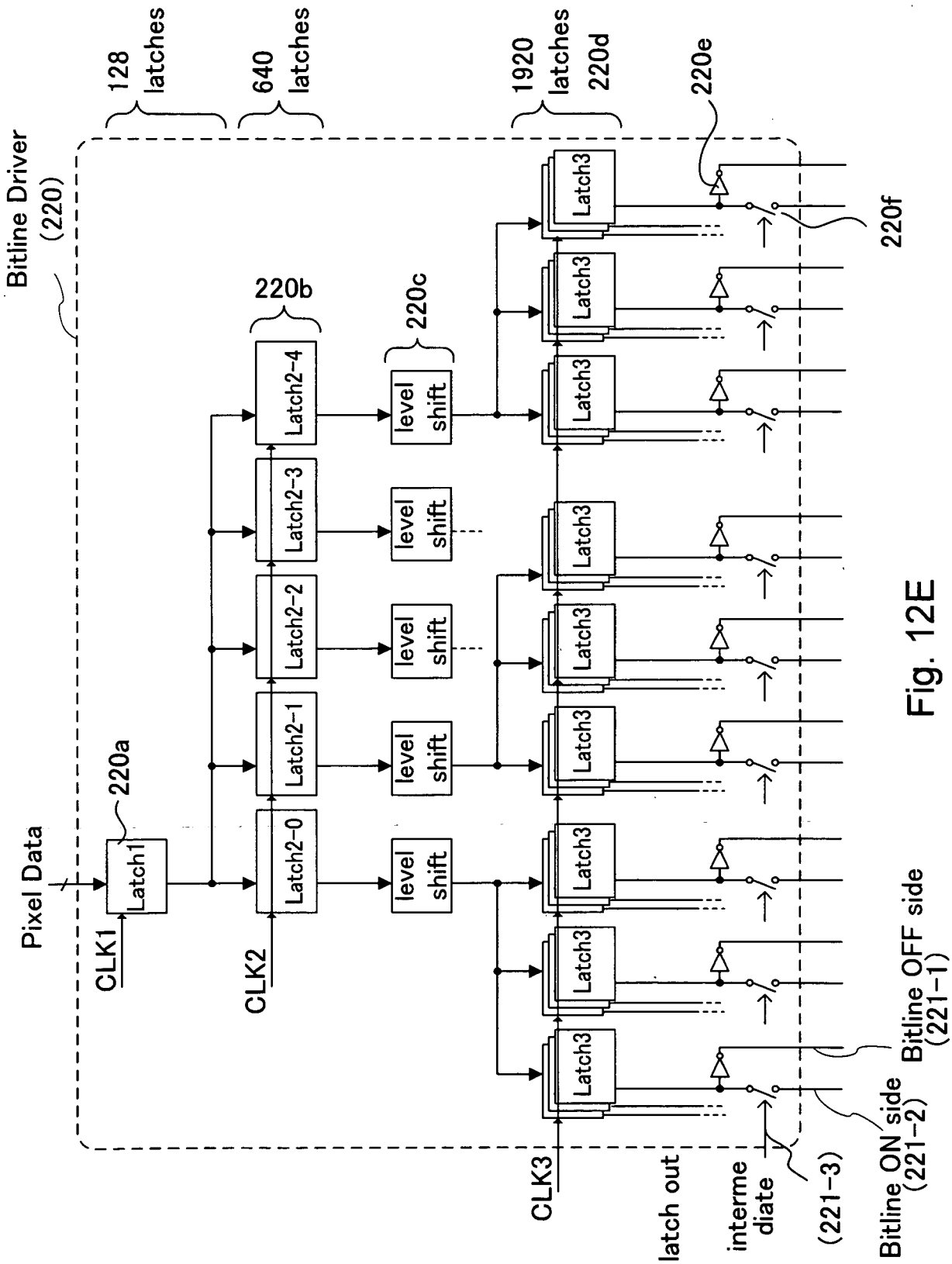

Bitline Driver
(220)
128
latches
640
latches
1920
latches
220d
220e
220f
220b
220c
220a
Pixel Data
CLK1
CLK2
CLK3
Latch1
Latch2-0
Latch2-1
Latch2-2
Latch2-3
Latch2-4
level
shift
Latch3
latch out
interme
diate
(221-3)
Bitline ON side
(221-2)
Bitline OFF side
(221-1)

Fig. 12E

Intermediate	latch out	Bitline OFF side	Bitline ON side
1 (SW ON)	1	0	1
1 (SW ON)	0	1	0
0 (SW OFF)	1	0	0
0 (SW OFF)	0	1	0
221-3	220d	221-1	221-2

Fig. 12F

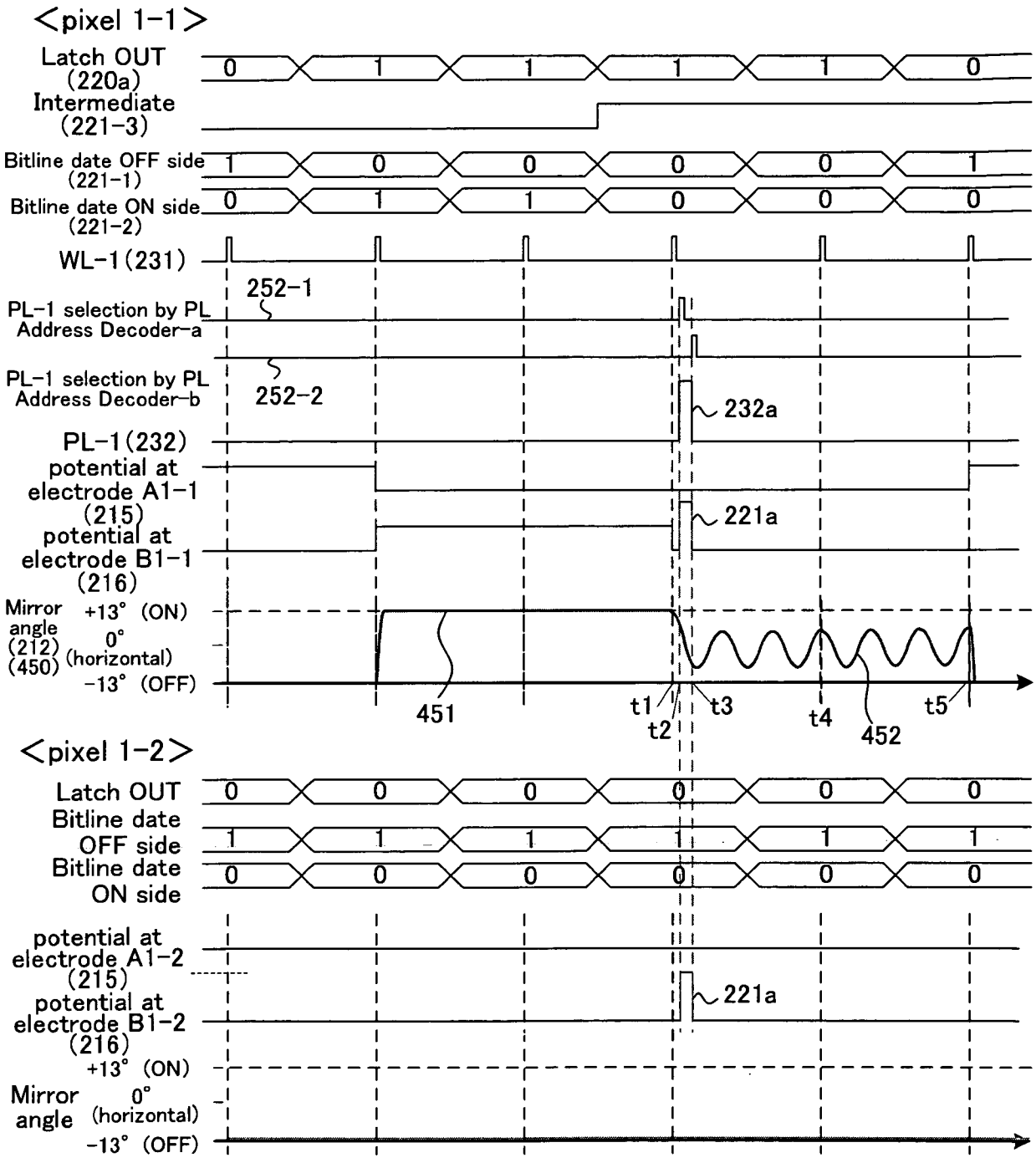

<pixel 1-1>
Latch OUT (220a)
Intermediate (221-3)
Bitline date OFF side (221-1)
Bitline date ON side (221-2)
WL-1(231)
252-1
PL-1 selection by PL Address Decoder-a
PL-1 selection by PL Address Decoder-b
252-2
232a
PL-1(232)
potential at electrode A1-1 (215)
221a
potential at electrode B1-1 (216)
Mirror angle (212) (450)
+13° (ON)
0° (horizontal)
-13° (OFF)
451
t1
t2
t3
t4
452
t5
<pixel 1-2>
Latch OUT
Bitline date OFF side
Bitline date ON side
potential at electrode A1-2 (215)
221a
potential at electrode B1-2 (216)
+13° (ON)
Mirror angle
0° (horizontal)
-13° (OFF)

Fig. 13

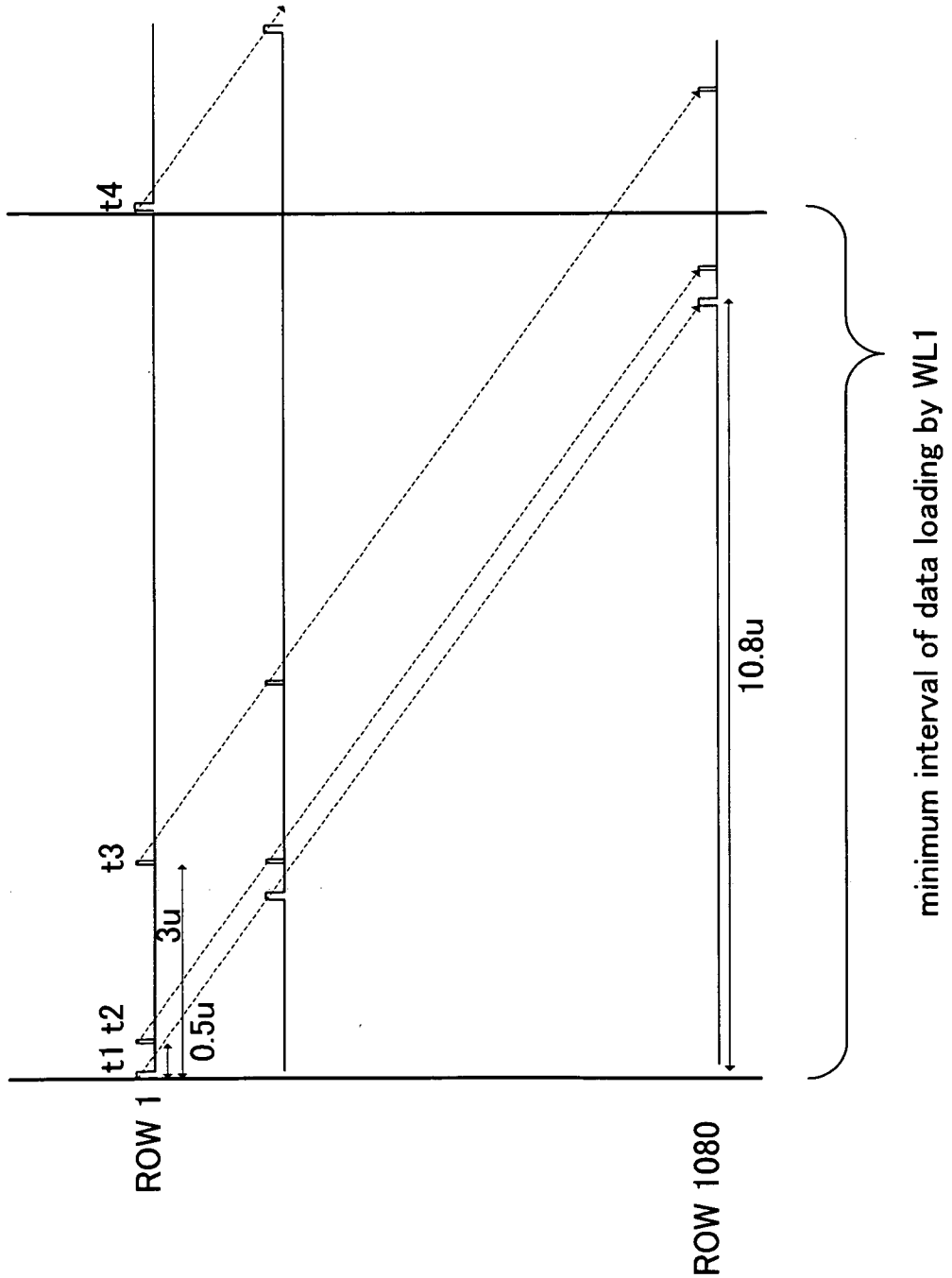

t4
t3
3u
t1 t2
0.5u
ROW 1
ROW 1080
10.8u
minimum interval of data loading by WL1

Fig. 14

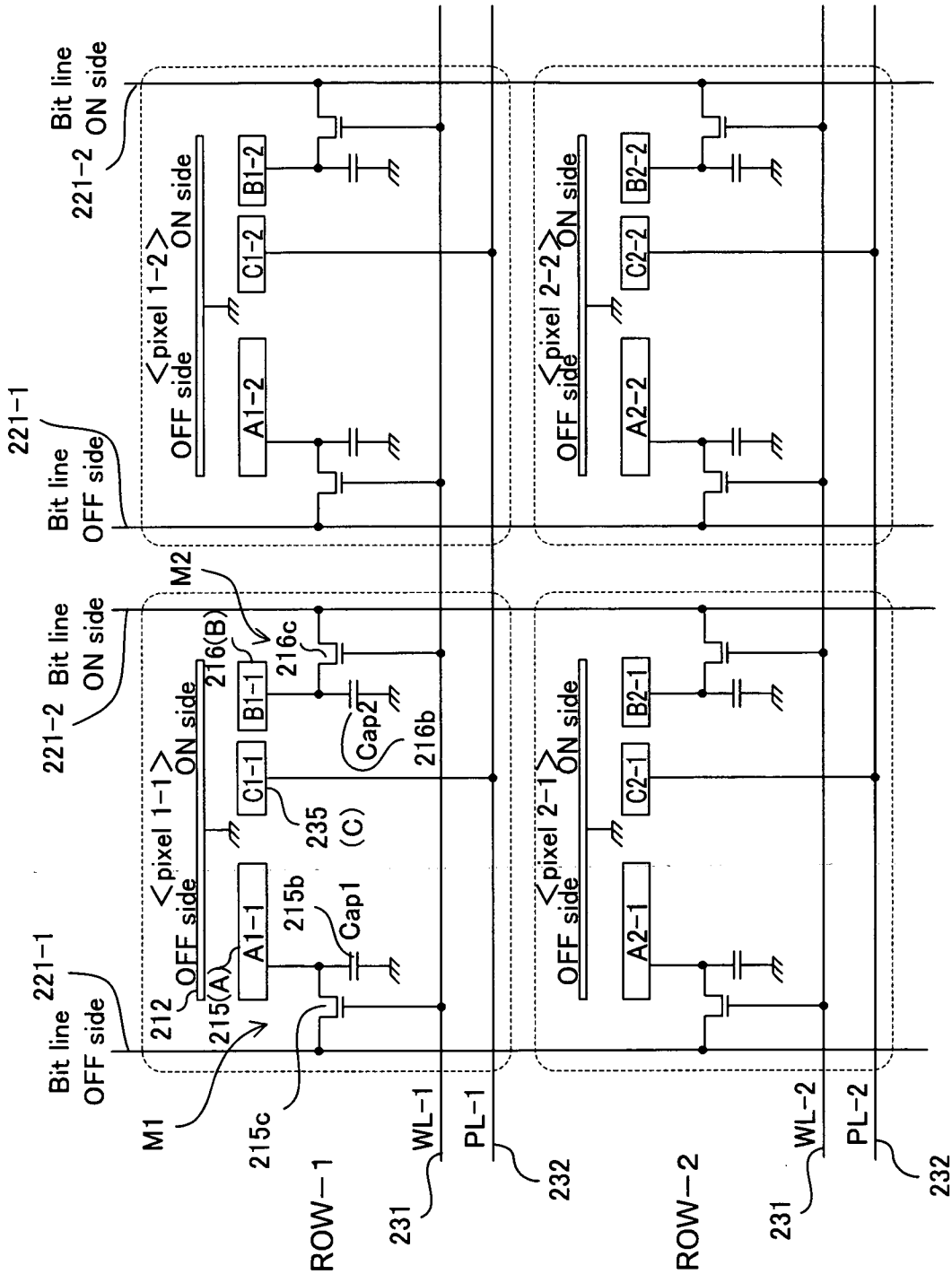

Bit line OFF side
221-1
Bit line ON side
221-2
M1
M2
212
215(A)
215c
215b
216(B)
216c
216b
235 (C)
Cap1
Cap2
A1-1
B1-1
C1-1
A1-2
B1-2
C1-2
A2-1
B2-1
C2-1
A2-2
B2-2
C2-2
<pixel 1-1> OFF side ON side
<pixel 1-2> OFF side ON side
<pixel 2-1> OFF side ON side
<pixel 2-2> OFF side ON side
ROW-1
ROW-2
231
WL-1
WL-2
232
PL-1
PL-2

Fig. 15

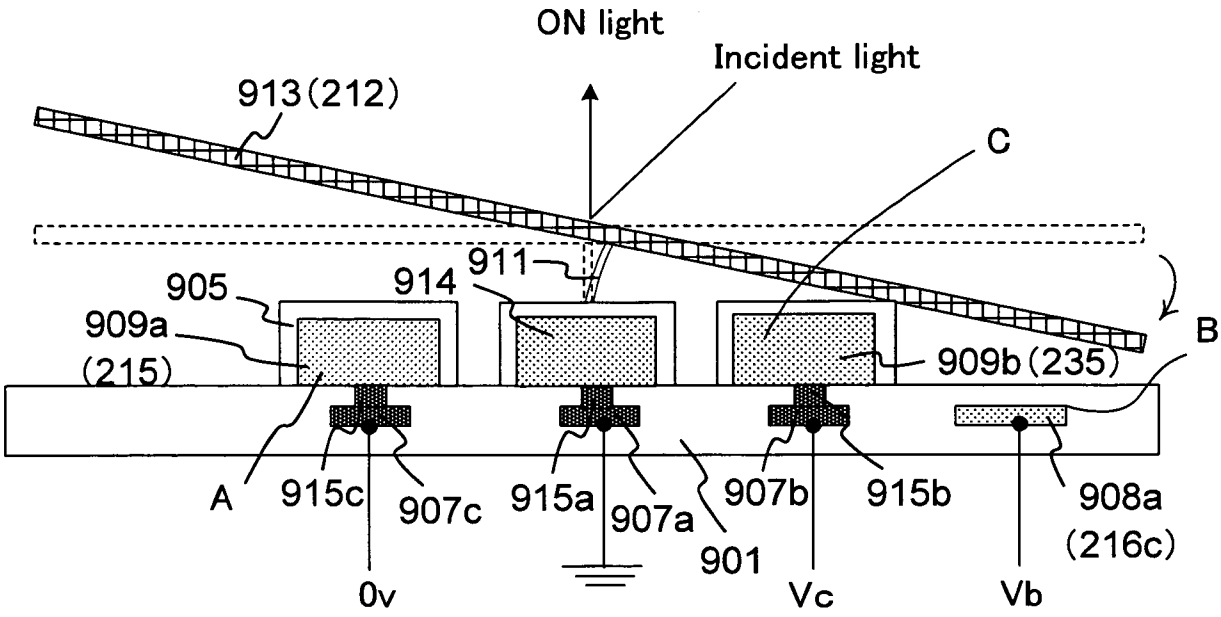


Fig. 15A

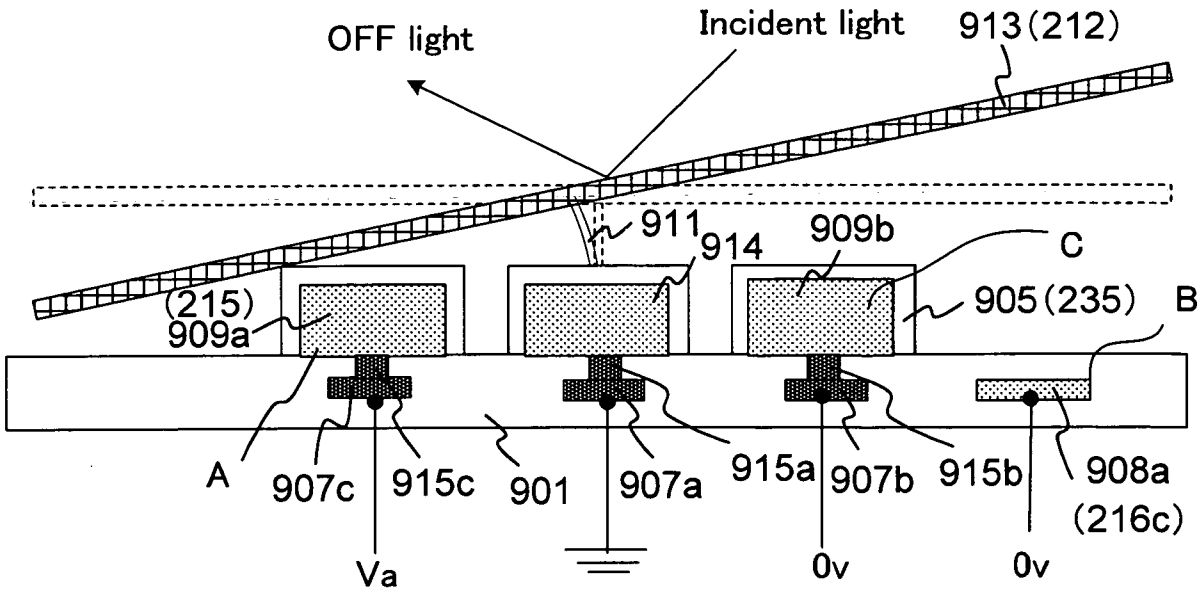


Fig. 15B

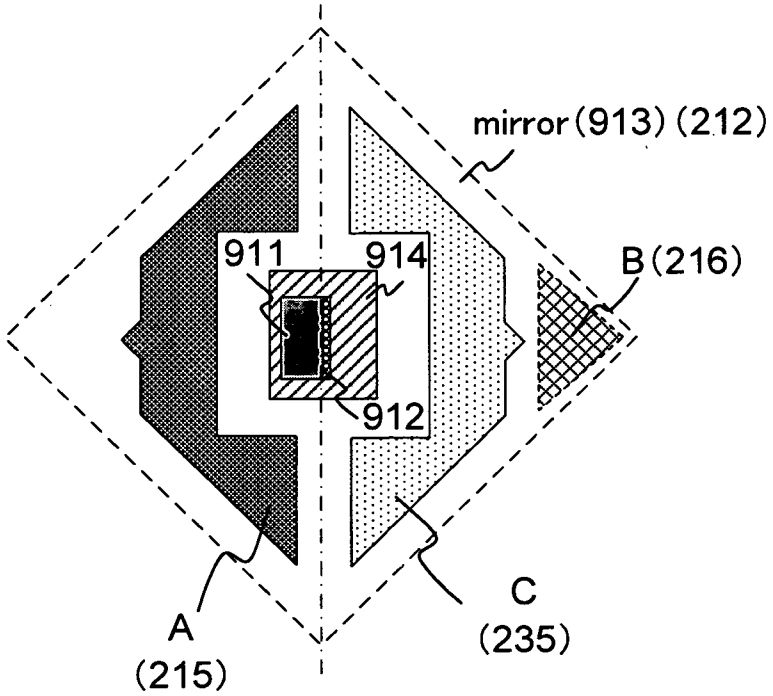


Fig. 15C

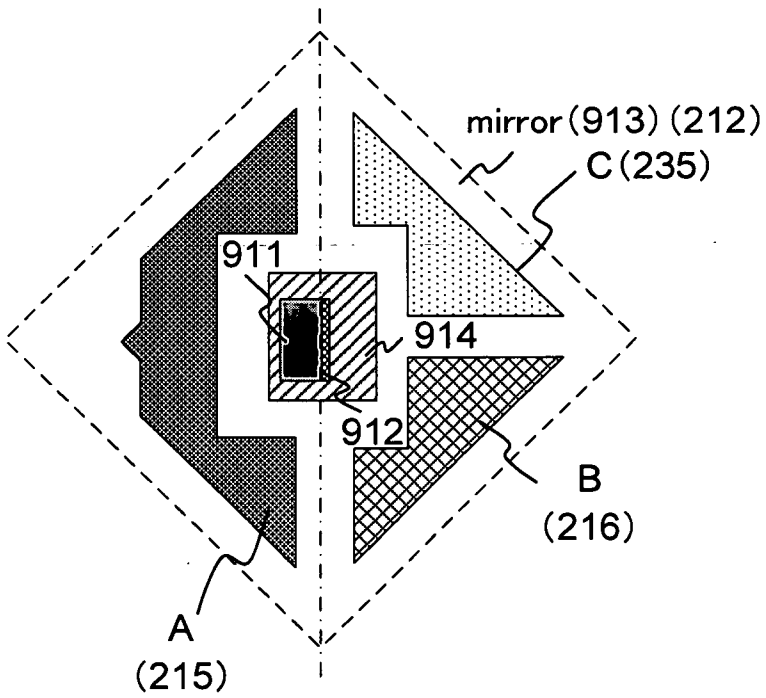


Fig. 15D

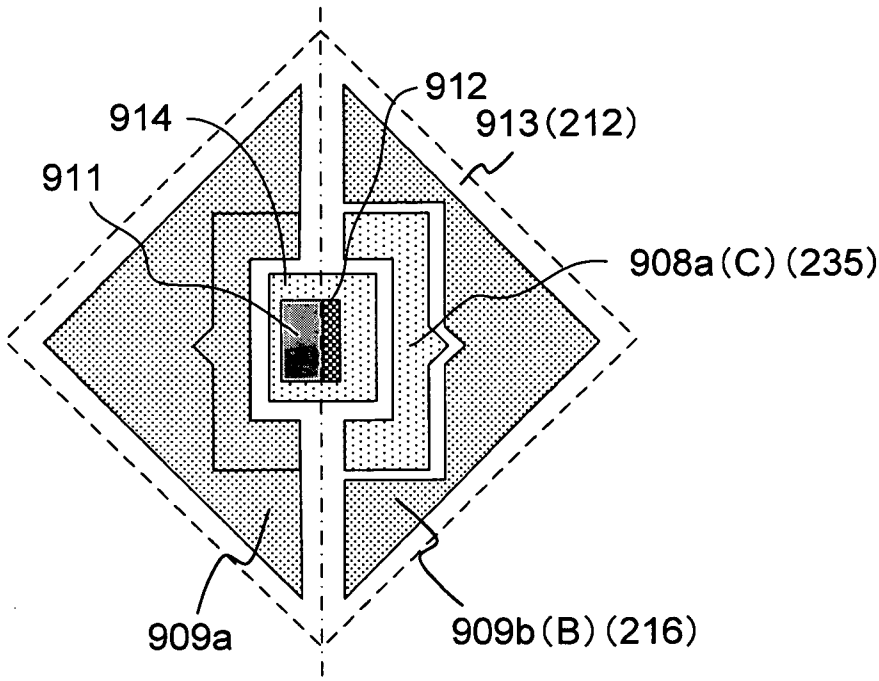


Fig. 15E

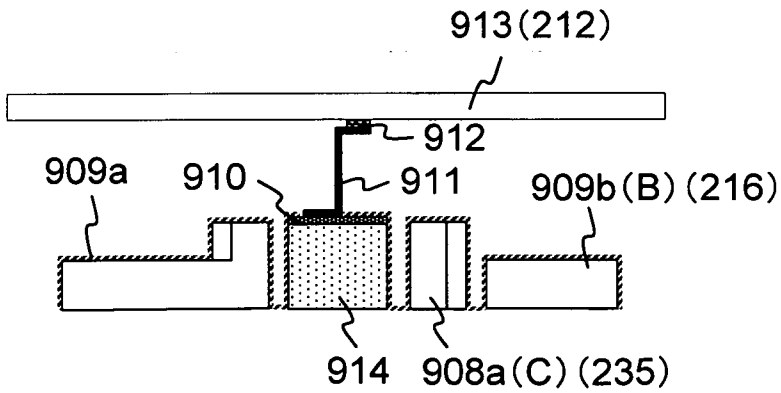


Fig. 15F

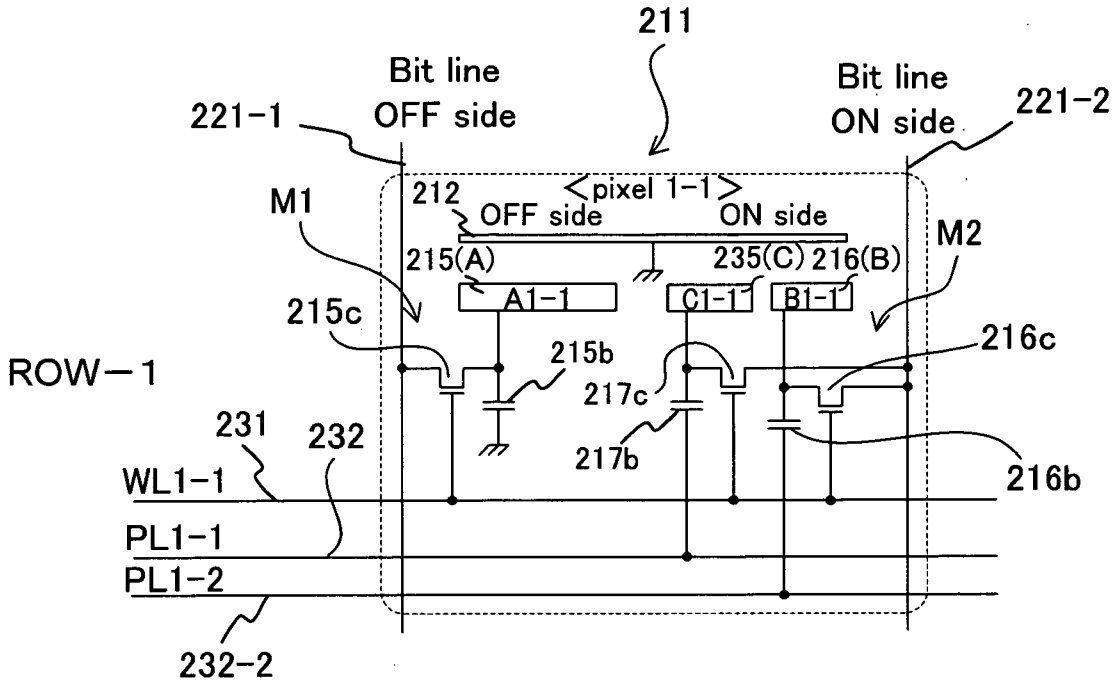


Fig. 15G

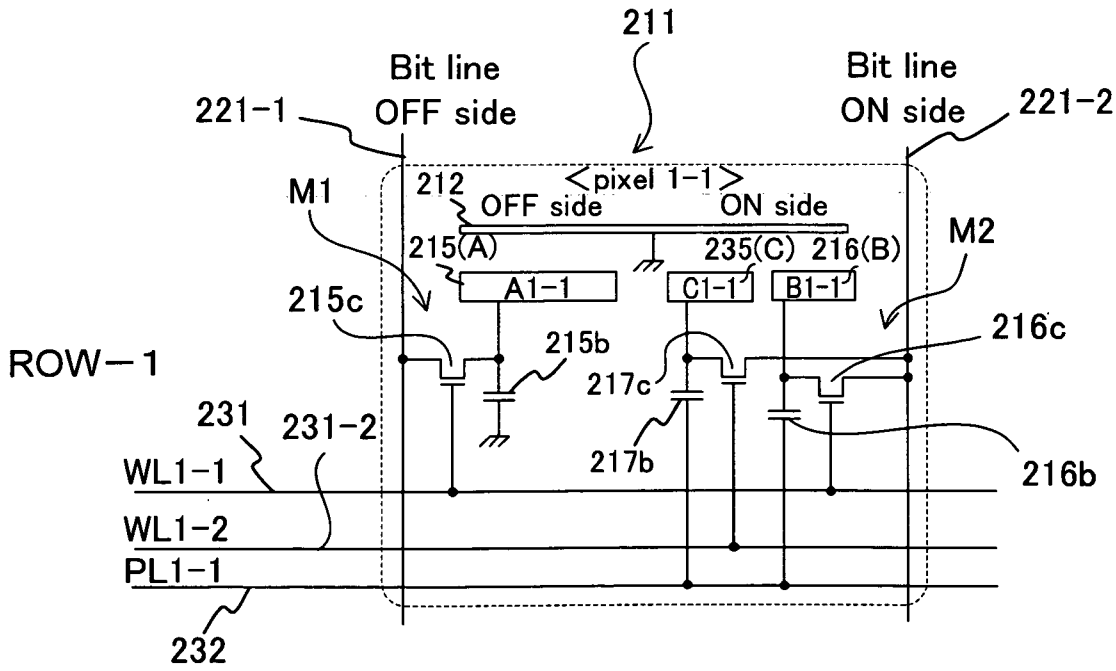


Fig. 15H

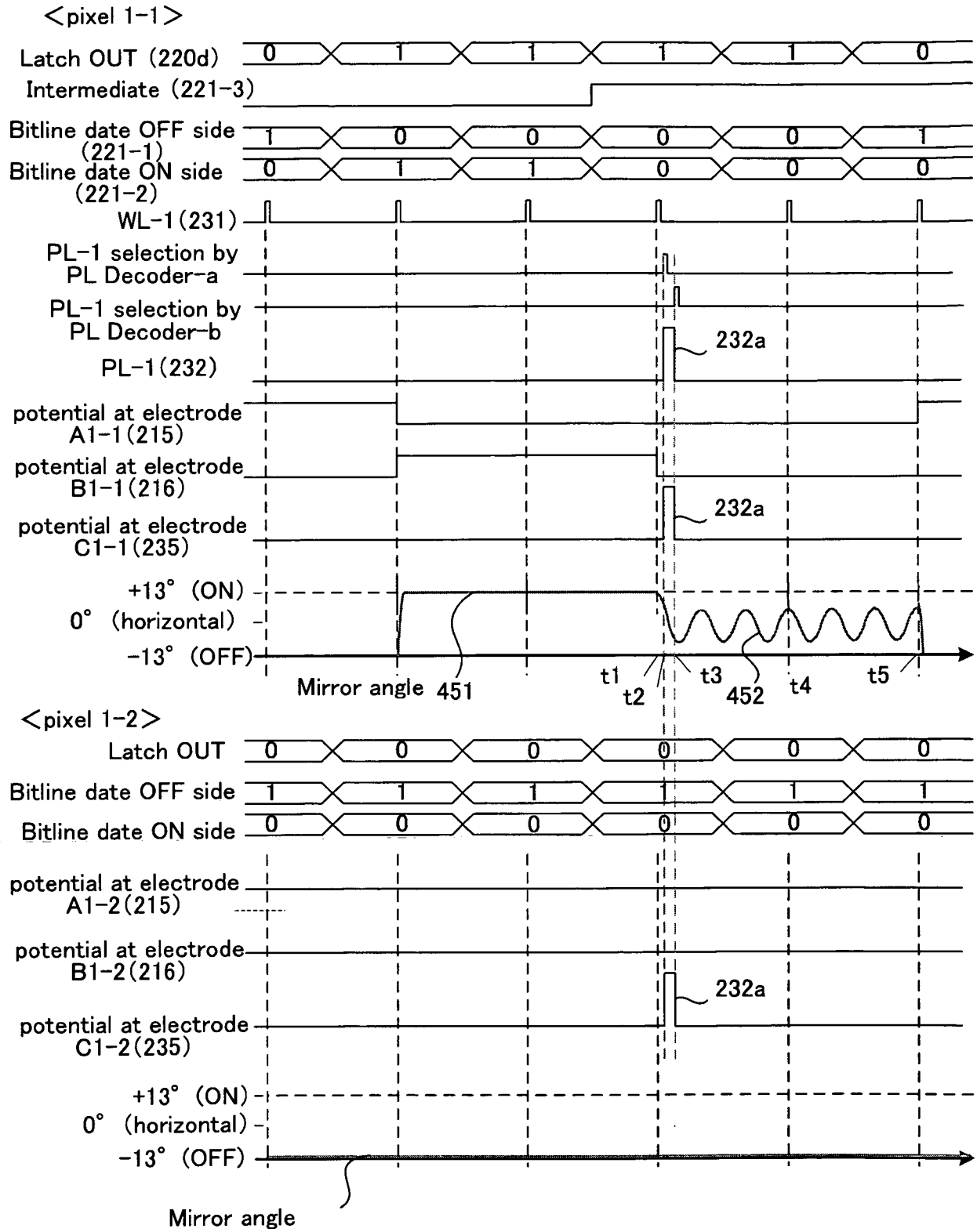

<pixel 1-1>
Latch OUT (220d)
Intermediate (221-3)
Bitline date OFF side (221-1)
Bitline date ON side (221-2)
WL-1(231)
PL-1 selection by PL Decoder-a
PL-1 selection by PL Decoder-b
PL-1(232)
232a
potential at electrode A1-1(215)
potential at electrode B1-1(216)
232a
potential at electrode C1-1(235)
+13° (ON)
0° (horizontal)
-13° (OFF)
Mirror angle
451
t1
t2
t3
452
t4
t5
<pixel 1-2>
Latch OUT
Bitline date OFF side
Bitline date ON side
potential at electrode A1-2(215)
potential at electrode B1-2(216)
232a
potential at electrode C1-2(235)
+13° (ON)
0° (horizontal)
-13° (OFF)
Mirror angle

Fig. 16

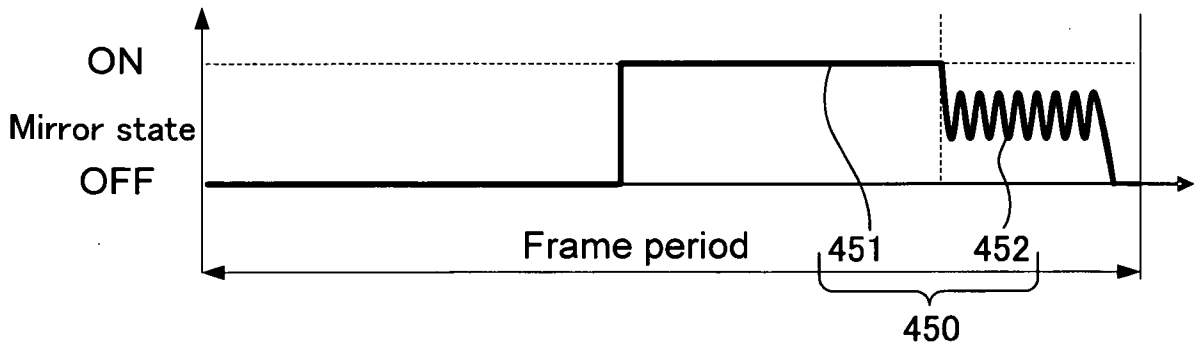


Fig. 17A

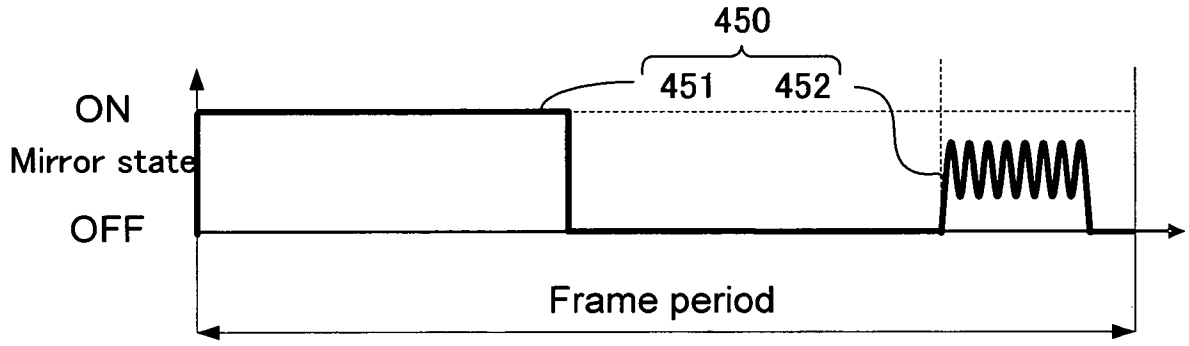


Fig. 17B

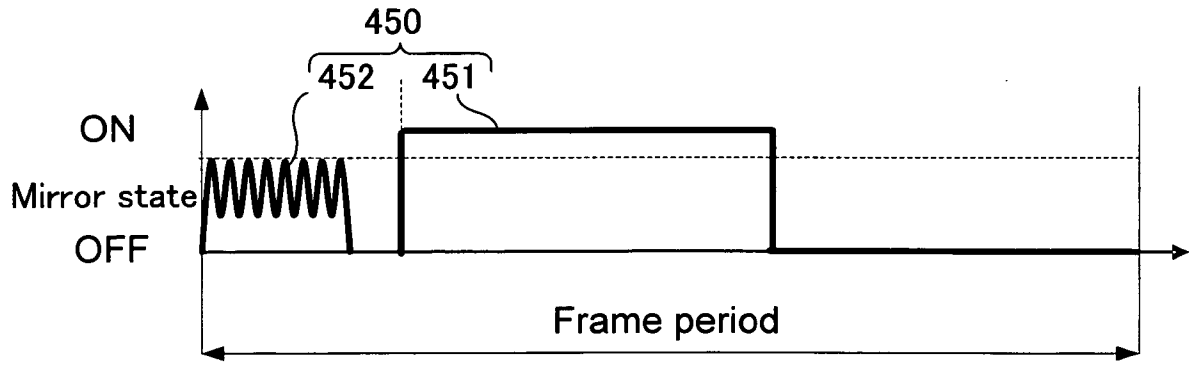


Fig. 17C

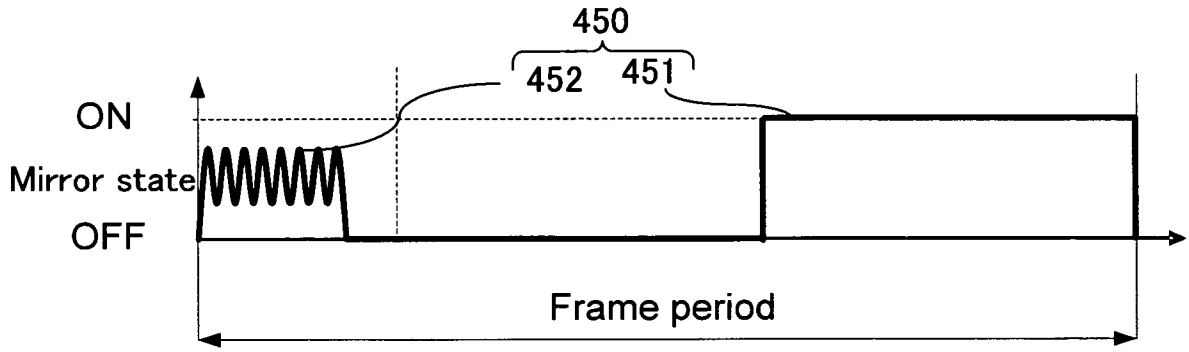


Fig. 17D

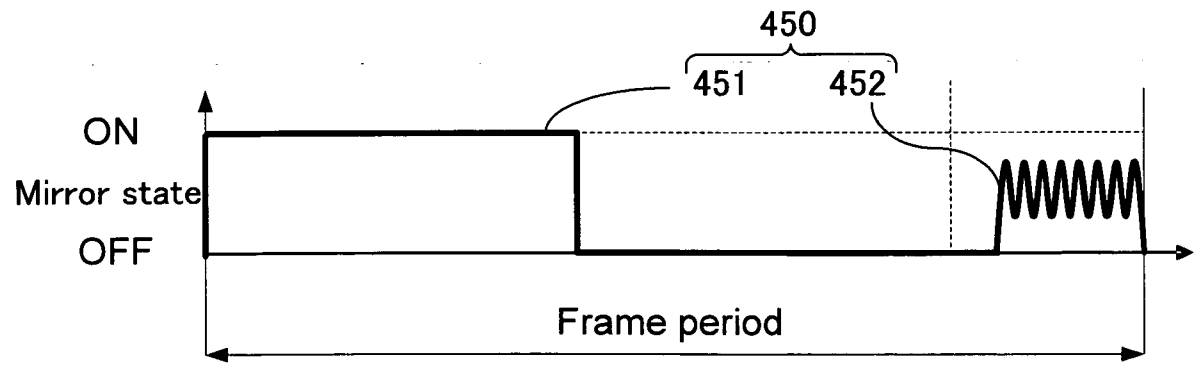


Fig. 17E

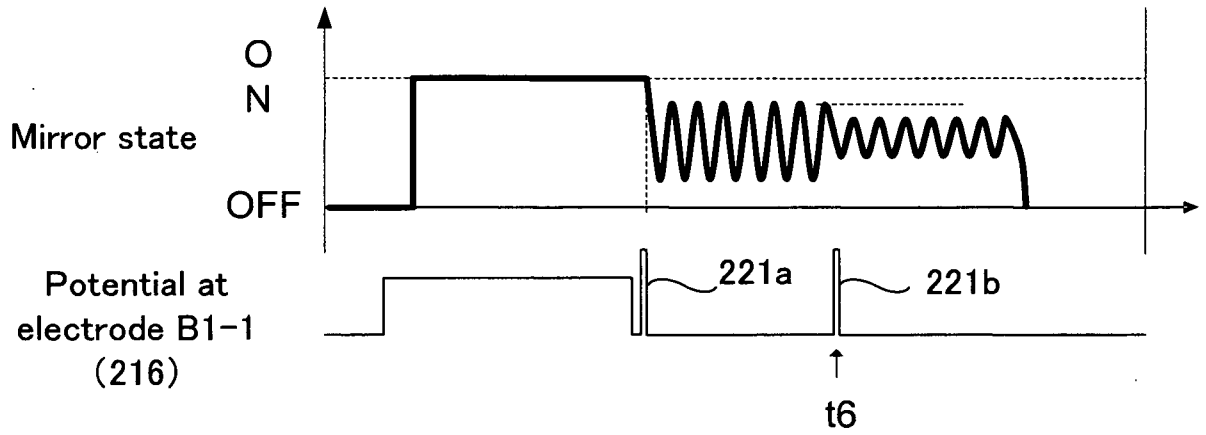


Fig. 17F

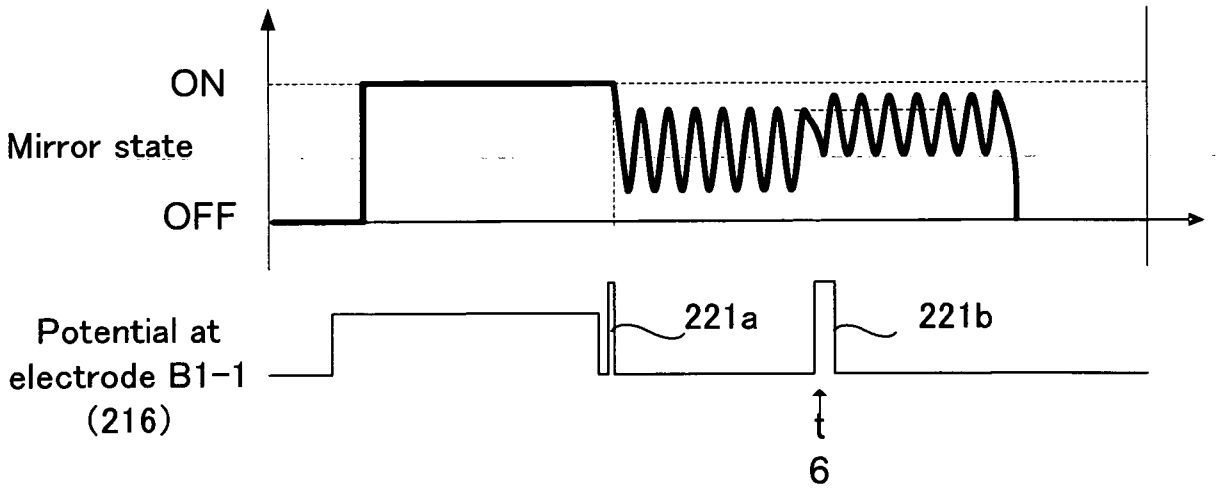


Fig. 17G

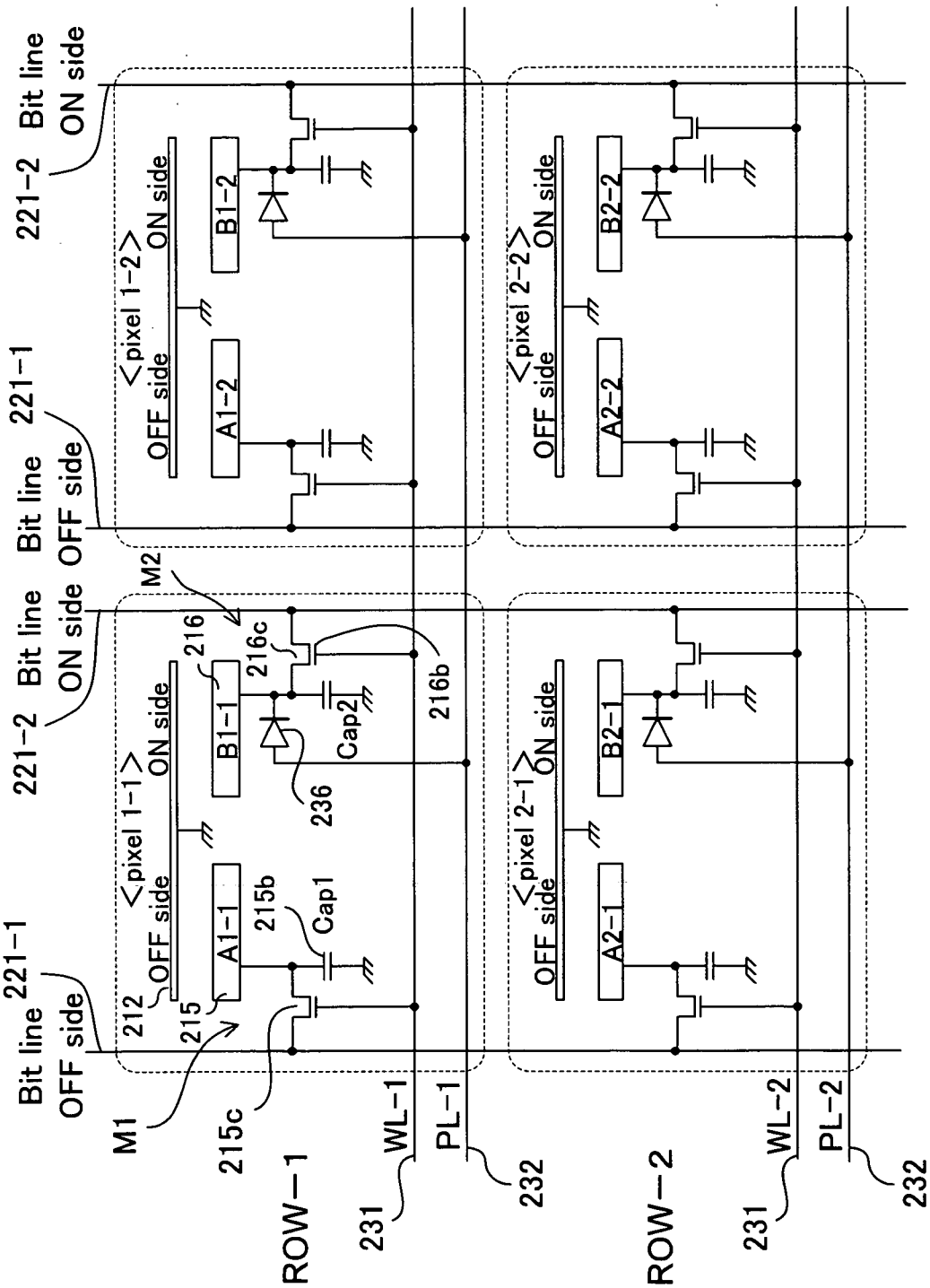

Bit line
OFF side
221-1
Bit line
ON side
221-2
Bit line
OFF side
221-1
Bit line
ON side
221-2
<pixel 1-1>
OFF side
ON side
<pixel 1-2>
OFF side
ON side
<pixel 2-1>
OFF side
ON side
<pixel 2-2>
OFF side
ON side
A1-1
A1-2
A2-1
A2-2
B1-1
B1-2
B2-1
B2-2
212
215
216
M1
M2
215b
215c
216b
216c
Cap1
Cap2
236
ROW-1
ROW-2
231
WL-1
WL-2
PL-1
PL-2
232

Fig. 18

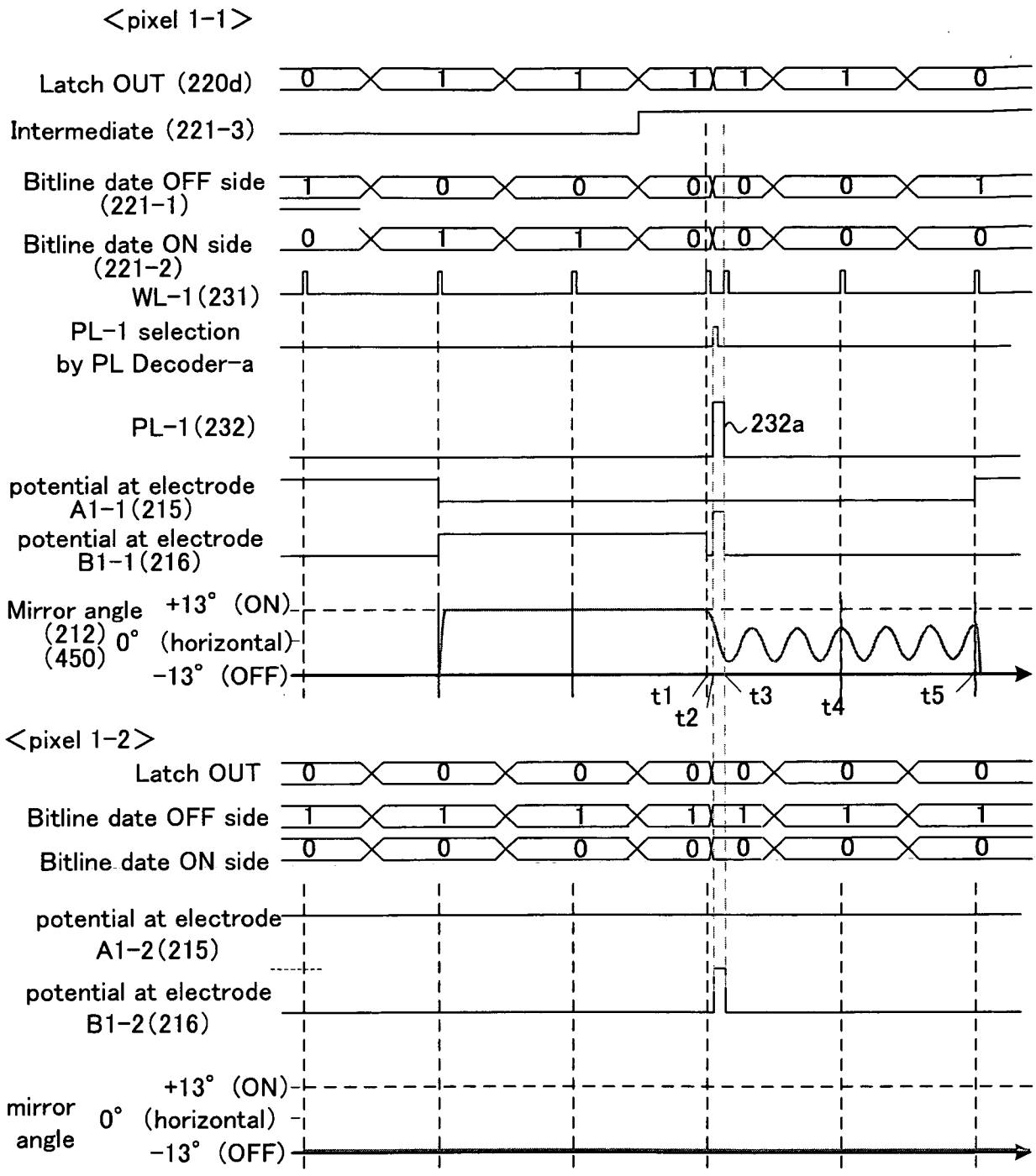

<pixel 1-1>
Latch OUT (220d)
Intermediate (221-3)
Bitline date OFF side (221-1)
Bitline date ON side (221-2)
WL-1(231)
PL-1 selection by PL Decoder-a
PL-1(232)
232a
potential at electrode A1-1(215)
potential at electrode B1-1(216)
Mirror angle (212) (450)
+13° (ON)
0° (horizontal)
-13° (OFF)
t1
t2
t3
t4
t5
<pixel 1-2>
Latch OUT
Bitline date OFF side
Bitline date ON side
potential at electrode A1-2(215)
potential at electrode B1-2(216)
mirror angle
+13° (ON)
0° (horizontal)
-13° (OFF)

Fig. 19

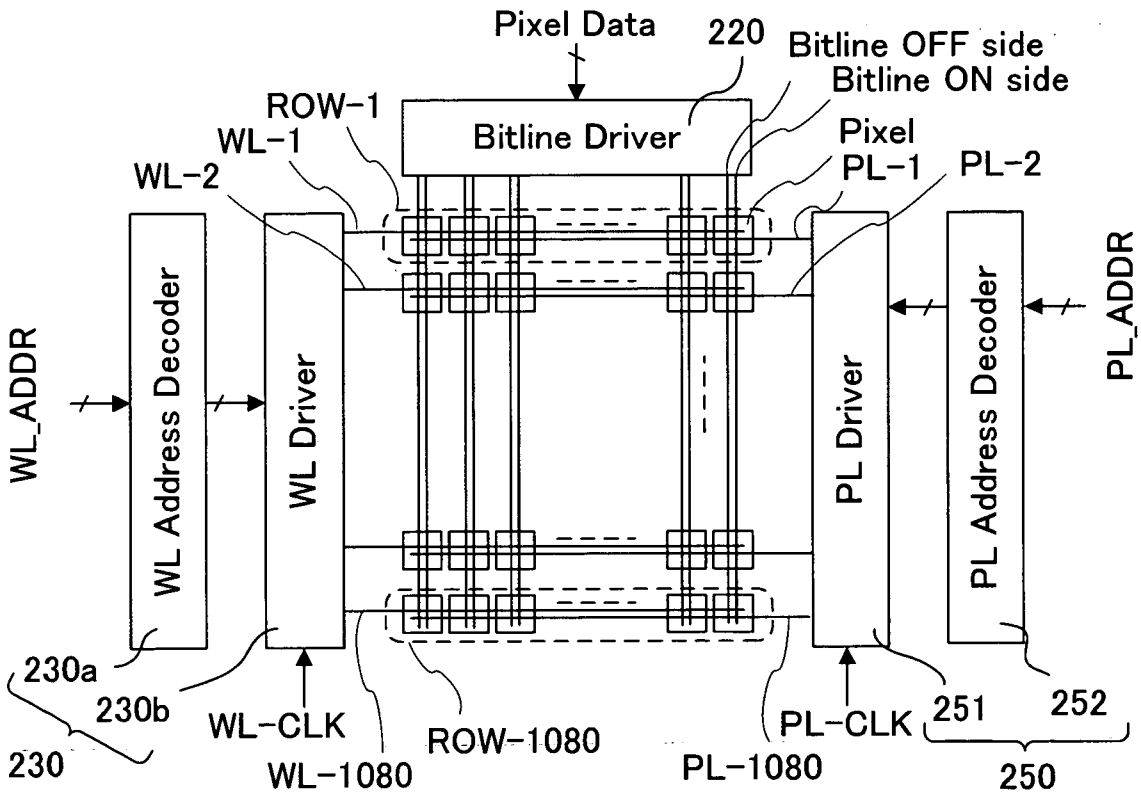

Pixel Data
220
Bitline OFF side
Bitline ON side
ROW-1
WL-1
WL-2
Bitline Driver
Pixel
PL-1
PL-2
WL_ADDR
WL Address Decoder
WL Driver
PL Driver
PL Address Decoder
PL_ADDR
230a
230b
230
WL-CLK
WL-1080
ROW-1080
PL-1080
PL-CLK
251
252
250

Fig. 20

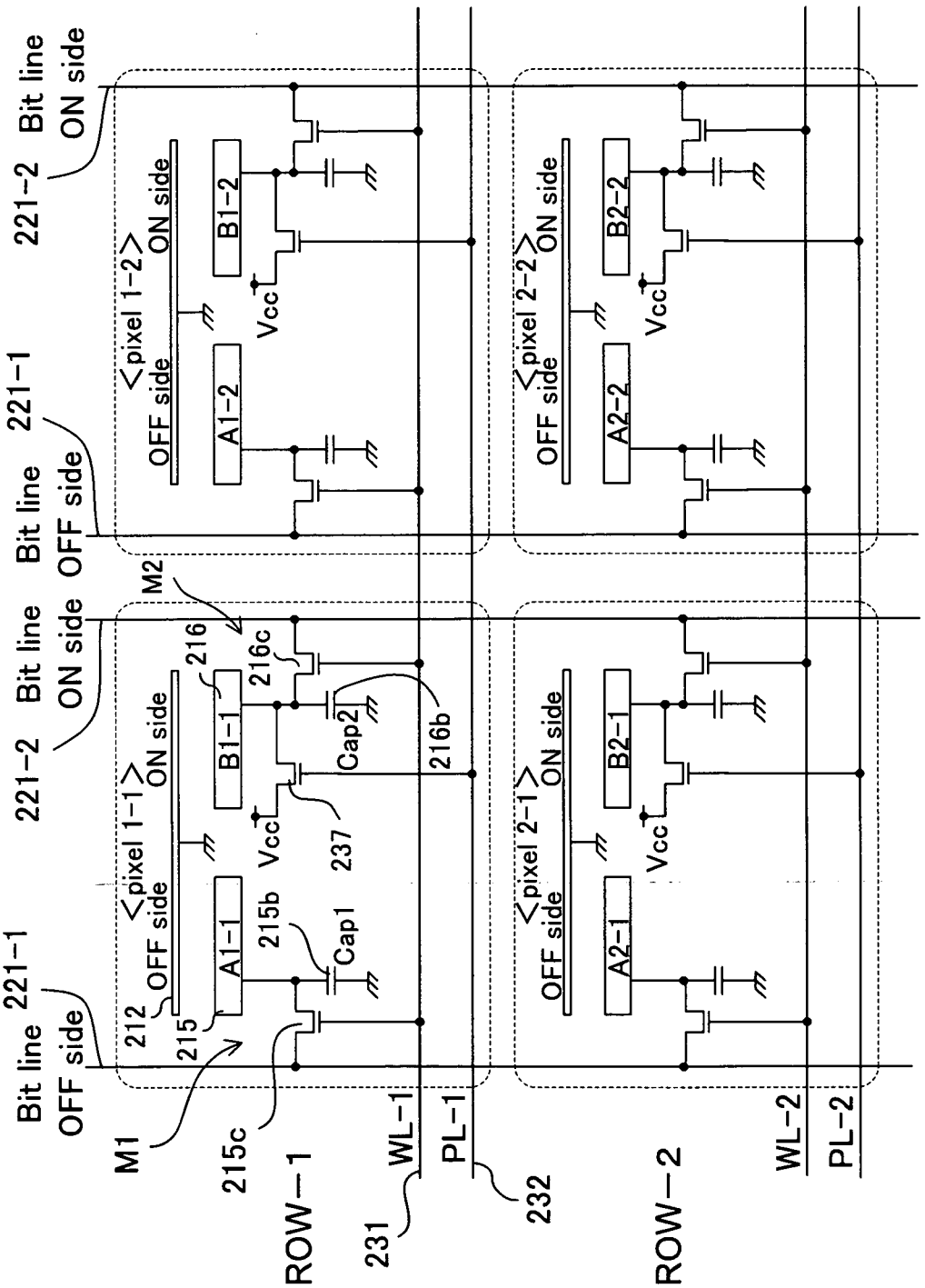

Bit line
OFF side
221-1
Bit line
ON side
221-2
<pixel 1-1>
OFF side
ON side
<pixel 1-2>
<pixel 2-1>
<pixel 2-2>
A1-1
A1-2
A2-1
A2-2
B1-1
B1-2
B2-1
B2-2
Vcc
Cap1
Cap2
M1
M2
212
215
215b
215c
216
216b
216c
237
ROW-1
ROW-2
231
232
WL-1
WL-2
PL-1
PL-2

Fig. 21

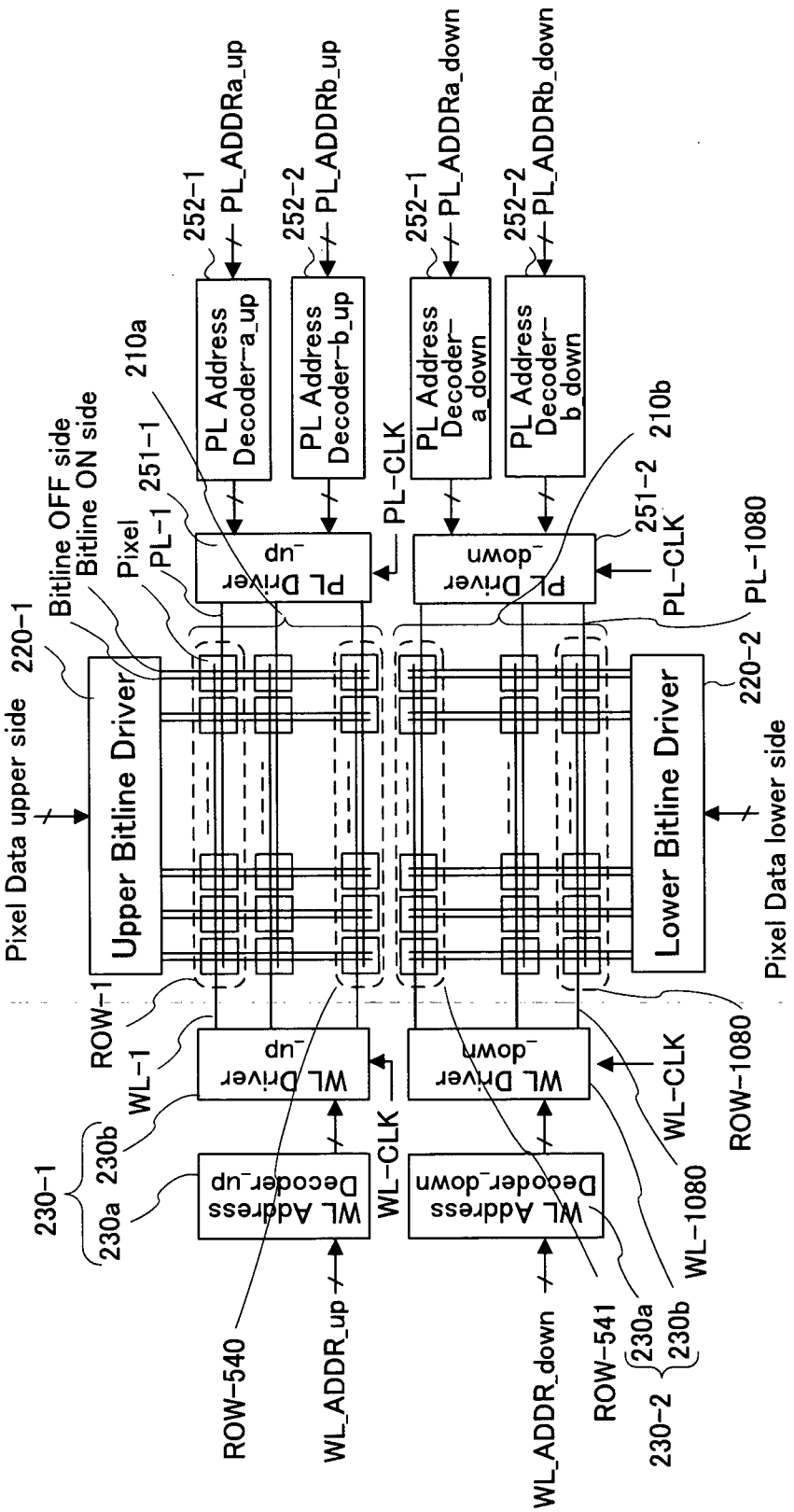

Pixel Data upper side
220-1
Upper Bitline Driver
Bitline OFF side
Bitline ON side
Pixel
PL-1
251-1
210a
PL Address Decoder-a_up
PL Address Decoder-b_up
PL Address Decoder-a_down
PL Address Decoder-b_down
252-1
PL_ADDRa_up
252-2
PL_ADDRb_up
252-1
PL_ADDRa_down
252-2
PL_ADDRb_down
PL-CLK
PL Driver_up
PL Driver_down
251-2
210b
PL-CLK
PL-1080
220-2
Lower Bitline Driver
Pixel Data lower side
ROW-1
WL-1
WL Driver_up
WL Driver_down
WL-CLK
ROW-1080
230-1
230b
230a
WL Address Decoder_up
WL Address Decoder_down
WL-CLK
WL-1080
ROW-540
WL_ADDR_up
WL_ADDR_down
ROW-541
230-2
230a
230b

Fig. 22A

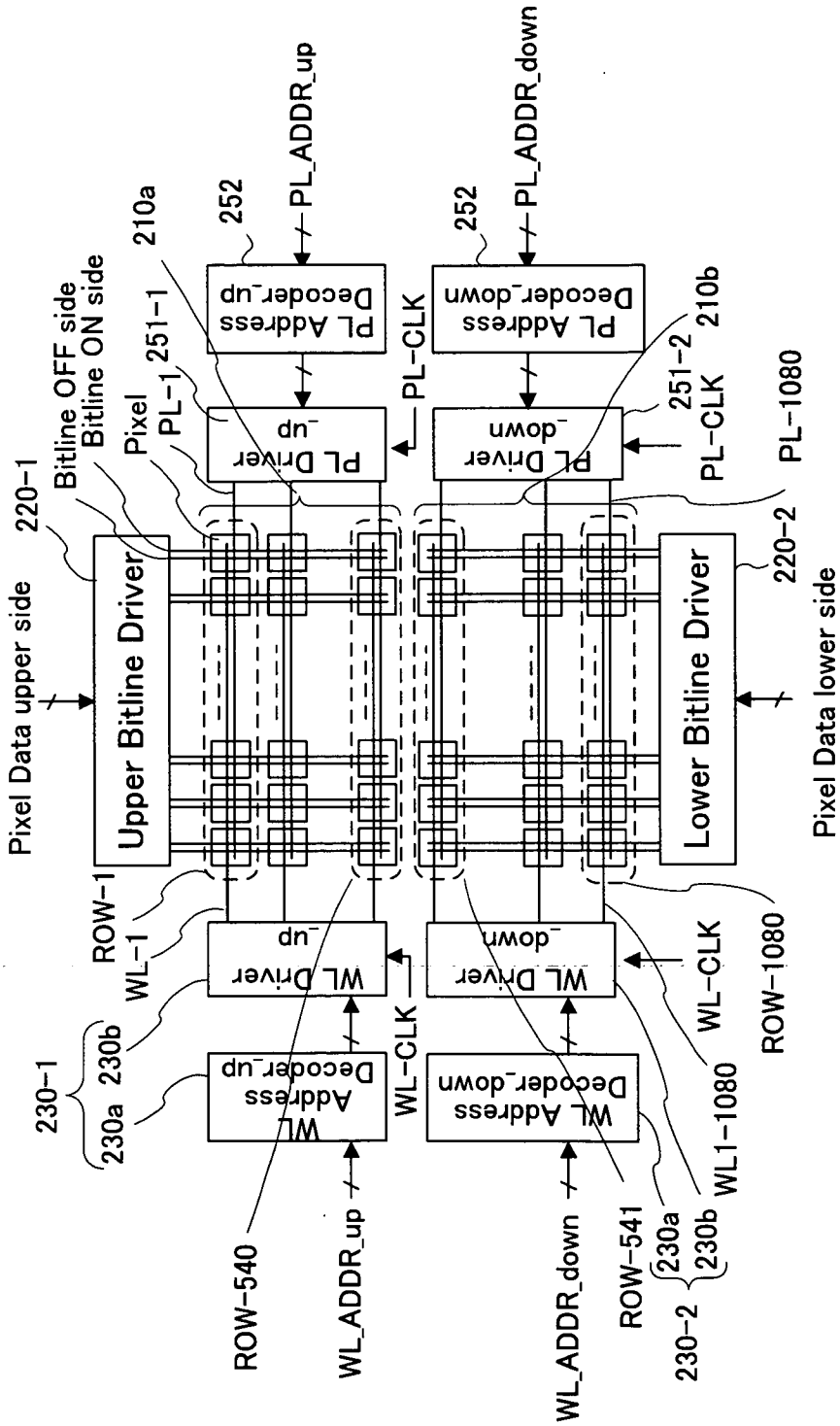

Pixel Data upper side
Upper Bitline Driver
220-1
Bitline OFF side
Bitline ON side
Pixel
PL-1
251-1
210a
252
PL_ADDR_up
PL Address Decoder_up
PL Driver_up
PL-CLK
PL_ADDR_down
PL Address Decoder_down
PL Driver_down
251-2
210b
PL-1080
PL-CLK
220-2
Lower Bitline Driver
Pixel Data lower side
ROW-1
WL-1
230-1
230b
230a
WL Address Decoder_up
WL Driver_up
WL-CLK
WL Address Decoder_down
WL Driver_down
WL-CLK
ROW-1080
WL1-1080
ROW-540
WL_ADDR_up
WL_ADDR_down
ROW-541
230a
230b
230-2

Fig. 22B

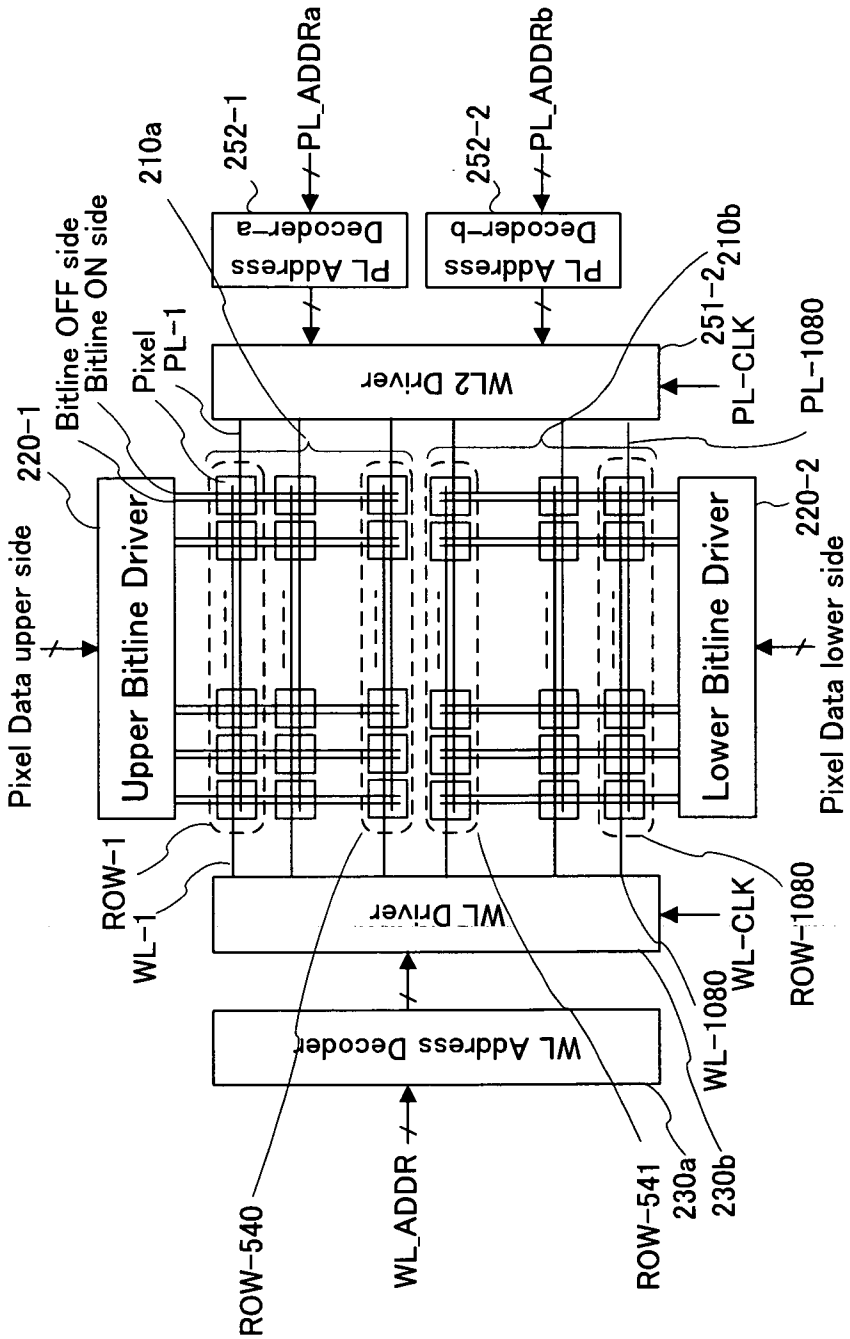

PL_ADDRa
PL_ADDRb
252-1
252-2
210a
210b
PL Address Decoder-a
PL Address Decoder-b
WL2 Driver
251-2
PL-CLK
PL-1080
Pixel PL-1
Bitline OFF side
Bitline ON side
220-1
220-2
Upper Bitline Driver
Lower Bitline Driver
Pixel Data upper side
Pixel Data lower side
ROW-1
WL-1
WL Driver
WL-CLK
WL-1080
ROW-1080
WL Address Decoder
WL_ADDR
ROW-540
ROW-541
230a
230b

Fig. 22C

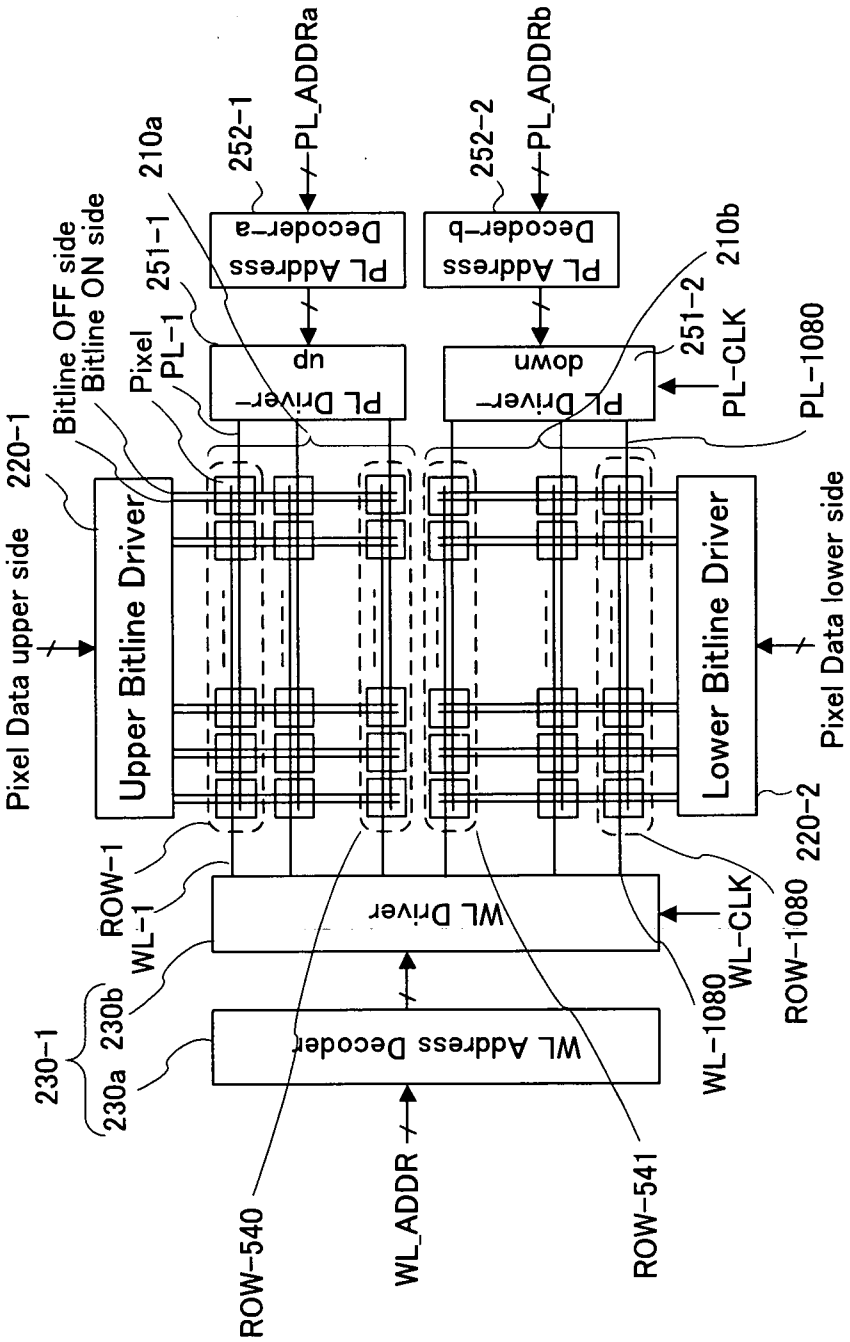

Pixel Data upper side
220-1
Bitline OFF side
Bitline ON side
Upper Bitline Driver
Pixel
PL-1
251-1
210a
252-1
PL_ADDRa
PL Address Decoder-a
PL Driver-up
PL Address Decoder-b
PL Driver-down
251-2
210b
PL-CLK
PL-1080
Lower Bitline Driver
Pixel Data lower side
220-2
ROW-1
WL-1
WL Driver
WL-CLK
ROW-1080
WL-1080
230-1
230b
230a
WL Address Decoder
WL_ADDR
ROW-540
ROW-541

Fig. 22D

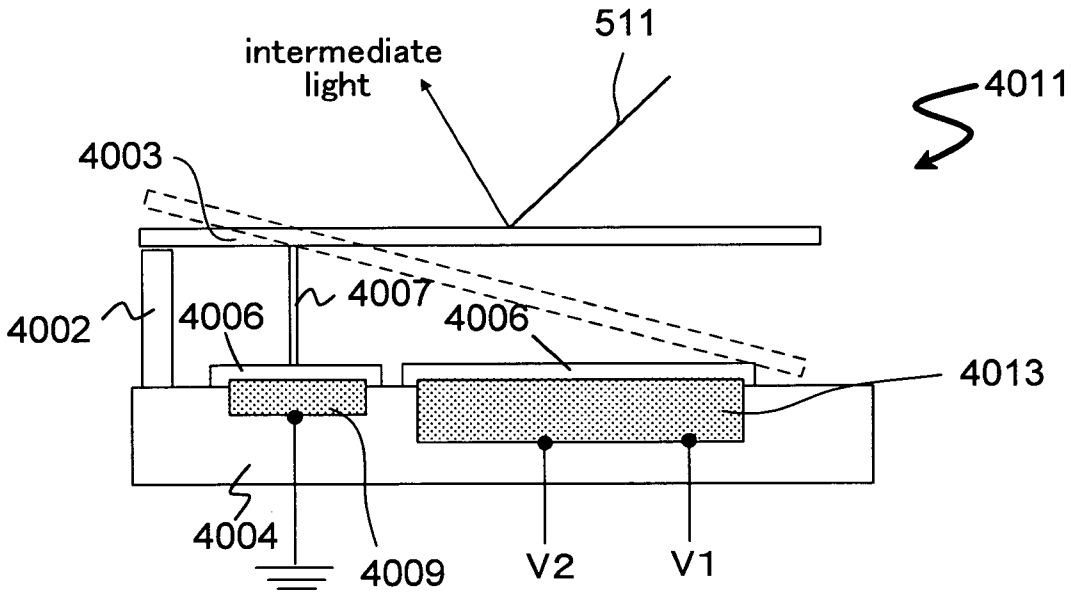

511
intermediate
light
4011
4003
4002
4006
4007
4006
4013
4004
4009
V2
V1

Fig.23A

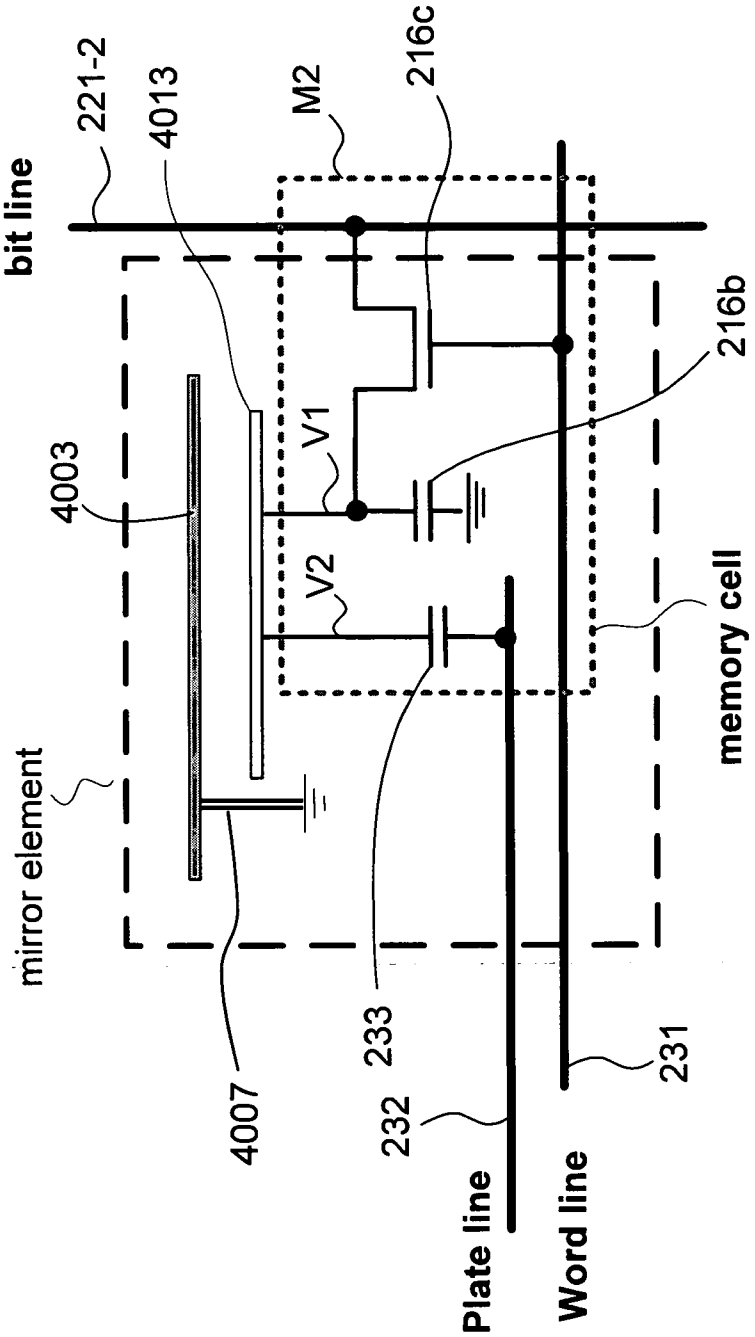

bit line
221-2
4013
M2
216c
216b
4003
V1
V2
memory cell
(M2)
mirror element
4007
233
232
231
Plate line
Word line

Fig.23B

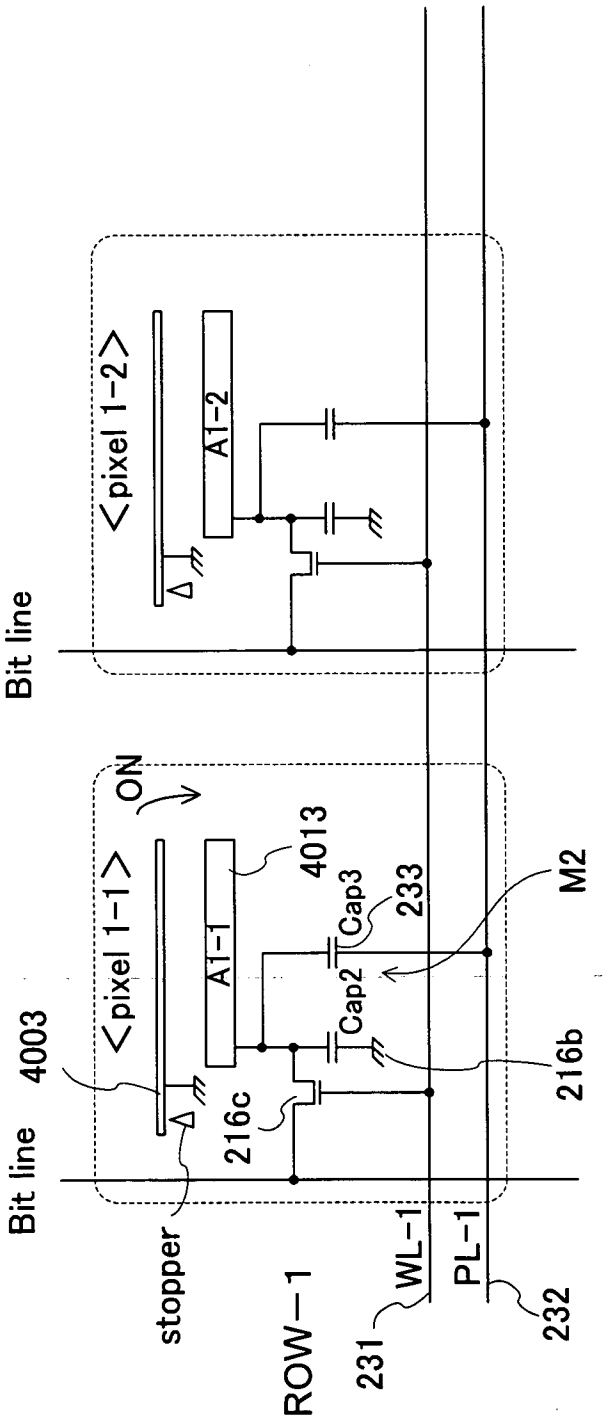

Bit line
<pixel 1-2>
A1-2
Bit line
ON
<pixel 1-1>
A1-1
4013
Cap3
233
M2
Cap2
4003
216c
216b
stopper
ROW−1
231
WL-1
PL-1
232

Fig. 24

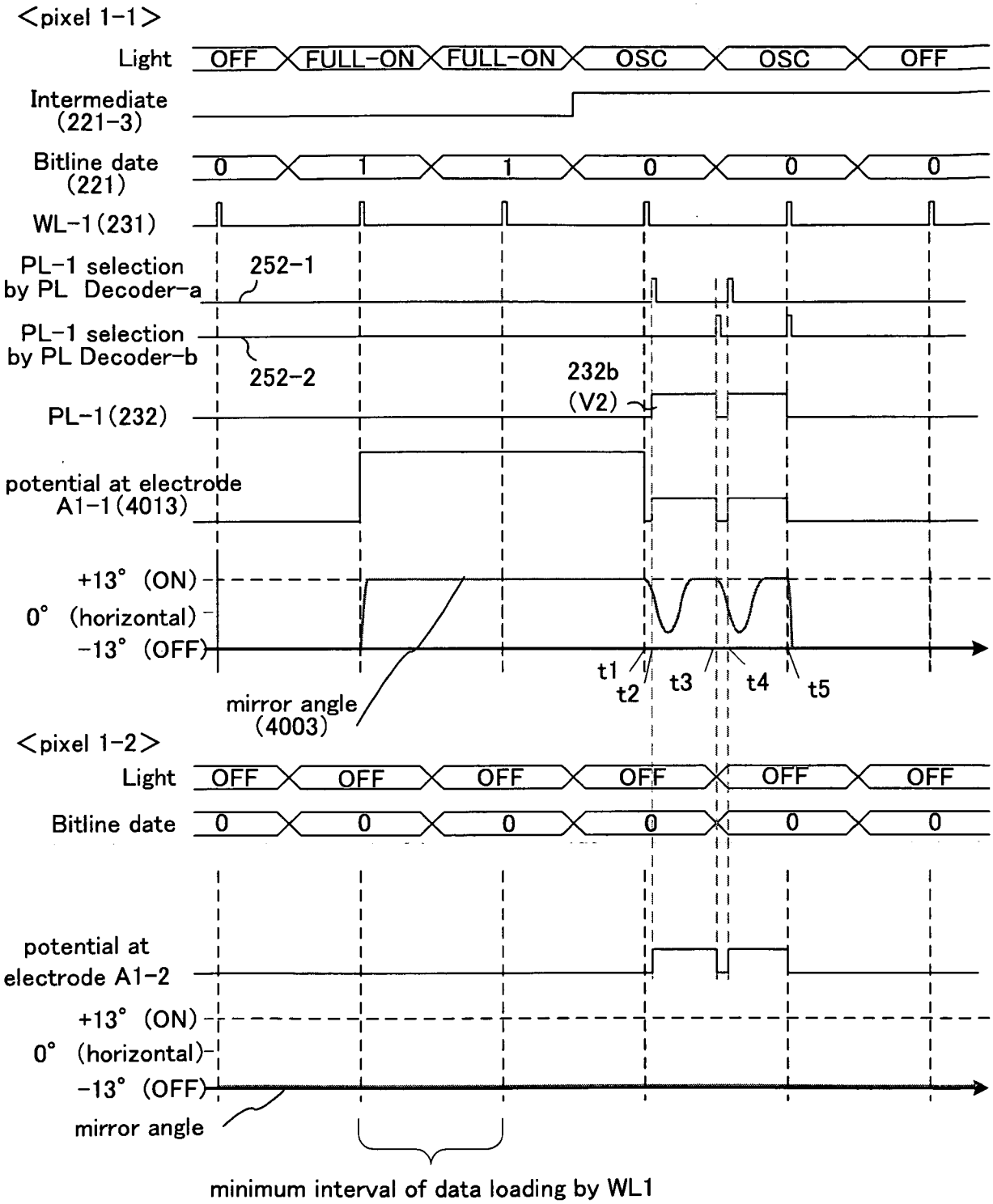

<pixel 1-1>
Light
OFF
FULL-ON
FULL-ON
OSC
OSC
OFF
Intermediate (221-3)
Bitline date (221)
0
1
1
0
0
0
WL-1(231)
PL-1 selection by PL Decoder-a
252-1
PL-1 selection by PL Decoder-b
252-2
232b (V2)
PL-1(232)
potential at electrode A1-1(4013)
+13° (ON)
0° (horizontal)
-13° (OFF)
mirror angle (4003)
t1
t2
t3
t4
t5
<pixel 1-2>
Light
OFF
OFF
OFF
OFF
OFF
OFF
Bitline date
0
0
0
0
0
0
potential at electrode A1-2
+13° (ON)
0° (horizontal)
-13° (OFF)
mirror angle
minimum interval of data loading by WL1

Fig. 25

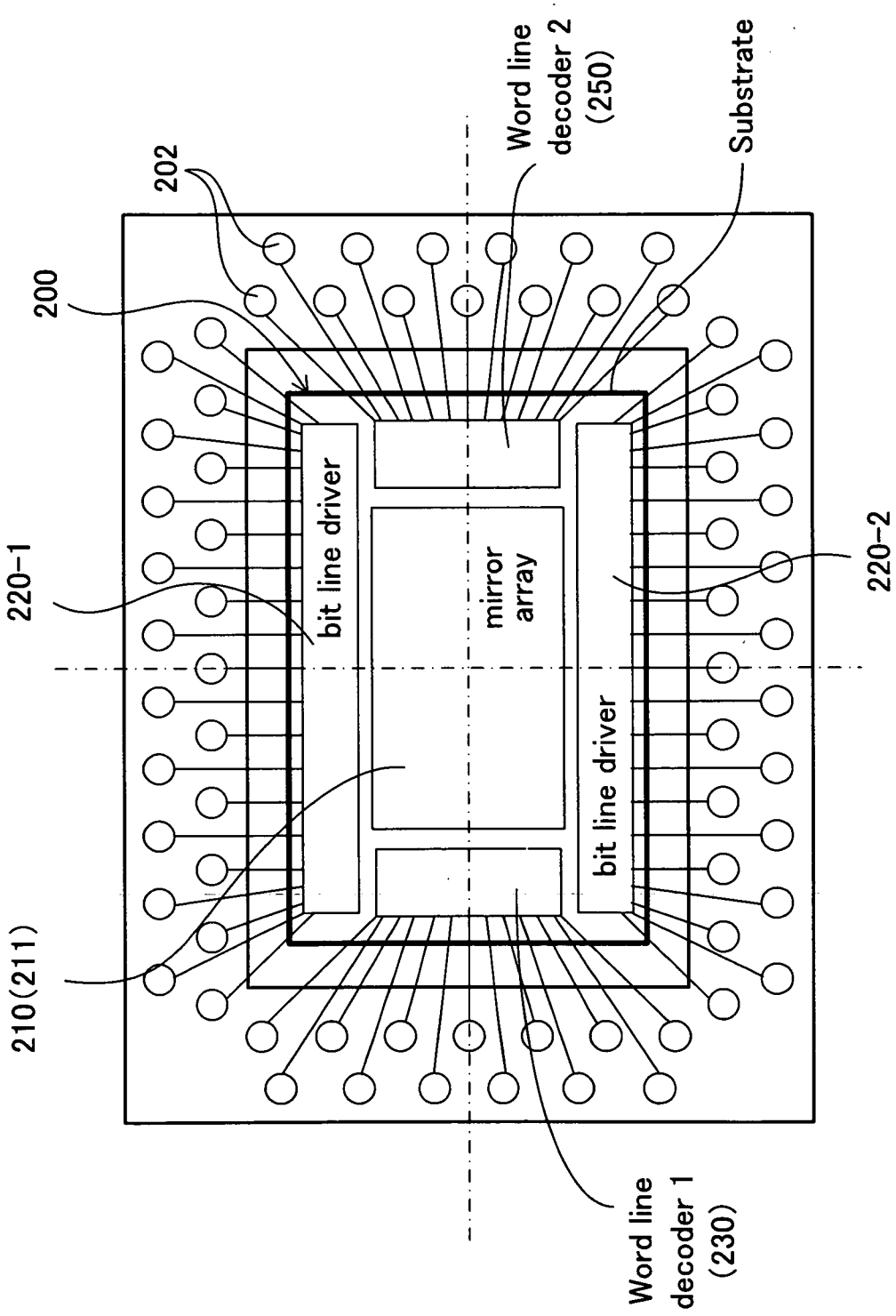

Word line decoder 2 (250)
Substrate
202
200
bit line driver
mirror array
bit line driver
220-1
220-2
210(211)
Word line decoder 1 (230)

Fig.26A

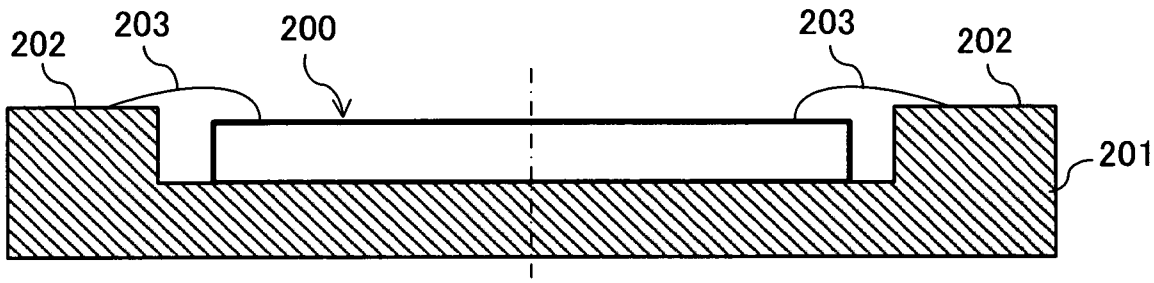


Fig.26B

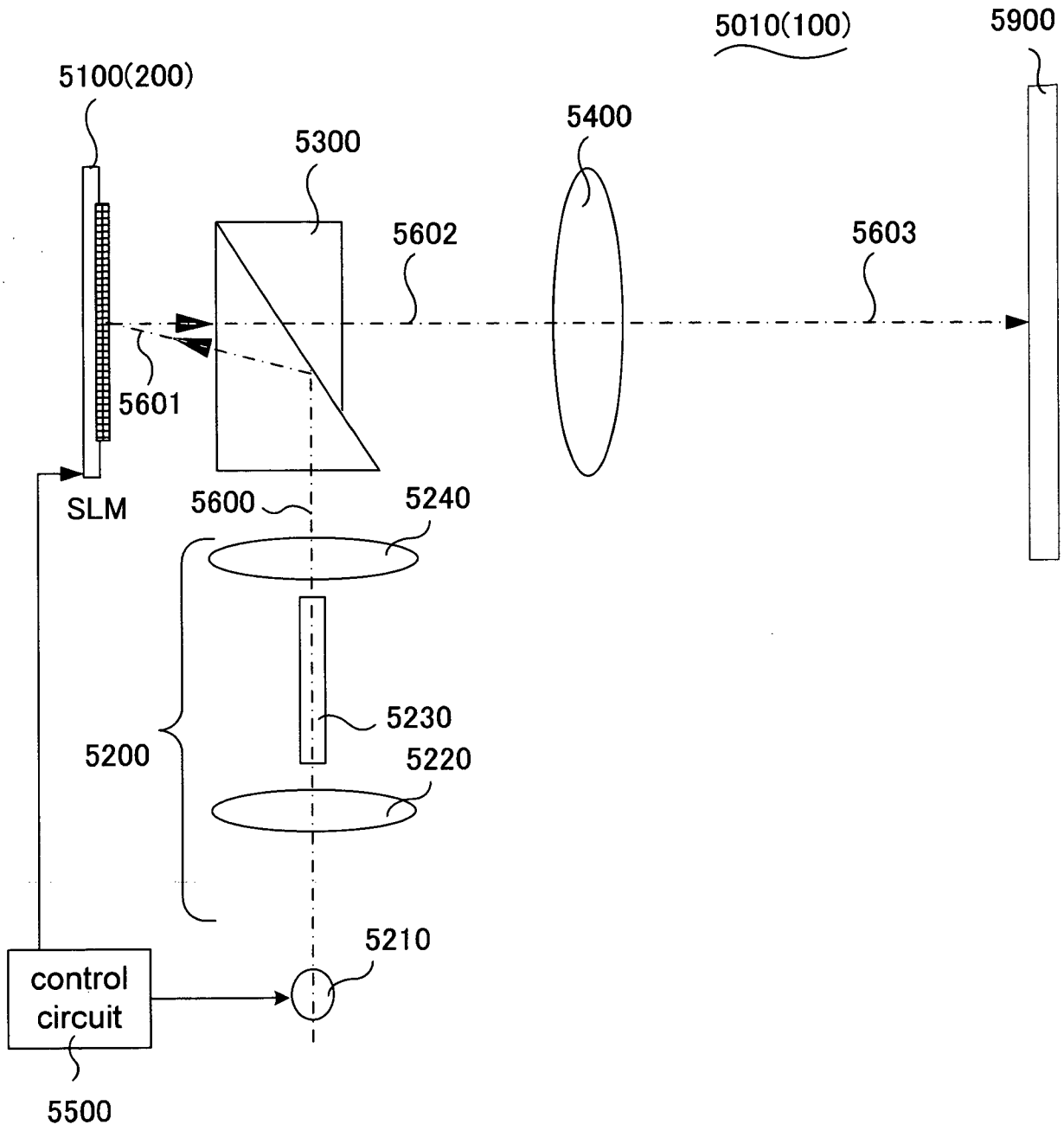

5010(100)
5900
5100(200)
5400
5300
5602
5603
5601
SLM
5600
5240
5230
5200
5220
5210
control circuit
5500

FIG. 27

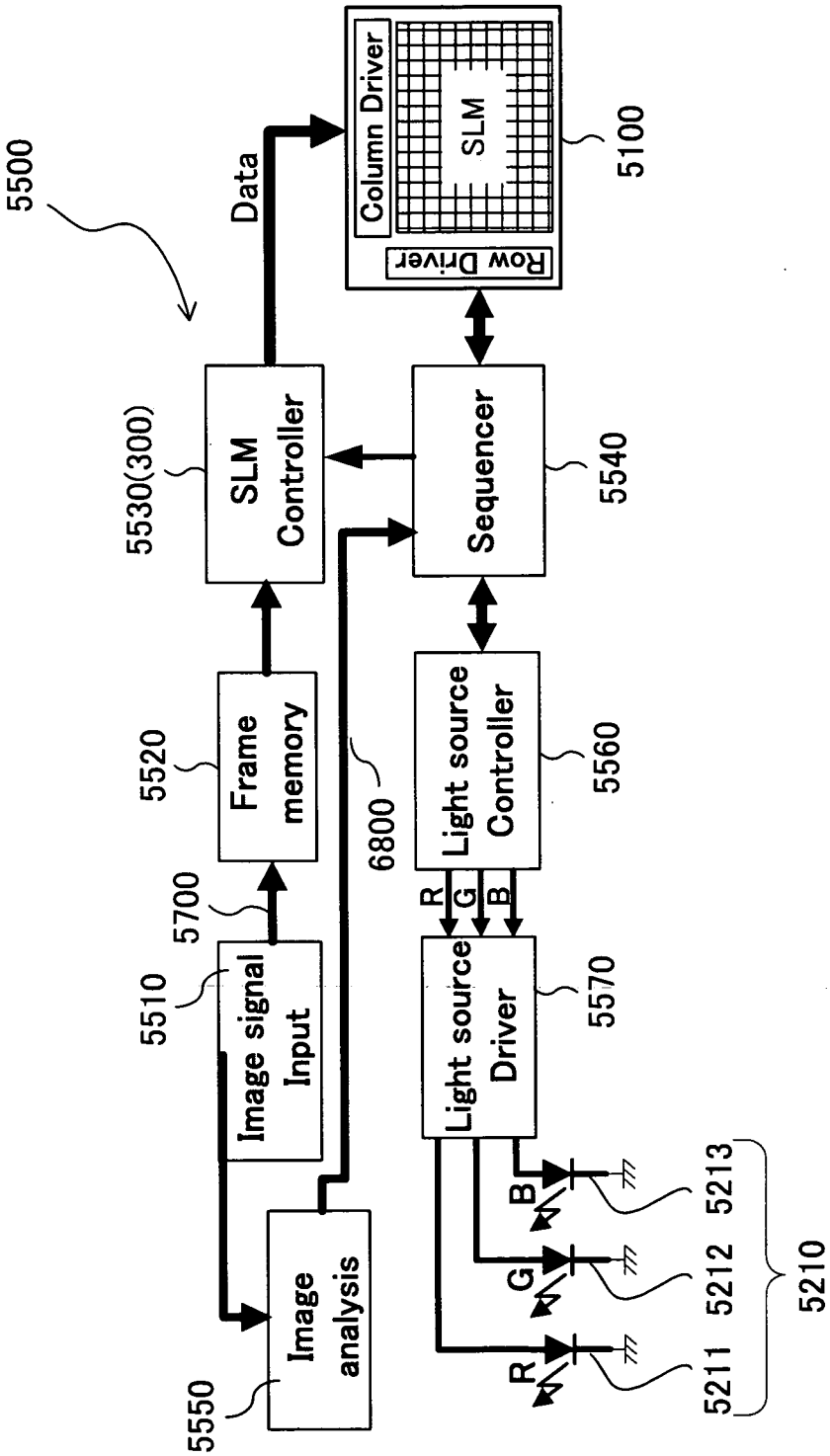

5500
Data
Column Driver
SLM
Row Driver
5100
5530(300)
SLM Controller
Sequencer
5540
5520
Frame memory
6800
Light source Controller
5560
R
G
B
5700
5510
Image signal Input
Light source Driver
5570
B
G
R
5213
5212
5211
5210
5550
Image analysis

FIG. 28

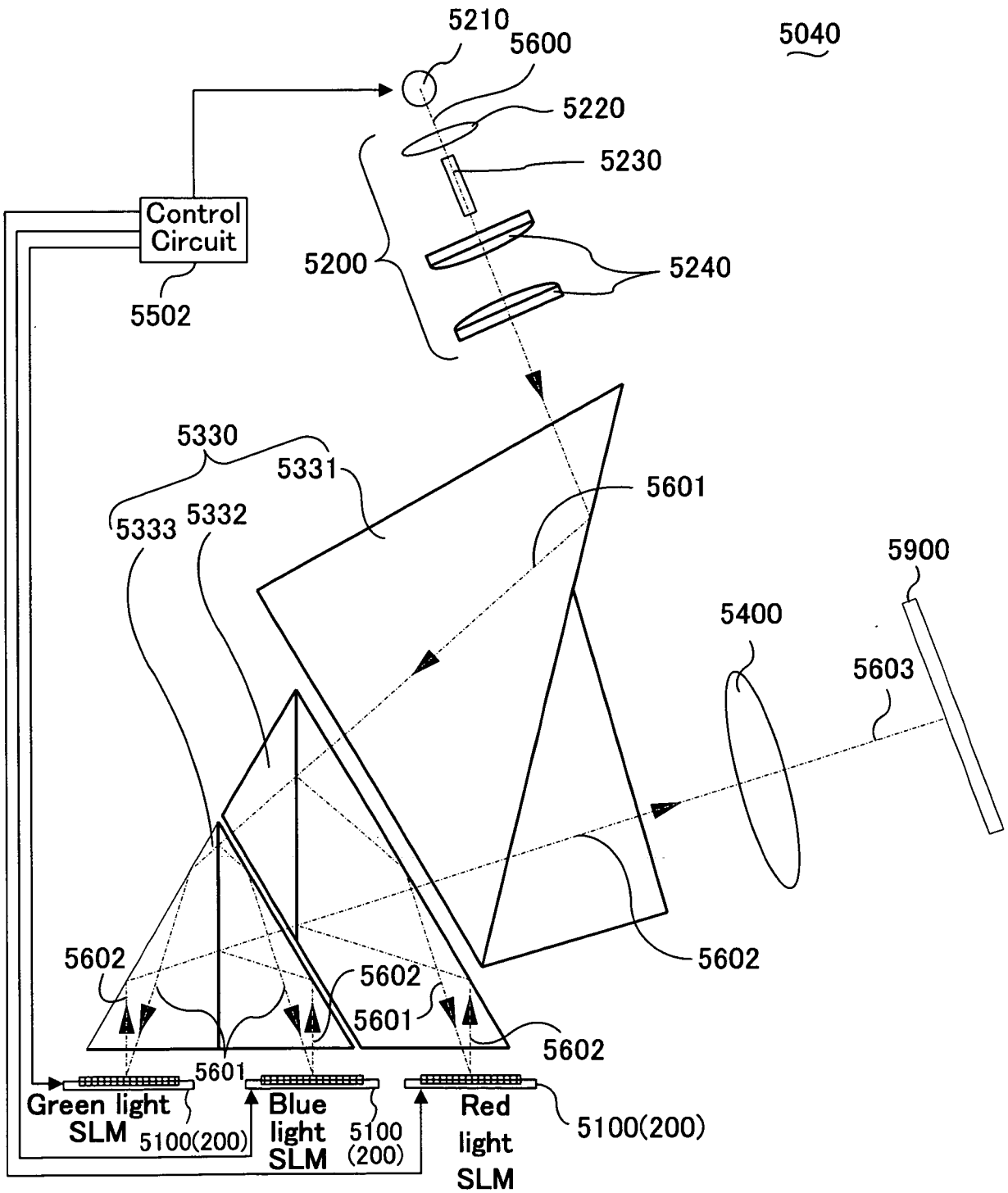

5210
5600
5040
5220
5230
Control Circuit
5200
5240
5502
5330
5331
5601
5333
5332
5900
5400
5603
5602
5602
5601
5602
5602
5601
Green light SLM
5100(200)
Blue light SLM
5100 (200)
Red light SLM
5100(200)

FIG. 29

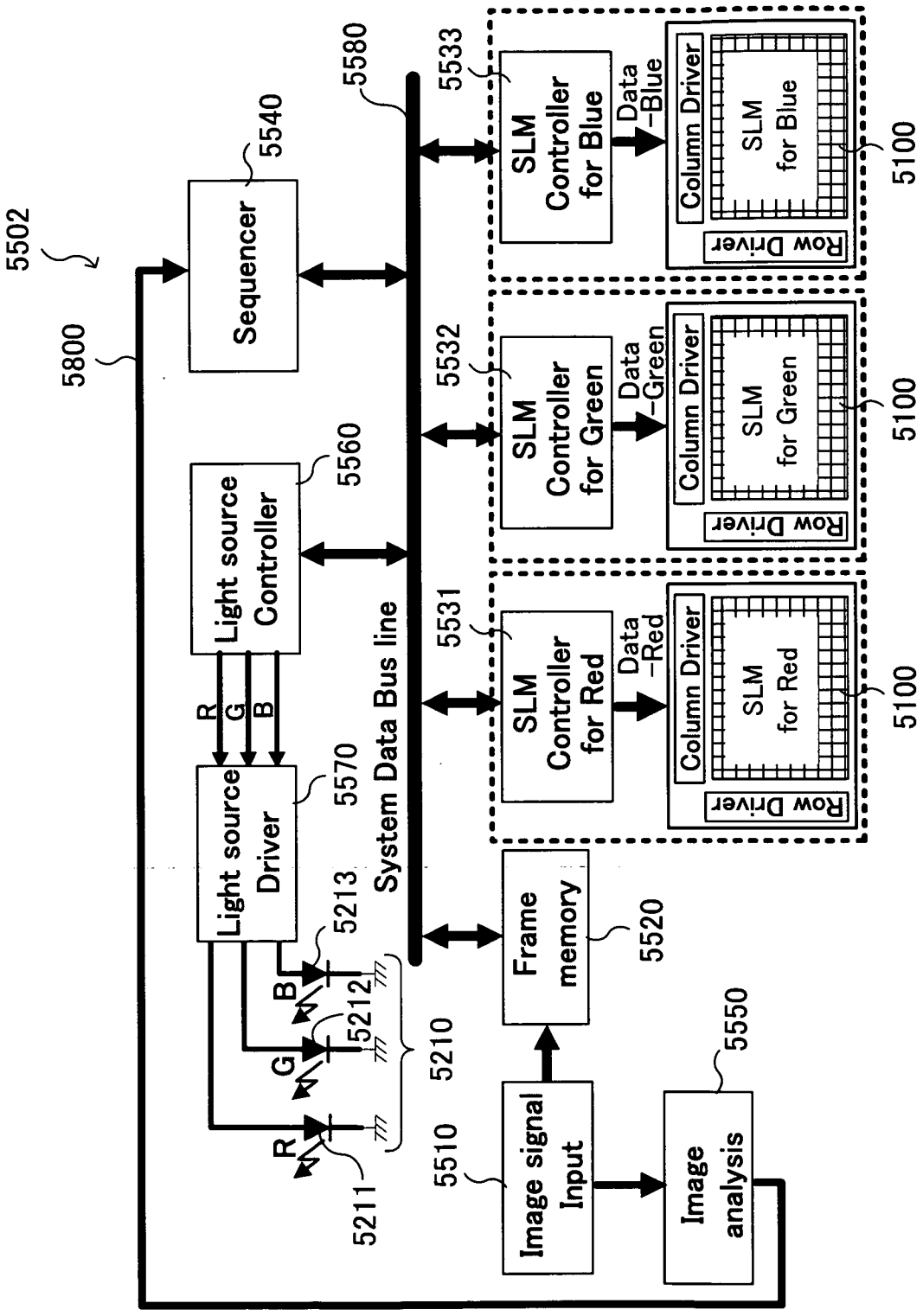

5502
5800
Sequencer
5540
5580
5533
SLM Controller for Blue
Data -Blue
Column Driver
SLM for Blue
Row Driver
5100
5532
SLM Controller for Green
Data -Green
SLM for Green
5560
Light source Controller
R
G
B
5531
SLM Controller for Red
Data -Red
SLM for Red
5570
Light source Driver
System Data Bus line
5213
5212
5210
5211
Frame memory
5520
5510
Image signal Input
5550
Image analysis

FIG. 30

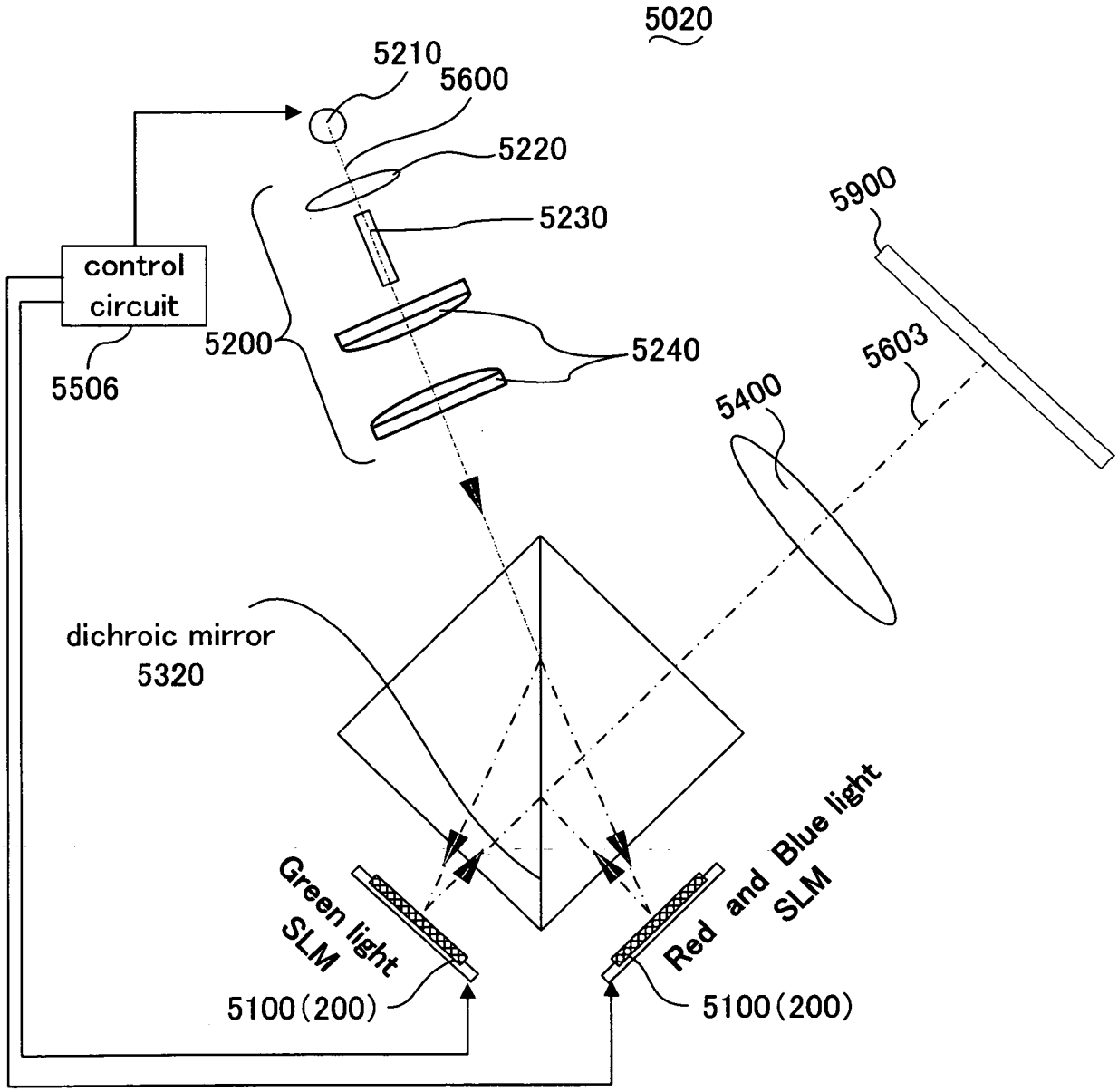

5020
5210
5600
5220
5230
5900
control circuit
5200
5240
5603
5506
5400
dichroic mirror
5320
Green light SLM
Red and Blue light SLM
5100(200)
5100(200)

FIG. 31

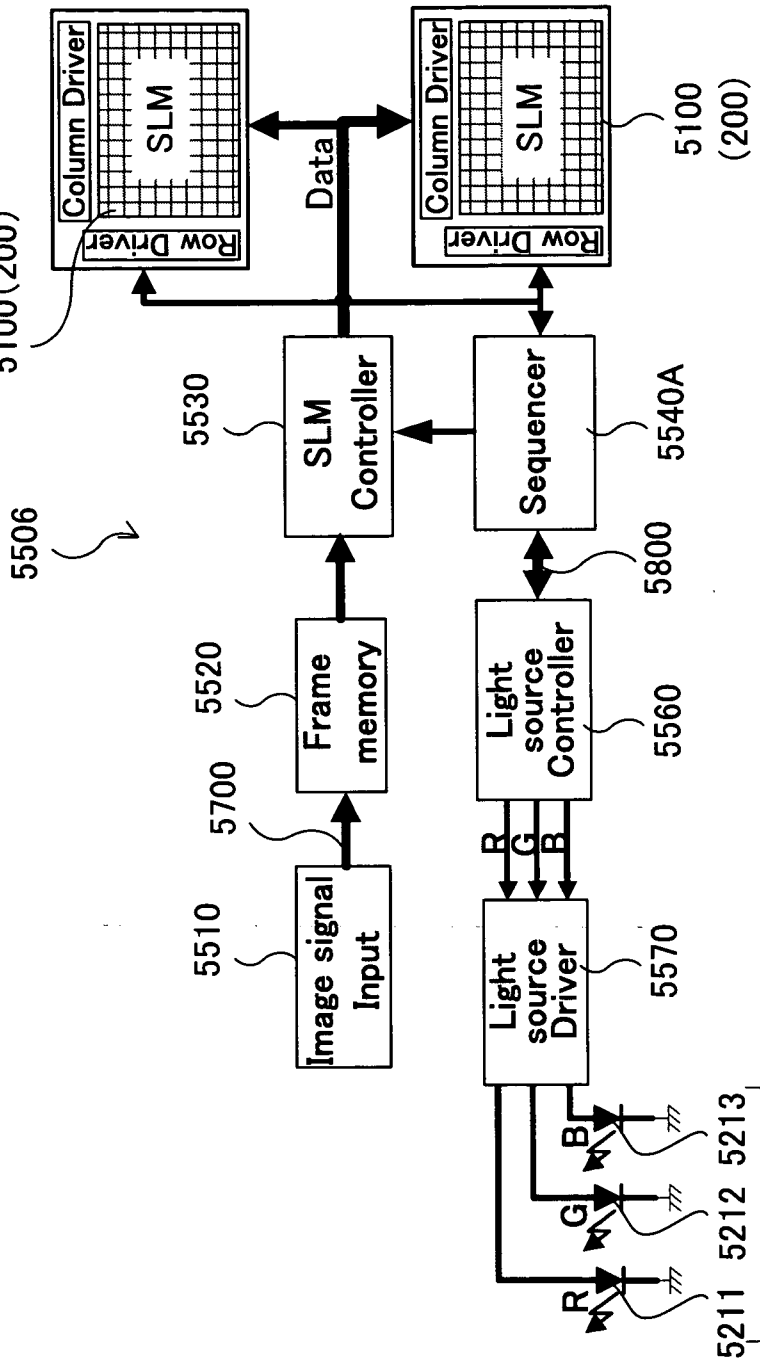

Column Driver
SLM
Row Driver
5100(200)
Data
5100
(200)
5530
SLM Controller
Sequencer
5540A
5506
5800
5520
Frame memory
Light source Controller
5560
5700
R
G
B
5510
Image signal Input
Light source Driver
5570
B
G
R
5213
5212
5211
5210

FIG. 32

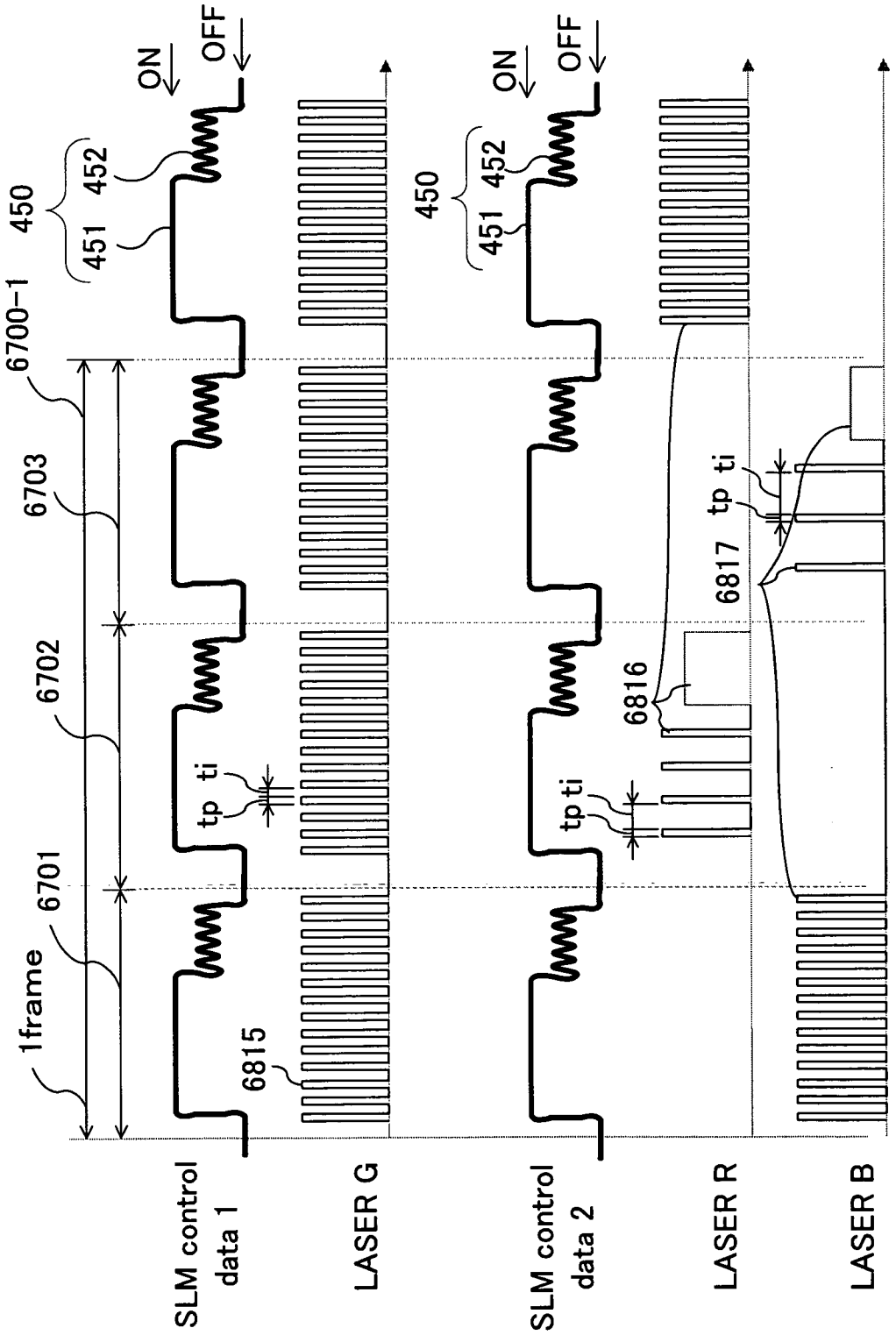

1frame
6701
6702
6703
6700-1
450
451
452
ON
OFF
tp
ti
6815
6816
6817
SLM control data 1
LASER G
SLM control data 2
LASER R
LASER B

FIG. 33

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/12788

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G02B 5/08 (2009.01)
USPC - 359/850
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC 359/850

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC 359/838, 850, 851, 861, 862, 871, 872; 235/462.36 (text search--see below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWest (PGPB,USPT,EPAB,JPAB); Google Scholar
Search terms: micro-mirror, plate line, word line, bit line, SLM, spatial light modulator, projection, HDTV, high definition, display, gray scale, DMD, digital micromirror device

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2005/0254116 A1 (ISHII) 17 November 2005 (17.11.2005) FIG. 1C, 2, and 4, and para [0004]-[0006], [0030]-[0032]	1-13
Y	US 2004/0189548 A1 (TAKEUCHI et al.) 30 September 2004 (30.09.2004) FIG. 1, and para [0037], [0144]	1-13
Y	US 6,431,714 B1 (SAWADA et al.) 13 August 2002 (13.08.2002) FIG. 1 and 27, and col.4, ln 48 -67, col. 6, ln 15-22, and col. 17, ln 27-36	1-9
Y	US 2004/0223240 A1 (HUIBERS) 11 November 2004 (11.11.2004) FIG. 8 and para [0078]	6-7
Y	US 5,444,566 A (GALE et al.) 22 August 1995 (22.08.1995) FIG. 13 and col. 6, ln 45-67 and col. 7, ln 1-10	8, 10-13

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 January 2009 (07.01.2009)	16 JAN 2009
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774