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Thorne-Booth et al.

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[45] **Feb. 26, 1974**

[54] **MULTIPLEX CONTROL SYSTEM FOR CONTROLLING THE OPERATION OF A PLURALITY OF STATIONS**

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[21] Appl. No.: **123,258**

Related U.S. Application Data

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[52] **U.S. Cl.** ..... **340/163 R,** 340/147 SY

[51] **Int. Cl.** **H04q 11/00**

[58] **Field of Search** ..... 340/163 R, 147 SY

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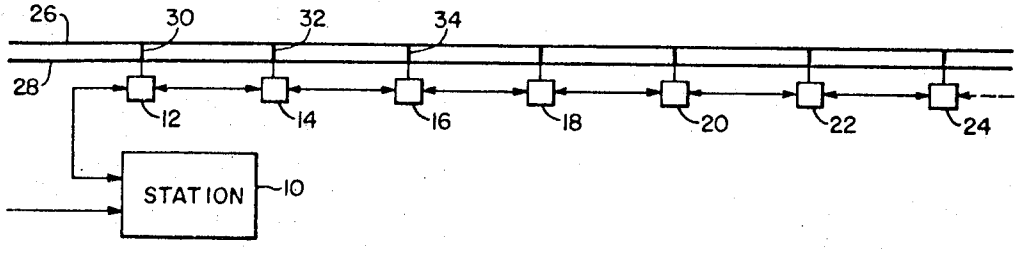
Attorney, Agent, or Firm—J. M. Arnold

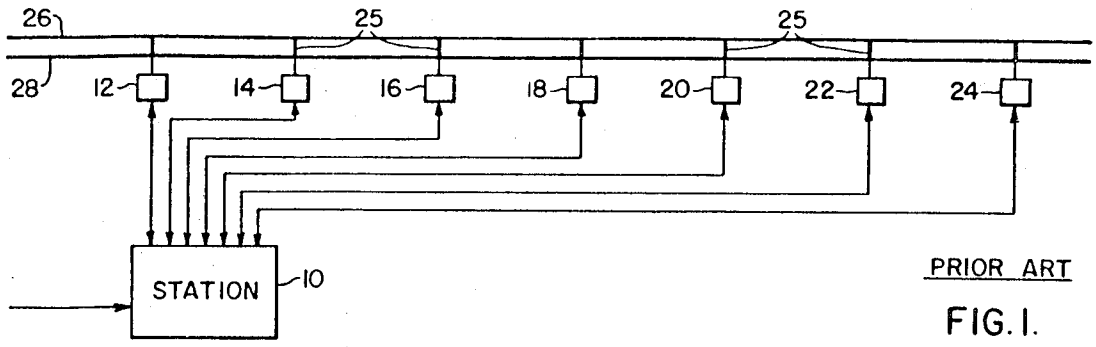
[57] **ABSTRACT**

A train control signalling system is provided for train speed command signals and train position detection signals which system is operative in a fail-safe manner with a plurality of isolated track circuit blocks. For a given train system, a plurality of wayside stations is provided, with each station being operative through a limited number of conductors to energize a predetermined number of track circuit blocks. Each station includes a crystal controlled signal generator to assure an accurate coherent base frequency control of the communicated signals and provide control signals for the signal communication operation relative to each station to thereby control, in effect as an extension of the crystal control concept, accuracy to each of the associated track circuit blocks.

Up to 32 separated track circuit block locations receive information from each wayside station, for this particular system as described, over a common time division multiplexed signalling system, so it is necessary that each location receive its particular information only at the correct time period. This is accomplished by an appropriate control signal sent for this purpose to each track circuit block location.

7 Claims, 10 Drawing Figures





PRIOR ART

FIG. 1.

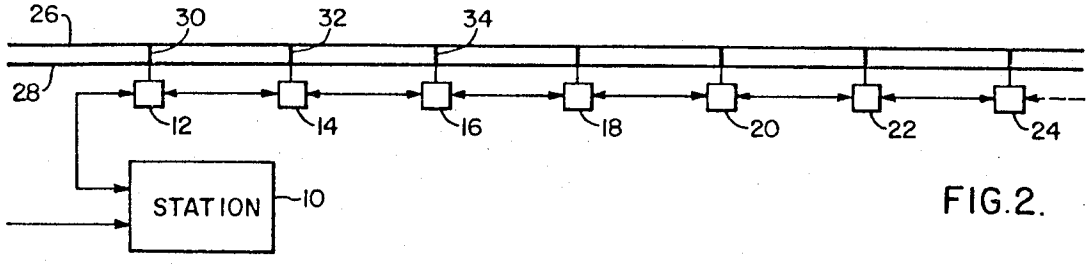


FIG. 2.

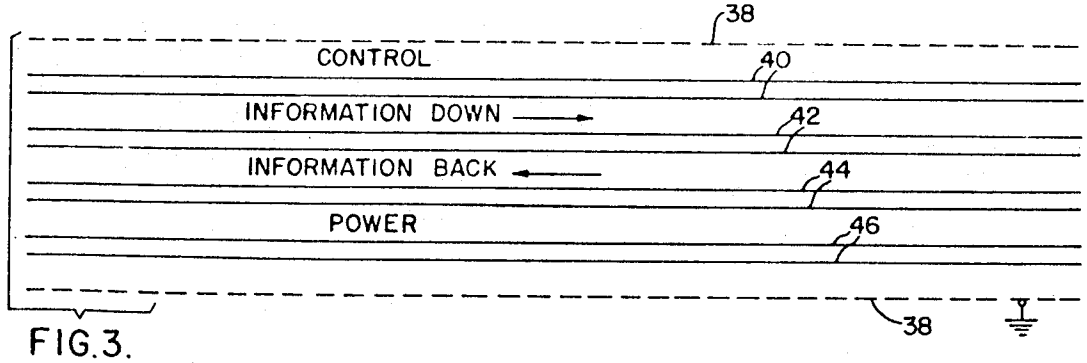


FIG. 3.

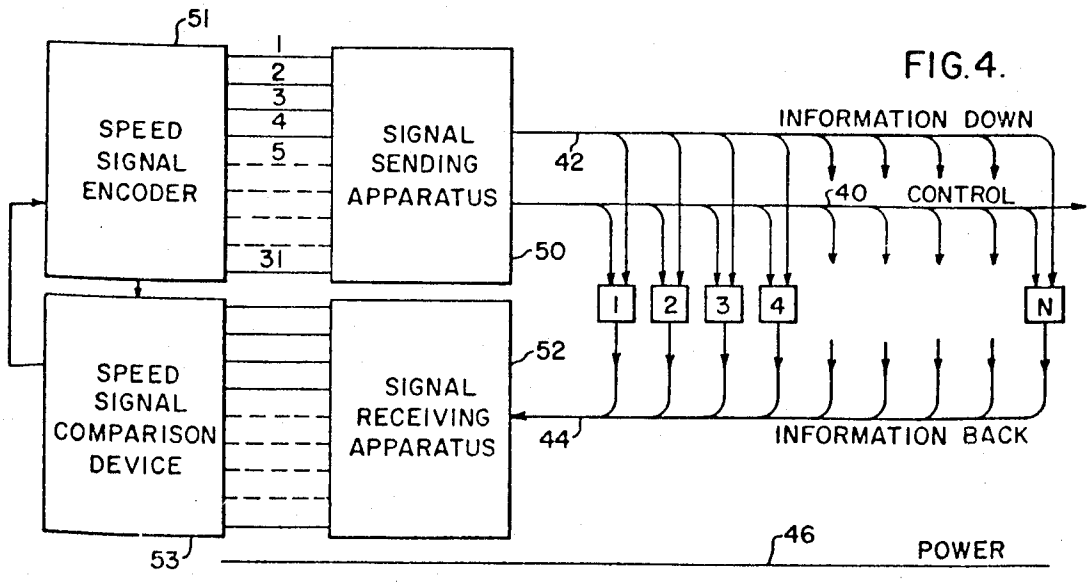


FIG. 4.

FIG.5.

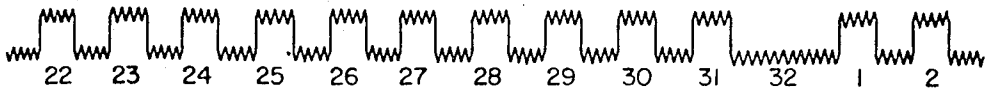


FIG.6.

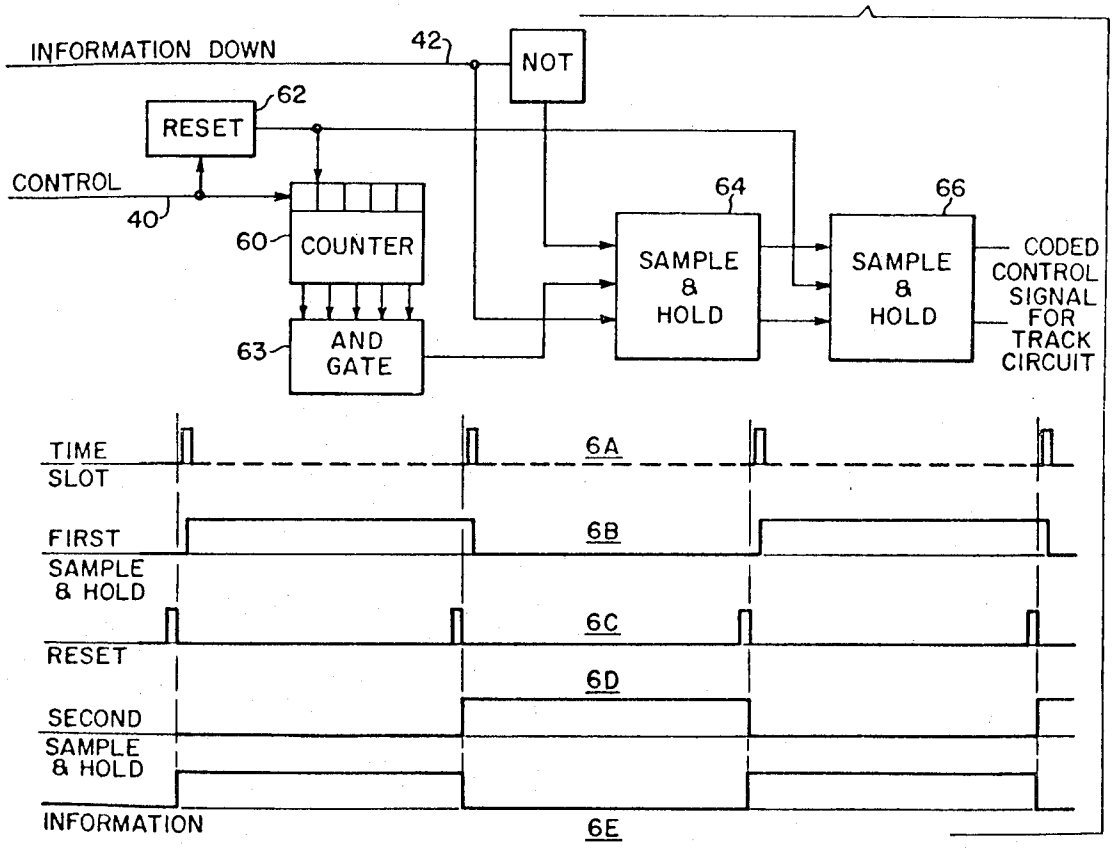
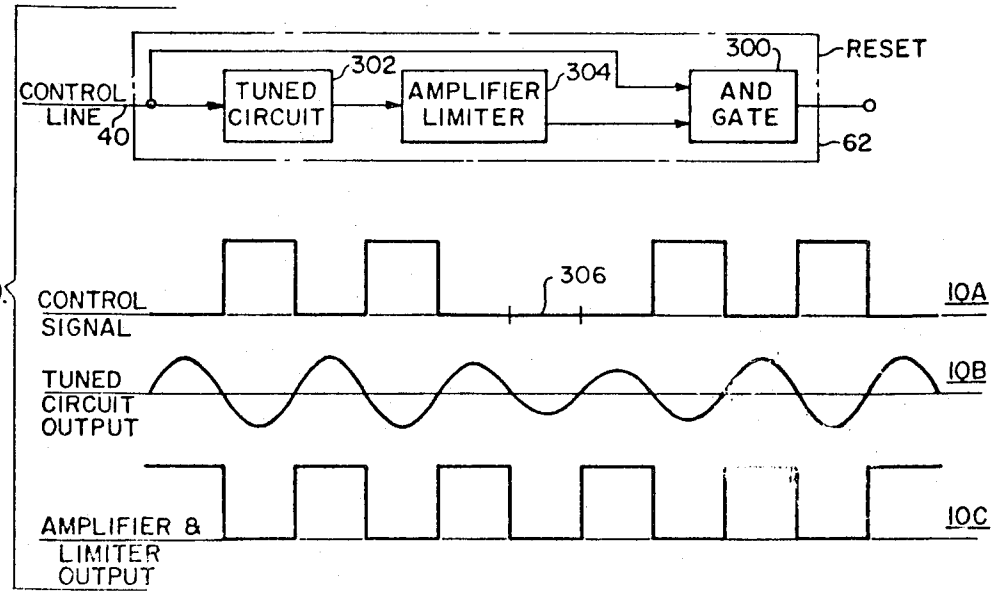


FIG.10.



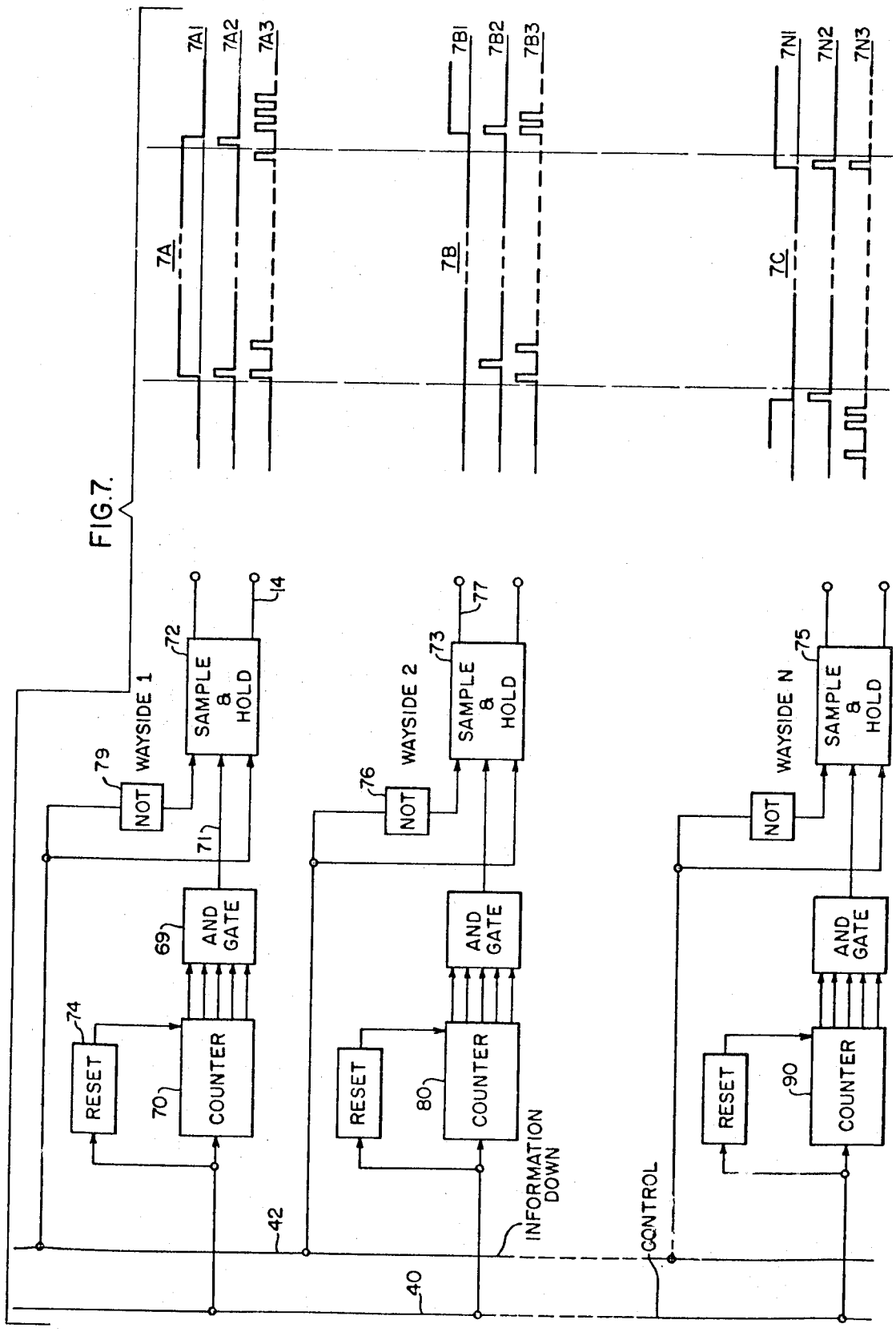

7A1
7A2
7A3
7A
7B1
7B2
7B3
7B
7N1
7N2
7N3
7C
WAYSIDE 1
WAYSIDE 2
WAYSIDE N
SAMPLE & HOLD
NOT
AND GATE
COUNTER
RESET
INFORMATION DOWN
CONTROL
14
42
40
71
69
70
74
72
73
75
76
77
79
80
90

FIG. 7.

FIG. 8.

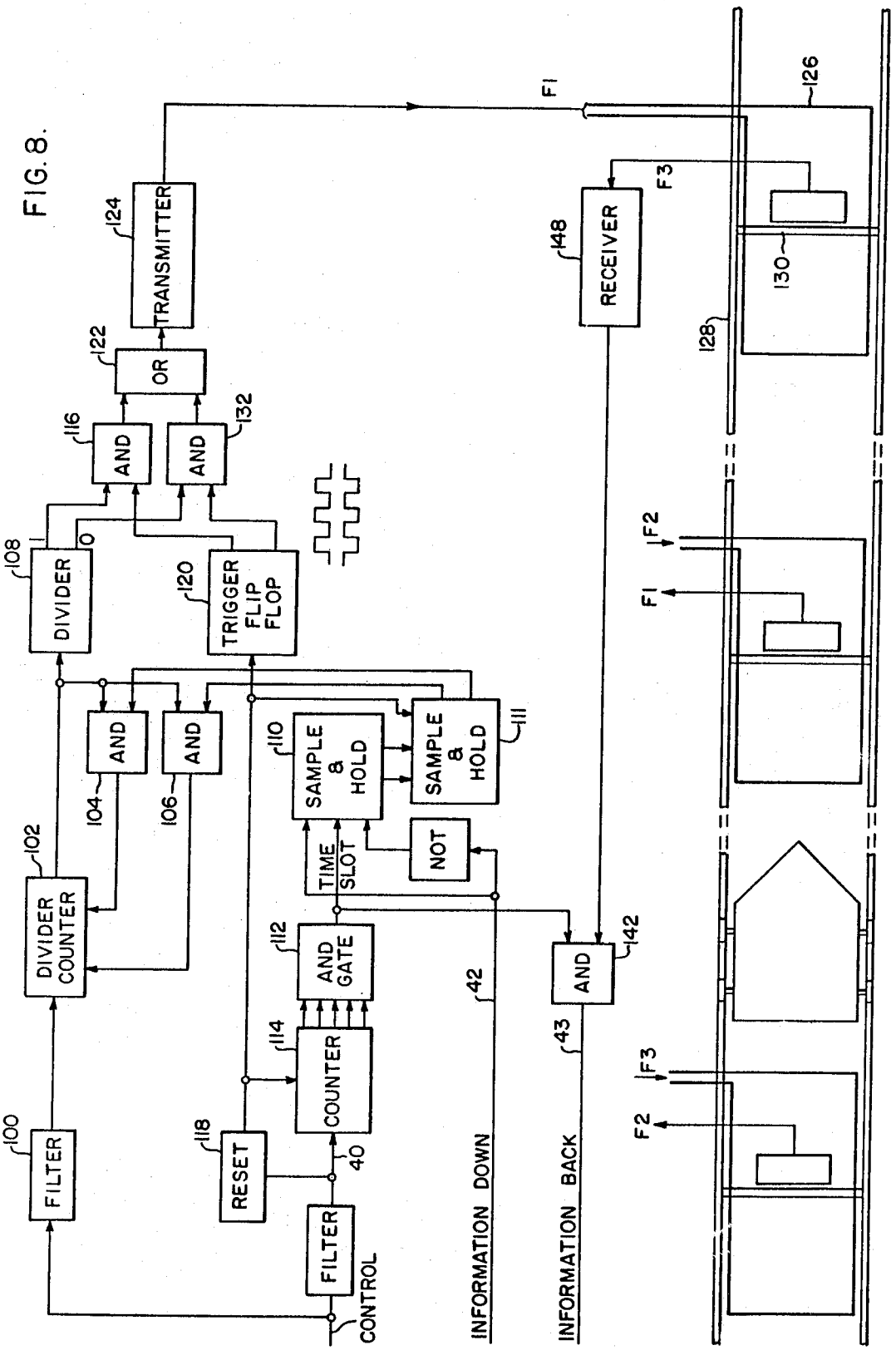
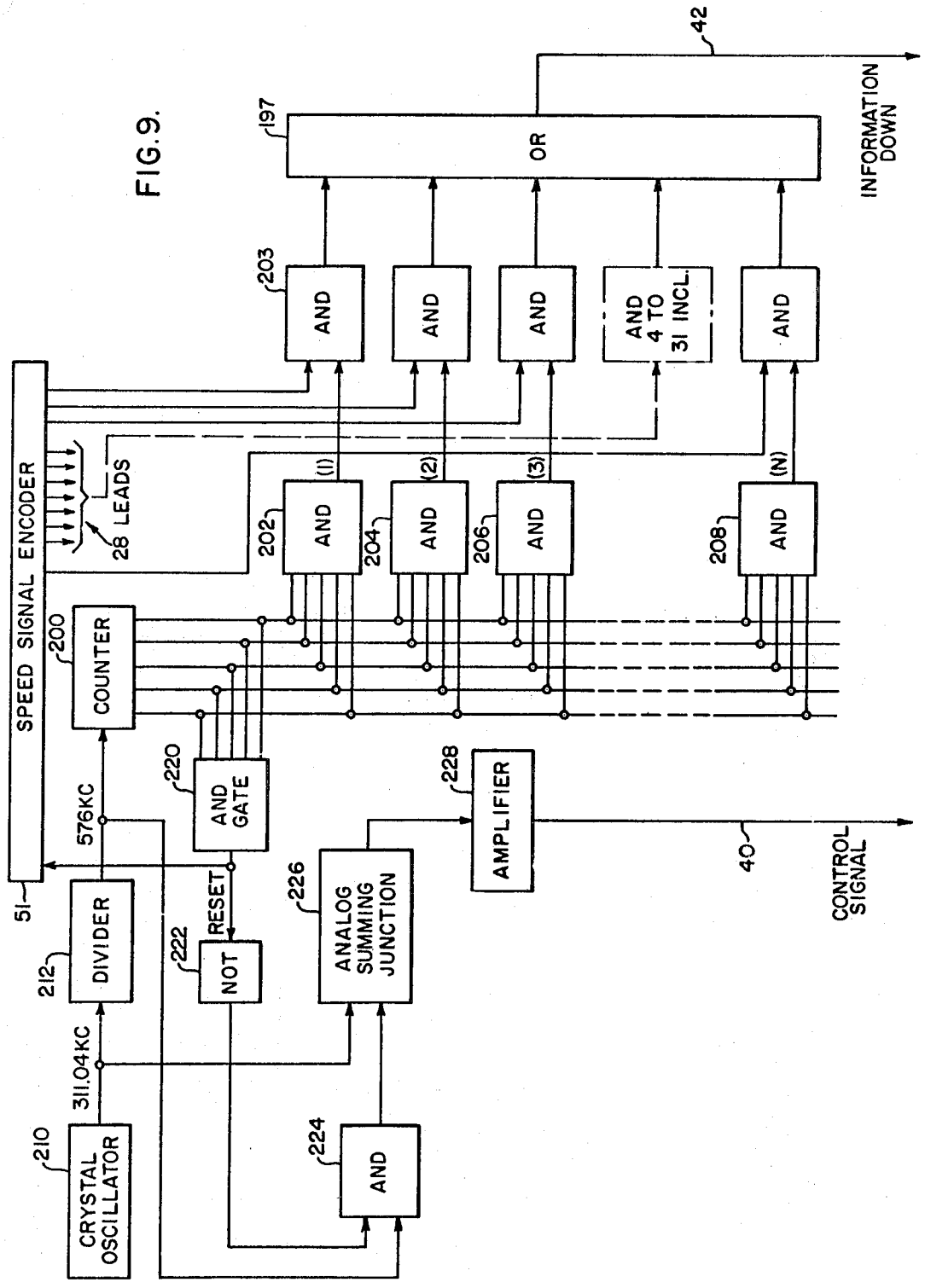

F1
126
TRANSMITTER
124
OR
122
AND
116
AND
132
DIVIDER
108
TRIGGER FLIP FLOP
120
AND
104
AND
106
DIVIDER COUNTER
102
FILTER
100
RESET
118
COUNTER
114
AND GATE
112
SAMPLE & HOLD
110
SAMPLE & HOLD
111
NOT
TIME SLOT
40
FILTER
CONTROL
INFORMATION DOWN
42
AND
142
INFORMATION BACK
43
RECEIVER
148
F3
130
128
F2
F1
F3
F2

FIG. 9.


42
INFORMATION DOWN
197
OR
203
AND
AND
AND
AND 4 TO 31 INCL.
AND
SPEED SIGNAL ENCODER
28 LEADS
(1)
(2)
(3)
(N)
202
AND
204
AND
206
AND
208
AND
200
COUNTER
220
AND GATE
228
AMPLIFIER
576KC
51
RESET
226
ANALOG SUMMING JUNCTION
40
CONTROL SIGNAL
212
DIVIDER
222
NOT
311.04KC
210
CRYSTAL OSCILLATOR
224
AND

MULTIPLEX CONTROL SYSTEM FOR CONTROLLING THE OPERATION OF A PLURALITY OF STATIONS

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. Pat. No. 3,593,022 "Control Of A Vehicle Along A Path Divided Into A Plurality Of Signal Blocks", application Ser. No. 762,563, filed Sept. 25, 1968.

BACKGROUND OF THE INVENTION

This invention relates to a multiplex control system applicable to the control of a vehicle along a path divided into a plurality of signal blocks. In certain broader aspects it relates to multiplex system of utility in any situation where dangerous failure modes must be avoided. It also generally relates to "telecontrol" of vehicle operation.

A train control system must fully meet the safety standards historical in the rapid transit and railroad industry. In addition, a centralized traffic control system is desired which is suitable for a high degree of automation far above the level of service commonly provided today and in addition the cost of this system has to be reasonable.

In the past systems for train control signalling purposes, insulated joints have been required between the respective track circuit blocks. Another provision of the prior art control systems has been to utilize signal frequency separation between respective track circuit blocks and to provide some means to separate the respective frequency signal energization of the so provided discrete track circuit blocks.

SUMMARY OF THE INVENTION

In accordance with the present invention a multiplex control system such as a train control signalling system or the like is provided for the transmission of information signals such as speed command signals from separate wayside stations to each of an associated group of isolated track circuit blocks, and for the transmission of train position detection signals back from those track circuit blocks to the wayside station associated with a given group of said track circuit blocks. A time division multiplexing of these signals is provided in conjunction with limited number of conductors between each wayside station and a central control station. All coded speed command signals and train position detection signals change at the same time to increase the system synchronism or continuity. For controlling train movement in close proximity and within 100 feet or so of each passenger station, which can also be a wayside station, direct wiring of signals is provided, and for greater distances from each station the control signals are multiplexed to each track circuit block.

For each wayside station, up to 32 track circuit blocks are controlled in the illustrative example herein given, but it should be understood that 64 or 128 or other multiples of these values could be readily accommodated, by simple modification of the apparatus, if desired. Each control signal has six respectively reverse phased bits of information and is operative with three different signal frequencies such that 18 bits per second of information is sent to each of up to 32 track circuit blocks, with the 32nd bit position being used for synchronization and reset purposes. The train control information is supplied at the rate of 576 bits per second to the signalling system. A ZERO bit signal has a voltage of 0 volts and a ONE bit signal has a voltage of 12 volts. The coded speed command signals and the coded position detection signals are induced to flow in the track rails, which have a generally undesirable signal to noise characteristic such that crystal controlled signallying is desirable. A 311.04 kilocycle crystal oscillator signal is provided by a suitable oscillator at each wayside station, and this signal is divided by 540 to provide a 576 cycle/sec. multiplex bit signal; the latter signal is further divided by the number of available track circuit blocks 32 to yield an 18 cycle/sec. multiplex word signal. These three signals are then combined to be sent on one conductor as follows: the 18 cycle/sec. word signal is subtracted from the 576 cycle/sec. bit signal, and the 311.04 kilocycle oscillator signal is added to the result to provide an operation control signal.

For the purpose of providing an example, the following comma free coded speed command signals are illustrative of those that can be utilized with the present train control signalling system:

101111—80 MPH
100111—70 MPH
100011—50 MPH
101011—34 MPH
100101—27 MPH
101001—18 MPH
100000—12 MPH
100001—6 MPH
101000—0 MPH

In the course of the actual signal transmission reverse phasing of successive signal bits permits sensing aboard the train a bit rate to assist in decoding the train speed command signals.

The vehicle communication signals, such as vehicle speed command signals and vehicle presence detection signals, pass through a pair of conductors which can be the track rails if desired and which conductors are periodically short circuited by a low impedance conductor connected between those conductors to provide discrete signal blocks, and which are operative relative to the vehicle such that the vehicle as it moves along the support track member is effective to short-circuit or provide a low impedance path between these two signal conductors for the purpose of notifying the attendant control system of the actual position of the vehicle as it moves along the support structure.

It is contemplated in accordance with the present invention that both frequency and modulation phase operation will be applicable in reference to contiguous track circuit signal blocks. More specifically a plurality of three signal frequencies is provided to the signal blocks and in addition each frequency includes a six-bit command signal with the provision that between the adjacent signal blocks a phase shift takes place such that through the combination of three frequencies and six phase shifts it is possible to provide signal communication to eighteen track circuit blocks before it is necessary to repeat the signal characteristics.

In general, any given particular track circuit block receives the same frequency and phase shift speed command signal all the time. For example a particular track circuit block will receive signal frequency F-1, phase shift three and its associated receiver will be tuned to receive a signal at F-1 frequency and will feed

back the phase three frequency to the provided speed signal comparison circuit for comparison with the transmitted phase three speed command signal occurring at an 18 cycle per second rate. The neighboring track circuit blocks are supplied with a different frequency and a different phase shifted speed command signal arrangement such that for a combination of three signal frequencies and six phase shift arrangements 18 unique combinations of speed command signal can be provided to thereby permit a separation between identical signal transmission relative to the track circuit blocks of 18 track circuit blocks. Thusly, for the track circuit signal blocks operative with a given wayside multiplex station, the first track circuit signal block and the 19th could be energized with signal frequency F-1, phase one, the second and the 20th signal blocks could be energized by signal frequency F-2, phase one, the third and the 21st signal blocks could be energized with signal frequency F-3, phase one, the fourth and the 22nd signal blocks could be energized by F-1, phase two and so forth. This has been decided as a desired way to transmit the signals in a reliable and failsafe manner to the track circuit signal blocks. This provides the desired number of isolated orthogonal train vehicle speed control and position sensing channels, which channels are repeated only at separation distances large enough to assure fail-safe vehicle control and position sensing through adequate signal attenuation between two otherwise similar control signals for the purpose of avoiding erroneous vehicle control and position sensing information being received even under fault conditions, the number of different signal frequencies can be reduced to a small number such as three with the desired orthogonality between adjacent signal block channels operating at the same frequency being separated by orthogonal signal coding of the modulation impressed upon the transmission carrier. For this purpose comma free coded vehicle command signals are utilized, and are phase shifted relative to adjacent signal channels, to effect in this manner three signal frequencies and six phase shifts to provide adequate separation of the respective signal block channels.

The train vehicle carries a command signal receiver that senses the transmitted bits of the command signal in groups of six such bits, such that the entire vehicle command signal is thereby sensed and causes the vehicle to follow the desired speed of movement along the track. By the use of a wayside control station operative with up to 32 track circuit blocks the wayside control unit can monitor the movement of a vehicle moving in either a first direction along the track or the opposite direction along that same track, by sensing the effect of the train vehicle to short-circuit and thereby remove the detection of the provided vehicle speed command signal relative to a particular track circuit signal block within which the vehicle is positioned in relation to the position detecting signal receiver and its operation. A single central digital computer can be provided for an entire train control system and be operative with the required plurality of wayside control stations, with each said wayside control station operating entirely by itself to provide a programmed vehicle movement through the up to 32 track circuit blocks controlled by that wayside station control unit, and cooperative with the central computer in regard to changing this predetermined vehicle movement pattern when the vehicle is within the particular group of track circuit signal blocks operative with any given wayside station control unit. In other words, the wayside station control provides vehicle speed command signals to each of its track circuit blocks in accordance with a predetermined vehicle movement pattern when traveling through that group of track circuit blocks, and in the event of a need to reduce the travel speed of a given vehicle for the reason that several vehicles are tied up ahead of the vehicle or for the reason that a construction program is under way somewhere along the proposed travel path of that vehicle, then the central computer can override and reduce the movement speed of the train vehicle when passing through that particular group of track circuits or when passing through any one or more track circuits within that group of track circuits. Thusly each wayside station control unit operates as a signal multiplex center relative to its particular group of up to 32 track circuit blocks, and it has its own crystal oscillator and signal operation in accordance with the present invention. The central computer operates with as many as these wayside station multiplex control units as are necessary to provide the desired number of track circuit blocks for the entire system, and can be operative to change the predetermined speed command signal pattern provided by any wayside station multiplex control unit in response to happenings within a different wayside station territory. Additional data transmission equipment is provided to interface one group of track circuit blocks and the associated wayside station multiplex control unit with the next adjacent group of track circuit signal blocks and their associated wayside station multiplex control unit. Ech of these groups of track circuit signal blocks is not correlated with the other groups of track circuit signal blocks, however their frequencies are chosen in advance and are generally correlated through inherent operation of the crystal oscillator control. In addition the signal multiplex control system of the present invention can be operated as one small group of track circuit signal blocks within another unrelated type of control system and receive an overriding vehicle speed command pattern to change its own predetermined speed command pattern if desired. It would be desirable to have certain information from adjacent control systems to correlate the operation of the signal multiplex system in accordance with the present invention. The central computer can provide more restrictive running where desired, however, it cannot cause any given group of track circuit signal blocks to provide a greater vehicle speed pattern than is in accordance with the predetermined and scheduled speed pattern for that group of track circuit blocks. Thusly the maximum speed limits are provided by each multiplex control system in accordance with the present invention, unless the central control unit overrides and restricts to reduce the vehicle speed through any group of track circuit signal blocks or one or more track circuit signal blocks within any group of track circuit signal blocks. The local wayside control unit has preset into its scheduling the maximum and desired vehicle travel speed through each of its associated track circuit signal blocks. If a given wayside control unit senses the occupancy of one of its track circuit blocks ahead of where a particular train vehicle is located, then the wayside control can provide a suitable control signal, such as a zero speed command signal, to the train in adquate time to reduce the speed of the particular controlled train vehicle to prevent a collision by a

predetermined safe distance margin. If the track circuit blocks ahead of a given vehicle are not occupied, and no restrictive speed pattern is provided by the central computer, then the wayside control station provides speed command signals to the train vehicle to cause it to move through each particular track circuit block at the desired optimum travel speed. The wayside control unit is a station multiplex center. The provision of the multiplex system adds flexibility to the control system because it is so readily chageable in relation to track occupancy ahead of a particular train vehicle, and further so changeable relative to construction efforts along the track, the sensing of a landslide which would cause an obstruction to the train vehicle at a location ahead of its movement, and things of this type.

BRIEF DESCRIPTION OF THE DRAWINGS

In FIG. 1 there is shown a prior art information transmission arrangement for sending train control signals through individual conductors directely to selected track circuit blocks.

In FIG. 2 there is generally shown the improved signal transmission arrangement of the present invention.

In FIG. 3 there is shown the signal conductor arrangement for sending the multiplexed control signals between a wayside station and individual track circuit blocks.

In FIG. 4 there is illustrated the general signal transmission arrangement of a wayside station operative with a plurality of track circuit signal blocks.

In FIG. 5 there is shown the information signal waveform sent down the control conductor between a wayside station and the individual track circuit blocks.

In FIG. 6, including curves 6A, 6B, 6C, 6D and 6E, there is illustrated one circuit arrangement utilized and its function to provide the desired time slot control signal and information down signal separation function.

In FIG. 7, including curves 7A, 7B and 7N, there is schematically shown the speed command signal decoding circuit and its function of the present invention for a plurality of track circuit locations.

In FIG. 8 there is shown the speed command signal decoding circuit arrangement for inducing the speed command signals into a given track circuit block and the circuit arrangement for sensing the vehicle position detecting signal.

In FIG. 9 there is shown the centrally located control station apparatus provided in accordance with the teachings of the present invention.

In FIG. 10 there is shown the reset signal generating circuit for the apparatus of FIGS. 6, 7 and 8.

One purpose of the signal multiplexing system of the present invention is to transmit and receive over a total of four pairs of conductors, in a very reliable manner, all the required train control signals between some wayside station location and each of a plurality of remote signal block locations serving individual track circuit transmitters and receivers, train identification receivers, programmed stop transmitters and the like. These signals can include train movement speed commands, train presence signals, identification information signals, synchronization pulses, a crystal controlled frequency standard, and power. The four pairs of conductors provide respective paths in this regard for information down, information back, control signals and the power. The prior art train control signalling system teachings would provide a multiplicity of individual cables from the central location to each of the remote locations to carry the individual signals; since the distance involved amounts to several miles this latter approach becomes much greater in cost and the cable density at the source becomes a problem.

For the cost, the signal multiplex concept gives a lot more flexibility and more ability to control the movement of the train vehicle. For monitoring the movement of the train vehicle in respectively opposite directions a duplicate of a hardwired train control system would be required. The addition of another wayside station location is easier with a multiplex control system or another program stop transmitter. If extra time slots are available, additional operational functions can readily be included during a given scanning cycle of the multiplex control unit. In general, a typical application will utilize only 25 of the 32 signal time slots for controlling vehicle movement through respective track circuit signal blocks, and the additional six or seven time slot position would then be available for additional communication functions that may be required. If additional time slot positions are available, and not being used for directly controlling the vehicle movement, these additional time slots can be tied into an additional piece of sensing equipment for example positioned along the track for the purpose of detecting a landslide or some other desired bit of information relative to the operation of the transit system without requiring the running of an additional hardwire circuit from the remote position back to the wayside control station. Any information in this regard can be transmitted, if the bandwidth requirements of this information are low enough, for utilizing the available time slots in the provided multiplex control ssystem. A rock fall sensing device or the like could be an example of this type of information. The needed bandwidth for returning this type of information is very low. A hardwire system would require the provision of additional wires including the cost of installations plus the cost of the wire, and many thousands of feet of distance may be involved for providing this hardwire communication. Thusly a substantial large savings of investment and cost can be taken advantage of by utilizing the already available time slot signal communication positions.

The present signal multiplex control system has as an objective to provide a fail-safe train control system suitable for the movement of passengers and valuable property. There is an integration between the manner in which the coded signals are supplied to the train control the movement of the train and the way in which the signals are multiplexed back to the wayside control station. The combination of the comma free coded signals and the bit by bit phase reversal operation between successively transmitted bits of a given train control signal enhances the fail-safe operation, when considered in conjunction with the operation of the speed and coding apparatus to be sensitive to and make a comparison between the transmitted signal and the signal which is fed back for a comparison with a transmitted signal, with the operation of the speed encoding unit being controlled in accordance with this signal comparison operation, such that should a transmitted signal not compare to a received signal or should a signal not be received at all to indicate the occupancy of a given track circuit block by a train vehicle or some failure in the signal transmission operation, the apparatus is operative to then provide a reduced speed command to the

train vehicle or a zero speed command. The multiplex concept allows a more economical application of this signalling system.

The prior art frequency variable type of a signalling system would not be readily applicable to a signal multiplex concept in accordance with the present invention. The very early prior art apparatus utilized only three speeds zero, middle and fast. This is typically done by a carrier which is modulated at 75 cycles a minute or 120 cycles a minute; this provides in effect a modulation of on and off, and no signal at all is 0 speed. This can be extended by going to 80 cycles a minute, 270 cycles a minute, and so forth to give more speed signals. With the number of speeds required for a modern transit system, the prior art approach becomes hopelessly saturated in terms of the available frequency spectrum, because of the great difficulty of separation of signals due to harmonics and lower frequencies and the like. For example a 75 cycle signal has harmonics at 150, 225, 300, 375 and so forth and this makes it extremely difficult to separate the respectively different frequencies which are utilized. Additionally the harmonics of the AC power system utilized to energize the signalling system must be separated. The number of freqfencies required do not bear a simple synchronous relationship one to the other and the required different frequencies for the various desired speed command signals become difficult to accommodate. With a bit rate of 18 cycles a second, the present control apparatus could readily code 1 cycle a second, 2 cycles a second, 3 cycles a second, 6 cycles a second, 9 cycles a second and 18 cycles a second. Additionally it is desired to keep the various bandwidth requirements to the bare minimum. The 18 cycle per second bit rate is a low frequency signal which does not present very difficult bandwidth problems.

The train control system requirements are typically that the control system be in command of a given train vehicle with a drop out of no more than one second. The Q of a narrow bandwidth filter is so high that it would take about 10 seconds for the vehicle control to be effected, since a filter having a one cycle bandwidth requires about 10 seconds to build up to the required signal level and it is not feasible to allow the train to operate for a period of 10 seconds with no command correlation relative to the control system. It also takes 10 seconds for the given filter to die down in signal intensity and for this reason the bandwidths of the respective signal filters must be widened such that a Q not much greater than 1 or 2 is provided and this requires frequency differences across a substantial frequency spectrum in order to get the desired 8 or 9 speed command communication channels desired for the train vehicle. The primary requirement is to sense track occupancy in addition to providing desired speed command signals to the train. In the prior art this track occupancy was sensed by laying a second control system carrier on top of the speed command control system carrier and a first track circuit had a first carrier filter requirement, the next adjacent track circuit had a different carrier frequency filter requirement and 10 or 12 different carriers were required to get the desired separation between the respective track circuits. In the present control system the track occupancy is sensed through a signal feedback operation and a signal comparison is made in relation to the transmitted speed command signal as compared to the feedback received vehicle presence signal, and if the two properly compare the system continues to transmit the prescheduled vehicle speed command signals. Thusly the present multiplex control system requires only one transmitter instead of two, and the total required bandwidth of the system has been narrowed through the use of the comma free signal coding system and additionally an improved capability for a multiplicity of speed command signals up to 8 or 9 such signals.

The comma free speed command codes have advantages for utilization in conjunction with the present signal multiplexing system, which advantages are related to the greater reliability of digital signal communication systems and the provision of the phase reversal between successive bits of the 6 bit, comma free speed command word signals, and the ability to operate a train control system in a fail-safe manner without the requirement for signal synchronization to indicate the transmission of the respective speed command word signals. The signal multiplexing concept enables the train control system to be implemented with a substantially decreased amount of wire between the respective wayside control stations and the associated track circuit blocks. The prior art has continuously taught that a singal multiplexing system is not reliable enough for a fail-safe train control application. The vehicle occupancy feedback signals of the present invention provide the fail-safe reliability required in the operation of the present multiplex system. Unless there is fed back for comparison the "identical" speed command signal that has been transmitted to a particular circuit signal block, the signal comparison operation will not permit the train vehicles to move into that particular track circuit signal block in that a vehicle occupancy condition is signaled to the train control. It is similar to a servomechanism theory application, where there is a forward loop having uncertain and unstable characteristics, and the feedback signal comparison monitors the operation of the unknown and unstable forward loop. The multiplex signal transmitter sends a signal down through the plurality of track circuit blocks and there are all sorts of opportunities for a failure of the communication, and by comparing the signal that it sent with the signal that is received back, it is not possible to get the correct signal back unless the forward loop is operating properly. This is substantially different than prior art systems using one set of frequencies for track occupancy detection and another set of frequencies for sending speed commands to the train vehicle, and no feedback of the signals transmitted to the train in regard to speed command is provided in the prior art. In the present system, the same speed command signals are utilized for the purpose of controlling the movement of the train vehicle through the respective track circuit blocks and in addition, for detecting the presence of a train vehicle within any of those track circuit blocks. We know what signal is sent and we know what signal should come back, and if it does not come back, the assumption is made that the track circuit signal block in question is occupied by a vehicle and therefore a succeeding vehicle should be reduced in speed and if necessary prevented from entering that particular track circuit signal block. A signalling circuit failure is considered in the same manner as a vehicle occupancy, such that the succeeding train vehicle is not permitted to enter a track circuit signal block where a signal failure has occurred in that the present control system in-

terprets this to be a previous vehicle occupancy condition.

For a rubber tired transit system, it is contemplated that a pair of parallel vehicle grounding wires can be placed parallel to the vehicle track, which two parallel grounding wires can be short-circuited by a suitable brush connector carried by the train vehicle in a manner substantially similar to the short-circuiting effect provided by a steel wheeled train vehicle operating upon electrically conductive steel track members. This has substantial advantage over an active signal transmitter carried by each train vehicle for sending back to a wayside control station a signal which can be sensed and utilized to indicate the position of that particular train vehicle. The present control system utilizing the time slot position signal multiplex transmission concept in conjunction with the comma free coded speed command signals provides an integrated train control system which is reliable and has substantial advantage over prior art hardwired train control systems particularly for a large transit system application where a substantial number such as 2,000 track circuit signal blocks are employed and communication with each of these track circuit signal blocks is desired.

The antennas coupled to the vehicle track are provided on each side of the individual short-circuiting conductors which define the respective ends of the individual track circuit signal blocks. Therefore, the signal frequency is coupled into each of the track circuit signal blocks adjacent to any given antenna. For this reason, it is feasible to provide signal receivers tuned to the particular frequency and signal phase shift which is introduced at any given antenna at the location of the next adjacent short-circuiting conductor on either side of that particular antenna.

In FIG. **1** there is shown a wayside control station **10** which is direct wired to each of a plurality of track circuit signal block control devices **12, 14, 16, 18, 20, 22** and **24.** It should be understood that the station **10,** can be operative with any suitable desired number of such control devices. Further it should be noted that this arrangement requires a direct connecting multiple conductor between the station **10** and each of the track circuit signal block control devices. The track circuit signal blocks are here defined by low impedance conductors **25** respectively connected between the train rails **26** and **28** at each end of the individual track circuit signal blocks as generally shown in FIG. **1.**

In FIG. **2** there is shown one embodiment of the signal communication system in accordance with the present invention wherein the wayside control station **10** contains signal communication equipment which is cooperative with each of the control devices **12, 14, 16, 18, 20, 22** and **24.** Each wayside station generates coded speed command signals for each of its associated track circuit signal blocks based on information coming back from each others track circuit signal block and from the central control station. The control device **12** is operative at the location of a low impedance conductor **30,** the control device **14** is operative at the location of the low impedance conductor **32,** the control device **16** is operative at the location of the low impedance conductor **34,** and so forth, such that a track circuit signal block is defined between the respective low impedance conductors **30** and **32** and another track circuit signal block is defined between the low impedance conductors **32** and **34** and so forth.

In FIG. **3** there is shown a suitable grounded shield **38** which surrounds the pair of control signal conductors **40,** the pair of information down signal conductors **42,** the pair of information back signal conductors **44** and the pair of power conductors **46.** The multiplexed signal connection between a wayside station and each of the associated control devices **12, 14, 16, 18, 20, 22** and **24** as shown in FIG. **2** could comprise a signal transmission conductor arrangement as shown in FIG. **3.**

In FIG. **4** there is generally shown a wayside station multiplex signal sending apparatus **50** operative with the control signal conductors **40,** and the information down signal conductors **42,** the information back signal conductors **44,** and a multiplex signal receiving apparatus **52.** This signal sending apparatus **50** and the signal receiving apparatus **52** would be located at a wayside control station **10,** such as shown in FIG. **2.** The multiplex signal sending apparatus **50** sends a plurality of coded vehicle speed command signals for each of up to **32** track circuit signal blocks in a time division multiplex arrangement such that for a first time division period one bit of the coded vehicle command signal for the first track circuit signal block **1** is sent, and then for the next succeeding second time period one bit of the coded vehicle command signal for the second track circuit signal block **2** is sent, and so forth until the **32**nd time period when a synchronizing or reset signal is sent for coordinating the operation of the signal transmission system. The speed signal encoder **51** provides the programmed in advance scheduled train vehicle speed command signals for controllng train vehicle movement in the respective track circuit signal blocks. The speed signal comparison circuit **53** senses the received feedback train position detection signals, to sense train vehicle occupied track circuit signal blocks, by comparing on a bit by bit basis the speed command signal sent to each particular track circuit signal block with the signal received back from the same track circuit signal block; the presence of a train vehicle short circuits the signal information to prevent the signal block receiver from returning over the information back line **44** any feedback signal information from an occupied track circuit signal block.

The signal comparison device **53,** for determination of vehicle occupancy purposes, includes the necessary time delay provided between the initial transmission of a given speed comannd signal bit to a track circuit block and the feedback return of this same speed signal bit within the speed signal comparison device **53.** A typical signal bit delay between two and three bits has been found in actual practice to be required to match properly the signals for comparison. In the event the transmitted signal bit does not compare with the feedback return signal bit, then the speed signal comparison device **53** interprets this as a vehicle occupied track circuit block condition or a failure of the system in either of which cases it causes the speed signal encoder **51** to transmit an appropriate vehicle speed command signal for safe operation of the train system. This speed comparison operation in effect controls what speed should be sent to each of the track circuit blocks. The use of FM signals enables what is called an FM capture effect to occur, with the FM receivers inherently picking up the stronger of two received signals. In the prior art AM receiver operations, a 50 db signal strength difference may be required before the receiver preferred one sig-

nal over the other. In the operation of an FM receiver, only **10** db signal strength difference is required and this permits desirable signal discrimination relative to undesired signals from adjacent track circuit blocks which undesired signals might happen to be received by the FM receiver and which are not desired to pass through the FM receiver and erroneously inform the wayside station control equipment in regard to track circuit vehicle occupancy and the like.

In FIG. **5** there is generally shown the multiplex control signal that is transmitted over the control line **40,** shown in FIG. **4,** and which control signal includes bits of information occurring at the rate of 576 cycles/sec., or 576 signal bits per second, upon which there is summed a 311.04 kilocycles crystal oscillator signal. The time slot bit signals **22** through **31** are shown out of the total or **32** that is transmitted, with the 32nd bit position being omitted as shown for system synchronization and reset purposes, followed by the 1st and 2nd time slot bit signal for the next successive time slot positions.

In FIG. **6** there is shown the control signal line **40** and the information down signal line **42** supplying information to the speed command signal decoding portion of a typical track circuit signal block control device. The control signal line **40** supplies the signal waveform shown in FIG. **5** to the counter **60,** with the counter **60** being operative like a shift register, to receive the successive signal bits. The reset circuit **62** is operative during the 32nd bit position to reset the counter **60** at a zero count. The sensor gate **63** comprises in effect an AND circuit selectively connected to be responsive to a selected status of the counter **60**; for example, for the first track circuit block, when the first time slot bit signal is received by the counter **60** and a ONE in binary form is stored by the counter an output signal will be supplied by the selectively wired sensor gate **63** to enable the sample and hold circuit **64** for obtaining from the information down signal line **42** whatever bit of speed command signal information either a ONE or a ZERO, is being transmitted during the first time slot position for the first track circuit signal block. This first signal bit of information from the information down line **42,** for example a ONE as shown by curve **6E,** during the first time slot, as shown by curve **6A,** passes through the sample and hold circuit **64** to set the sample and hold flip-flop **66** in a corresponding ONE position, as shown by curve **6B.** With the first information bit from the line **42** being a ONE, the waveform **6D** shows the memory function of the sample and hold clocked flip-flop **66** to receive this information bit, when the reset pulse occurs as shown by curve **6C,** and to change its state accordingly. The wave-form **6A** shows the output signal from the sensor gate **63,** which is selectively wired to be responsive only to the storage of a ONE in binary form or 00001 within the counter **60.** The sensor gate **63** operates in this regard in a manner similar to the well known function of an AND gate, sensing the ONE output of the first stage flip-flop and sensing the ZERO output of the flip-flops for the other stages. The output signal for time slot (1) shown as waveform **6A** is applied to enable the sample and hold circuit **64,** which in function is a clocked flip-flop, such that a sampling of the information signal bit carried by the information down line **42,** for example a ONE as shown by curve **6E,** occurs by operation of the sample and hold **64** to provide the output as shown in waveform **6B.** The reset circuit **62** provides the output waveform **6C** by operation that will be explained in greater detail in reference to FIG. **10,** and this latter output is applied to enable the sample and hold **66** such that the output waveform **6d** results. The second sample and hold **66** is provided such that the signal change for all track circuit signal blocks will occur together and thereby provide a simpler train control operation, which is due to the reset pulse being the same for all time slot position signals.

Since vehicle speed command information is sent to all the wayside locations for a given multiplex station on the same information down line **42,** it is necssary that each track circuit signal block location receive its speed command information only during its particular time slot. As shown in FIG. **7,** the appropriate time slot position signal is determined by the operation of the respective signal block counters, such as the counters **70, 80** and **90,** which sample the speed command information signal bits from the information down line **42,** when a predetermined number count of bit pulses have been received by their respective counters **60, 70** and **80.** The individual speed command information bit signal for each time slot position is stored in the associated flip-flop sample and hold circuit **72,** and corresponding respective sample and hold circuits for the other time slot positions, until all locations have similarly received their speed command information bit signal. Each reset circuit **74** at the "same time" senses the occurrence of the 32nd signal bit of control line **40** and operates to provide a reset signal. For the first signal block counter **70,** this reset pulse would reset the counter **70.** Each wayside location, as generally shown in FIG. **7,** performs a similar operation in its own assigned time slot. The respective track circuit signal blocks receive a speed command signal bit in accordance with the command signal information bit received and stored during the previous time slot signal bit time. Simultaneously the next set of speed command signal bits begin to pass down the information down line **42** to be stored in the first sample and hold circuits until all locations again modify their track circuit block signals as desired. Thus the transmission of one bit of the vehicle speed command signal to each of up to **32** track circuit signal block locations requires one multiplex cycle or word consisting of 32 multiplex bit signals. Since in this example each of the up to 32 track circuit block locations receives six bits of information per given speed command signal, at a rate of three commands per second, the overall multiplex rate is 18×32 or 576 speed command information bits per second.

The multiplex system control line **40** provides an absence of a pulse at the reset time slot, which is the 32nd time slot position. However, a pulse is generated during the 32nd time slot for reset purposes by the reset circuit **74** and corresponding other signal block reset circuits. The time slot pulses are provided for each of the other time slot positions, other than the 32nd position. At time slot one, the enable pulse on line **71** enables the sample and hold **72** to sense either a ONE or ZERO signal from the information down line **42.** If a ONE signal is provided the output of sample and hold **72** goes to a ONE as shown by curve **7A1.** In order for the signal shown by the curve **7A1** to go to a ZERO at time slot one, it requires ZERO information to be coming through on the information down line **42.** The time slot one signal is shown in curve **7A2,** and this time slot one

signal is applied to the sample and hold 72 over line 71. Curve 7A3 shows a ONE value information pulse is provided at the time slot one position such that the output of the sample and hold 72 goes high as shown in curve 7A1.

As shown in curve 7B1, the output of the sample and hold 73 remains at a low output condition in that the information line 42 contains a ZERO information signal at time slot two, corresponding to the second track circuit signal block, and this passes through the NOT circuit 76 to cause the sample and hold 73 to have a ZERO or low output signal at its output connection 77. Thusly, if a pulse is provided on the information line 42 for a given time slot position, the associated sample and hold is caused to have a high value output whereas if a ZERO pulse condition occurs on the information line at a particular time slot position, due to the provided inversion NOT circuit, the associated sample and hold has a ZERO or low output signal provided.

A ONE value information signal on the information down line 42 is applied to the bottom of the sample and hold 72 for the time slot one; and during the time slot position when an enabling pulse is supplied over the conductor 71 this causes the output of the sample and hold 72 to provide a ONE value output signal as shown in curve 7A1. If on the other hand, a ZERO value information signal occurs on the information down line 42, concurrent with the time slot are enabling pulse, the NOT circuit causes the sample and hold to have a low level output signal. If the information down line 42, at the next occurrence of the time slot one enabling pulse, remains at a high value the output of the sample and hold similarly remains at a high value. Thusly, for each successive occurrence of the time slot enabling pulse applied by the AND gate 69 over the conductor 71 to the sample and hold 72, the signal value on the information down line 42 is thereby sampled, and if it is a ONE value signal a high level output is provided by the sample and hold 72. However, during the occurrence of a time slot one enabling pulse on the conductor 71 if the information down line 42 at this time has a ZERO value signal, the output of the sample and hold through operation of the NOT circuit 79 is changed to provide a low level output signal.

There is a similar circuit provided for each of the respective time slot signal positions, as generally shown in FIG. 7, with a second time slot operating circuit being shown and an N position time slot signal circuit being shown. If were desired in accordance with the present teachings to control the movement of a train vehicle in 25 track circuit signal blocks associated with a given multiplex station, 25 such circuits would be required. It can be desired to utilize the available time slot positions 26 through 31 for sensing the occurrence of a landslide or some other happening which should be sensed for the proper and reliable operation of the transit system.

The individual signal block command signal bit sensing circuits sample the information on the information down line 42, at the occurrence of its particular time slot enabling signal, and holds this information until the occurrence of the next succeeding time slot enabling signal at which time the information then preset on the information down line 42 is again sampled and held until the occurrence of its next similar time slot enabling signal. Thusly, the information down line signals would be the same for the three illustrated signal sampling circuits shown in FIG. 7, however, the time slot enabling signal senses for its associated signal block the occurrence of only the information signal bit present on the information down line 42 at the time of its own particular time slot signal. Thusly as shown in curve 7B3, for time slot circuit operative with the second signal block a ZERO information signal is present on the information down line 42 for the first illustrated multiplex time period so the output of the sample and hold 73 remains at a low output condition. The respective signal equipments shown in FIG. 7 are wayside located, with each of the signal sensing circuits being provided at the location of a particular track circuit signal block. The multiplex line traveling the length of the associated track circuit signal blocks operative with a given wayside control station is shown in the form of control line 40 and information down line 42. At the location of each track circuit signal block, one of the information signal bit sensing circuits as shown in FIG. 7 is provided. The 7N curves are for time slot 31. and the curve 7N1 indicates that the previous time slot signal occurred when the information down line 42 had a ONE signal on it and a ZERO signal has now been provided to cause the output of the sample and hold 75 to have a low level value.

The reset 74 does not influence the sample and hold circuit 72 other than to reset the counter 70 back to a ZERO count level, however, there is a succeeding sample and hold circuit as shown in FIG. 6 to which the reset 74 does apply an enable signal. This reset signal causes the respective vehicle command signal information signal bits which are supplied to the respective track circuits signal blocks associated with a given wayside location control station to all change signal values together. In other words, the signal bit supplied to everyone of the track circuit signals blocks is changed simultaneously in relation to a given wayside location control station.

The reason for leaving the pulse out rather than allowing the counter to count through 32 pulses and then reset is that if the reset generating circuit should fail a greater reliability of operation is provided in that there would be a shifting of stored signal information within the control line signal pulse counter due to the counter's ability to count 32 pulses and only 31 pulses of time slot information are transmitted for each speed signal bit. By leaving out the 32nd time slot position pulse this assures that the reset will occur at the 32nd time slot position, and further if the reset equipment should fail the counter will count the provided 31 pulses and will miss the 32nd time slot position since no pulse is provided and for the first pulse of the subsequent signal bit transmission the counter will count to 32 and then reset and if the particular time slot position is the fifth the counter will for the next cycle count the time slot four information and then time slot three and so forth which will result in meaningless information that can be sensed. Otherwise, if some equipment failure should occur there is a likelihood that the counter would sit on some time slot other than five, providing unauthorized information. This in turn could cause unsafe train control operation.

In reference to FIG. 8, the track vehicle presence is indicated by the feedback of signals picked up by the receivers associated with the respective track circuit signal blocks to indicate the respective unoccupied track circuit signal blocks. If a train vehicle is located

in a signal block no signal is fed back. These presence indicating signals are multiplexed back to the central control station. The same time slot that is used for multiplex information down transmission is used for retransmission of feedback signals on the information back line.

A more detailed block diagram of a typical wayside track circuit signal block control device is shown in FIG. **8.** The word and bit synchronization pulses are obtained from the control line **40.** After passing through the high pass filter **100,** the 311.04 kilohertz signal from the control line **40** is put into a divider counter **102** which provides out a predetermined one of three pairs of frequencies F-**1,** F-2 or F-3 each to have an output ONE or an output ZERO signal. The AND gates **104** and **106** operate to determine the selection of a ONE or a ZERO as will be later explained. The divider counter **102** in this regard operates as a well known feedback counter to generate a signal in conjunction with the divider **108.** For purposes of illustration, for an F-**1** frequency signal, a ONE will be provided at 5KHz and a ZERO will be provided at 8KHz; for an F-**2** frequency signal, a ONE will be provided at 6KHz and a ZERO will be provided at 9KHz; for an F-**3** frequency signal, a ONE will be provided at 7KHz and a ZERO will be provided at 10KHz. The divider **108** functions in general as a wave-shaping circuit.

Assuming the wayside track circuit signal block position for the circuit shown in FIG. **8** is the first time slot one location, such that the speed command signal bit supplied to the clocked flip-flop **110,** operative as a sample and hold device, is fed in when the flip-flop **110** is enabled by the time slot one signal from the logic gate **112** operative with the signal counter **114** in response to the first bit only after reset of the 576 cycle control signal supplied by the control line **40.** If the particular information down signal bit at this time had been a ONE, the following pulse will transfer this into sample and hold **111,** thereby enabling AND gate **106** to cause the divider **102** in conjunction with the divider **108** to supply, for example, the F-**1** frequency signal ONE at a frequency of 8KC to the AND gate **116.** Upon the occurrence of the 32nd bit or reset pulse on the control line **40,** the reset circuit **118** will provide an output signal to reset the counter **114,** to enable the second sample and hold **111** and to trigger the flip-flop **120** to energize the other input of AND gate **116** such that an F-**1** frequency ONE signal of 8KC is supplied through the OR gate **122** and transmitter **124** to energize the signal transmission antenna **126** operative with the track **128** and having the short circuit conductor **130** at the illustrated position relative to the antenna **126** so that substantially no current at frequency 8KC flows in the conductor **130** thereby. The following reset pulse will cause flip-flop **120** to enable AND gate **132,** thereby providing the opposite phase signal from divider **108** to the transmitter.

The reset circuit **118** is operative by applying the control signal, as shown in FIG. **10** to a resonant circuit which will ring through the absent or 32nd bit pulse, and the output from the resonant circuit is then squared to produce a second continuous signal. When this second continuous signal is compared to the original control signal in an AND gate, the output will be the 18 cycle per second reset pulses. Each reset pulse is used to reset the five bit counter **114** to ZERO at the beginning of each multiplex word, and this counter then begins to count the control signal bit pulses. The AND gate **112** is connected to respond when the counter reaches the predetermined count level corresponding to the assigned time slot. During this time slot, the output of the gate **112,** operative with the sample and hold flip-flop **110** samples the vehicle command information bit signal on the information down line **42** by enabling the flip-flop **110,** and this information bit signal is then stored in the flip-flop **110** for later use. After all the wayside signal block locations have responded to their respective vehicle command signal bits, during their assigned time slots in like manner, the next reset or 32nd bit pulse comes along. In addition to resetting the counter **114,** for each wayside location, to ZERO, it also transfers the stored bits from the flip-flop **110** to the succeeding sample and hold flip-flop **111** and then to one of the AND gate **104** or AND gate **106,** which will determine the ONE signal or ZERO signal frequency of the track signal supplied by divider **108** during the next muliplex cycle, and through operation of the trigger flip-flop **120** inverts the phase of the command signal bit from the divider **108.** In this way all track circuit blocks change their vehicle command signal bits simultaneously, even though they receive these signal bits sequentially.

The counter **114** that is used for time slot determination consists of five binary stages. The **32**nd bit pulse resets the counter **114** to zero, after which each successive control signal bit pulse increases the count by one. The AND gate **112** is connected to give an output at a selected count level corresponding to the respective assigned time slot in accordance with the circuit logic chosen for the AND gate **112.**

The 311.04 kilocycle carrier from the filter **100** is divided down to a predetermined one of the track signalling pairs of frequencies F-**1,** F-2 or F-3 by the feedback divider counter **102** as determined in advance. The logic including AND gates **104** and **106** must now select one of two possible frequencies for the respective ZERO and ONE outputs.

In this manner, one of the two resulting frequencies corresponding to ONE or ZERO signals is selected for transmission to the track, and reversed in phase by each reset pulse for synchronization purpuses on the train. This is accomplished by selecting twice the desired frequency from the divider **102** and then dividing by two once more in an additional divider **108.** The phase of the bits supplied to the track is shifted at each word transition by the AND gates **116** and **132** for timing information to the train by selecting alternate outputs from the flip-flop **120.** In addition since the signal from the counter **108** does not necessarily have a 50 percent duty cycle, this final division by two assures that this is so.

For the purpose of multiplex encoding, the output of the discriminator of the vehicle position sensing track receiver **148** consists of either a ONE or ZERO for each time slot period, which must be returned to the multiplex center over the information back line **44.** The receiver output from the receiver **148** is passed through the AND gate **142** for each enable pulse from the time slot counter **114** and AND gate **112** to read out the signal information from the track receiver **148** and to send onto the information back line **44** this signal information.

The antenna **126** shown in FIG. **8** gives bidirectional running capability in that it energizes the track circuit

blocks on either side of the short circuit connection **130** with a particular F-1 vehicle speed command signal. Any given receiver receives in one direction because of the frequency of the filters it has in it to operate with that receiver, and any given signal receiver can show whether its associated track circuit block is occupied or is not occupied regardless of the movement direction of the train vehicle which is occupying that track circuit block.

With a bit rate of 18 bits per second, three vehicle speed command signals per second can be sent from a wayside station location control unit to each of the associated track circuit signal blocks. The 18 bits per second cycle rate indicates the capacity of the present multiplex signal system to transmit 18 bits of information for each second, and if a given speed command signal has 6 bits then three such speed command signals can be transmitted to each track circuit block in each second of time. For one particular train control system where the present multiplex apparatus is intended for application, the train control requirement was that the wayside control unit could not be out of control of a given train vehicle for a longer period than one second of time. When the vehicle is going from one multiplex block of track circuit to the next adjacent multiplex block of track circuits, there can occur a transient loss of one word of speed command signal. Thusly, the transmitted speed command signal frequency rate must be at least two speed commands per second. However, in accordance with the present invention we have three complete speed command signals transmitted per second, and we could lose two of them. One multiplex territory to the next multiplex territory would be considered from one group of up to 32 track circuit signal blocks associated with a given wayside control station to the next adjacent group of 32 track circuit signal blocks associated with the next adjacent wayside control station. There is the further possibility of losing another word because of noise conditions, since there are random noise conditions throughout the entire train system. Thusly, with the present system one or two words of speed command can be lost due to noise or moving from one multiplex territory to the next adjacent multiplex territory and still provide the required one speed command to the train in each second of time. This gives a significant improvement in the reliability of the train control system. Upon losing contact with the train for over a period of one second, emergency braking is automatically applied in the train vehicle. The emergency braking condition of the train is irrevocable after 60 seconds of time and this allows an occurrence of random noise conditions and the like to now and then lose contact with the train for over a period of one second of time, and if communication with the train vehicle is lost for one or two or three seconds, the emergency braking would be applied; however, once the communication was reestablished the control of the vehicle would go out of emergency braking back to normal running condition. The application of emergency braking condition for one or tow or three seconds would probably not be physically noticed by the passengers carried by the train; it is questionable if emergency braking applied for one or two seconds would get through the jerk limit control which is also in operation relative to stopping the movement of a given train vehicle. Also, the train mass is so enormous that a change of control application of three or four second variation is probably not going to have a substantial noticeable effect upon the riding comfort of the passengers.

It should be further understood that it is not necessary to use a six bit comma free speed command signal, but rather a three bit signal or a four bit signal or a seven bit signal or other bit length coded speed command signals can be employed in accordance with the teachings of the present invention.

Referring to FIG. **8** the frequency F-**1**, F-**2** or F-**3** is "preset" by the divider counter **102** which is selected for example for a particular track circuit block. The divider counter **102** will be set to some frequency such as F-**1**, having a high and a low frequency in its frequency pair. The subsequent divider **108** is a simple divide by two divider circuit, such as a single stage flip-flop, to assure an on-off one-to-one ratio and this squares up to the one-to-one on-ff ratio. The second sample and hold **111** determines the dividing of the 311.04 kilocycle signal, with the second divider **108** squaring it up to a one-to-one on-off ratio. This provides an in phase signal and an out of phase signal from the respective outputs of the divider **108.** Each time a reset signal is provided by the reset circuit **118,** the trigger flip-flop **120** selected alternate AND gate **116** and **132** such that when a given reset pulse comes along, for example the high output signal is selected and the next reset pulse causes the low output signal to pass through the AND gates, a signal phase reversal occurs each time a reset pulse is provided. These phase reversed alternate output signals are applied through the amplifier **124,** which can be considered to comprise a signal transmitter, for the energization of the antenna **126.** To illustrate the operation of this circuitry, assume that an 80 mph speed signal were to be supplied to the antenna **126** including six bits of information of the arrangement 101111. For the first ONE signal bit, a 5 kilocycle signal would pass from the divider **108** through the AND circuit **116** to the transmitter amplifier **124** and energize the antenna **126.** The reset pulse would then occur for the next ZERO signal bit, such that an 8 kilocycle signal woudl pass through the AND gate **132** to the transmitter amplifier **124** and energize the antenna **126.** The third signal bit of this given speed command is a ONE which would again cause a 5 kilocycle signal to pass through the transmitter and amplifier **124** to energize the antenna **126.** The fourth, fifth and sixth signal bits are ONE to provide a group of 5 kilocycle signal bits. Without the provided phase reversals, the train equipment would have difficulty recognizing the occurrence of the respective signal bits and the complete six bit speed command signal. By changing the phase of the respective bits, this permits the train equipment to sense the respective signal bits. When going from a 5KC signal to an 8KC signal, this is readily detected in that a frequency change has occurred; however, for the last four signal bits of the 80 mph speed command signal there is no frequency change, and the phase reversal permits the train carried receiving equipment to sense the occurrence of the respective signal bits. Between the **101** signal bits the phase reversal is not required, however, it is more simple in the operation of the flip-flop circuit **120** to reverse phase for each respective signal bit whether needed or not, and this simplifies the receipt of the speed command signal by train carried equipment.

As shown in FIG. 9, as part of the station equipment there is provided a counter **200** and a multiplicity of sampling AND gates **202, 204, 206** and so forth through **208,** and with one AND gate being provided for each time slot being used. The bit and word pulses are derived from the 311.04 kilocycle oscillator **210** in the manner previously described; thus the wayside station multiplexer serving up to **32** remote track circuit blocks requires one oscillator **210,** one five bit counter **200,** one nine bit divider **212** and a maximum of **64** AND gates are required for interfacing with the control system. The sampling AND gate **202** is connected to the appropriate high and low level outputs of each stage to be operative to sense the count level of one within the counter **200,** and provides an output signal to the AND gate **203** which is connected to the speed command providing information down line **42** from the station, such tha the first time slot information bit from the speed signal encoder **51** is thereby passed through the AND gate **203** and the subsequent OR gate **197** to the information down line **42.** When this first time slot information bit is a ONE, the ONE signal will pass through AND gate **203.** When this first time slot information bit is a ZERO, the AND gate **203** will have no output signal so in effect a ZERO is supplied through the OR gate **197.** The other sampling time slot AND gates and associated AND gates are similarly operative for their respective time slot periods. In this manner the predetermined train vehicle speed patterns are established and sent to each signal block location.

When the counter **200** has a 32 count level, corresponding to the 32nd bit position, the AND gate **200** has been wired in a predetermined manner to sense the stage output signals so as to provide an output signal which is inverted by the NOT **222** such that AND gate **224** passes the 576 cycle output signal from the divider **212** except when the output signal corresponding to the 32nd time slot is supplied by the AND gate **220.** The analog summing junction **226** adds the 311.04 kilocycle signal from the oscillator **210** to the 576 cycle signal from the divider **212** and supplies the resulting control signal through the amplifier **228** to the control line **40.** Thusly when the AND gate **220** senses the 32nd time slot, the control line **40** receives no 576 cycle signal through the AND gate **224** and the 32nd time slot bit shown in FIG. **5** is thereby provided.

In FIG. **10** there is illustrated the operation of the reset circuit **62,** such as shown in FIG. **6.** In FIG. **10** there is shown the control line **40** which carries the control signal shown in waveform **10A.** This latter waveform is supplied to one input of the AND gate **300.** The waveform **10A** is also supplied to the tuned circuit **302,** where a ringing effect occurs when the 32nd bit pulse occurs as shown in waveform **10B,** and the amplifier **304,** which includes a limiter circuit, provides the output waveform **10C.** It should be noted at the position **306** of the 32nd time slot signal having a ZERO value in waveform **10A,** there occurs a reproduced signal bit in waveform **10C.** Due to the signal inversion which occurs because of signal delay, the AND gate **300** senses similar signals only during the 32nd bit signal time slot period to provide an output reset signal only during the 32nd bit signal of control waveform **10A.**

In one particular application of the present signalling control system, some 75 miles of double track rapid transit system is operative including 33 wayside stations which control the energization of approximately 2,000 track circuit blocks and 140 switches. In a signal block system of train control, speed commands for the individual train are communicated to any train vehicle positioned within a particular signal block through track circuits. The feedback of the speed control signals from the same track circuits is used for detecting the presence of a train vehicle in each block. Coded audio frequency speed command signals are sent to the track signal blocks for this purpose and then received back to indicate train vehicle presence.

A signal multiplex system utilizing four pairs of twisted conductors rather than a larger number of hardwire pairs is employed. The traffic control system receives back signal information in regard to each track circuit block occupancy as well as the condition of the provided switches, and delivers switch position control signals and train vehicle speed command signals to each train vehicle. A command signal terminal is located at each wayside station which communicates with up to 32 track circuit blocks associated with each wayside station. The individual track circuit blocks are driven by respective signal transmitters operative with the end of each circuit block. The track circuits operate in the audio frequency range and the signals are coupled into the individual track circuit blocks by a simple loop antenna system generally shown in FIG. **8** and placed about a low impedance conductor connected between the two rails of this location. The latter conductor is provided to simplify and balance the conductive of substantial traction currents within the rails. Receivers are inductively coupled to the short circuit conductors by means of small pickup coils or antennas which can if desired in addition be coupled to the rail at intermediate points between the shorting conductors for a secondary train control operation. The transmitter loop antenna and the receiver coils are essentially air core transformers. Two way running capability is achieved by extending the transmitter loops to both sides of the respective shorting conductors.

It was decided in the operation of the present system to utilize transmitted constant voltage signals and current signal detection, from the viewpoint of signal attenuation as a function of distance, which is implemented by the transmitter loops in the small detection coils and the short circuit conductors between the rails; this is compared to the various combinations of constant voltage signal transmission, constant current signal transmission, track signal voltage sensing and track signal current sensing that could otherwise be employed. This permits a longer track circuit signal block with a given degree of assurance that the system will operate properly over the full range of valid operation conditions such as dry and wet track conditions.

The transmitter is modulated with frequency shift modulation, which offers the considerable advantage that useful information is transmitted all of the time instead of leaving the receiver with no signal half of the time, and during which time the receiver would otherwise be highly susceptible to niose conditions. Frequency shift keying provides a signal which can be noise reduced through limiting.

The frequency shift modulation information signal is carried by an information down line which communicates in serial bit form all of the desired vehicle command signal information to each of the respective track circuit blocks. Each block location has its own assigned

time slot which is built into the translating equipment. This time slot signal enables the information down line to deliver its information into a memory circuit where it is stored for the duration of the one signal bit code cycle. The information that is delivered to the memory tells the wayside transmitter to go to either of two frequencies, and in this way the actual shift of frequency of each track circuit block transmitter is controlled from the wayside station and can be coded in its own unique way so as to communicate the desired speed signals to the train vehicle. The information down line contains the speed command signal, and the control line contains a predetermined code including synchronizing pulses, which latter signal consist of a train of 31 successive pulses followed by a reset or synchronizing pulse followed by 31 more information pulses and so on. The space between the 31st and the 1st pulse is for synchronizing and reset purposes so that the proper time is thereby selected. A time slot select circuit counts these pulses and at its prewired count level delivers a signal to enable the pulse occurring in the speed command information down line through to the memory circuit which is then set at either a ONE or a ZERO depending on the information pulse which occurs on the information down line at the time assigned to the particular block location. This memory circuit will not change until the cycle is repeated during the next 31 pulses, with the signal stored in memory being used to shift the frequency of the local transmitter between its two assigned frequencies. In the actual operation of the multiplex system it is desirable to have all transmitters shifted simultaneously, so that information in each of the track circuit block memory circuits is stored until the reset space between the 31st and the 1st pulse occurs, at which time whatever is stored is respectively used to set the frequency of the local transmitter. In this way, although information is delivered to all local transmitters on a serial basis, all local transmitters are actually modulated in synchronism with each other.

In reference to the train presence information back signal receivers, these include crystal filters which allow them to only respond to the frequency of the corresponding crystal controlled transmitters associated with and located at the oppsoite end of the respective track circuit blocks. When transmitters and receivers are combined at one wayside block location, the same time slot selector that was used for the transmitters is also used to enable the receiver output to deliver the information it is receiving to the receiver information back line. The latter information is decoded into a ONE or a ZERO signal depending on which of the two assigned frequency pairs is being received.

The time slot generator drive enable circuits allow each multiplex system to transmit and receive in the assigned time slots. During the receive operation of the system the information is first delivered to a speed signal code comparison circuit, and if it passes this test, it is then delivered to a fial relay safety protection system of conventional design. This safety protection system, including the speed signal encoder **51**, develops speed commands for the vehicles located in the track circuit signal block with which it is connected. The speed commands are delivered to the transmitter information down line through appropriate time slot enable circuits. The feature which makes the present system substantially immune to errors in synchronization is the feedback and signal comparison taking place between the speed signal code generator and the speed signal code comparison circuit; if the receiver operative with a given track circuit signal block does not receive exactly, pulse bit by pulse bit, the same signal information introduced to this track circuit signal block by its associated transmitter, no speed command signal information will be relased to the safety protection circuit. This provides double protection of the track circuit block; first, the frequency must be correct in order to be received by the crystal filtered receiver and, second, the receiver must receive exactly what the associated transmitter transmit before a valid signal condition is recognized.

The safety of the communication system is further enhanced by the use of comma free coded speed command signals, which reduce to a vanishing point the possiblity of external interference producing a recognizable but erroneous vehicle speed command. The speed signal code consists of six bits of information to transmit nine desired speed command signals. Only those signals which have the comma free characteristic are utilized. A repetitive sequence of any of these coded command speed signals will never be confused with any other code regardless of the time or random signal bit selected as the beginning of a vehicle command signal message. In this way no synchronization is required in the vehicle decoding system in order to recognize a speed command signal. The additional bits required for this type of code are an advantage in the track circuits, since the more bits that are compared at the receiving end with those introduced in the transmitting end before validity is recognized reduces the probability that a false signal will not be detected. Six bits of signal information reduces this possiblity as a function of time down to a mathematically insignificant level. The comma free speed command signal now offers a further opportunity to protect adjacent track circuits from receiving erroneous information over and beyond that which is provided by the frequency separation; if all track circuits were being commanded at the same speed, it otherwise would be only the frequency separation and attenuation that keeps the respective adjacent track circuits separated. This is a situation that exists in prior art conventional audio frequency track circuit operation; however with comma free coded speed command signals, it is possible to phase shift or delay each successie transmitter by one pulse of the speed command code without the vehicle recognizing the difference. This phase shift of the pulse then makes it possible to get a signal separation between the command signals of successive track circuit blocks even if each were asking for the same vehicle speed. Three sets of frequecy pairs are utilized for the respective track circuit blocks and there are six possible time positions for each signal frequency for a given speed command. It then follows that 18 uniquely identifiable track circuit signals, when consideration of the three frequency pairs used and the six phase shifts obtainable, are thereby possible before it is necessary to repeat an identical speed commany signal format. This provides high attenuation of signals through any given length of train track and the negligible probability of occurrence of 18 multiple failures before an unsafe operating condition might occur.

The train control equipment carried by each train vehicle consists of two systems; the first system is for the control of the speed of the vehicle, and the second sys-

tem is for the control of the vehicle during station stopping. The train vehicle carries a speed control antenna system suitably shielded and coupled to the train rails to receive all three frequency pairs from the track. The train carried receiver filters this speed control information and delivers it to a speed decoder aboard the train. The speed decoder recognizes a comma free code without benefit of word synchronization and delivers one of up to nine speed commands to the train. These speed commands are interpreted by the speed regulation equipment and compared with a tachometer, with the resulting output signal then controlling as desired the propulsion equipment and the brake equipment. The same speed command signals are delivered to an overspeed protection equipment carried by the train which also compares the speed commands with a tachometer and provides independent overriding control of the brake equipment in the event that an overspeed condition exists. The second subsystem carried by the train vehicle is concerned with station stopping.

The safety system thereby provided is dynamic in operation and demands that it continually be checking itself before delivering the vehicle speed commands to the train propulsion equipment and further utilizes fail-safe comma free coding to make it substantially impossible for interference and noise signals to cause unsafe train vehicle operation.

One advantage of using only four twisted pairs of conductors, plus the above described interface equipment for a complete system covering many miles, is the attractiveness from the standpoint of cost and cable density as compared to the use of individual hardwired cables to each remote location. The 311.04 kilocycle frequency standard transmitted to each track signal block location allows precise crystal control of all track signal block transmitters while requiring only a single crystal oscillator in each of the associated wayside control stations. The implementation of the time division multiplexing system and digital circuitry allows for greater flexibility, greater reliability, more fail-safe operation and lower cost than can be achieved with prior art train control systems.

In general it should be understood that the scope of this invention is not limited to the above specifically described system. For example, if desired, any other suitable frequency could be used in place of the 311.04 kilocycle frequency standard, with the 311.04 kilocycle frequency being chosen to obtain signalling frequencies between 5 to 10 KC by an even integer number of divisions within a divider circuit, and none of which are harmonics of the power supply and other presently used signalling frequencies. The number of destinations or track circuit signal blocks operative with a given wayside control station could be modified by factors of two by the addition or deletion of counter stages, and the type of command signal information is not limited to that described.

While the invention has been described with respect to A.F. track signal circuits, it should be recognized that certain of the "telecontrol" multiplexing features may be utilized with other types of signal transmission lines. For example, the comma-free code control signals could be multiplexed to remote stations via a radio transmission link using the technique of time slot multiplexing with phase shifting of the multiple bits of the multiple bit multiplex word. The remote station would in this instance include a means for sensing the status of operation which is being controlled, and would provide a local TRUE state signal when the operation status and the command status match. The sensed signal would be ANDED with this TRUE signal and returned to the telecontrol transmission station for comparison to provide assurance of proper operation of the telecontrol multiplex. Suitable time buffering is provided in the coupling channels to effect comparison of corresponding parts of the transmitted and returned signals.

An article generally descriptive of a related train vehicle centralized control system was published in Railway Signaling and Communications magazine for Dec. 1967 at pages 18 to 23.

The present invention has been described with a certain degree of particularity. However, it should be understood that various modifications and changes can be made in the arrangement and operation of the individual parts without departing from the scope and spirit of this invention.

We claim as our invention:

1. In a multiplex system for controlling the operation of a plurality of stations, the combination comprising:

a first signal means for providing in sequence a plurality of multiple bit digital information signals and a multiple bit digital control signal to each of said plurality of stations for controlling the operation of same, with a given bit in each of said information signals being intended for a given station;

a second signal means located at each of said plurality of stations for successively sensing one predetermined bit in each one of said plurality of multiple bit information signals at a given time during each information signal sequence determined by the provision of a predetermined number of bits of said multiple bit digital control signal;

comparator means for determining the operational status of said given station by comparing said given bit intended for said given station in each one of said plurality of multiple bit digital information signals with each said one predetermined bit which is successively sensed by said second signal means at said given station; and

means for modifying the sequence of digital information bits intended for said given station in response to the comparison of bits not being identical.

2. The combination claimed in claim **1**, with said second signal means including a counter which counts in response to the provision of said multiple bit digital control signal; and

means for sensing the provision of said one predetermined bit in each one of said plurality of multiple bit information signals in response to said counter counting to a predetermined count.

3. In a multiplex system for controlling the operation of a plurality of remote stations, the combination comprising:

means for providing in sequence a plurality of N bit, where N is an integer, digital information signals to each of said plurality of remote stations for controlling the operation of same, with at least a given one of the bits in each one of said bit information signals being intended for a given station;

means for providing an M bit, where M is an integer, digital control signal to each of said plurality of remote stations;

means for sensing at said given station, the provision of said given one of said N digital information bits

in each one of said plurality of digital information signals at a given time during each information signal sequence determined by the provision of a predetermined one of said M digital control bits to said given station;

comparator means for determining the operational status of said given station by comparing said given one of the bits in each one of said N digital information signals intended for said given station with the bit sensed, during each successive information signal sequence, by said means for sensing at said given station; and

means for modifying the sequence of digital information bits intended for said given station in response to the comparison of bits not being identical on a bit by bit comparison basis.

4. In a multiplex system for controlling the operation of a plurality of remote stations, the combination comprising:

means for sequentially providing a plurality of N bit, where N is an integer, digital information signals to each of said plurality of remote stations for controlling the operation of same, with a given one of the bits in each one of said N bit information signals being intended for a given station;

means for providing an M bit time, where M is an integer, digital control signal to each of said plurality of remote stations;

a counter at each station for counting in response to the provision of said digital control signal;

means at each station for providing a timing signal in response to said counter reaching a predetermined count;

means at each station for sensing a predetermined one of said N digital information bits in each digital information signal sequence in response to the provision of said timing signal;

comparator means for determining the operational status of said given station by comparing said given bit intended for said given station in each one of the digital information signals with each said predetermined one of said N digital information bits which is successively sensed by said means for sensing at said given station; and

means for modifying the sequence of digital information bits intended for said given station in response to the comparison of bits not being indentical on a bit by bit comparison basis.

5. The combination claimed in claim **4** with said N bit signal information signal being coded in a comma free code.

6. The combination claimed in claim **5** with means for resetting each counter during the Mth bit time of said digital control signal.

7. The combination claimed in claim **6** including means for determining said operational status of a given station during the Mth bit time of said digital control signal.

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