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Ando et al. (43) **Pub. Date: May 31, 2007**

(54) **OPTICAL RECORDING MEDIUM, INFORMATION REPRODUCTION APPARATUS AND INFORMATION RECORDING/REPRODUCTION**

(75) Inventors: **Hideo Ando**, Hino-shi (JP); **Kazuo Watabe**, Yokohama-shi (JP); **Hiroharu Sato**, Tokyo (JP); **Toshihiro Sugaya**, Kitasoma-gun (JP); **Chosaku Noda**, Kawasaki-shi (JP)

Correspondence Address:
PILLSBURY WINTHROP SHAW PITTMAN, LLP
P.O. BOX 10500
MCLEAN, VA 22102 (US)

(73) Assignee: **KABUSHIKI KAISHA TOSHIBA**, Tokyo (JP)

(21) Appl. No.: **11/699,039**

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Related U.S. Application Data

(63) Continuation of application No. 10/233,671, filed on Sep. 4, 2002, now Pat. No. 7,190,663.

(30) **Foreign Application Priority Data**

Sep. 7, 2001 (JP) 2001-271895

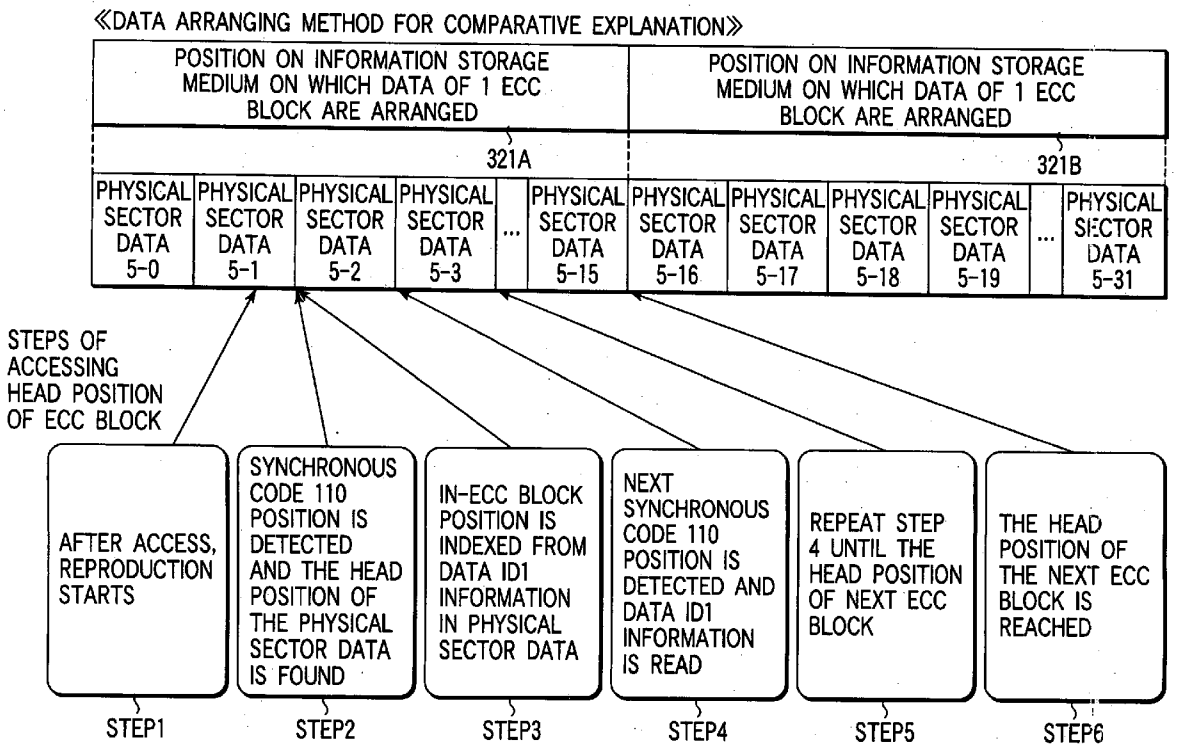
Publication Classification

(51) **Int. Cl.**
G11B 7/24 (2006.01)

(52) **U.S. Cl.** **369/275.3**

(57) **ABSTRACT**

User data recording areas and intermediate areas are alternately arranged on a disk. The intermediate area records at least information for synchronization.



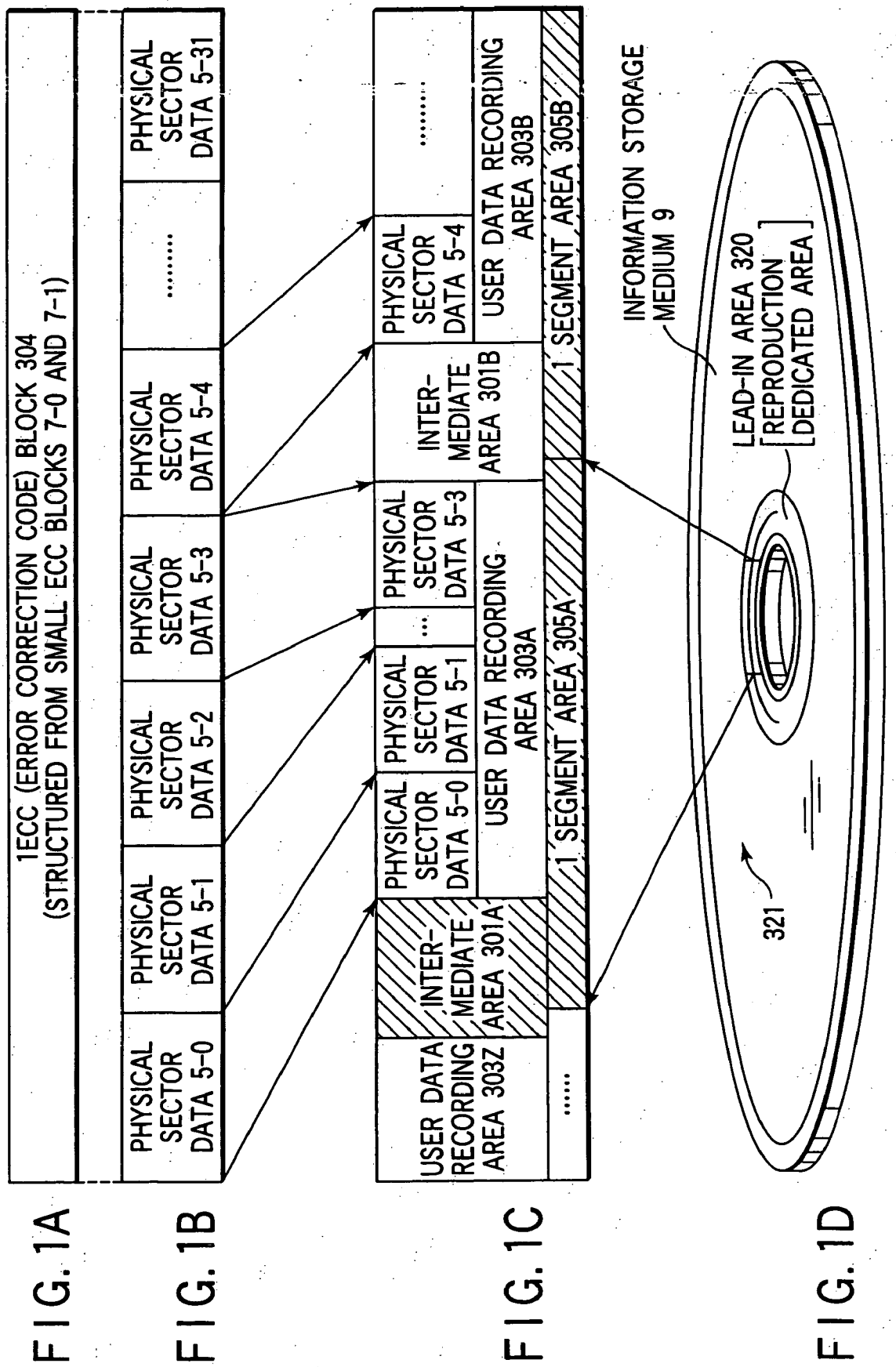


FIG. 1A

FIG. 1B

FIG. 1C

FIG. 1D

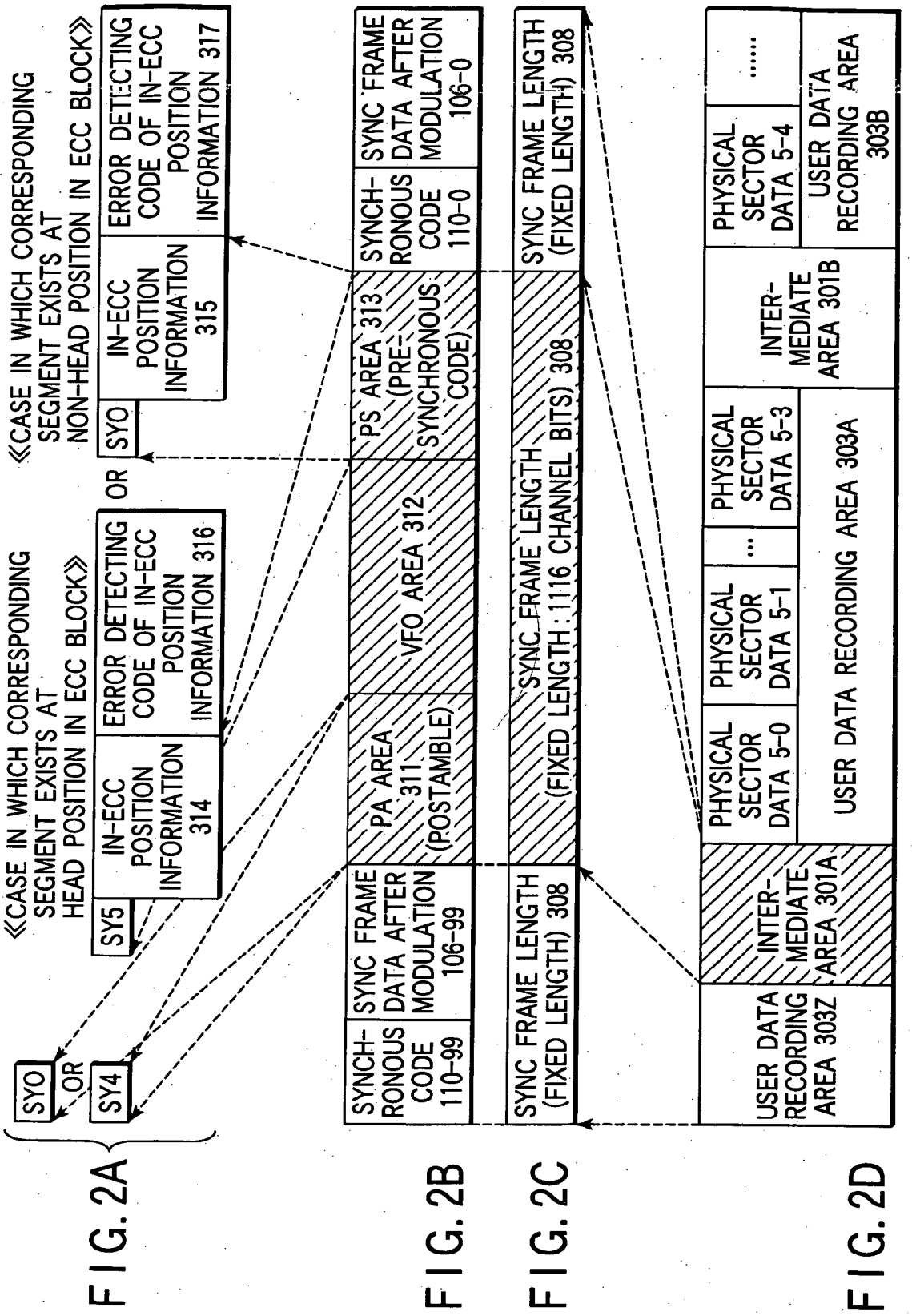


FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

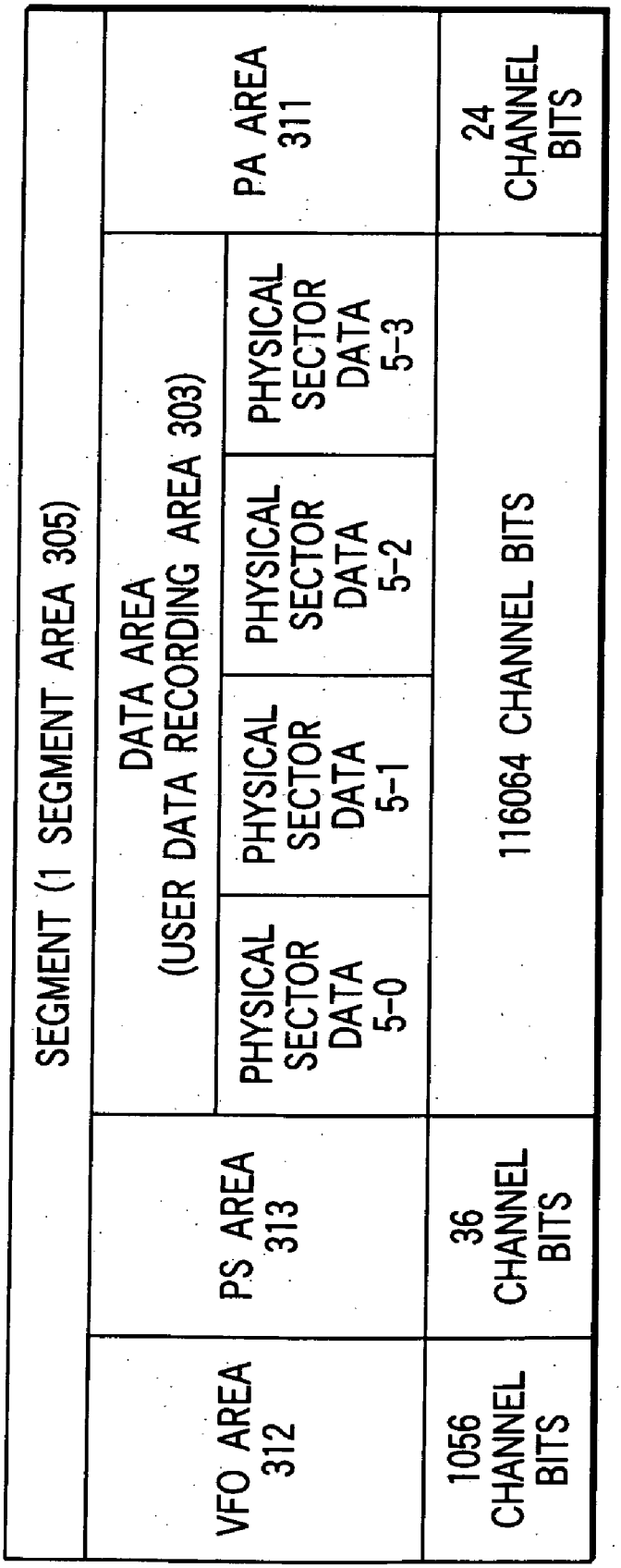

SEGMENT (1 SEGMENT AREA 305)
VFO AREA 312
PS AREA 313
DATA AREA (USER DATA RECORDING AREA 303)
PHYSICAL SECTOR DATA 5-0
PHYSICAL SECTOR DATA 5-1
PHYSICAL SECTOR DATA 5-2
PHYSICAL SECTOR DATA 5-3
PA AREA 311
1056 CHANNEL BITS
36 CHANNEL BITS
116064 CHANNEL BITS
24 CHANNEL BITS

FIG. 3

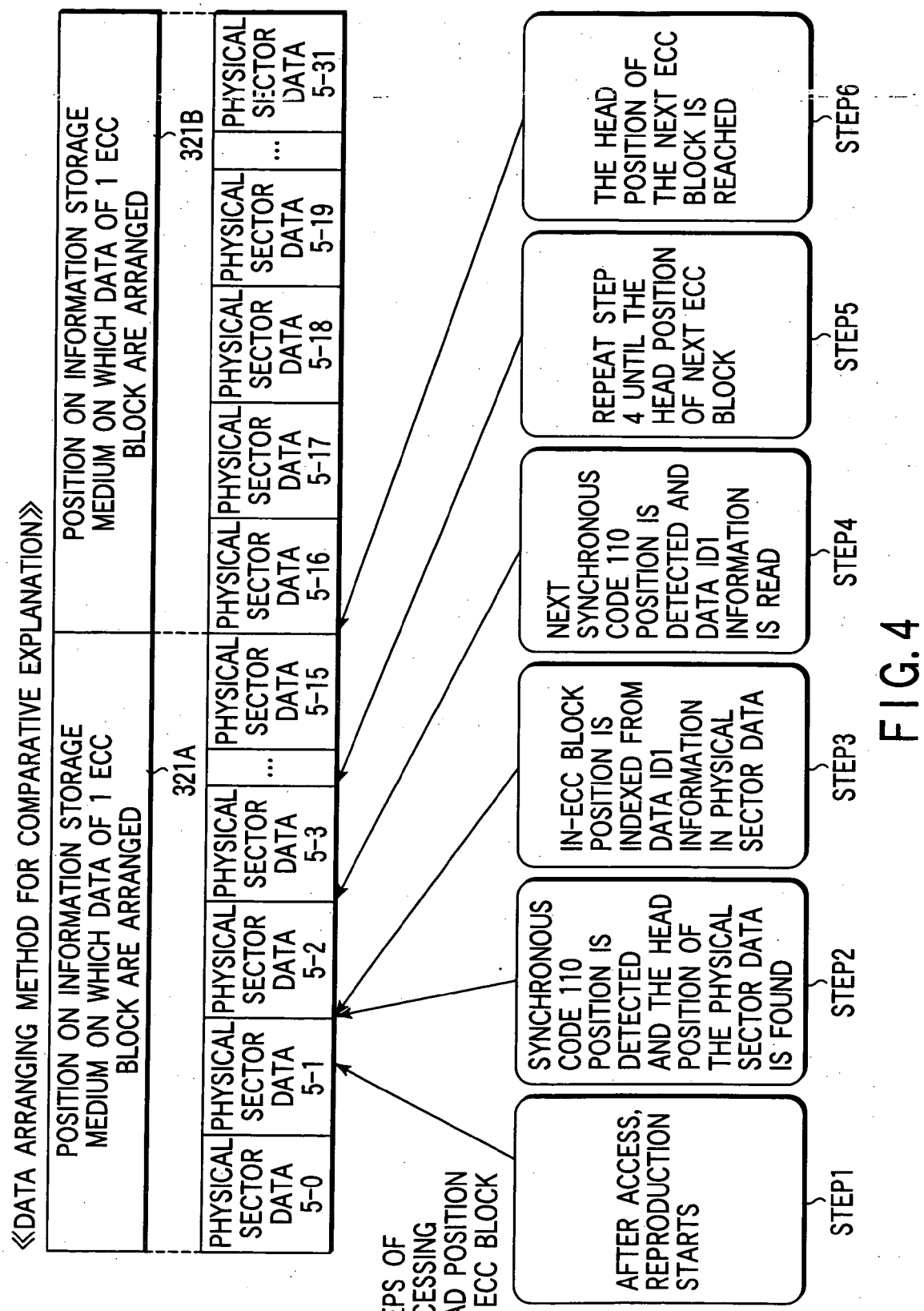

«DATA ARRANGING METHOD FOR COMPARATIVE EXPLANATION»
POSITION ON INFORMATION STORAGE MEDIUM ON WHICH DATA OF 1 ECC BLOCK ARE ARRANGED
321A
321B
PHYSICAL SECTOR DATA 5-0
PHYSICAL SECTOR DATA 5-1
PHYSICAL SECTOR DATA 5-2
PHYSICAL SECTOR DATA 5-3
PHYSICAL SECTOR DATA 5-15
PHYSICAL SECTOR DATA 5-16
PHYSICAL SECTOR DATA 5-17
PHYSICAL SECTOR DATA 5-18
PHYSICAL SECTOR DATA 5-19
PHYSICAL SECTOR DATA 5-31
STEPS OF ACCESSING HEAD POSITION OF ECC BLOCK
AFTER ACCESS, REPRODUCTION STARTS
STEP1
SYNCHRONOUS CODE 110 POSITION IS DETECTED AND THE HEAD POSITION OF THE PHYSICAL SECTOR DATA IS FOUND
STEP2
IN-ECC BLOCK POSITION IS INDEXED FROM DATA ID1 INFORMATION IN PHYSICAL SECTOR DATA
STEP3
NEXT SYNCHRONOUS CODE 110 POSITION IS DETECTED AND DATA ID1 INFORMATION IS READ
STEP4
REPEAT STEP 4 UNTIL THE HEAD POSITION OF NEXT ECC BLOCK
STEP5
THE HEAD POSITION OF THE NEXT ECC BLOCK IS REACHED
STEP6

FIG. 4

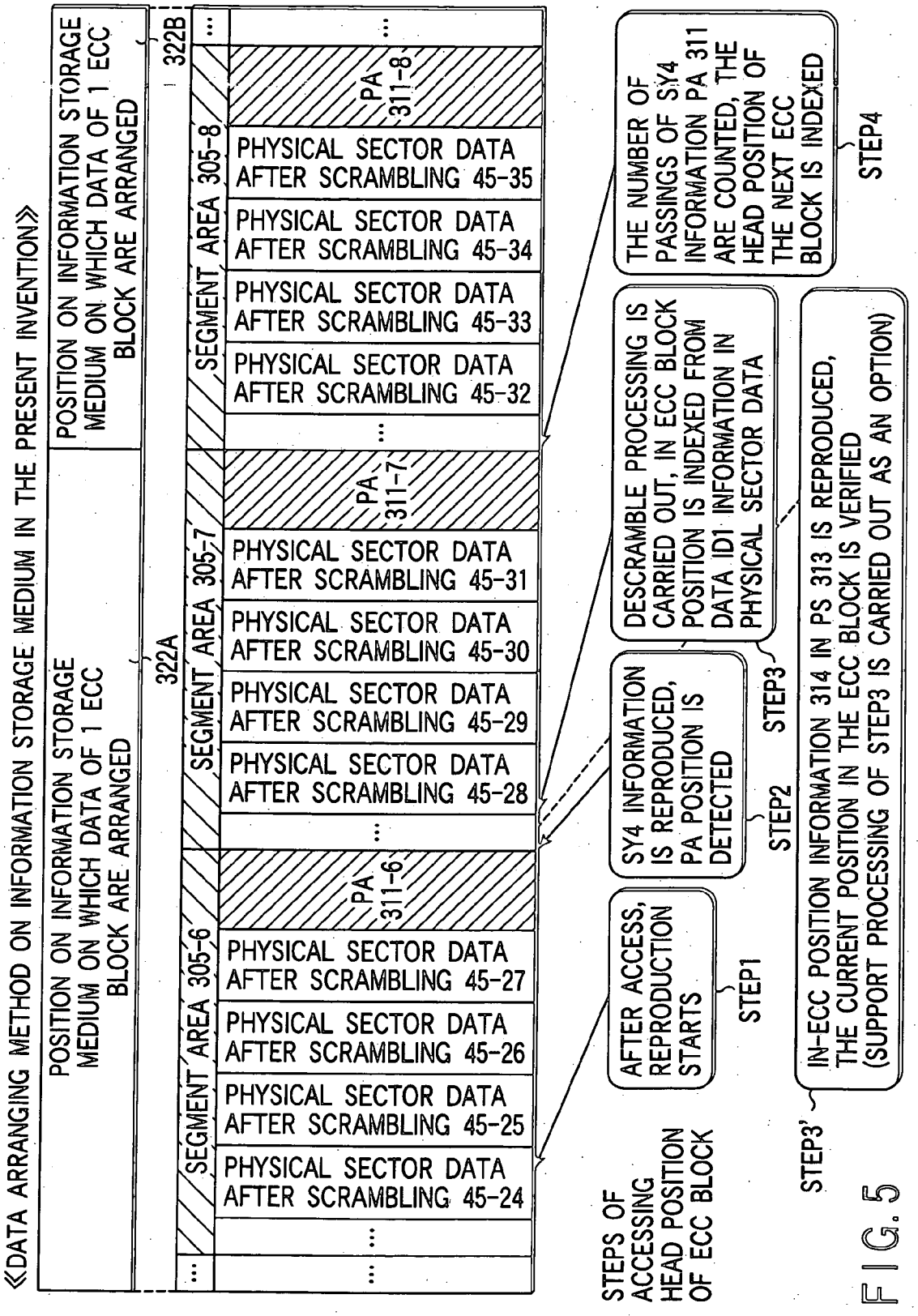

«DATA ARRANGING METHOD ON INFORMATION STORAGE MEDIUM IN THE PRESENT INVENTION»
POSITION ON INFORMATION STORAGE MEDIUM ON WHICH DATA OF 1 ECC BLOCK ARE ARRANGED
322A
POSITION ON INFORMATION STORAGE MEDIUM ON WHICH DATA OF 1 ECC BLOCK ARE ARRANGED
322B
SEGMENT AREA 305-8
SEGMENT AREA 305-7
SEGMENT AREA 305-6
PA 311-8
PA 311-7
PA 311-6
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-35
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-34
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-33
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-32
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-31
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-30
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-29
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-28
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-27
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-26
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-25
PHYSICAL SECTOR DATA AFTER SCRAMBLING 45-24
THE NUMBER OF PASSINGS OF SY4 INFORMATION PA 311 ARE COUNTED, THE HEAD POSITION OF THE NEXT ECC BLOCK IS INDEXED
STEP4
DESCRAMBLE PROCESSING IS CARRIED OUT, IN ECC BLOCK POSITION IS INDEXED FROM DATA ID1 INFORMATION IN PHYSICAL SECTOR DATA
STEP3
SY4 INFORMATION IS REPRODUCED, PA POSITION IS DETECTED
STEP2
AFTER ACCESS, REPRODUCTION STARTS
STEP1
STEPS OF ACCESSING HEAD POSITION OF ECC BLOCK
STEP3'
IN-ECC POSITION INFORMATION 314 IN PS 313 IS REPRODUCED, THE CURRENT POSITION IN THE ECC BLOCK IS VERIFIED (SUPPORT PROCESSING OF STEP3 IS CARRIED OUT AS AN OPTION)

FIG. 5

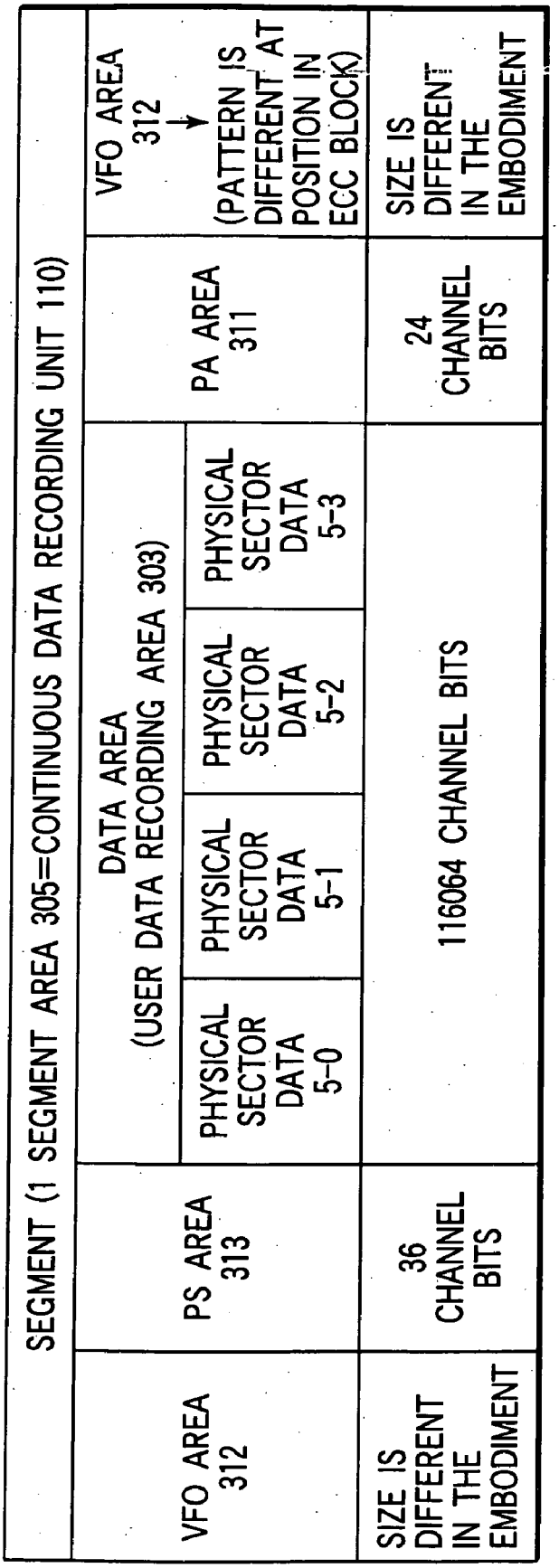

SEGMENT (1 SEGMENT AREA 305=CONTINUOUS DATA RECORDING UNIT 110)
VFO AREA 312
PS AREA 313
DATA AREA (USER DATA RECORDING AREA 303)
PHYSICAL SECTOR DATA 5-0
PHYSICAL SECTOR DATA 5-1
PHYSICAL SECTOR DATA 5-2
PHYSICAL SECTOR DATA 5-3
PA AREA 311
VFO AREA 312 (PATTERN IS DIFFERENT AT POSITION IN ECC BLOCK)
SIZE IS DIFFERENT IN THE EMBODIMENT
36 CHANNEL BITS
116064 CHANNEL BITS
24 CHANNEL BITS
SIZE IS DIFFERENT IN THE EMBODIMENT

FIG.6

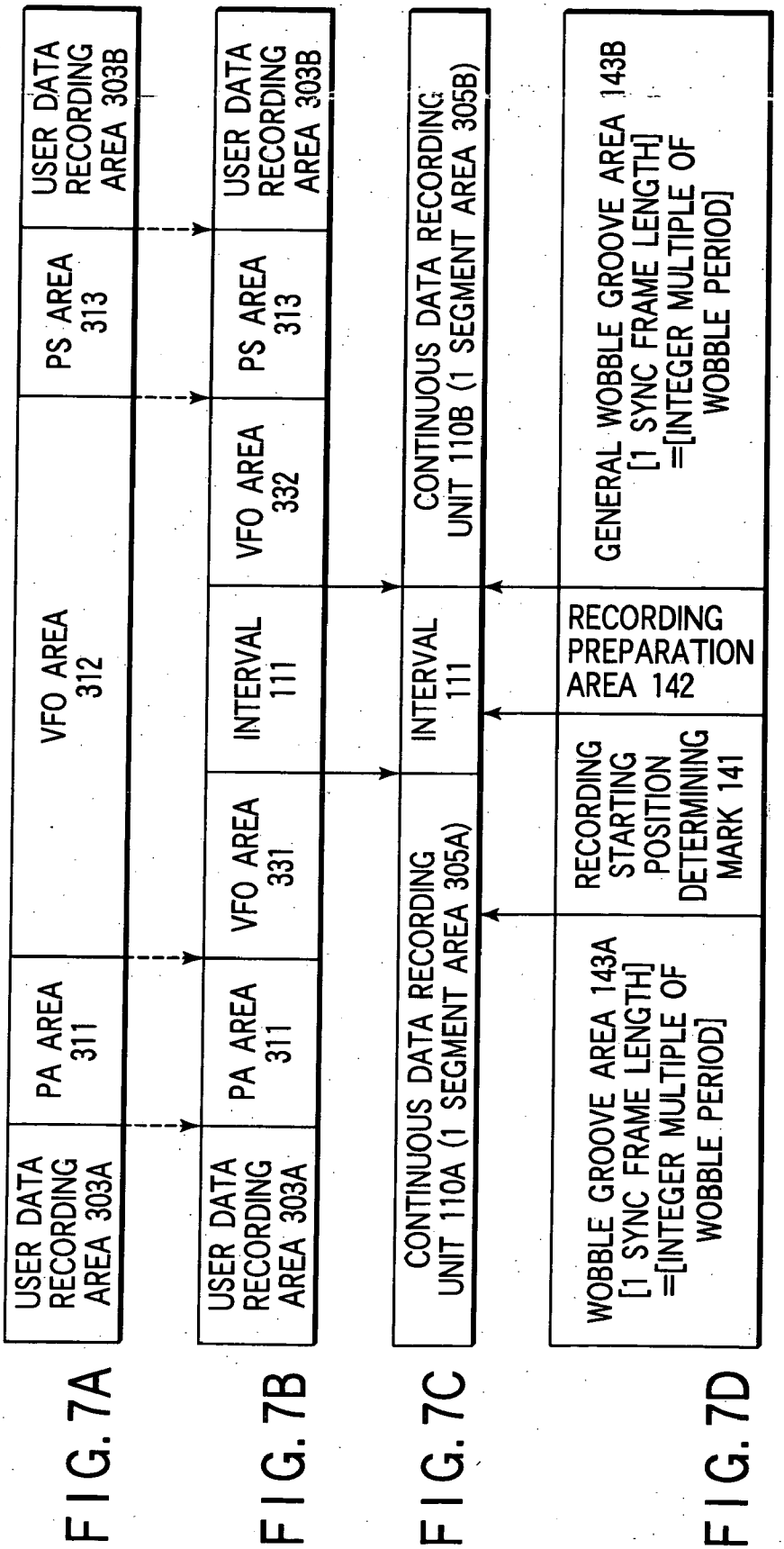


FIG. 7A

FIG. 7B

FIG. 7C

FIG. 7D

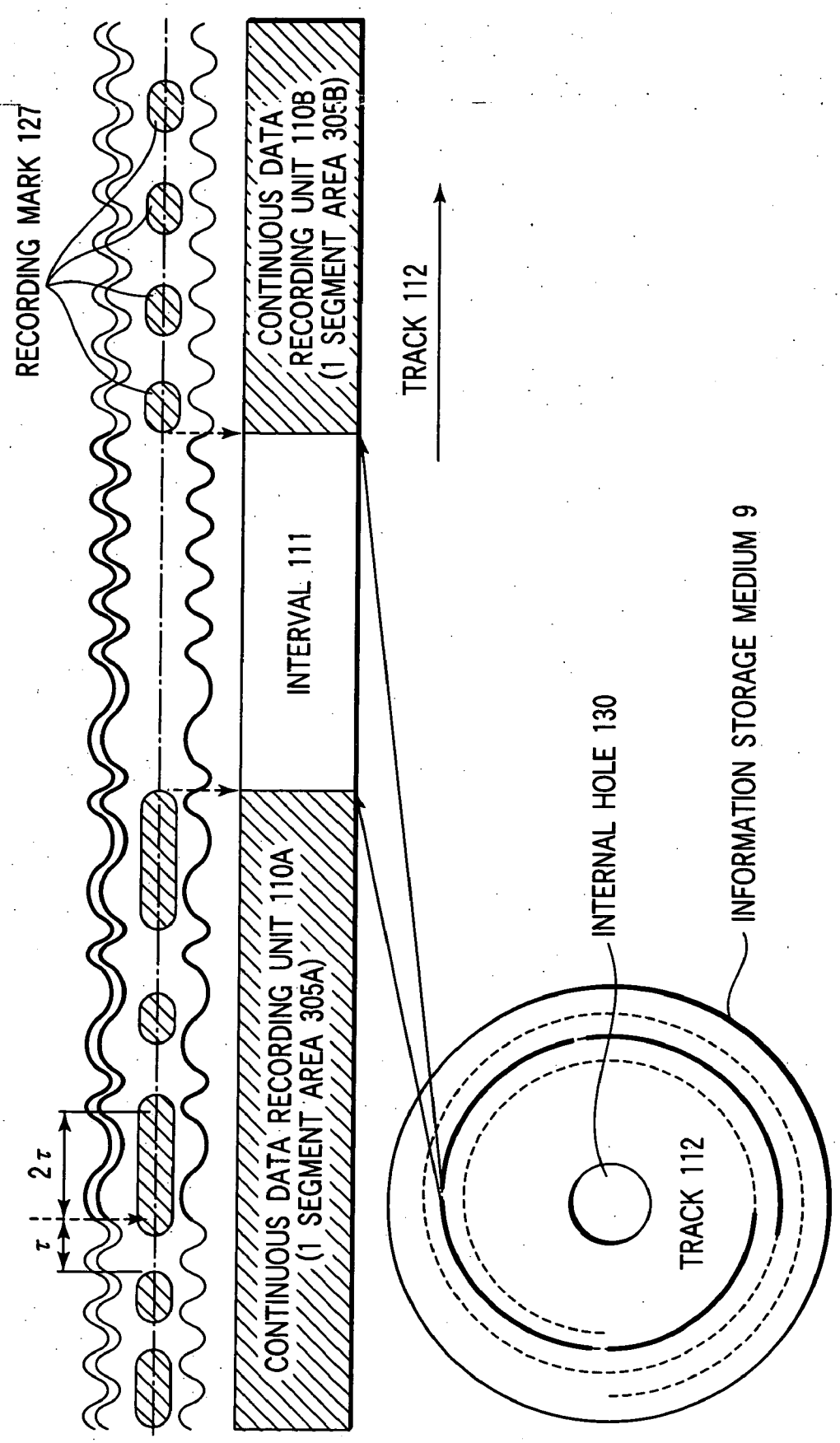

RECORDING MARK 127
CONTINUOUS DATA RECORDING UNIT 110B (1 SEGMENT AREA 305B)
INTERVAL 111
CONTINUOUS DATA RECORDING UNIT 110A (1 SEGMENT AREA 305A)
TRACK 112
2τ
τ
INTERNAL HOLE 130
INFORMATION STORAGE MEDIUM 9
TRACK 112

FIG. 8

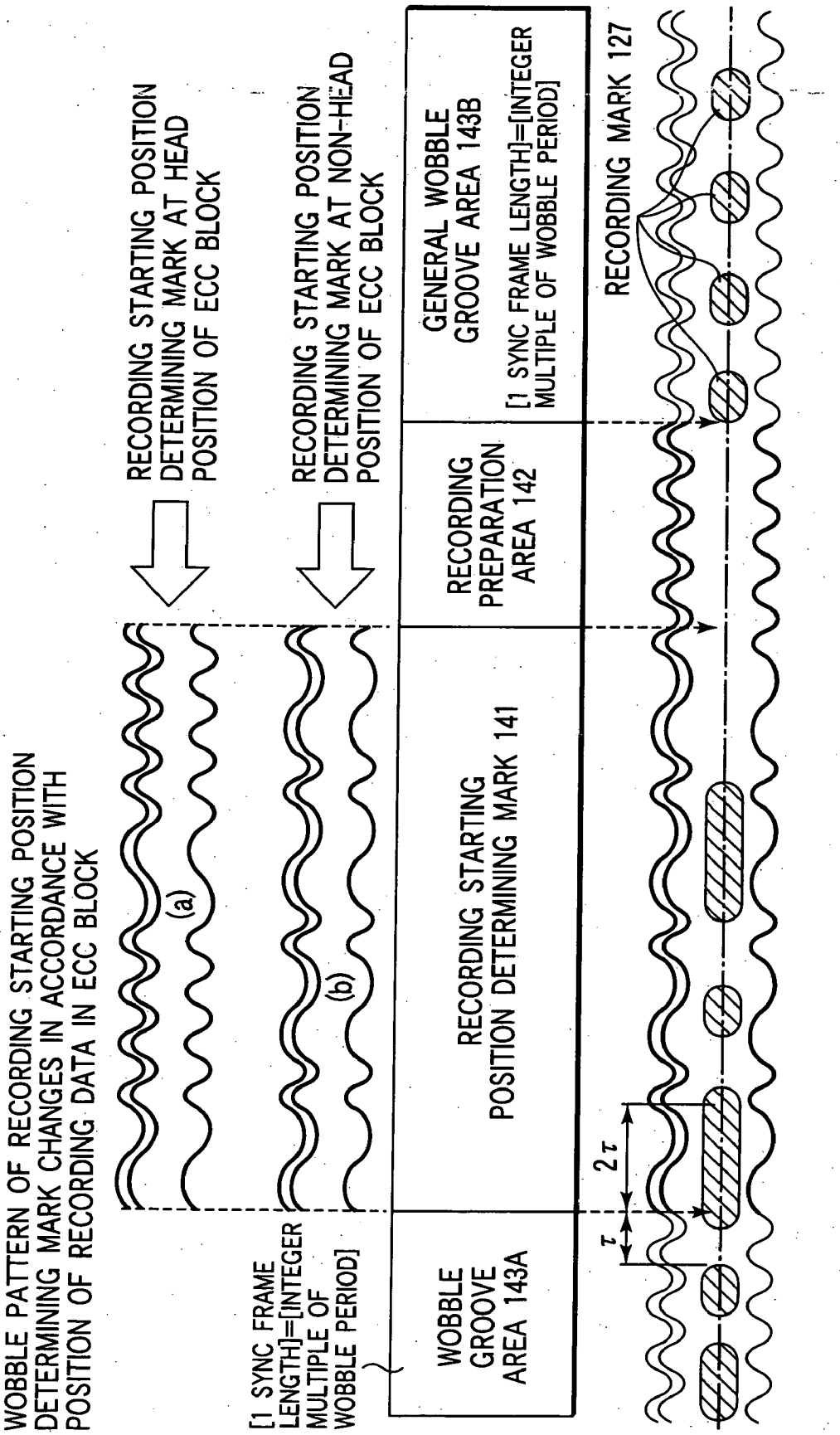

WOBBLE PATTERN OF RECORDING STARTING POSITION DETERMINING MARK CHANGES IN ACCORDANCE WITH POSITION OF RECORDING DATA IN ECC BLOCK
RECORDING STARTING POSITION DETERMINING MARK AT HEAD POSITION OF ECC BLOCK
RECORDING STARTING POSITION DETERMINING MARK AT NON-HEAD POSITION OF ECC BLOCK
(a)
(b)
[1 SYNC FRAME LENGTH]=[INTEGER MULTIPLE OF WOBBLE PERIOD]
WOBBLE GROOVE AREA 143A
RECORDING STARTING POSITION DETERMINING MARK 141
RECORDING PREPARATION AREA 142
GENERAL WOBBLE GROOVE AREA 143B
[1 SYNC FRAME LENGTH]=[INTEGER MULTIPLE OF WOBBLE PERIOD]
RECORDING MARK 127
2τ
τ

FIG. 9

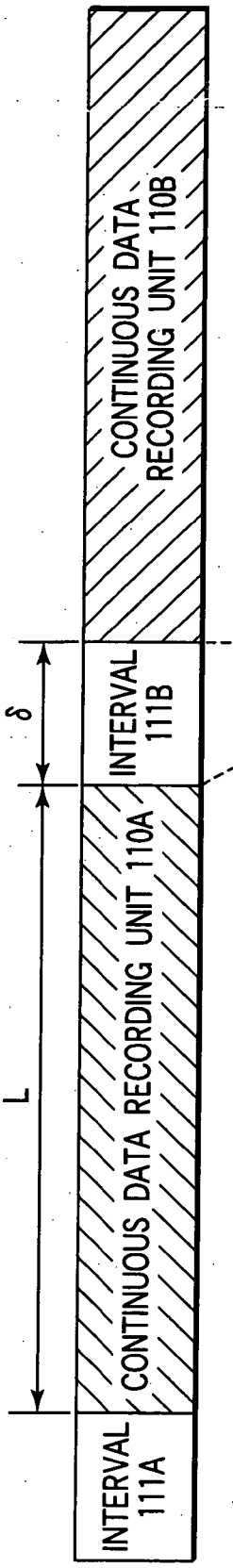


FIG. 10A

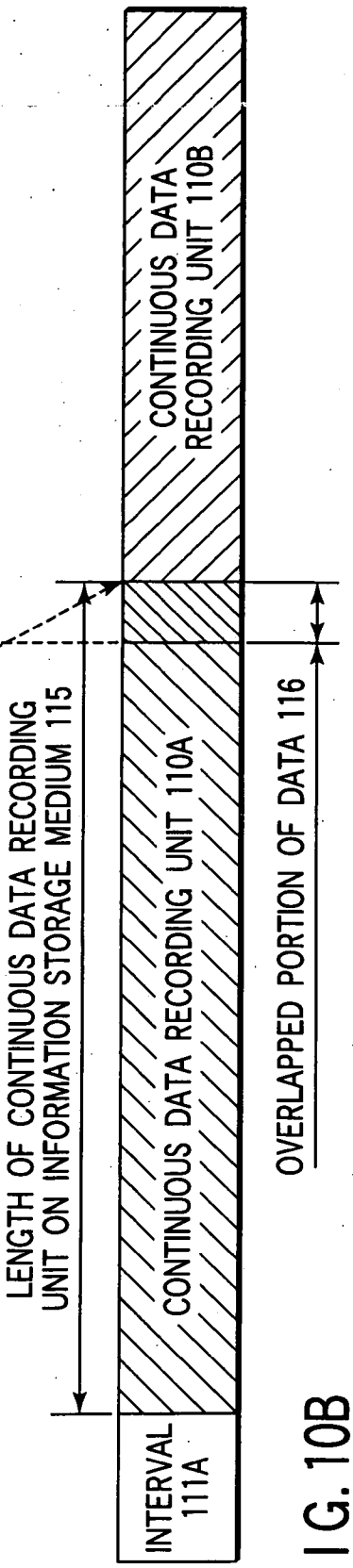
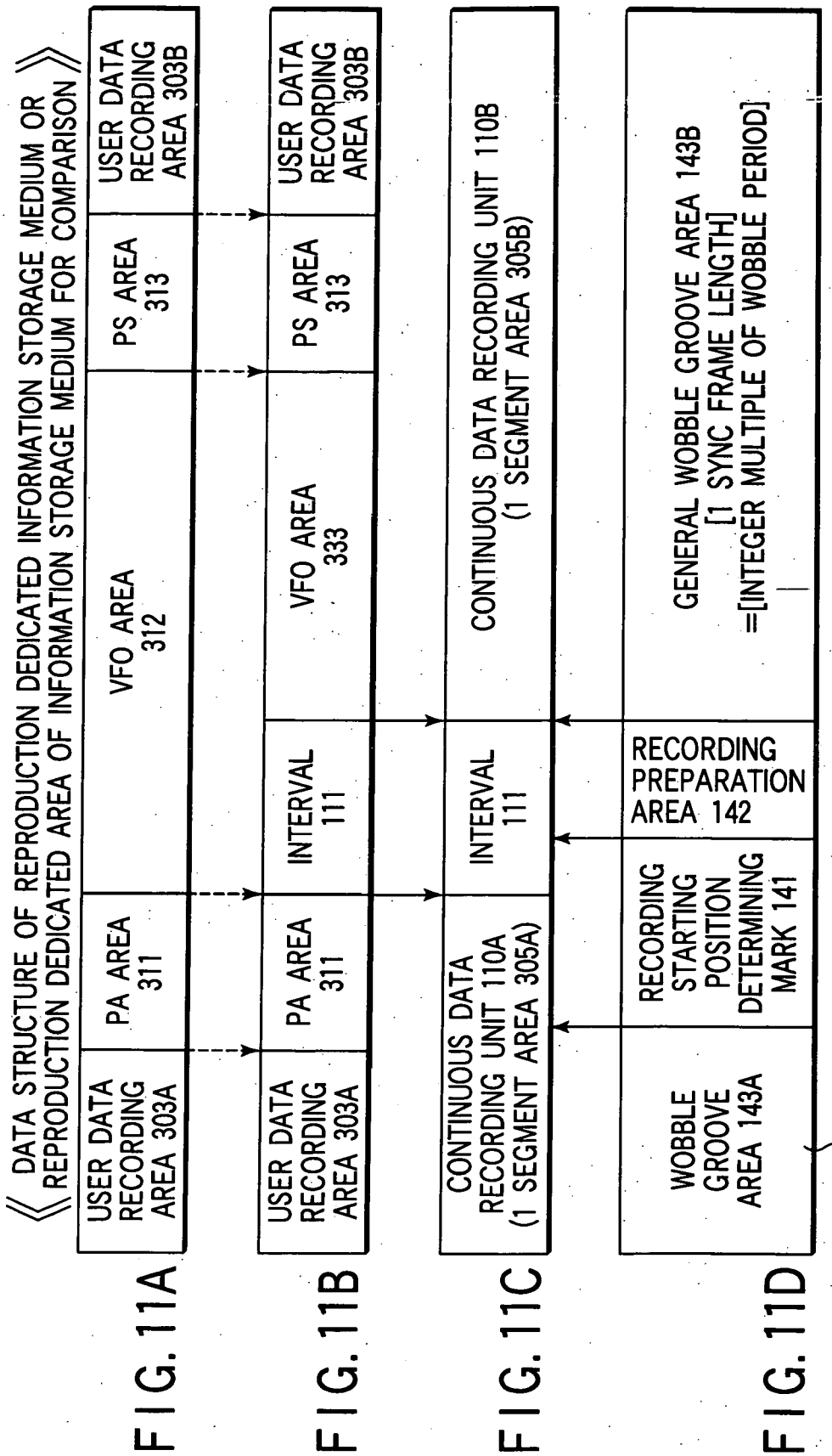
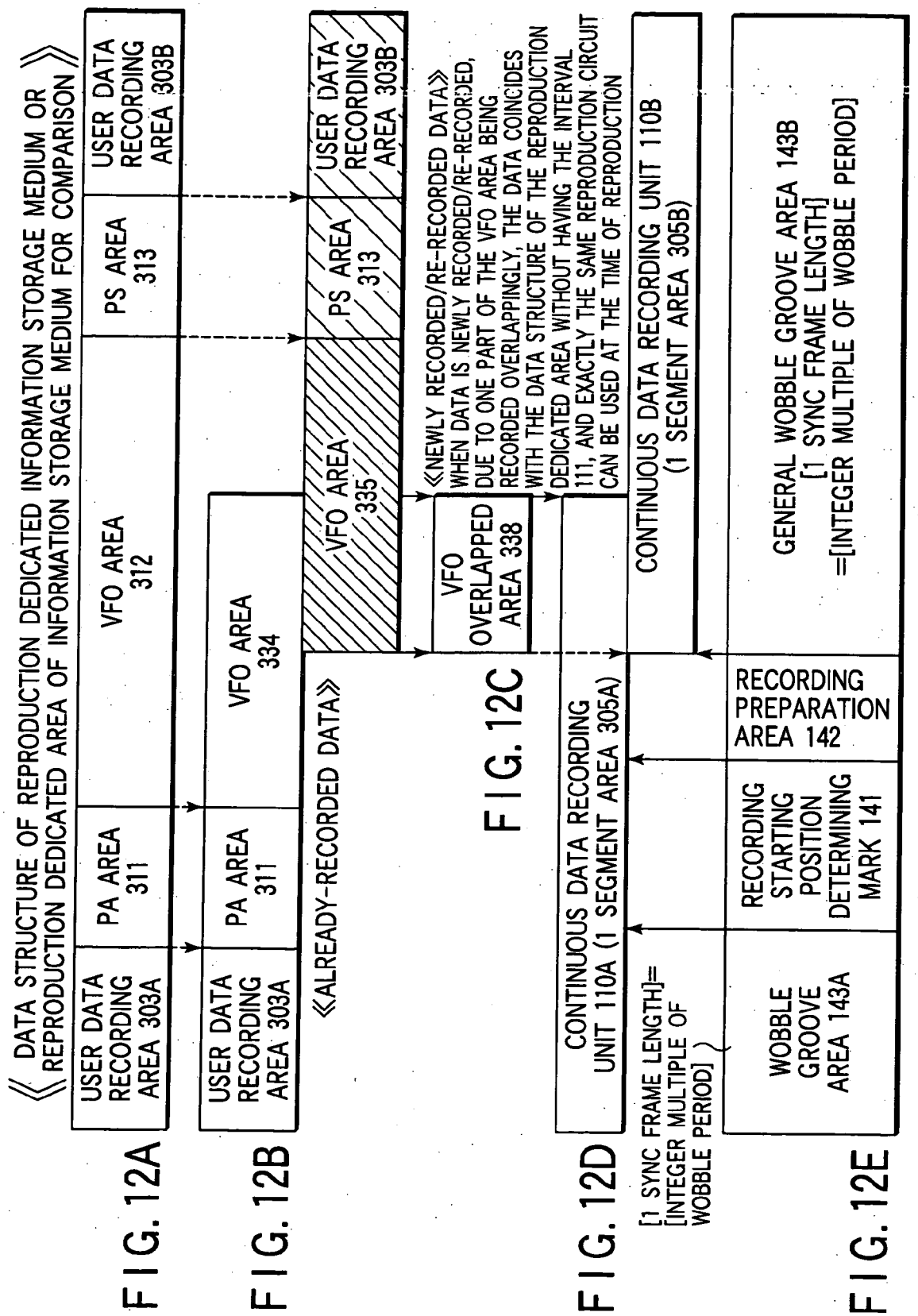


FIG. 10B


DATA STRUCTURE OF REPRODUCTION DEDICATED INFORMATION STORAGE MEDIUM OR REPRODUCTION DEDICATED AREA OF INFORMATION STORAGE MEDIUM FOR COMPARISON
USER DATA RECORDING AREA 303A
PA AREA 311
VFO AREA 312
PS AREA 313
USER DATA RECORDING AREA 303B
FIG. 11A
USER DATA RECORDING AREA 303A
PA AREA 311
INTERVAL 111
VFO AREA 333
PS AREA 313
USER DATA RECORDING AREA 303B
FIG. 11B
CONTINUOUS DATA RECORDING UNIT 110A (1 SEGMENT AREA 305A)
INTERVAL 111
CONTINUOUS DATA RECORDING UNIT 110B (1 SEGMENT AREA 305B)
FIG. 11C
WOBBLE GROOVE AREA 143A
RECORDING STARTING POSITION DETERMINING MARK 141
RECORDING PREPARATION AREA 142
GENERAL WOBBLE GROOVE AREA 143B
[1 SYNC FRAME LENGTH]
=[INTEGER MULTIPLE OF WOBBLE PERIOD]
[1 SYNC FRAME LENGTH]=[INTEGER MULTIPLE OF WOBBLE PERIOD]
FIG. 11D


《DATA STRUCTURE OF REPRODUCTION DEDICATED INFORMATION STORAGE MEDIUM OR REPRODUCTION DEDICATED AREA OF INFORMATION STORAGE MEDIUM FOR COMPARISON》
USER DATA RECORDING AREA 303A
PA AREA 311
VFO AREA 312
PS AREA 313
USER DATA RECORDING AREA 303B
FIG. 12A
USER DATA RECORDING AREA 303A
PA AREA 311
VFO AREA 334
《ALREADY-RECORDED DATA》
VFO AREA 335
PS AREA 313
USER DATA RECORDING AREA 303B
FIG. 12B
《NEWLY RECORDED/RE-RECORDED DATA》 WHEN DATA IS NEWLY RECORDED/RE-RECORDED, DUE TO ONE PART OF THE VFO AREA BEING RECORDED OVERLAPPINGLY, THE DATA COINCIDES WITH THE DATA STRUCTURE OF THE REPRODUCTION DEDICATED AREA WITHOUT HAVING THE INTERVAL 111, AND EXACTLY THE SAME REPRODUCTION CIRCUIT CAN BE USED AT THE TIME OF REPRODUCTION
VFO OVERLAPPED AREA 338
FIG. 12C
CONTINUOUS DATA RECORDING UNIT 110A (1 SEGMENT AREA 305A)
CONTINUOUS DATA RECORDING UNIT 110B (1 SEGMENT AREA 305B)
FIG. 12D
[1 SYNC FRAME LENGTH]= [INTEGER MULTIPLE OF WOBBLE PERIOD]
WOBBLE GROOVE AREA 143A
RECORDING STARTING POSITION DETERMINING MARK 141
RECORDING PREPARATION AREA 142
GENERAL WOBBLE GROOVE AREA 143B [1 SYNC FRAME LENGTH] =[INTEGER MULTIPLE OF WOBBLE PERIOD]
FIG. 12E

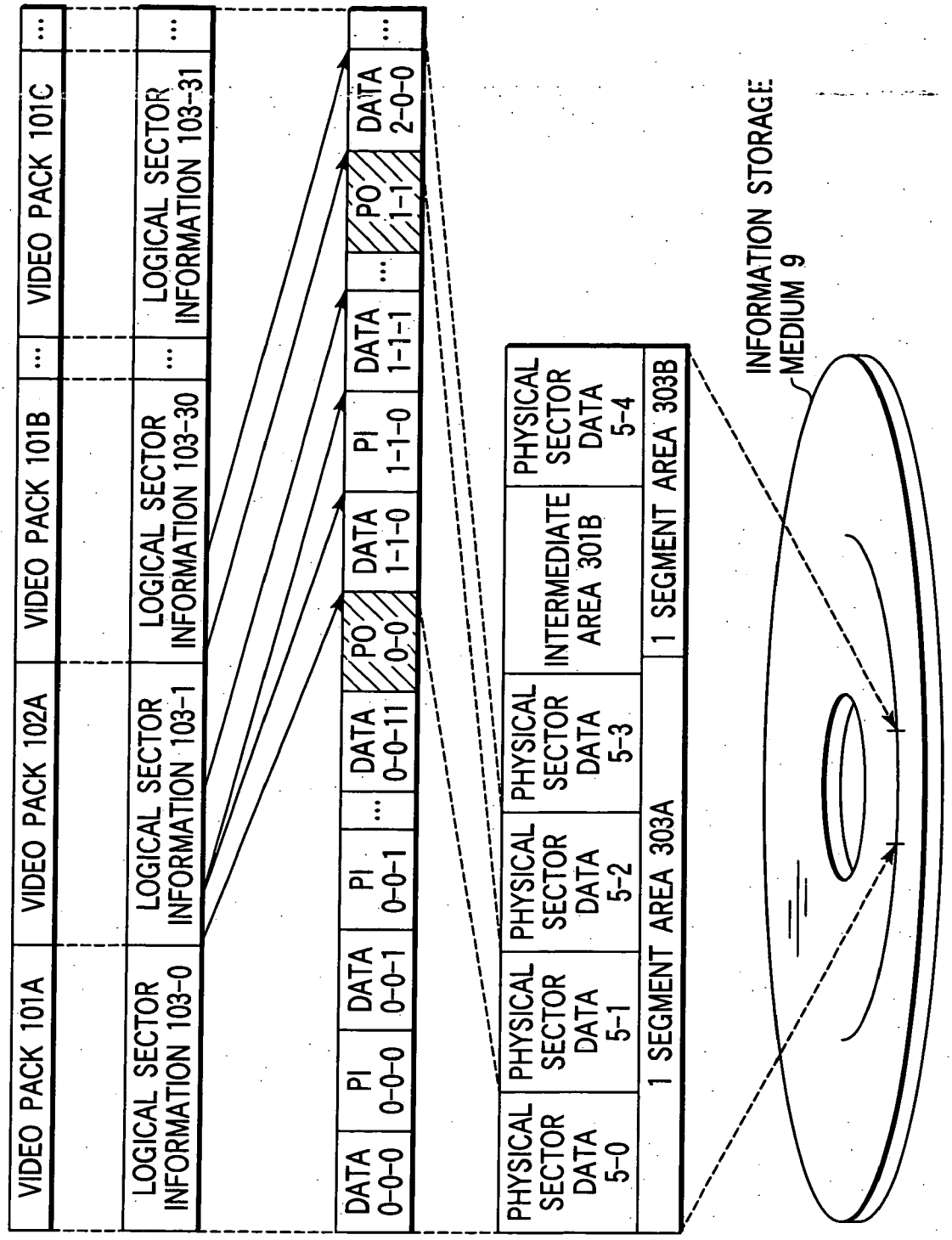


FIG. 13A

FIG. 13B

FIG. 13C

FIG. 13D

FIG. 13E

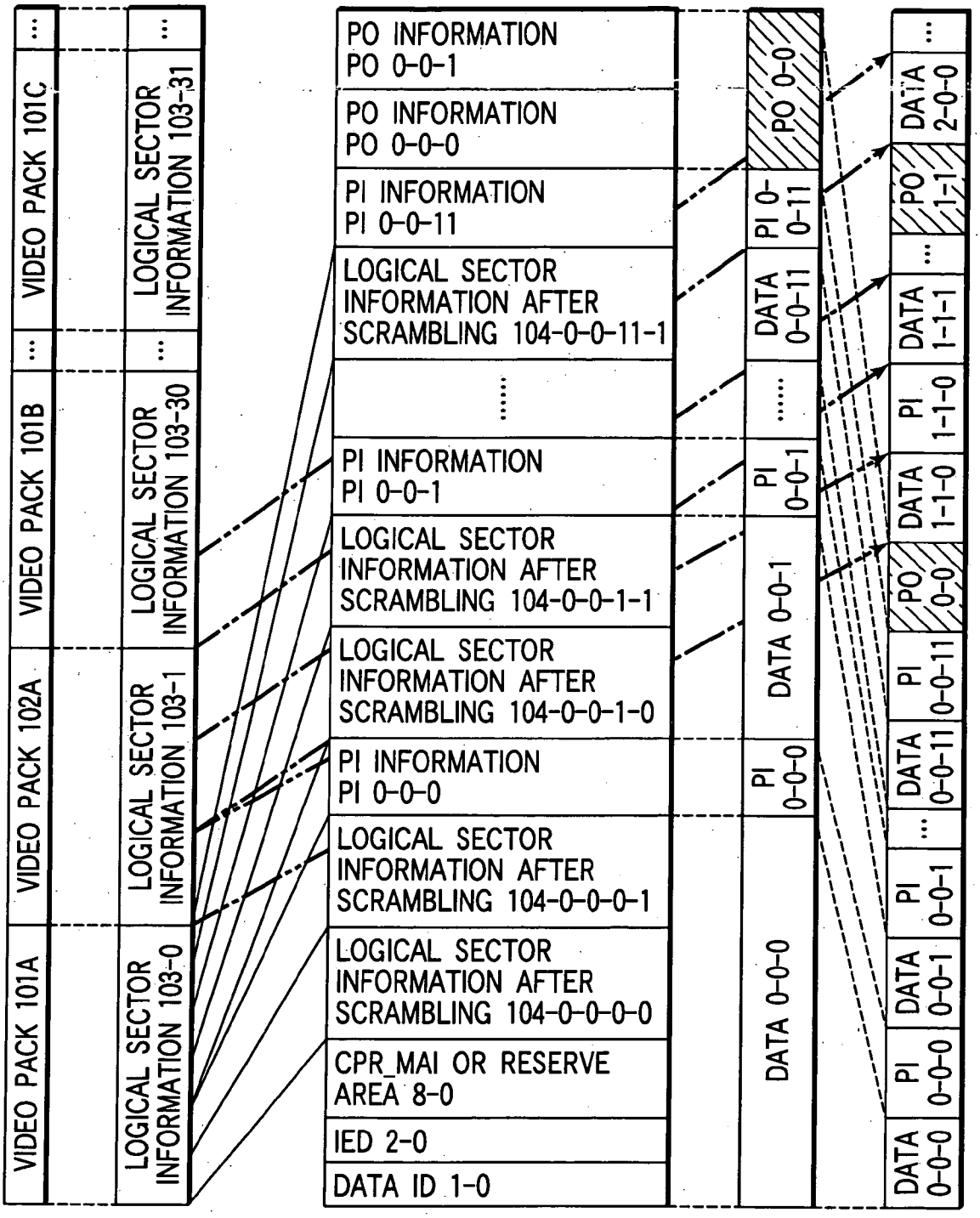


FIG. 14A FIG. 14B FIG. 14C FIG. 14D FIG. 14E

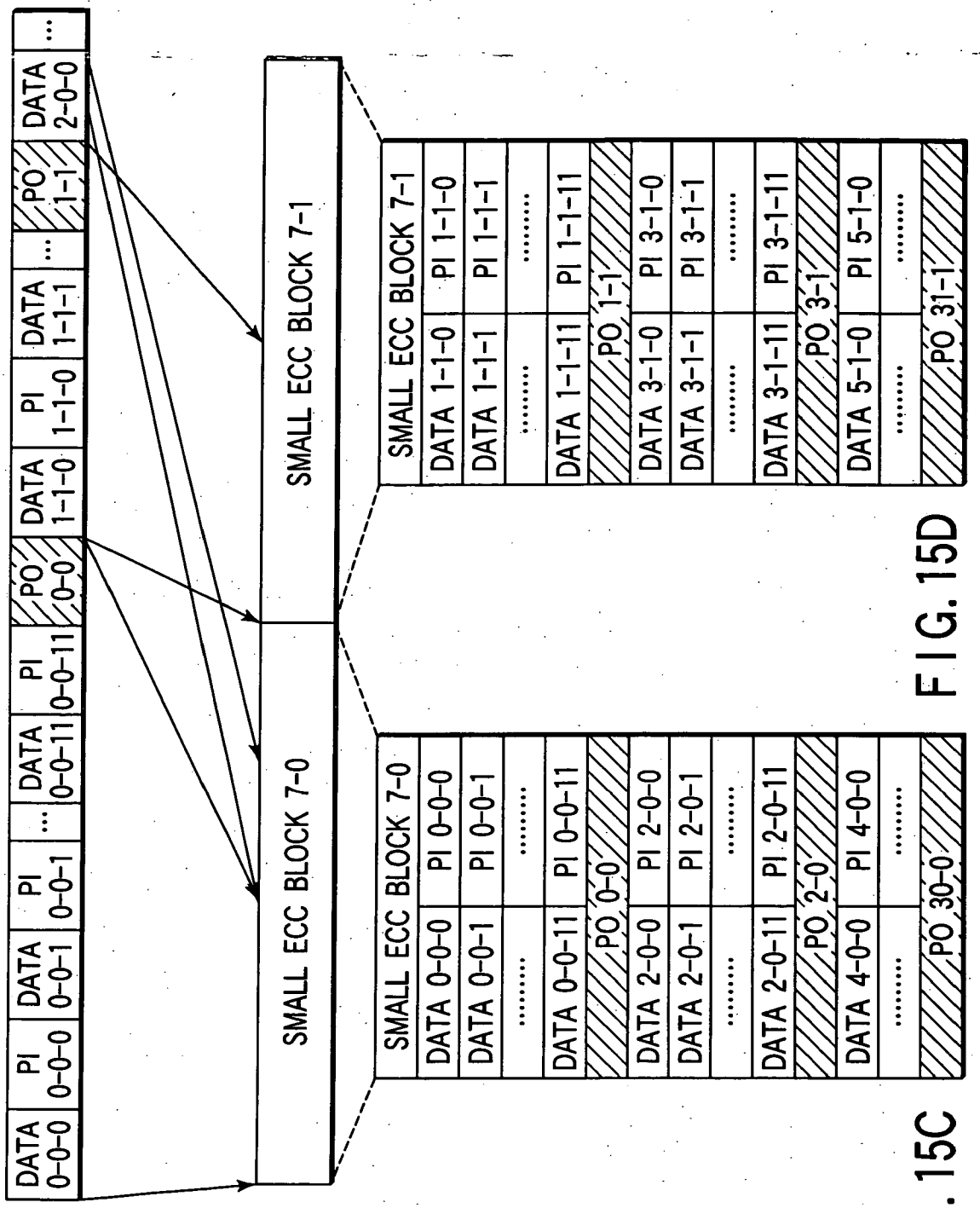


FIG. 15A

FIG. 15B

FIG. 15C

FIG. 15D

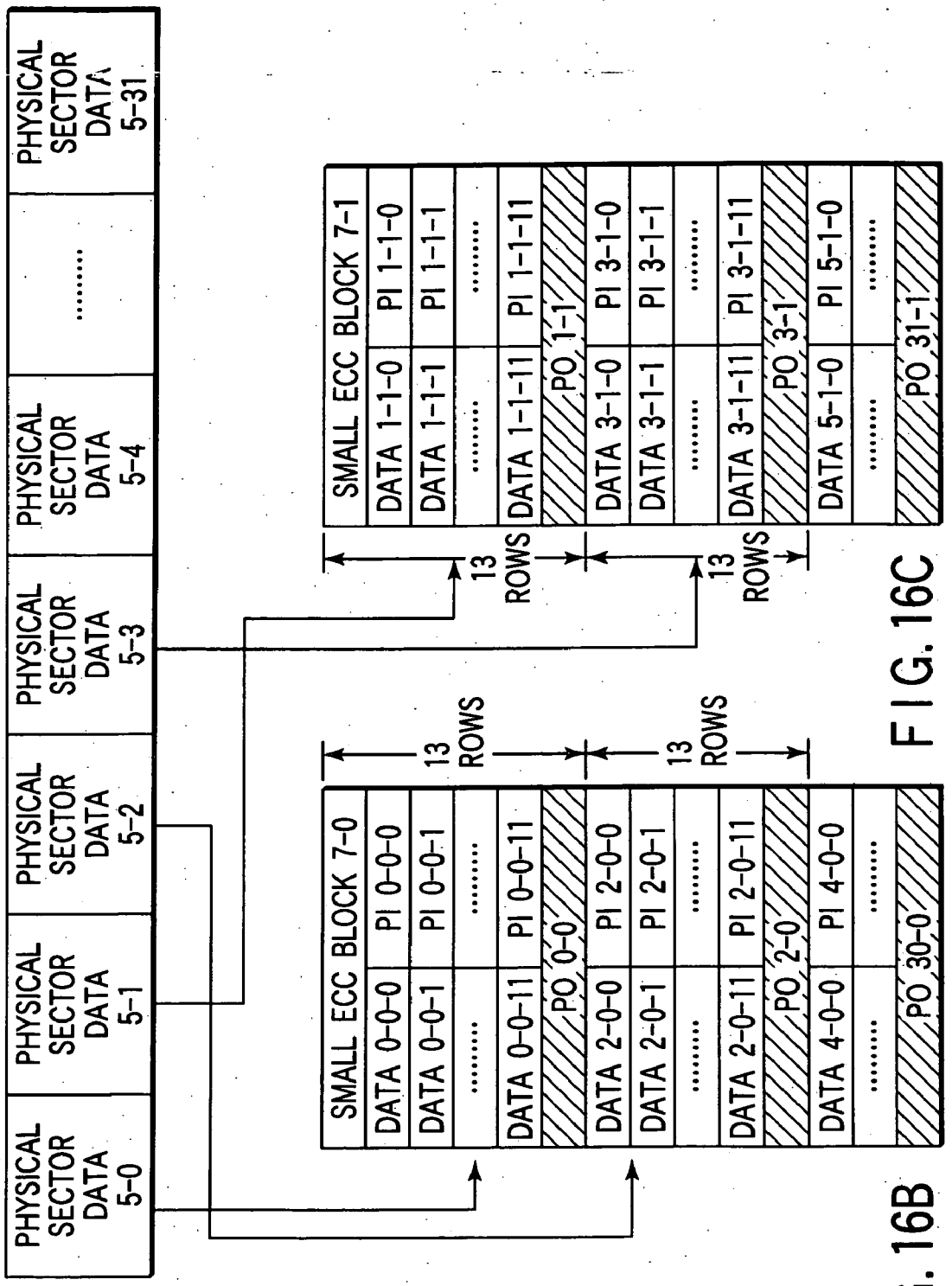


FIG. 16A

FIG. 16B

FIG. 16C

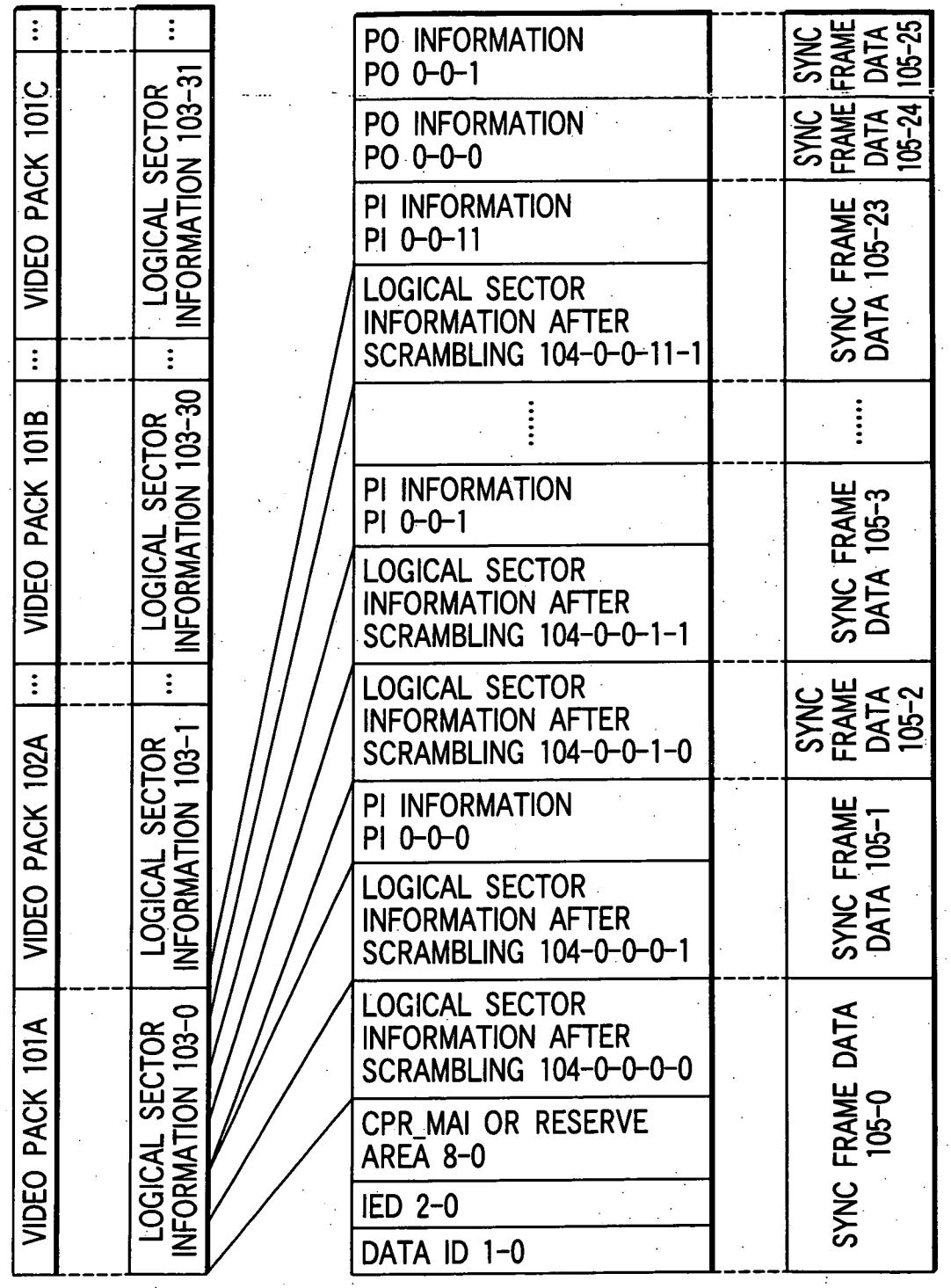


FIG. 17A FIG. 17B FIG. 17C FIG. 17D

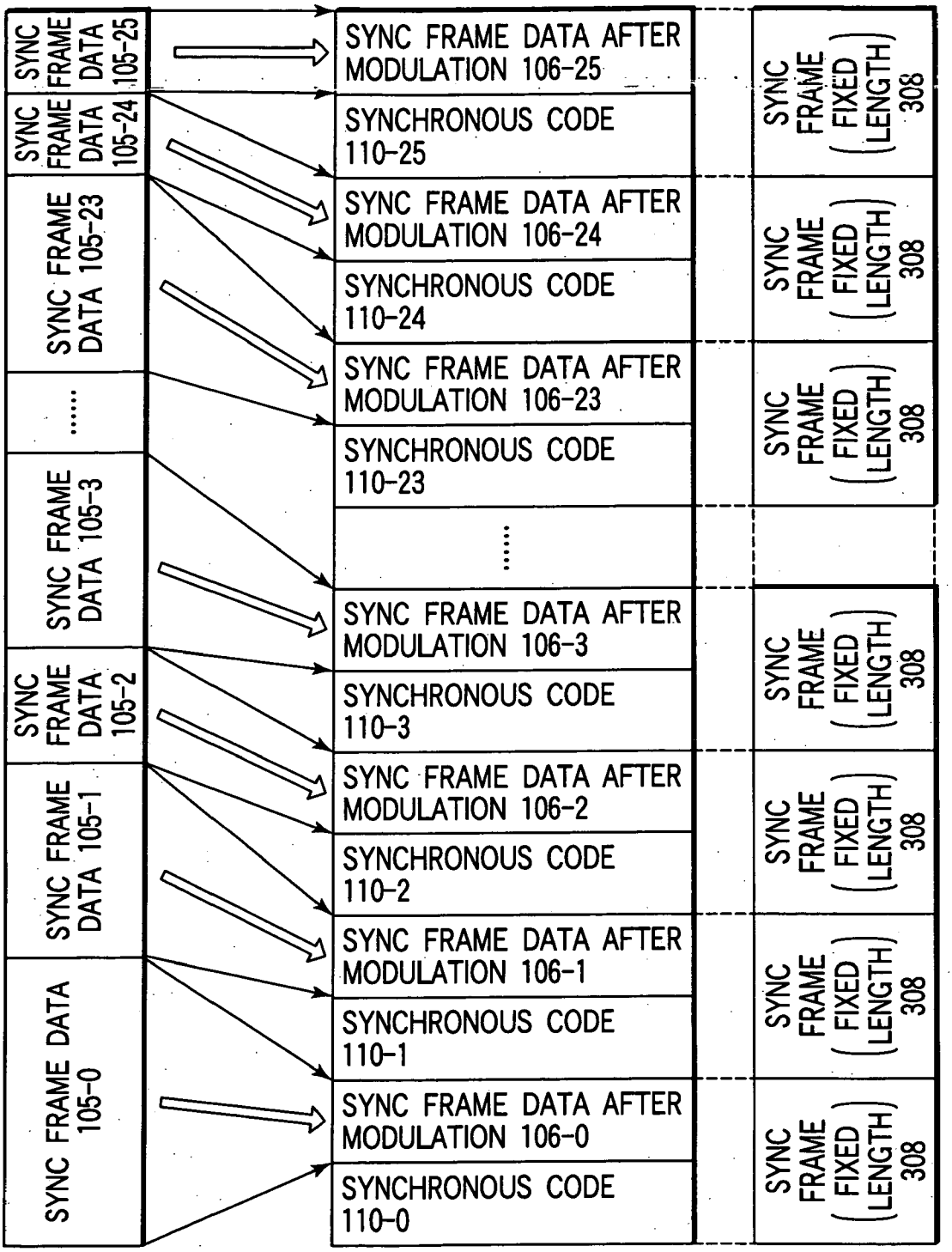


FIG. 18A FIG. 18B FIG. 18C

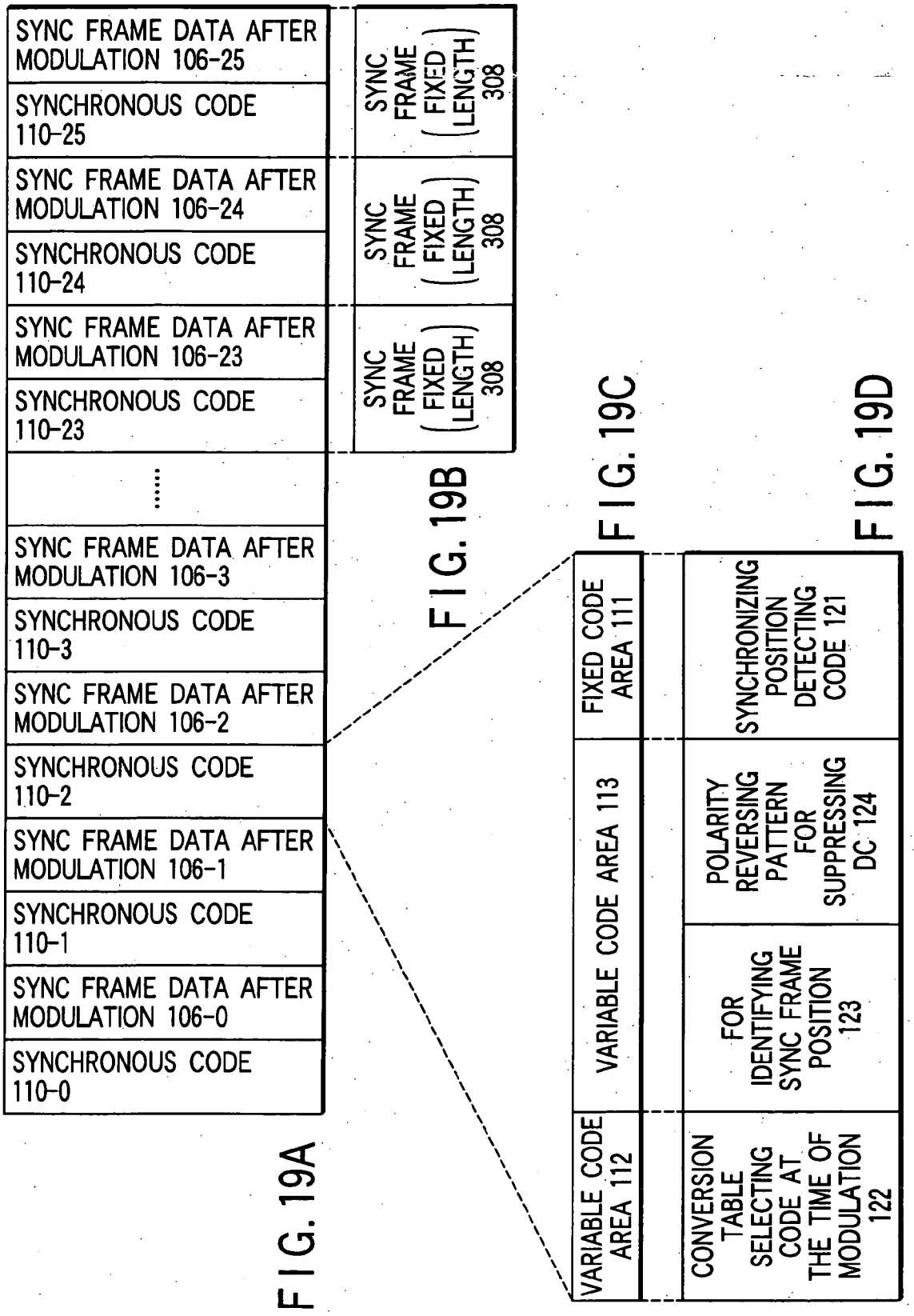


FIG. 19A

FIG. 19B

FIG. 19C

FIG. 19D

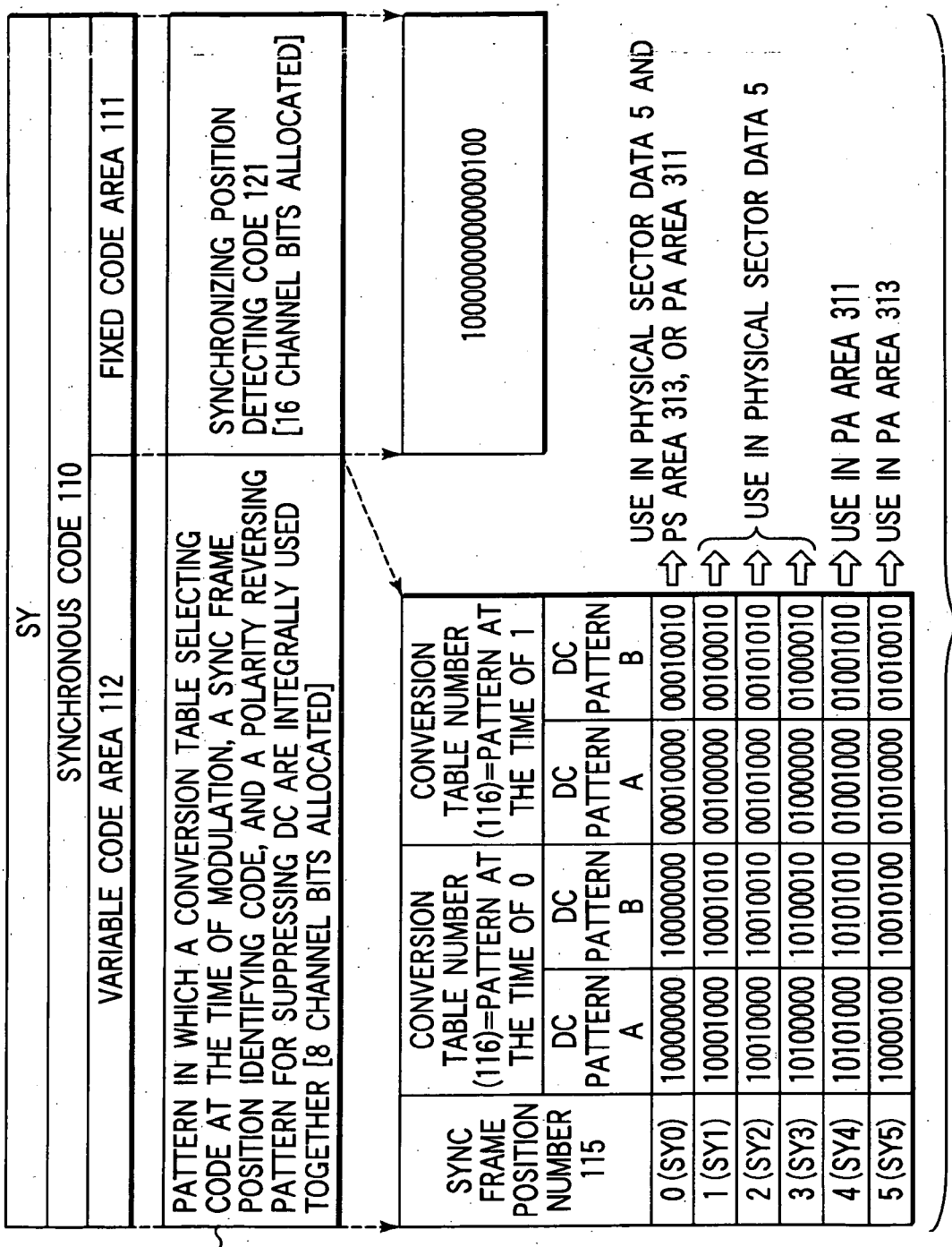


FIG. 20A

FIG. 20B

FIG. 20C

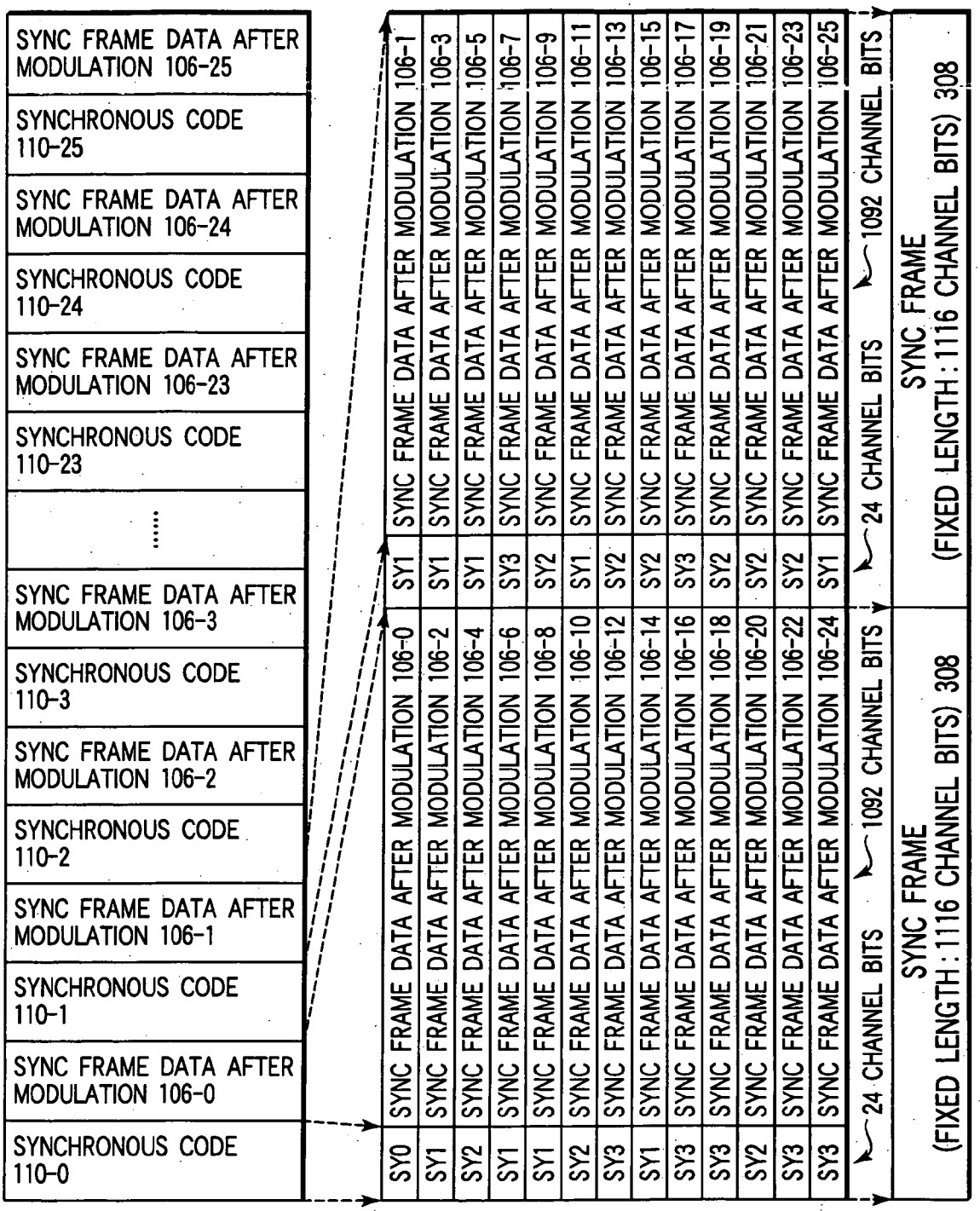


FIG. 21A

FIG. 21B

FIG. 21C

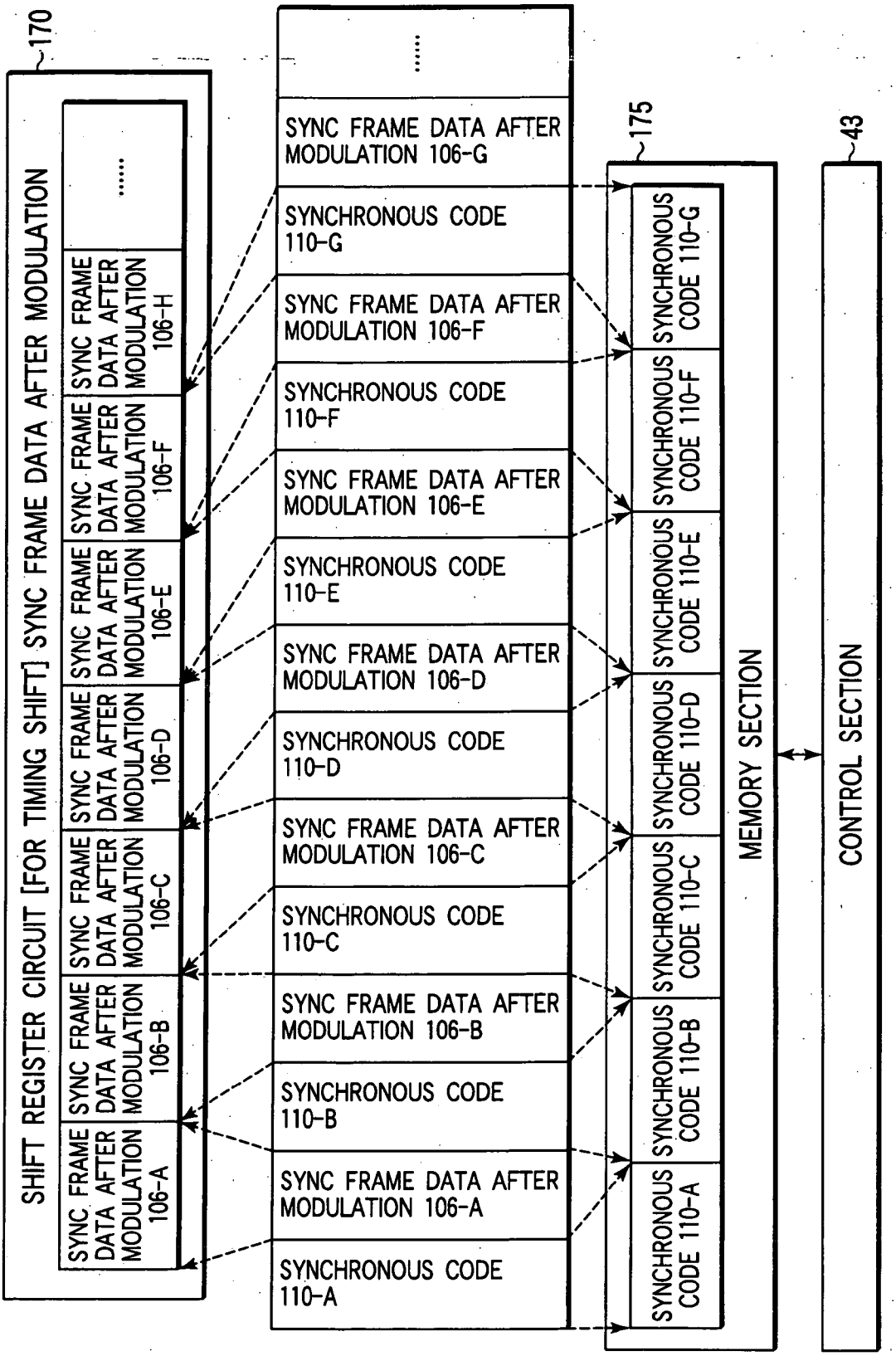

170
SHIFT REGISTER CIRCUIT [FOR TIMING SHIFT] SYNC FRAME DATA AFTER MODULATION
SYNC FRAME DATA AFTER MODULATION 106-A
SYNC FRAME DATA AFTER MODULATION 106-B
SYNC FRAME DATA AFTER MODULATION 106-C
SYNC FRAME DATA AFTER MODULATION 106-D
SYNC FRAME DATA AFTER MODULATION 106-E
SYNC FRAME DATA AFTER MODULATION 106-F
SYNC FRAME DATA AFTER MODULATION 106-H
SYNC FRAME DATA AFTER MODULATION 106-G
SYNCHRONOUS CODE 110-A
SYNC FRAME DATA AFTER MODULATION 106-A
SYNCHRONOUS CODE 110-B
SYNC FRAME DATA AFTER MODULATION 106-B
SYNCHRONOUS CODE 110-C
SYNC FRAME DATA AFTER MODULATION 106-C
SYNCHRONOUS CODE 110-D
SYNC FRAME DATA AFTER MODULATION 106-D
SYNCHRONOUS CODE 110-E
SYNC FRAME DATA AFTER MODULATION 106-E
SYNCHRONOUS CODE 110-F
SYNC FRAME DATA AFTER MODULATION 106-F
SYNCHRONOUS CODE 110-G
SYNC FRAME DATA AFTER MODULATION 106-G
175
SYNCHRONOUS CODE 110-A
SYNCHRONOUS CODE 110-B
SYNCHRONOUS CODE 110-C
SYNCHRONOUS CODE 110-D
SYNCHRONOUS CODE 110-E
SYNCHRONOUS CODE 110-F
SYNCHRONOUS CODE 110-G
MEMORY SECTION
43
CONTROL SECTION

FIG. 22

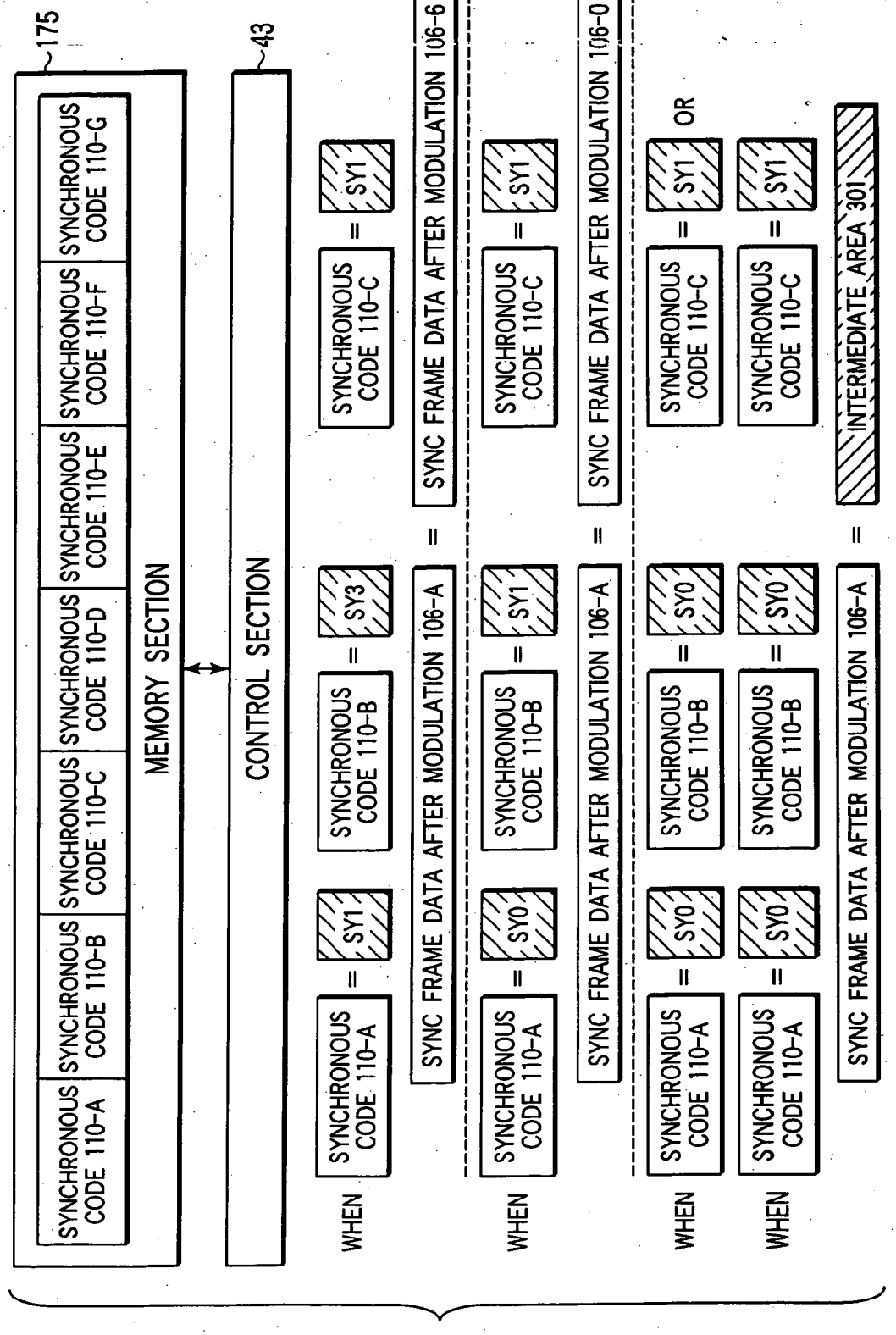

175
MEMORY SECTION
SYNCHRONOUS CODE 110-A
SYNCHRONOUS CODE 110-B
SYNCHRONOUS CODE 110-C
SYNCHRONOUS CODE 110-D
SYNCHRONOUS CODE 110-E
SYNCHRONOUS CODE 110-F
SYNCHRONOUS CODE 110-G
43
CONTROL SECTION
WHEN
SYNCHRONOUS CODE 110-A = SY1
SYNCHRONOUS CODE 110-B = SY3
SYNCHRONOUS CODE 110-C = SY1
= SYNC FRAME DATA AFTER MODULATION 106-6
SYNC FRAME DATA AFTER MODULATION 106-A
WHEN
SYNCHRONOUS CODE 110-A = SY0
SYNCHRONOUS CODE 110-B = SY1
SYNCHRONOUS CODE 110-C = SY1
=
SYNC FRAME DATA AFTER MODULATION 106-A
WHEN
SYNCHRONOUS CODE 110-A = SY0
SYNCHRONOUS CODE 110-B = SY0
SYNCHRONOUS CODE 110-C = SY1 OR
=
SYNC FRAME DATA AFTER MODULATION 106-0
WHEN
SYNCHRONOUS CODE 110-A = SY0
SYNCHRONOUS CODE 110-B = SY0
SYNCHRONOUS CODE 110-C = SY1
=
SYNC FRAME DATA AFTER MODULATION 106-A
INTERMEDIATE AREA 301

FIG. 23

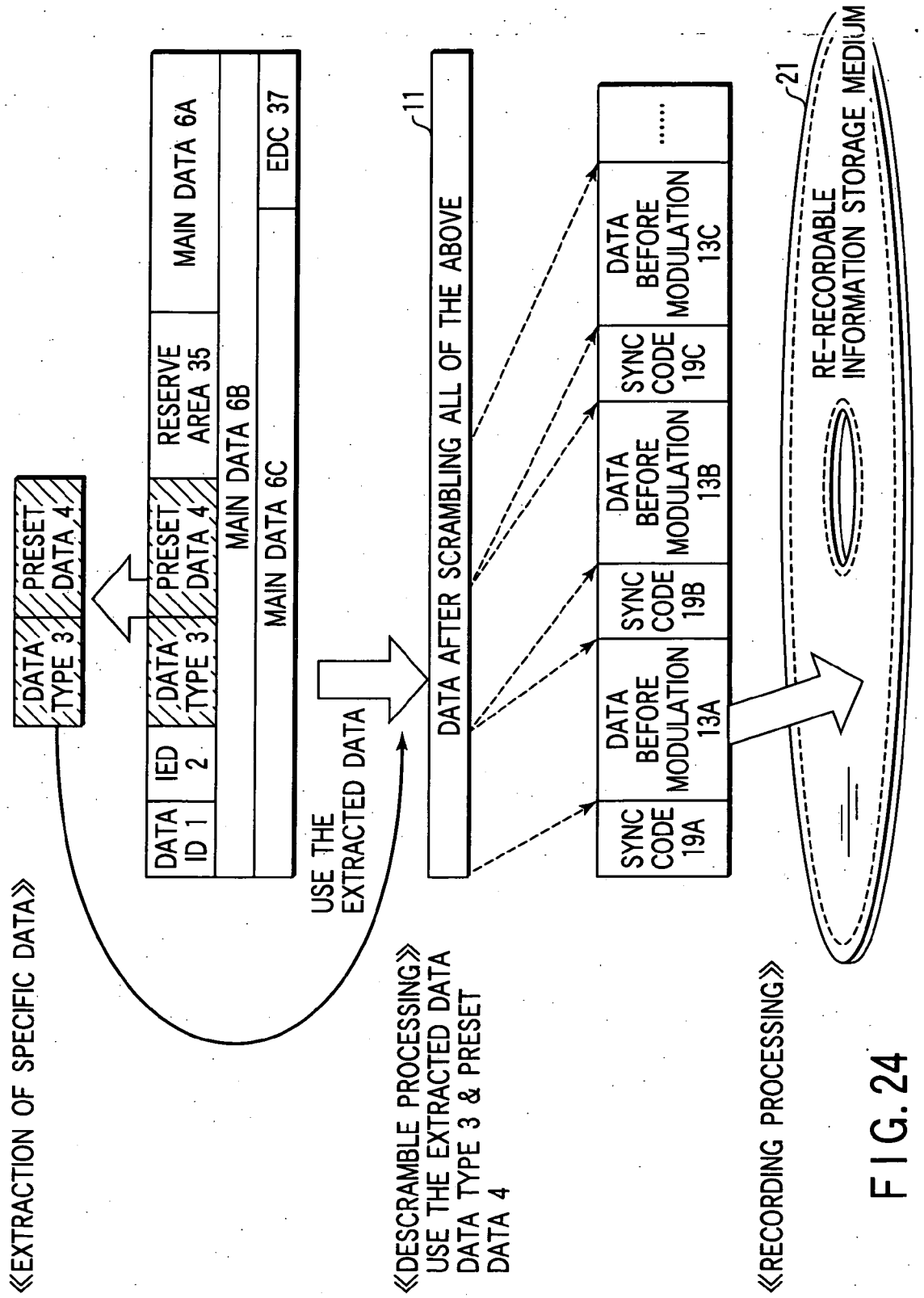

«EXTRACTION OF SPECIFIC DATA»
DATA TYPE 3
PRESET DATA 4
DATA ID 1
IED 2
DATA TYPE 3
PRESET DATA 4
RESERVE AREA 35
MAIN DATA 6A
MAIN DATA 6B
MAIN DATA 6C
EDC 37
USE THE EXTRACTED DATA
«DESCRAMBLE PROCESSING»
USE THE EXTRACTED DATA
DATA TYPE 3 & PRESET DATA 4
11
DATA AFTER SCRAMBLING ALL OF THE ABOVE
SYNC CODE 19A
DATA BEFORE MODULATION 13A
SYNC CODE 19B
DATA BEFORE MODULATION 13B
SYNC CODE 19C
DATA BEFORE MODULATION 13C
.....
«RECORDING PROCESSING»
21
RE-RECORDABLE INFORMATION STORAGE MEDIUM

FIG. 24

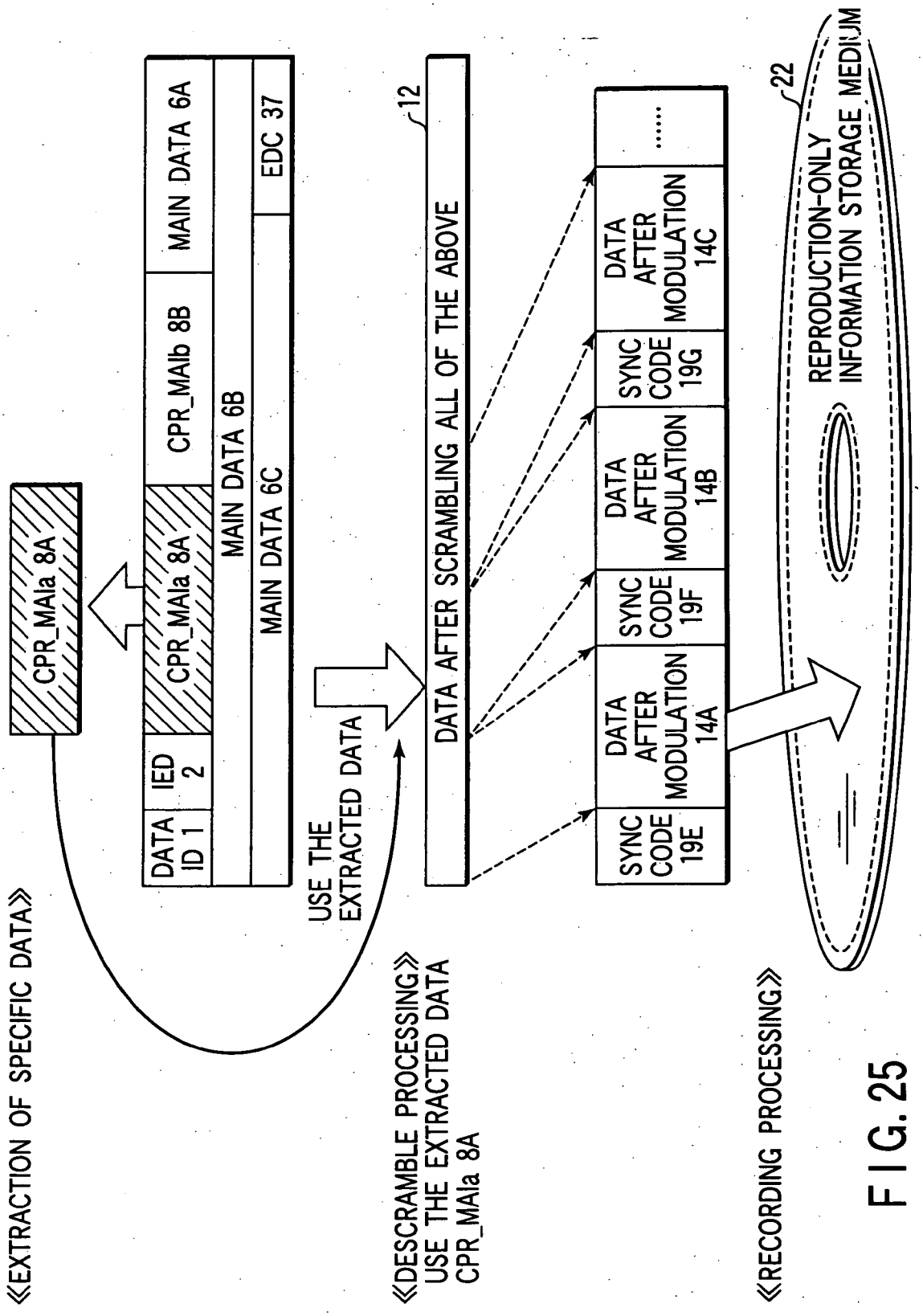

«EXTRACTION OF SPECIFIC DATA»
CPR_MAIa 8A
DATA ID 1
IED 2
CPR_MAIa 8A
CPR_MAIb 8B
MAIN DATA 6A
MAIN DATA 6B
MAIN DATA 6C
EDC 37
USE THE EXTRACTED DATA
«DESCRAMBLE PROCESSING» USE THE EXTRACTED DATA CPR_MAIa 8A
12
DATA AFTER SCRAMBLING ALL OF THE ABOVE
SYNC CODE 19E
DATA AFTER MODULATION 14A
SYNC CODE 19F
DATA AFTER MODULATION 14B
SYNC CODE 19G
DATA AFTER MODULATION 14C
.....
«RECORDING PROCESSING»
22
REPRODUCTION-ONLY INFORMATION STORAGE MEDIUM

FIG. 25

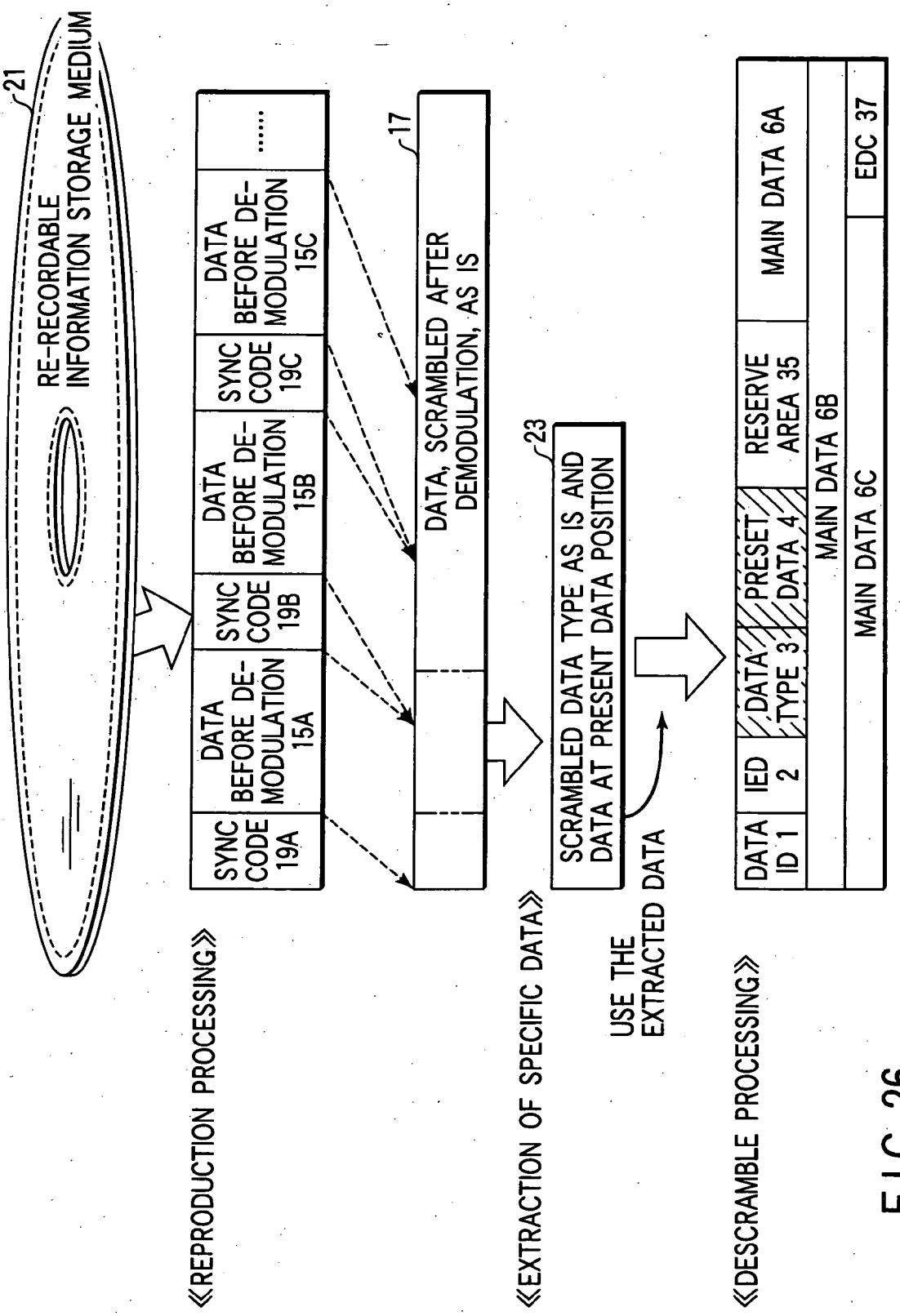

21
RE-RECORDABLE INFORMATION STORAGE MEDIUM
«REPRODUCTION PROCESSING»
SYNC CODE 19A
DATA BEFORE DE-MODULATION 15A
SYNC CODE 19B
DATA BEFORE DE-MODULATION 15B
SYNC CODE 19C
DATA BEFORE DE-MODULATION 15C
.....
17
DATA, SCRAMBLED AFTER DEMODULATION, AS IS
«EXTRACTION OF SPECIFIC DATA»
23
SCRAMBLED DATA TYPE AS IS AND DATA AT PRESENT DATA POSITION
USE THE EXTRACTED DATA
«DESCRAMBLE PROCESSING»
DATA ID 1
IED 2
DATA TYPE 3
PRESET DATA 4
RESERVE AREA 35
MAIN DATA 6A
MAIN DATA 6B
MAIN DATA 6C
EDC 37

FIG. 26

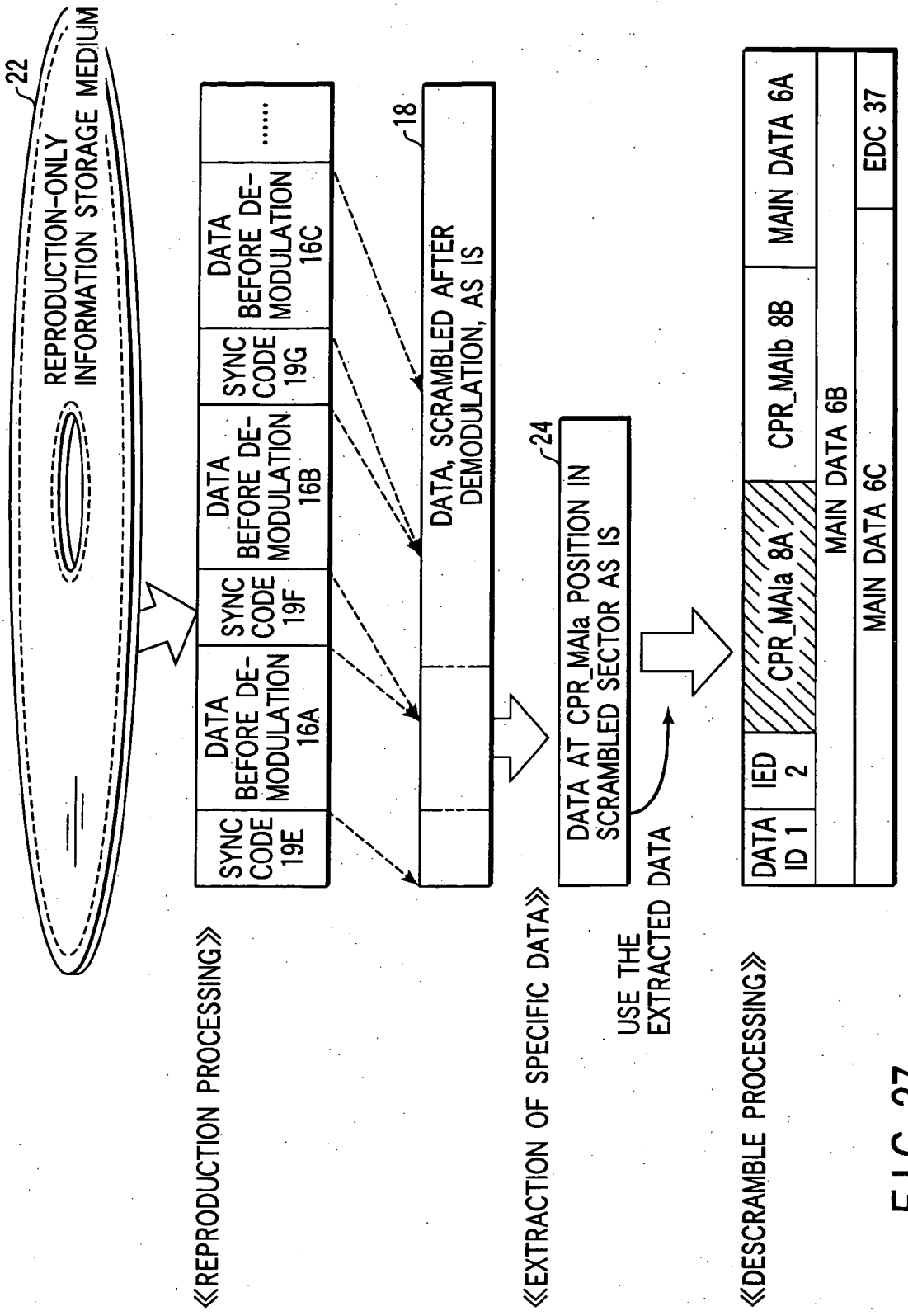

22
REPRODUCTION-ONLY INFORMATION STORAGE MEDIUM
SYNC CODE 19E
DATA BEFORE DE-MODULATION 16A
SYNC CODE 19F
DATA BEFORE DE-MODULATION 16B
SYNC CODE 19G
DATA BEFORE DE-MODULATION 16C
.....
18
DATA, SCRAMBLED AFTER DEMODULATION, AS IS
24
DATA AT CPR_MAIa POSITION IN SCRAMBLED SECTOR AS IS
USE THE EXTRACTED DATA
DATA ID 1
IED 2
CPR_MAIa 8A
CPR_MAIb 8B
MAIN DATA 6A
MAIN DATA 6B
MAIN DATA 6C
EDC 37
《REPRODUCTION PROCESSING》
《EXTRACTION OF SPECIFIC DATA》
《DESCRAMBLE PROCESSING》

FIG. 27

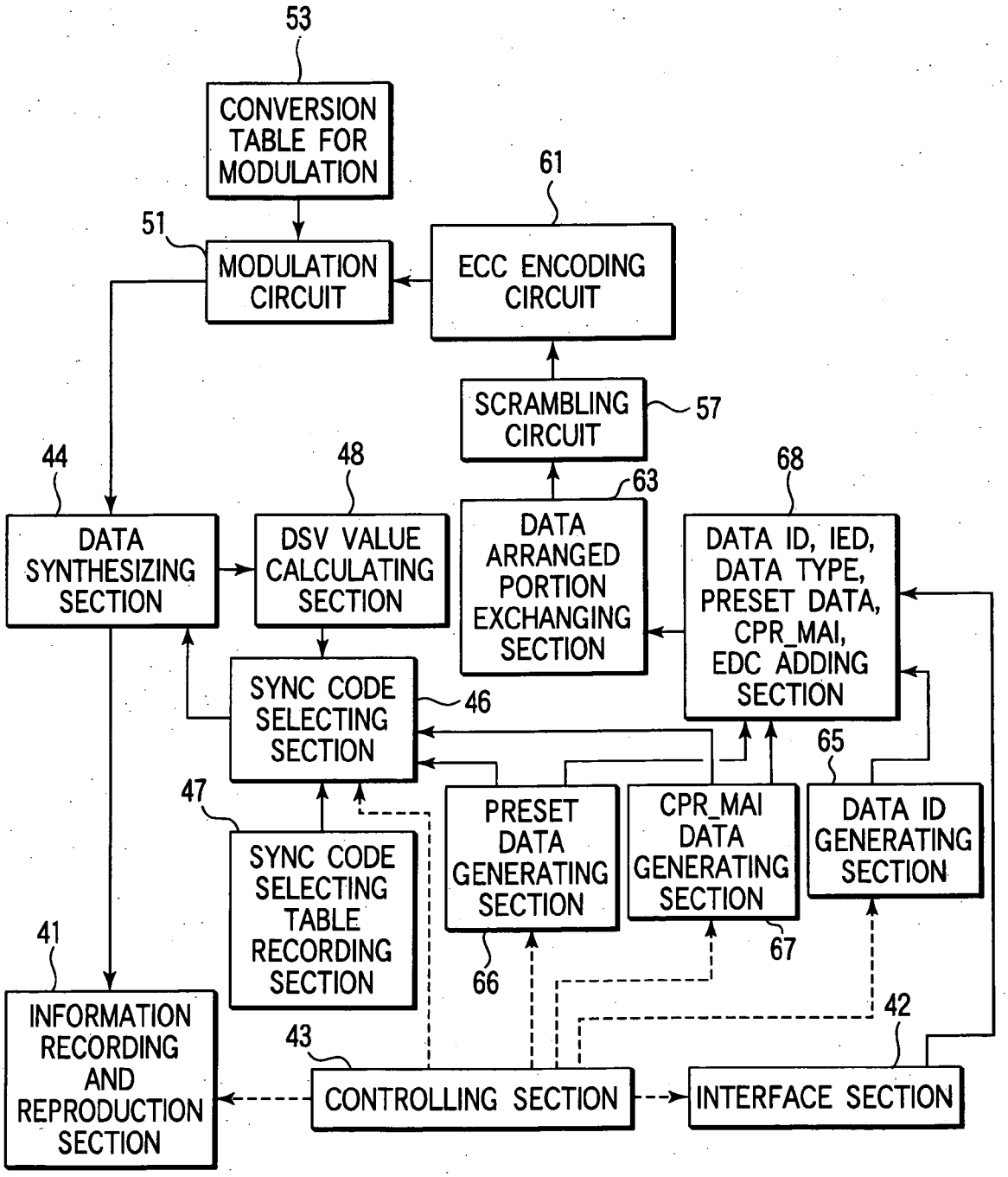

53
CONVERSION TABLE FOR MODULATION
61
51
MODULATION CIRCUIT
ECC ENCODING CIRCUIT
SCRAMBLING CIRCUIT
57
44
48
63
68
DATA SYNTHESIZING SECTION
DSV VALUE CALCULATING SECTION
DATA ARRANGED PORTION EXCHANGING SECTION
DATA ID, IED, DATA TYPE, PRESET DATA, CPR_MAI, EDC ADDING SECTION
SYNC CODE SELECTING SECTION
46
65
47
SYNC CODE SELECTING TABLE RECORDING SECTION
PRESET DATA GENERATING SECTION
CPR_MAI DATA GENERATING SECTION
DATA ID GENERATING SECTION
41
66
67
INFORMATION RECORDING AND REPRODUCTION SECTION
43
42
CONTROLLING SECTION
INTERFACE SECTION

FIG. 28

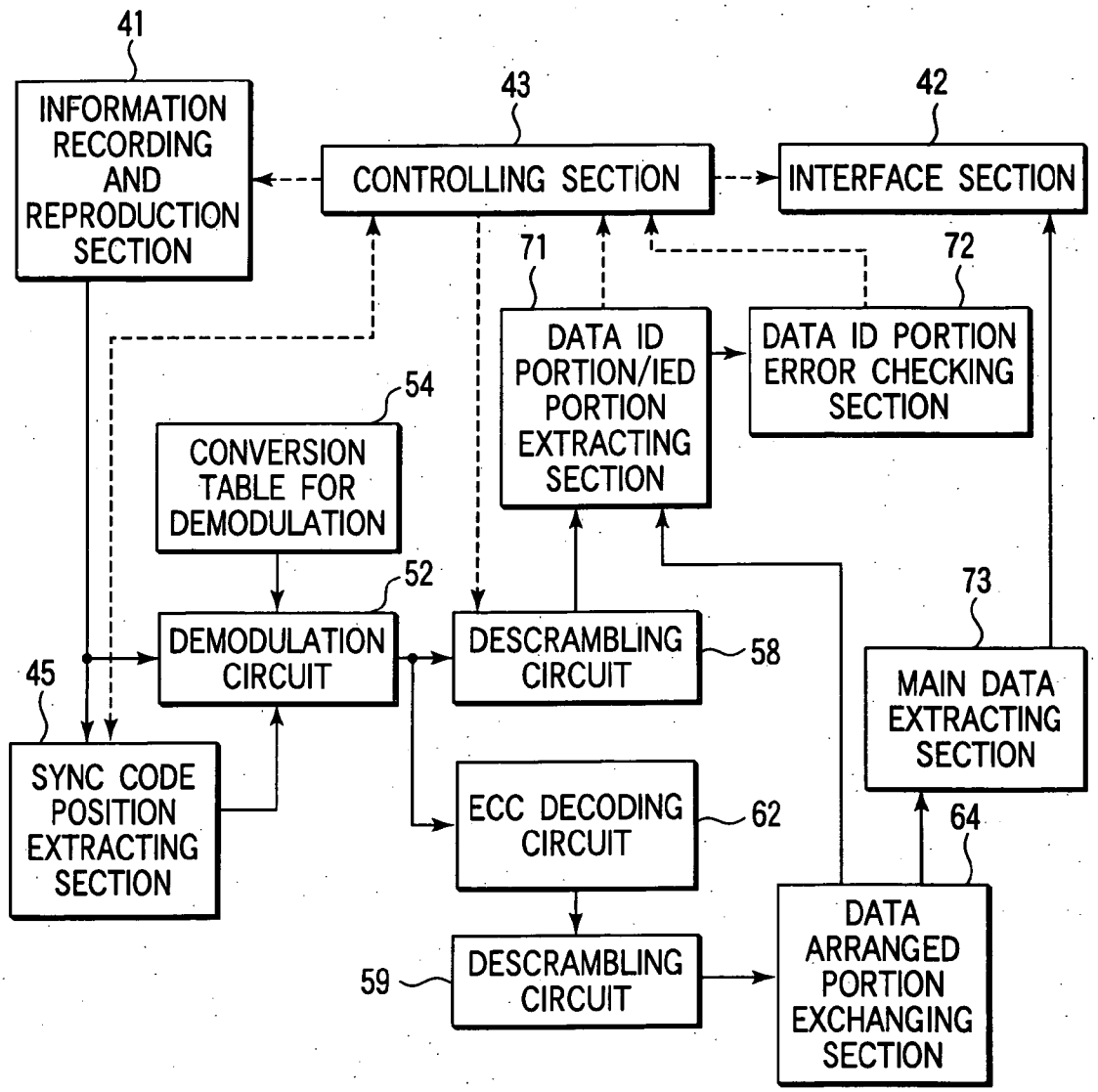

41
INFORMATION RECORDING AND REPRODUCTION SECTION
43
CONTROLLING SECTION
42
INTERFACE SECTION
71
DATA ID PORTION/IED PORTION EXTRACTING SECTION
72
DATA ID PORTION ERROR CHECKING SECTION
54
CONVERSION TABLE FOR DEMODULATION
52
DEMODULATION CIRCUIT
DESCRAMBLING CIRCUIT
58
73
MAIN DATA EXTRACTING SECTION
45
SYNC CODE POSITION EXTRACTING SECTION
ECC DECODING CIRCUIT
62
64
59
DESCRAMBLING CIRCUIT
DATA ARRANGED PORTION EXCHANGING SECTION

FIG. 29

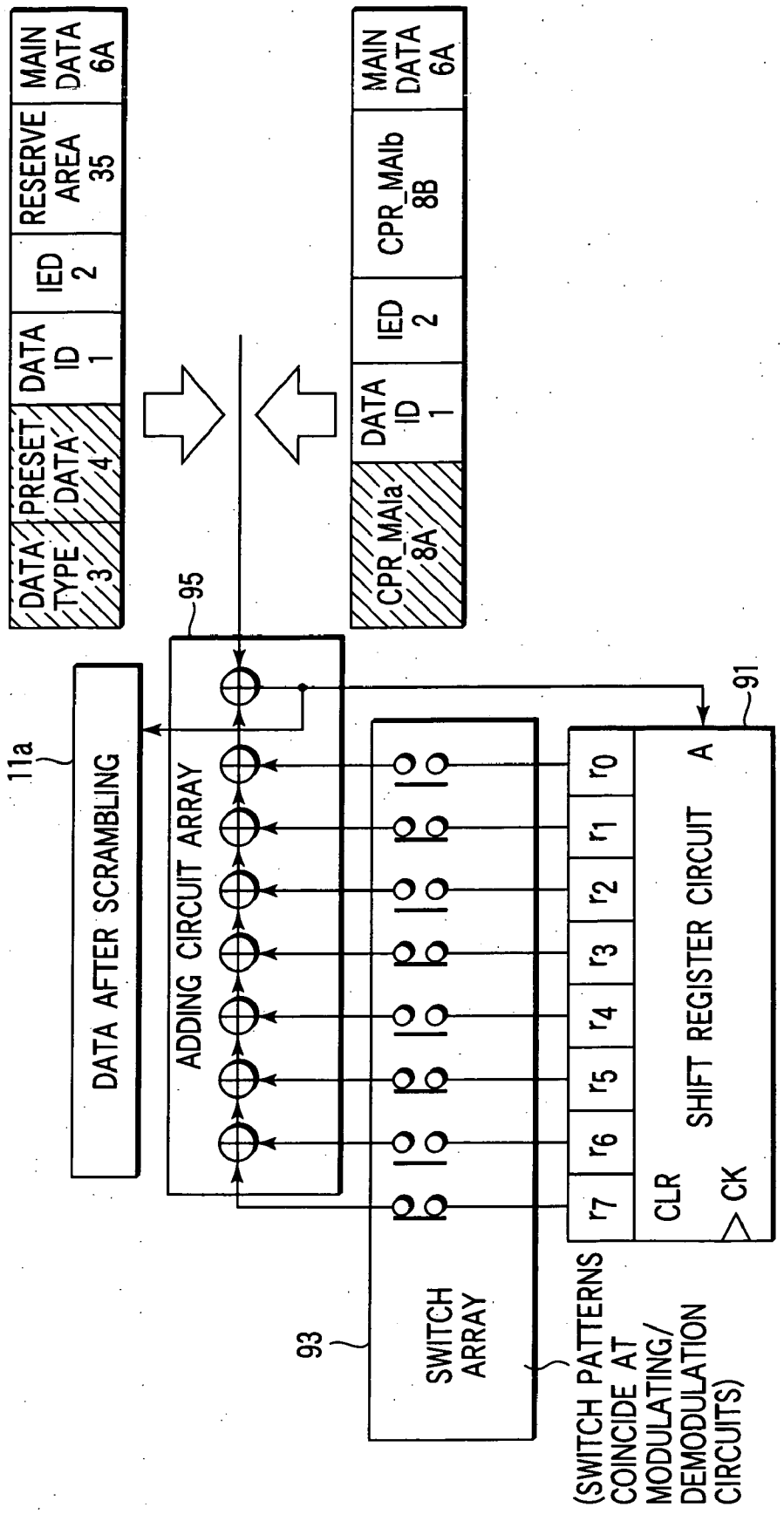

DATA TYPE 3
PRESET DATA 4
DATA ID 1
IED 2
RESERVE AREA 35
MAIN DATA 6A
CPR_MAIa 8A
DATA ID 1
IED 2
CPR_MAIb 8B
MAIN DATA 6A
95
11a
DATA AFTER SCRAMBLING
ADDING CIRCUIT ARRAY
93
SWITCH ARRAY
(SWITCH PATTERNS COINCIDE AT MODULATING/ DEMODULATION CIRCUITS)
91
SHIFT REGISTER CIRCUIT
A
CLR
CK
r0
r1
r2
r3
r4
r5
r6
r7

FIG. 30

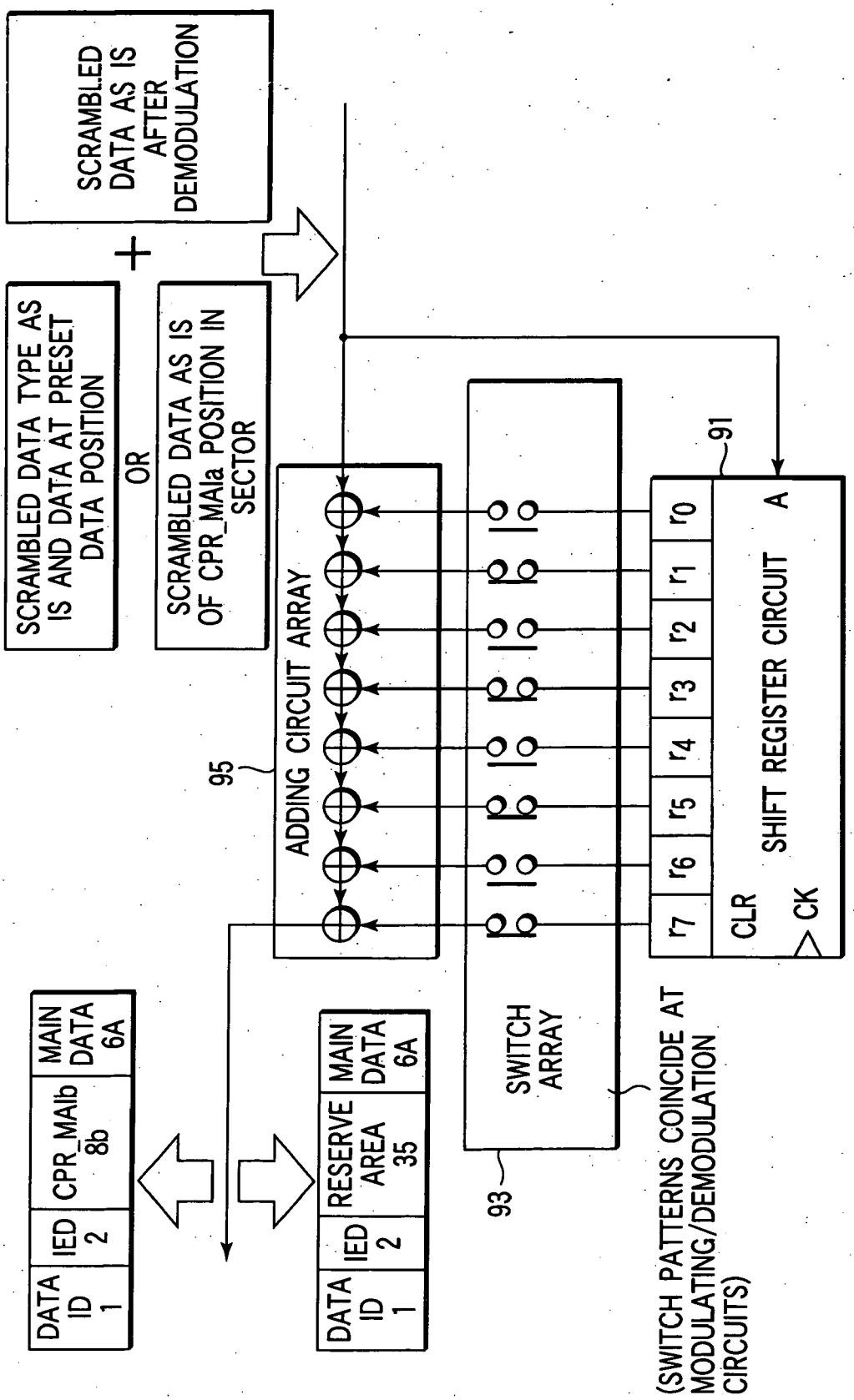

SCRAMBLED DATA AS IS AFTER DEMODULATION
+
SCRAMBLED DATA TYPE AS IS AND DATA AT PRESET DATA POSITION
OR
SCRAMBLED DATA AS IS OF CPR_MAIa POSITION IN SECTOR
95
ADDING CIRCUIT ARRAY
SWITCH ARRAY
93
91
SHIFT REGISTER CIRCUIT
A
CLR
CK
r0
r1
r2
r3
r4
r5
r6
r7
DATA ID 1
IED 2
CPR_MAIb 8b
MAIN DATA 6A
DATA ID 1
IED 2
RESERVE AREA 35
MAIN DATA 6A
(SWITCH PATTERNS COINCIDE AT MODULATING/DEMODULATION CIRCUITS)

FIG. 31

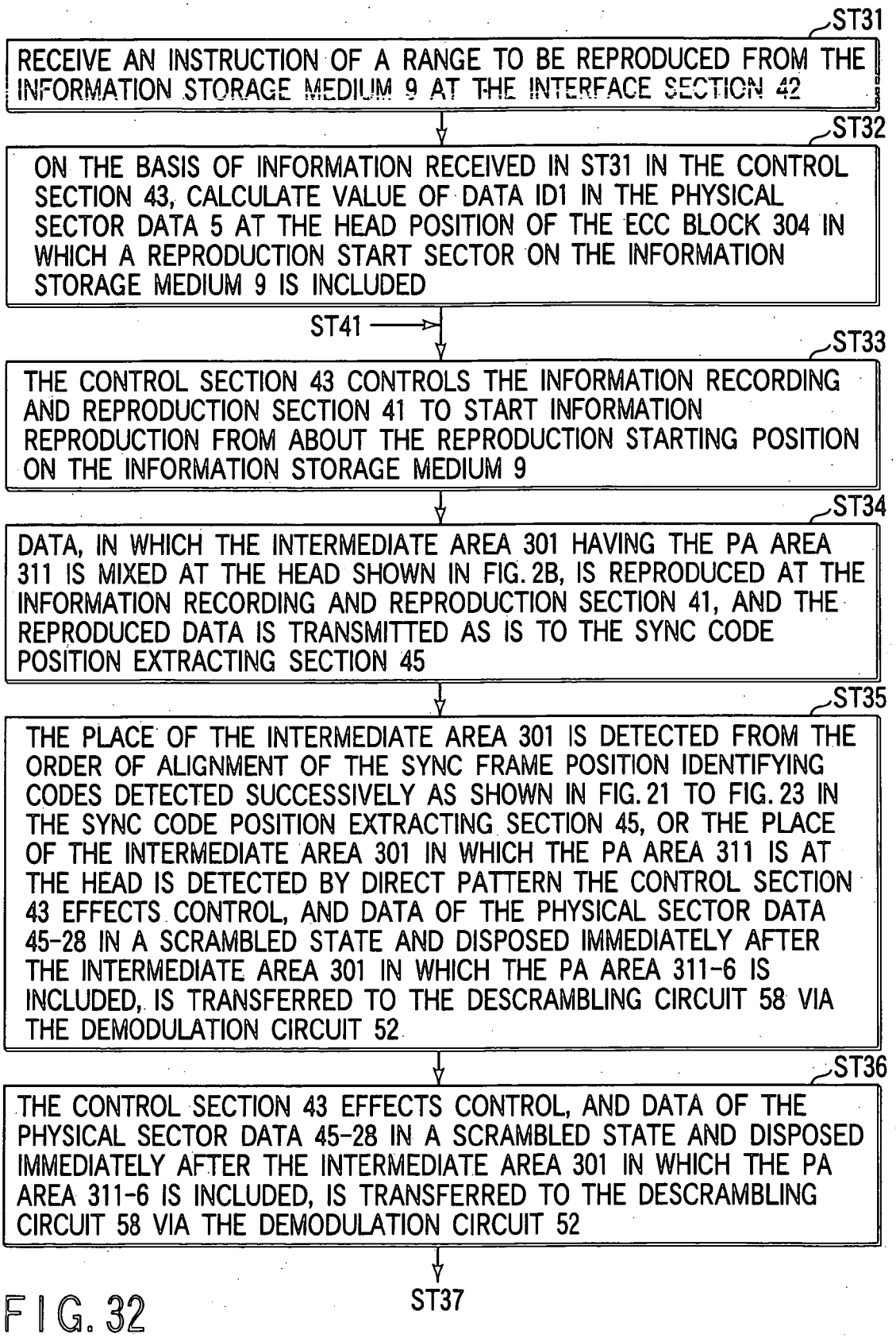

ST31
RECEIVE AN INSTRUCTION OF A RANGE TO BE REPRODUCED FROM THE INFORMATION STORAGE MEDIUM 9 AT THE INTERFACE SECTION 42
ST32
ON THE BASIS OF INFORMATION RECEIVED IN ST31 IN THE CONTROL SECTION 43, CALCULATE VALUE OF DATA ID1 IN THE PHYSICAL SECTOR DATA 5 AT THE HEAD POSITION OF THE ECC BLOCK 304 IN WHICH A REPRODUCTION START SECTOR ON THE INFORMATION STORAGE MEDIUM 9 IS INCLUDED
ST41
ST33
THE CONTROL SECTION 43 CONTROLS THE INFORMATION RECORDING AND REPRODUCTION SECTION 41 TO START INFORMATION REPRODUCTION FROM ABOUT THE REPRODUCTION STARTING POSITION ON THE INFORMATION STORAGE MEDIUM 9
ST34
DATA, IN WHICH THE INTERMEDIATE AREA 301 HAVING THE PA AREA 311 IS MIXED AT THE HEAD SHOWN IN FIG. 2B, IS REPRODUCED AT THE INFORMATION RECORDING AND REPRODUCTION SECTION 41, AND THE REPRODUCED DATA IS TRANSMITTED AS IS TO THE SYNC CODE POSITION EXTRACTING SECTION 45
ST35
THE PLACE OF THE INTERMEDIATE AREA 301 IS DETECTED FROM THE ORDER OF ALIGNMENT OF THE SYNC FRAME POSITION IDENTIFYING CODES DETECTED SUCCESSIVELY AS SHOWN IN FIG. 21 TO FIG. 23 IN THE SYNC CODE POSITION EXTRACTING SECTION 45, OR THE PLACE OF THE INTERMEDIATE AREA 301 IN WHICH THE PA AREA 311 IS AT THE HEAD IS DETECTED BY DIRECT PATTERN THE CONTROL SECTION 43 EFFECTS CONTROL, AND DATA OF THE PHYSICAL SECTOR DATA 45-28 IN A SCRAMBLED STATE AND DISPOSED IMMEDIATELY AFTER THE INTERMEDIATE AREA 301 IN WHICH THE PA AREA 311-6 IS INCLUDED, IS TRANSFERRED TO THE DESCRAMBLING CIRCUIT 58 VIA THE DEMODULATION CIRCUIT 52
ST36
THE CONTROL SECTION 43 EFFECTS CONTROL, AND DATA OF THE PHYSICAL SECTOR DATA 45-28 IN A SCRAMBLED STATE AND DISPOSED IMMEDIATELY AFTER THE INTERMEDIATE AREA 301 IN WHICH THE PA AREA 311-6 IS INCLUDED, IS TRANSFERRED TO THE DESCRAMBLING CIRCUIT 58 VIA THE DEMODULATION CIRCUIT 52
ST37

FIG. 32

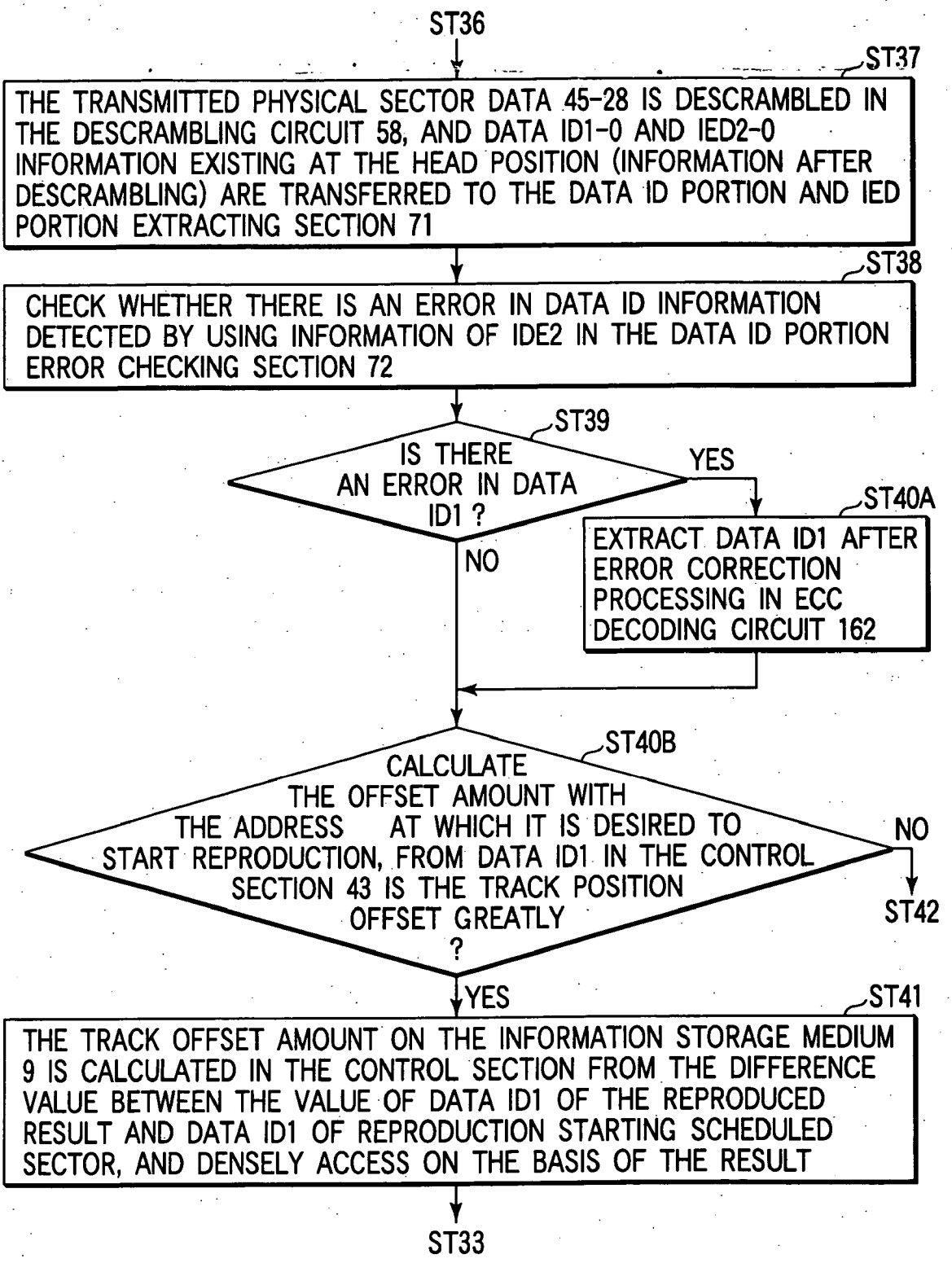

ST36
ST37
THE TRANSMITTED PHYSICAL SECTOR DATA 45-28 IS DESCRAMBLED IN THE DESCRAMBLING CIRCUIT 58, AND DATA ID1-0 AND IED2-0 INFORMATION EXISTING AT THE HEAD POSITION (INFORMATION AFTER DESCRAMBLING) ARE TRANSFERRED TO THE DATA ID PORTION AND IED PORTION EXTRACTING SECTION 71
ST38
CHECK WHETHER THERE IS AN ERROR IN DATA ID INFORMATION DETECTED BY USING INFORMATION OF IDE2 IN THE DATA ID PORTION ERROR CHECKING SECTION 72
ST39
IS THERE AN ERROR IN DATA ID1 ?
YES
NO
ST40A
EXTRACT DATA ID1 AFTER ERROR CORRECTION PROCESSING IN ECC DECODING CIRCUIT 162
ST40B
CALCULATE THE OFFSET AMOUNT WITH THE ADDRESS AT WHICH IT IS DESIRED TO START REPRODUCTION, FROM DATA ID1 IN THE CONTROL SECTION 43 IS THE TRACK POSITION OFFSET GREATLY ?
NO
ST42
YES
ST41
THE TRACK OFFSET AMOUNT ON THE INFORMATION STORAGE MEDIUM 9 IS CALCULATED IN THE CONTROL SECTION FROM THE DIFFERENCE VALUE BETWEEN THE VALUE OF DATA ID1 OF THE REPRODUCED RESULT AND DATA ID1 OF REPRODUCTION STARTING SCHEDULED SECTOR, AND DENSELY ACCESS ON THE BASIS OF THE RESULT
ST33

FIG. 33

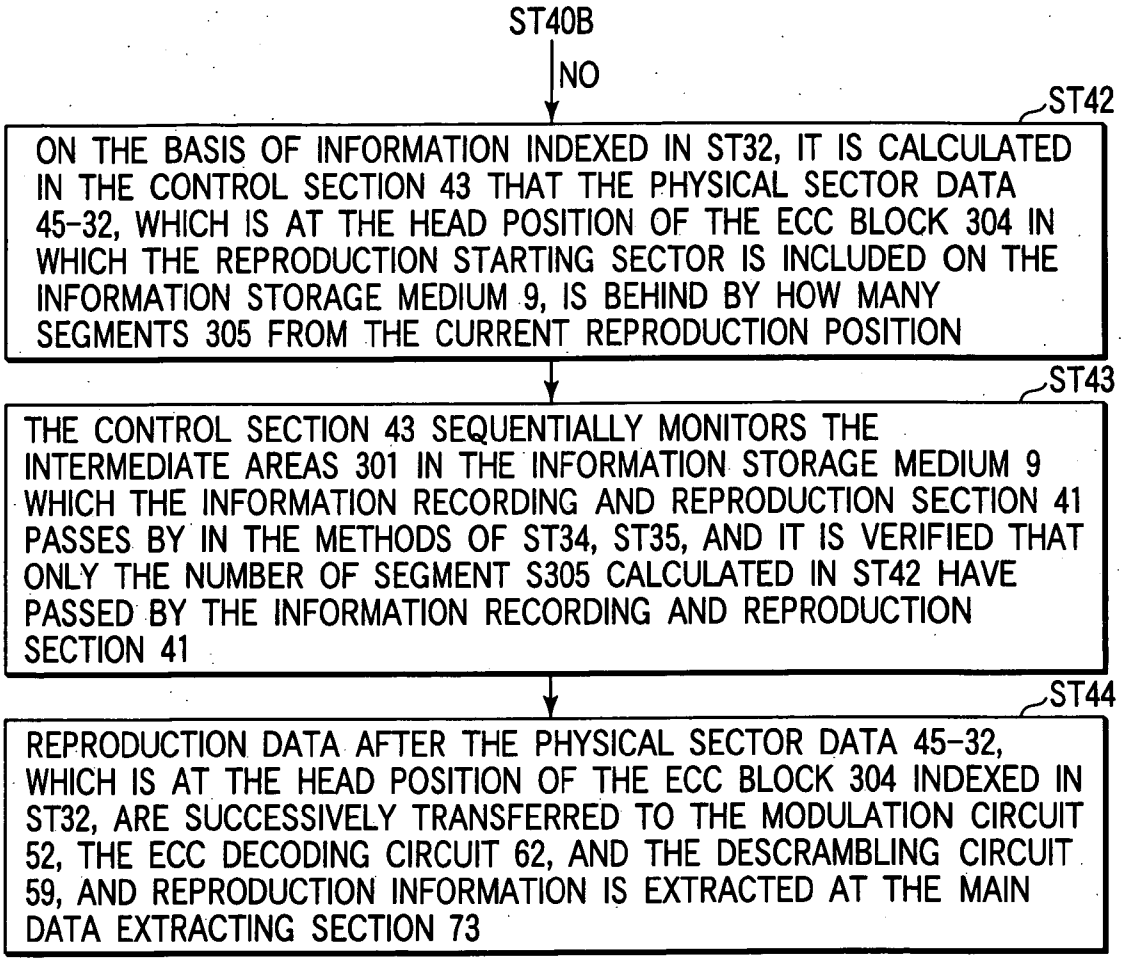

ST40B
NO
ST42
ON THE BASIS OF INFORMATION INDEXED IN ST32, IT IS CALCULATED IN THE CONTROL SECTION 43 THAT THE PHYSICAL SECTOR DATA 45-32, WHICH IS AT THE HEAD POSITION OF THE ECC BLOCK 304 IN WHICH THE REPRODUCTION STARTING SECTOR IS INCLUDED ON THE INFORMATION STORAGE MEDIUM 9, IS BEHIND BY HOW MANY SEGMENTS 305 FROM THE CURRENT REPRODUCTION POSITION
ST43
THE CONTROL SECTION 43 SEQUENTIALLY MONITORS THE INTERMEDIATE AREAS 301 IN THE INFORMATION STORAGE MEDIUM 9 WHICH THE INFORMATION RECORDING AND REPRODUCTION SECTION 41 PASSES BY IN THE METHODS OF ST34, ST35, AND IT IS VERIFIED THAT ONLY THE NUMBER OF SEGMENT S305 CALCULATED IN ST42 HAVE PASSED BY THE INFORMATION RECORDING AND REPRODUCTION SECTION 41
ST44
REPRODUCTION DATA AFTER THE PHYSICAL SECTOR DATA 45-32, WHICH IS AT THE HEAD POSITION OF THE ECC BLOCK 304 INDEXED IN ST32, ARE SUCCESSIVELY TRANSFERRED TO THE MODULATION CIRCUIT 52, THE ECC DECODING CIRCUIT 62, AND THE DESCRAMBLING CIRCUIT 59, AND REPRODUCTION INFORMATION IS EXTRACTED AT THE MAIN DATA EXTRACTING SECTION 73

FIG. 34

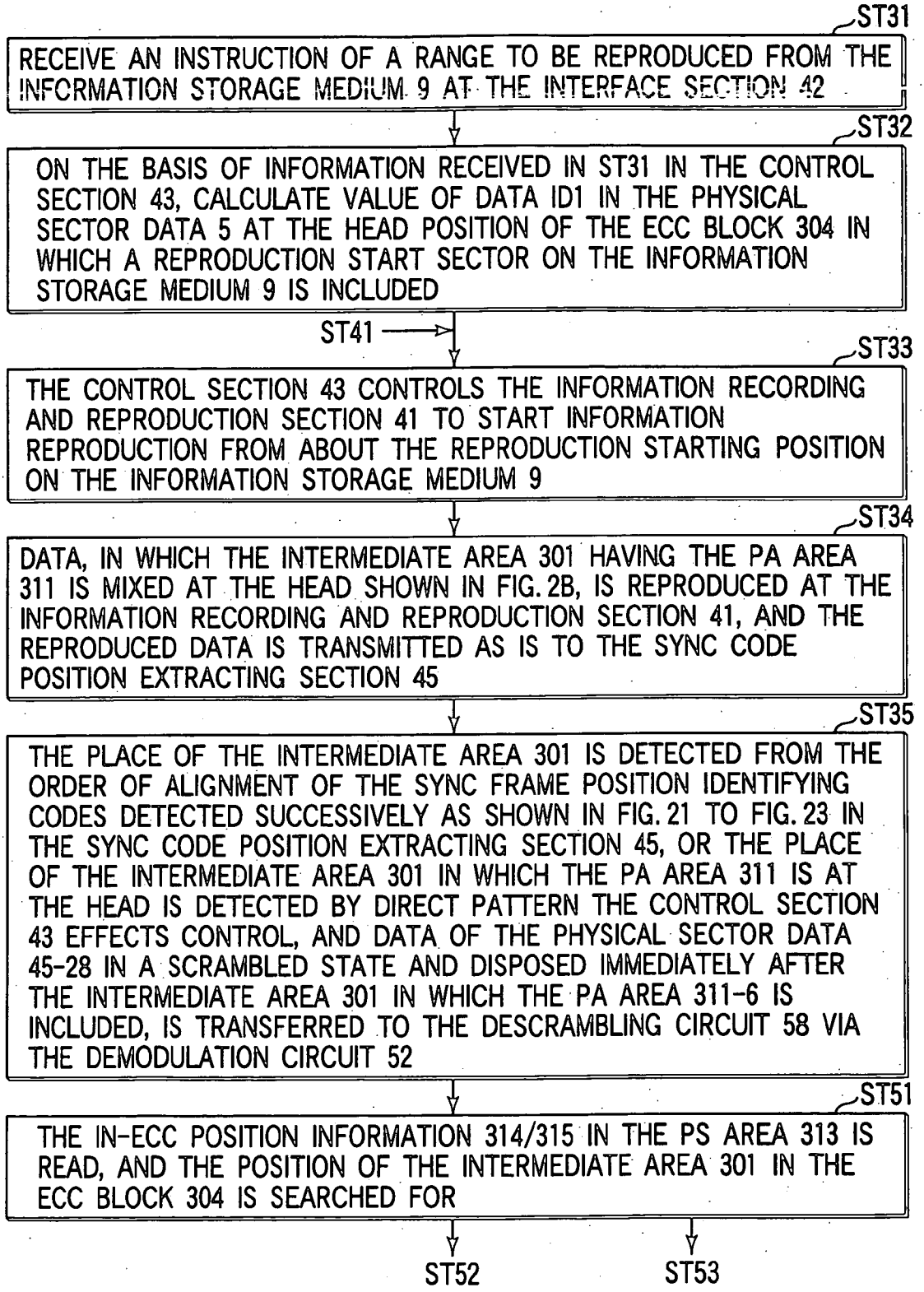

ST31
RECEIVE AN INSTRUCTION OF A RANGE TO BE REPRODUCED FROM THE INFORMATION STORAGE MEDIUM 9 AT THE INTERFACE SECTION 42
ST32
ON THE BASIS OF INFORMATION RECEIVED IN ST31 IN THE CONTROL SECTION 43, CALCULATE VALUE OF DATA ID1 IN THE PHYSICAL SECTOR DATA 5 AT THE HEAD POSITION OF THE ECC BLOCK 304 IN WHICH A REPRODUCTION START SECTOR ON THE INFORMATION STORAGE MEDIUM 9 IS INCLUDED
ST41
ST33
THE CONTROL SECTION 43 CONTROLS THE INFORMATION RECORDING AND REPRODUCTION SECTION 41 TO START INFORMATION REPRODUCTION FROM ABOUT THE REPRODUCTION STARTING POSITION ON THE INFORMATION STORAGE MEDIUM 9
ST34
DATA, IN WHICH THE INTERMEDIATE AREA 301 HAVING THE PA AREA 311 IS MIXED AT THE HEAD SHOWN IN FIG. 2B, IS REPRODUCED AT THE INFORMATION RECORDING AND REPRODUCTION SECTION 41, AND THE REPRODUCED DATA IS TRANSMITTED AS IS TO THE SYNC CODE POSITION EXTRACTING SECTION 45
ST35
THE PLACE OF THE INTERMEDIATE AREA 301 IS DETECTED FROM THE ORDER OF ALIGNMENT OF THE SYNC FRAME POSITION IDENTIFYING CODES DETECTED SUCCESSIVELY AS SHOWN IN FIG. 21 TO FIG. 23 IN THE SYNC CODE POSITION EXTRACTING SECTION 45, OR THE PLACE OF THE INTERMEDIATE AREA 301 IN WHICH THE PA AREA 311 IS AT THE HEAD IS DETECTED BY DIRECT PATTERN THE CONTROL SECTION 43 EFFECTS CONTROL, AND DATA OF THE PHYSICAL SECTOR DATA 45-28 IN A SCRAMBLED STATE AND DISPOSED IMMEDIATELY AFTER THE INTERMEDIATE AREA 301 IN WHICH THE PA AREA 311-6 IS INCLUDED, IS TRANSFERRED TO THE DESCRAMBLING CIRCUIT 58 VIA THE DEMODULATION CIRCUIT 52
ST51
THE IN-ECC POSITION INFORMATION 314/315 IN THE PS AREA 313 IS READ, AND THE POSITION OF THE INTERMEDIATE AREA 301 IN THE ECC BLOCK 304 IS SEARCHED FOR
ST52
ST53

FIG. 35

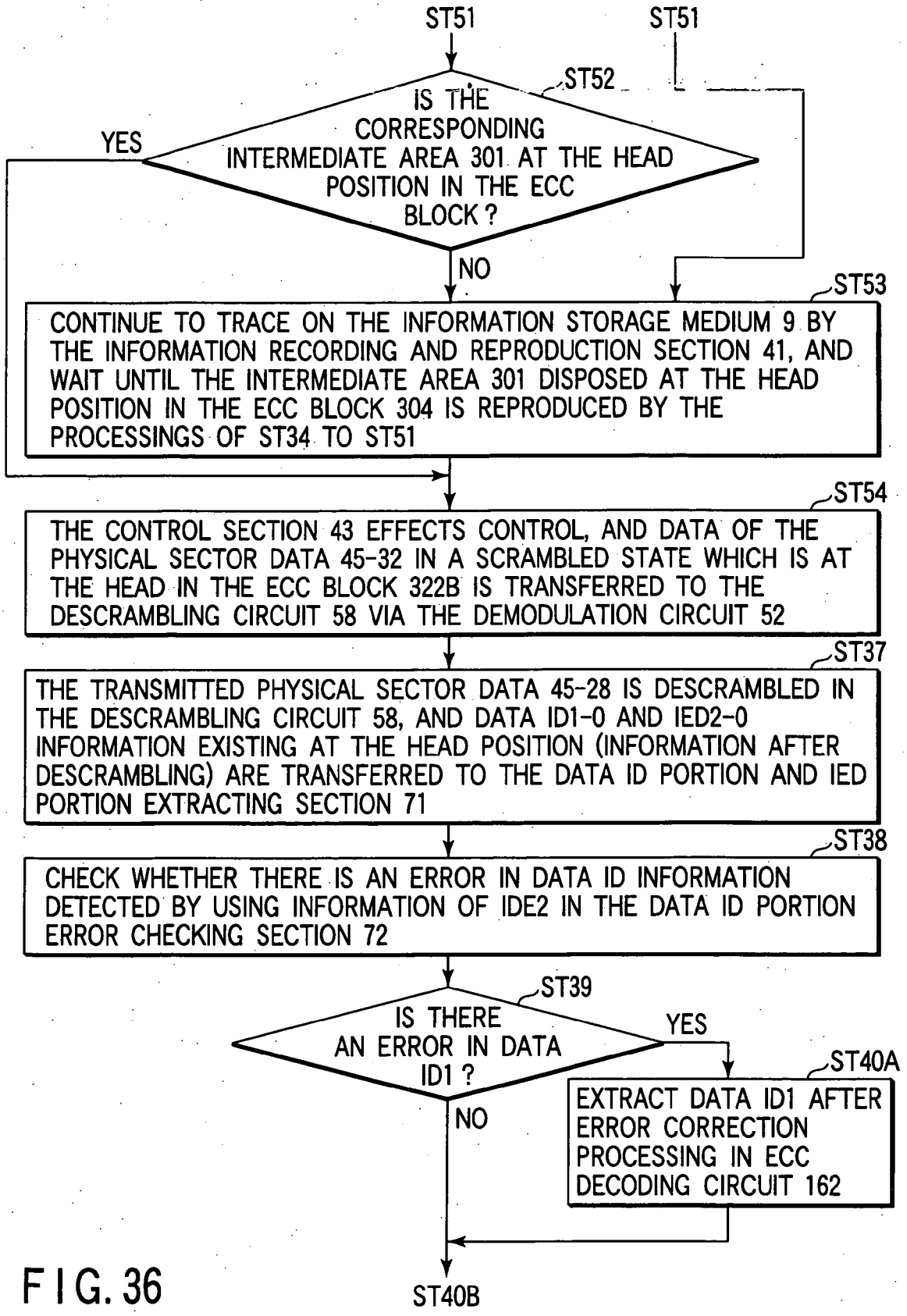

ST51
ST51
ST52
IS THE CORRESPONDING INTERMEDIATE AREA 301 AT THE HEAD POSITION IN THE ECC BLOCK ?
YES
NO
ST53
CONTINUE TO TRACE ON THE INFORMATION STORAGE MEDIUM 9 BY THE INFORMATION RECORDING AND REPRODUCTION SECTION 41, AND WAIT UNTIL THE INTERMEDIATE AREA 301 DISPOSED AT THE HEAD POSITION IN THE ECC BLOCK 304 IS REPRODUCED BY THE PROCESSINGS OF ST34 TO ST51
ST54
THE CONTROL SECTION 43 EFFECTS CONTROL, AND DATA OF THE PHYSICAL SECTOR DATA 45-32 IN A SCRAMBLED STATE WHICH IS AT THE HEAD IN THE ECC BLOCK 322B IS TRANSFERRED TO THE DESCRAMBLING CIRCUIT 58 VIA THE DEMODULATION CIRCUIT 52
ST37
THE TRANSMITTED PHYSICAL SECTOR DATA 45-28 IS DESCRAMBLED IN THE DESCRAMBLING CIRCUIT 58, AND DATA ID1-0 AND IED2-0 INFORMATION EXISTING AT THE HEAD POSITION (INFORMATION AFTER DESCRAMBLING) ARE TRANSFERRED TO THE DATA ID PORTION AND IED PORTION EXTRACTING SECTION 71
ST38
CHECK WHETHER THERE IS AN ERROR IN DATA ID INFORMATION DETECTED BY USING INFORMATION OF IDE2 IN THE DATA ID PORTION ERROR CHECKING SECTION 72
ST39
IS THERE AN ERROR IN DATA ID1 ?
YES
NO
ST40A
EXTRACT DATA ID1 AFTER ERROR CORRECTION PROCESSING IN ECC DECODING CIRCUIT 162
ST40B

FIG. 36

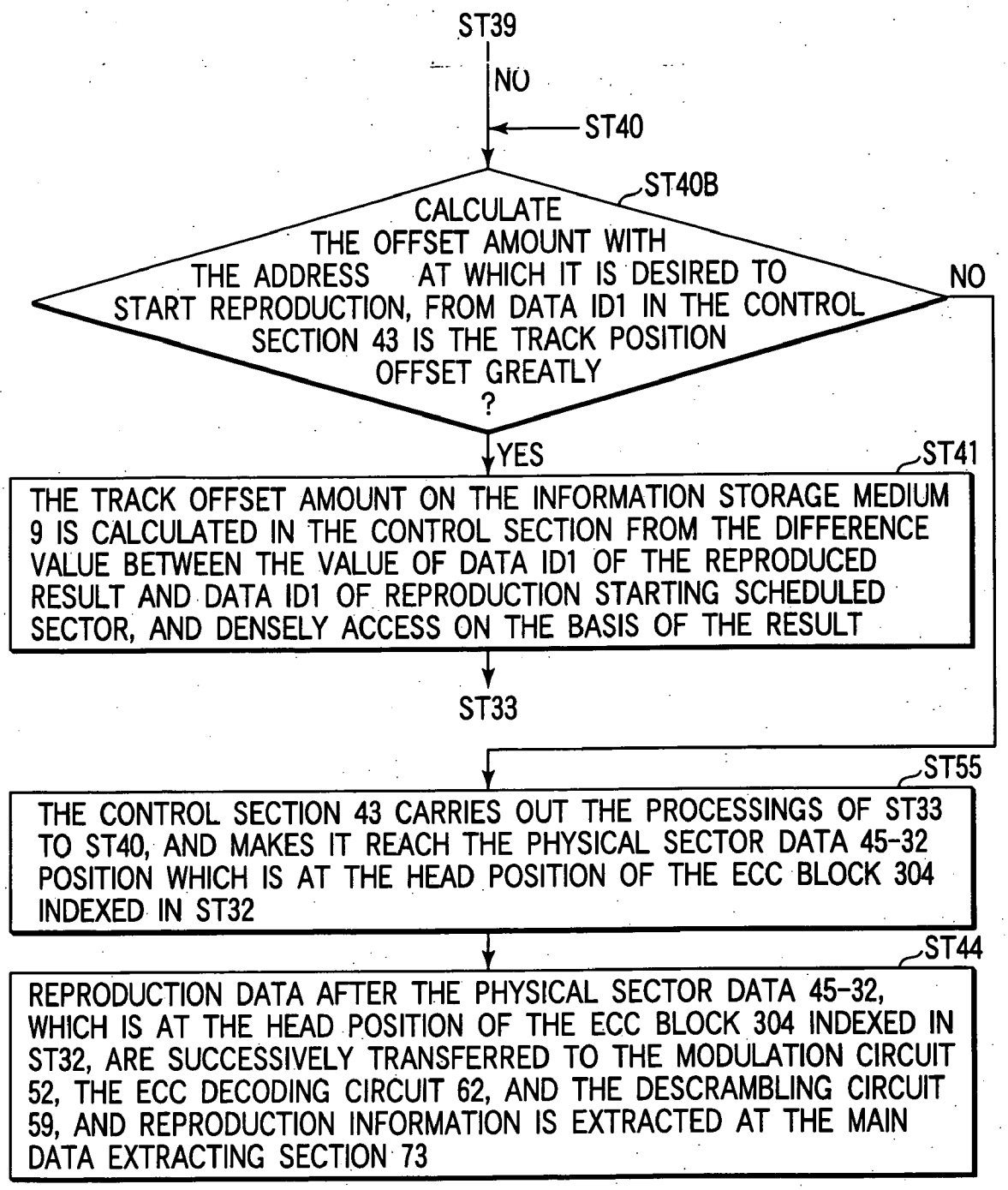

ST39
NO
ST40
ST40B
CALCULATE THE OFFSET AMOUNT WITH THE ADDRESS AT WHICH IT IS DESIRED TO START REPRODUCTION, FROM DATA ID1 IN THE CONTROL SECTION 43 IS THE TRACK POSITION OFFSET GREATLY ?
NO
YES
ST41
THE TRACK OFFSET AMOUNT ON THE INFORMATION STORAGE MEDIUM 9 IS CALCULATED IN THE CONTROL SECTION FROM THE DIFFERENCE VALUE BETWEEN THE VALUE OF DATA ID1 OF THE REPRODUCED RESULT AND DATA ID1 OF REPRODUCTION STARTING SCHEDULED SECTOR, AND DENSELY ACCESS ON THE BASIS OF THE RESULT
ST33
ST55
THE CONTROL SECTION 43 CARRIES OUT THE PROCESSINGS OF ST33 TO ST40, AND MAKES IT REACH THE PHYSICAL SECTOR DATA 45-32 POSITION WHICH IS AT THE HEAD POSITION OF THE ECC BLOCK 304 INDEXED IN ST32
ST44
REPRODUCTION DATA AFTER THE PHYSICAL SECTOR DATA 45-32, WHICH IS AT THE HEAD POSITION OF THE ECC BLOCK 304 INDEXED IN ST32, ARE SUCCESSIVELY TRANSFERRED TO THE MODULATION CIRCUIT 52, THE ECC DECODING CIRCUIT 62, AND THE DESCRAMBLING CIRCUIT 59, AND REPRODUCTION INFORMATION IS EXTRACTED AT THE MAIN DATA EXTRACTING SECTION 73

FIG. 37

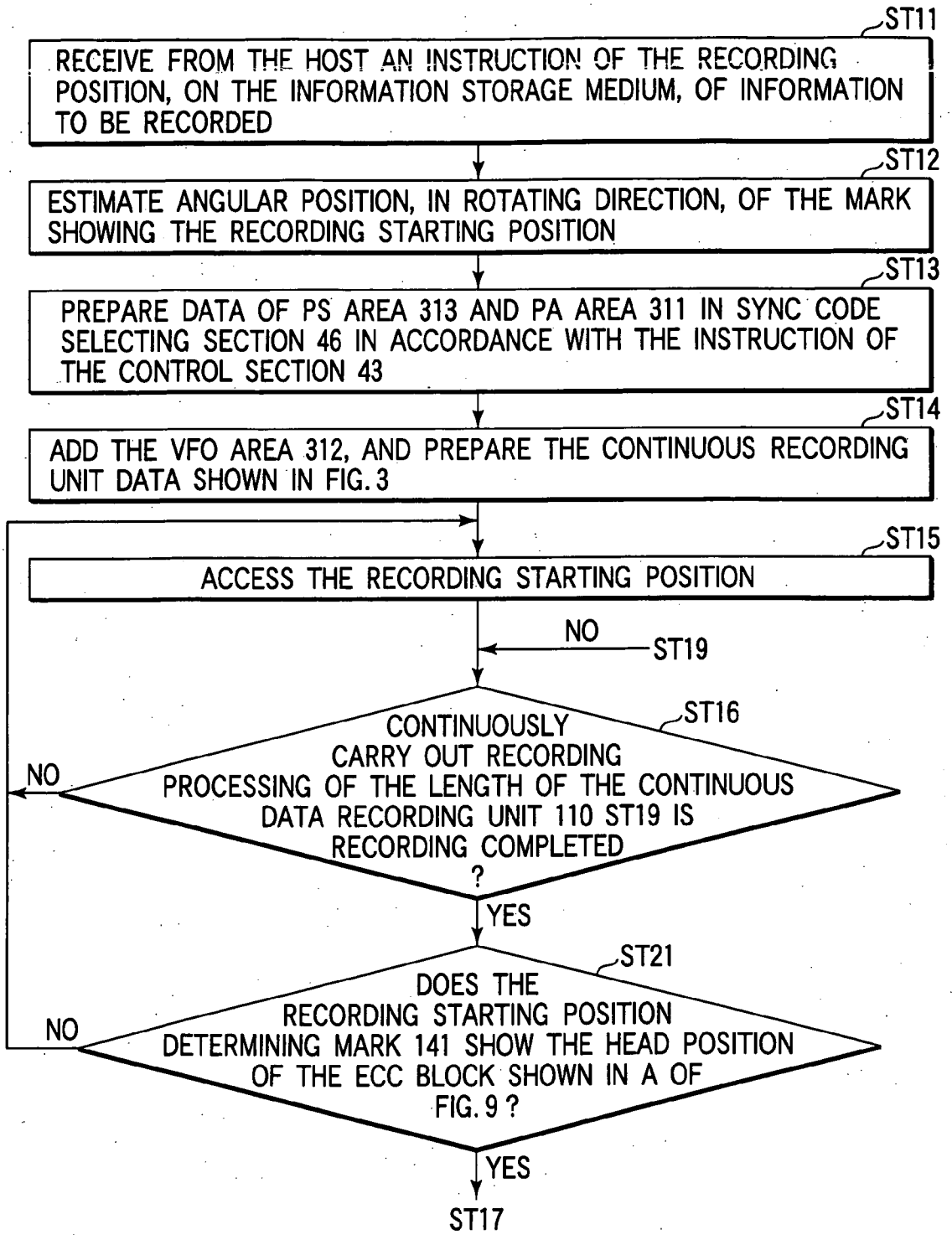

ST11
RECEIVE FROM THE HOST AN INSTRUCTION OF THE RECORDING POSITION, ON THE INFORMATION STORAGE MEDIUM, OF INFORMATION TO BE RECORDED
ST12
ESTIMATE ANGULAR POSITION, IN ROTATING DIRECTION, OF THE MARK SHOWING THE RECORDING STARTING POSITION
ST13
PREPARE DATA OF PS AREA 313 AND PA AREA 311 IN SYNC CODE SELECTING SECTION 46 IN ACCORDANCE WITH THE INSTRUCTION OF THE CONTROL SECTION 43
ST14
ADD THE VFO AREA 312, AND PREPARE THE CONTINUOUS RECORDING UNIT DATA SHOWN IN FIG. 3
ST15
ACCESS THE RECORDING STARTING POSITION
NO
ST19
ST16
CONTINUOUSLY CARRY OUT RECORDING PROCESSING OF THE LENGTH OF THE CONTINUOUS DATA RECORDING UNIT 110 ST19 IS RECORDING COMPLETED ?
NO
YES
ST21
DOES THE RECORDING STARTING POSITION DETERMINING MARK 141 SHOW THE HEAD POSITION OF THE ECC BLOCK SHOWN IN A OF FIG. 9 ?
NO
YES
ST17

FIG. 38

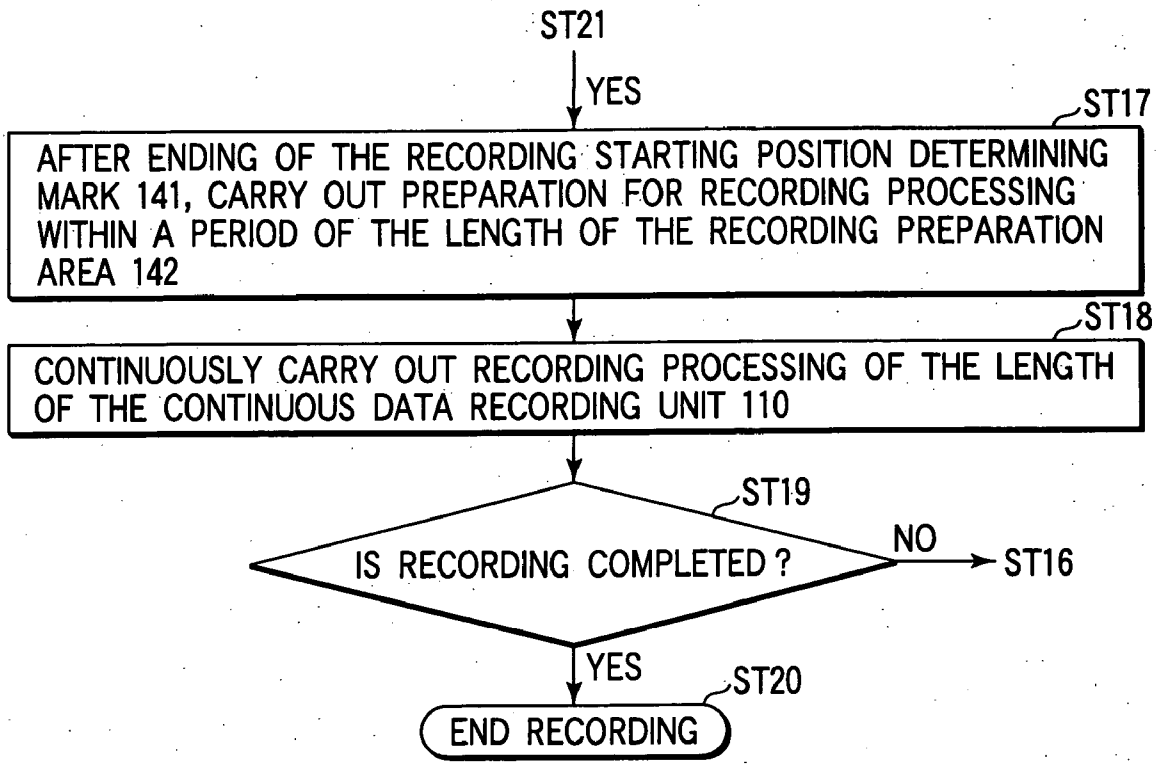

ST21
YES
ST17
AFTER ENDING OF THE RECORDING STARTING POSITION DETERMINING MARK 141, CARRY OUT PREPARATION FOR RECORDING PROCESSING WITHIN A PERIOD OF THE LENGTH OF THE RECORDING PREPARATION AREA 142
ST18
CONTINUOUSLY CARRY OUT RECORDING PROCESSING OF THE LENGTH OF THE CONTINUOUS DATA RECORDING UNIT 110
ST19
IS RECORDING COMPLETED ?
NO
ST16
YES
ST20
END RECORDING

FIG. 39

OPTICAL RECORDING MEDIUM, INFORMATION REPRODUCTION APPARATUS AND INFORMATION RECORDING/REPRODUCTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of co-pending U.S. application Ser. No. 10,233,671, filed Sep. 4, 2002, and for which priority is claimed under 35 U.S.C. §120. This application is based upon and claims the benefit of priority under 35 U.S.C. § 119 from the prior Japanese Patent Application No. 2001-271895, filed Sep. 7,2001, the entire contents of both applications are incorporated herein by reference in their entireties.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an optical recording medium, an information reproduction apparatus, and an information recording and reproduction apparatus.

[0004] 2. Description of the Related Art

[0005] In recent years, in the field of optical disks whose recording density is high, various types of formats are proposed. Read only information storage media (DVD-ROM), recordable information storage media (DVD-R), and re-recordable information storage media (DVD-RW or DVD-RAM) have been developed as optical disks.

[0006] In the field of optical disks in which various types of formats are present as described above, there are inconveniences for both the users and the manufacturers in the purchasing and manufacturing of reproduction apparatus, recording apparatus, and the like.

BRIEF SUMMARY OF THE INVENTION

[0007] The present invention is directed to an apparatus that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0008] According to an embodiment of the present invention, there is provided a read only storage medium comprising user data recording areas and intermediate areas which are alternately arranged, the intermediate areas recording at least information for synchronization.

[0009] According to another embodiment of the present invention, there is provided an information storage medium comprising sectors each of which is a first unit of information for recording; segments each of which is formed of at least one the sectors and is a second unit of information for recording, the segments recording information for synchronization; and an error correction block which is formed of at least one of the segments, has the same division point as a block division point of error correction, and is a third unit of information for recording.

[0010] Additional objects and advantages of the present invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the present invention.

[0011] The objects and advantages of the present invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0012] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the present invention and, together with the general description given above and the detailed description of the embodiments given below, serve to explain the principles of the present invention in which:

[0013] FIGS. **1**A, **1**B, **1**C, and **1**D are an explanatory diagram for explanation of a data arranging method within a read only information storage medium or a read only area of an information storage medium, according to an embodiment of the present invention;

[0014] FIGS. **2**A, **2**B, **2**C, and **2**D are an explanatory diagram for explanation of the data arranging method within the read only information storage medium or the read only area of the information storage medium, relating to FIG. **1**;

[0015] FIG. **3** is an explanatory diagram for explanation of one segment area (a continuous data recording unit) within the read only information storage medium or the read only area of the information storage medium;

[0016] FIG. **4** is an explanatory diagram, for comparison, which explains effects of the data arranging method on the information storage medium according to the embodiment of the present invention;

[0017] FIG. **5** is an explanatory diagram explaining effects of the data arranging method on the information storage medium according to the embodiment of the present invention;

[0018] FIG. **6** is an explanatory diagram showing one segment area (a continuous data recording unit) within a recording area (recordable area or re-recordable area) of a recordable information storage medium according to the embodiment of the present invention;

[0019] FIGS. **7**A, **7**B, **7**C, and **7**D are an explanatory diagram showing an example of a user data recording method within the recording area (recordable area or re-recordable area) of the recordable information storage medium according to the embodiment of the present invention;

[0020] FIG. **8** is a diagram explaining the structure of the recordable information storage medium according to the embodiment of the present invention, and the user data recording method shown in FIG. **7**;

[0021] FIG. **9** is a diagram shown for explanation, in relation to FIG. **8**, of the structure of the recordable information storage medium according to the embodiment of the present invention, and the user data recording method shown in FIG. **7**;

[0022] FIGS. **10**A and **10**B are an explanatory diagram relating to the necessity of interval areas shown in FIG. **8** according to the embodiment of the present invention;

[0023] FIGS. **11**A, **11**B, **11**C, and **11**D are an explanatory diagram showing a second example of a user data recording method within the recording area (recordable area or re-recordable area) of the recordable information storage medium according to the embodiment of the present invention;

[0024] FIGS. 12A, 12B, 12C, 12D, and 12E are an explanatory diagram showing a third example of a user data recording method within the recording area (recordable area or re-recordable area) of the recordable information storage medium according to the embodiment of the present invention;

[0025] FIGS. 13A, 13B, 13C, 13D, and 13E are a diagram for explanation of the relationship between a physical sector and a logical sector applied to the data structure of the read only area, the recordable area, and the re-recordable area of the information storage medium according to the embodiment of the present invention;

[0026] FIGS. 14A, 14B, 14C, 14D, and 14E are a diagram for explanation of the relationship between the physical sector and the logical sector applied to the data structure of the read only area, the recordable area, and the re-recordable area of the information storage medium according to the embodiment of the present invention, and information after scrambling;

[0027] FIGS. 15A, 15B, 15C, and 15D are a diagram for explanation of an ECC block applied to the data structure of the read only area, the recordable area, and the re-recordable area of the information storage medium according to the embodiment of the present invention;

[0028] FIGS. 16A, 16B, and 16C are a diagram for explanation of the relationship between the ECC block and the physical sector applied to the data structure of the read only area, the recordable area, and the re-recordable area of the information storage medium according to the embodiment of the present invention;

[0029] FIGS. 17A, 17B, 17C, and 17D are a diagram for explanation of an arrangement of synchronous frame data applied to the data structure of the read only area, the recordable area, and the re-recordable area of the information storage medium according to the embodiment of the present invention;

[0030] FIGS. 18A, 18B, and 18C are an explanatory diagram showing the relationship between the synchronous frame data and a synchronous code, and a synchronous frame length;

[0031] FIGS. 19A, 19B, 19C, and 19D are an explanatory diagram showing an example of the structure of the synchronous code according to the embodiment of the present invention;

[0032] FIGS. 20A, 20B, and 20C are an explanatory diagram showing a detailed example of the structure of the synchronous code according to the embodiment of the present invention;

[0033] FIGS. 21A, 21B, and 21C are an explanatory diagram showing an example of an arrangement pattern of the synchronous frame data and the synchronous code according to the embodiment of the present invention;

[0034] FIG. 22 is an explanatory diagram showing a method of indexing synchronous frame positions within one physical sector from the order in which the codes for synchronous frame position identification are aligned within the synchronization code;

[0035] FIG. 23 is a similar explanatory diagram showing a method of indexing synchronous frame positions within one physical sector from the order in which the codes for synchronous frame position identification are aligned within the synchronization code;

[0036] FIG. 24 is an explanatory diagram showing a method of scrambling processing of data to be recorded on the information storage medium according to the embodiment of the present invention;

[0037] FIG. 25 is an explanatory diagram showing a method of scrambling processing of data to be recorded on the information storage medium according to the embodiment of the present invention;

[0038] FIG. 26 is an explanatory diagram showing a method by which data recorded on the information storage medium according to the embodiment of the present invention is subjected to descrambling processing;

[0039] FIG. 27 is an explanatory diagram showing a method by which data recorded on the information storage medium according to the embodiment of the present invention is subjected to descrambling processing;

[0040] FIG. 28 is a diagram showing a recording system in an information recording and reproduction apparatus according to the embodiment of the present invention;

[0041] FIG. 29 is a diagram showing a reproduction system in the information recording and reproduction apparatus according to the embodiment of the present invention;

[0042] FIG. 30 is a diagram showing a structural example of a scrambling circuit according to the embodiment of the present invention;

[0043] FIG. 31 is a diagram showing a structural example of a descrambling circuit according to the embodiment of the present invention;

[0044] FIG. 32 is a flowchart showing a method of controlling access to a predetermined position by using a PA area in the information recording and reproduction apparatus according to the embodiment of the present invention;

[0045] FIG. 33 is a flowchart showing the continuation of FIG. 32;

[0046] FIG. 34 is a flowchart showing the continuation of FIG. 33;

[0047] FIG. 35 a flowchart showing a method of controlling access to a predetermined position by using a PS area in the information recording and reproduction apparatus according to the embodiment of the present invention;

[0048] FIG. 36 is a flowchart showing the continuation of FIG. 35;

[0049] FIG. 37 is a flowchart showing the continuation of FIG. 36;

[0050] FIG. 38 is a flowchart for explanation of a recording method or a re-recording method in the information recording and reproduction apparatus according to the embodiment of the present invention; and

[0051] FIG. 39 is a flowchart showing the continuation of FIG. 38.

DETAILED DESCRIPTION OF THE INVENTION

[0052] An embodiment of an information recording/reproduction apparatus according to the present invention will now be described with reference to the accompanying drawings.

[0053] Firstly, in order to easily understand the embodiment of the present invention, the data structure and the reproduction mechanism or the recording mechanism in current optical disks will be described.

[0054] DVD (Digital Versatile Disk) specifications have been described in specifications book issued by a DVD forum. Here, all of a method of scrambling main data, a data structure in a sector, a method of structuring an ECC (Error Correction Code) block, and a pattern of a sync code (Synchronous Code: a synchronization code at the time of reproduction) and a method of inserting the sync code common to a read only information storage medium (DVD-ROM), a recordable information storage medium (DVD-R), and a re-recordable information storage medium (DVD-RW or DVD-RAM), and compatibility of the formats at the time of reproduction is ensured.

[0055] In the embodiment of the present invention, as described above, an information storage medium in which a recording format (a data structure of information to be recorded on an information storage medium) is made common to the read only information storage medium (DVD-ROM), the recordable information storage medium (DVD-R), and the re-recordable information storage medium (DVD-RW or DVD-RAM), and compatibility of the formats at the time of reproduction is ensured, is defined as a multi-purpose information storage medium (Digital Versatile Disk) (which means being able to be adapted to the respective aims which are a read only aim, a recording aim, and a re-recording aim).

[Points of Interest for Various Types of Disks]

[0056] Here, the various types of optical disks will be described, and the problems thereof as well will be described.

[0057] (A) DVD-R exists as recordable information storage media.

[0058] In a DVD-R, data is recorded in the same format as a DVD-ROM which is a read only information storage medium. A Next Border Marker is recorded as the original data before scrambling/modulation at the ending position of a series of recording, and a "border-out" area in which repeated data of "00" is recorded for a long range is recorded after recording.

[0059] Thereafter, when new information is recorded, after a "border-in" area is recorded after the "border-out" area, user information (in the same format as a DVD-ROM) is recorded, and a "border-out" area is recorded again after ending of recording of the user information.

[0060] When such a method is adopted, if recording of the user information is frequently carried out on one information storage medium, recording areas of Borderout/Borderin, which are unnecessary from the standpoint of the user information, increases and a problem arises in that the amount of user information which can be recorded on one information storage medium decreases (a deterioration of recording efficiency occurs).

[0061] As reasons necessary for recording the Borderin/Borderout for each recording in this way, there are reasons (A1) and (A2) as follows.

[0062] Reason (A1): for ensuring tracking stability at the time of accessing

[0063] After standardizing and manufacturing of DVD-ROM, standardizing and manufacturing of DVD-R were carried out. It is necessary that information recorded on a DVD-R disk (recordable-type information storage medium) can be reproduced by a read only information reproduction apparatus for the previously-manufactured DVD-ROM disks. Currently, a DPD (Differential Phase Detection) method is used for most track offset detecting methods carried out at the time of reproducing a DVD-ROM disk.

[0064] A pregroove is continuously formed on the DVD-R disk in an unrecorded state, and a Push-Pull method is used as a track offset detecting method at unrecorded places. At the recorded area of the DVD-R disk, track offset detection is possible by the DPD method from the above-described reason.

[0065] Accordingly, the track offset detecting methods are different on the recorded areas and the unrecorded areas in the DVD-R disk. In such a situation, for example, when reproduction of data of a recorded area is attempted from immediately after carrying out rough accessing in which the reproduction position is moved by moving the entire optical head, the optical head moves to the unrecorded area by mistake at the stage of rough accessing. A problem arises in that, if tracking is attempted, tracking cannot be carried out because track offset detection by DPD is impossible. Thus, due to the Borderin/Borderout being recorded, tracking is stabilized.

[0066] Reason (A2): for solving the problem of synchronization offset between the data of the recorded area and the recorded data

[0067] A problem when other data is recorded in accordance with the format of the DVD-ROM from immediately after a recorded area on the DVD-R disk will be described. In this case, the frequency and the phase of a reference clock for use in preparing a recording pulse in the information recording reproduction apparatus cannot completely coincide with the frequency and the phase of a (past) reference clock at the time of recording data in the recorded area which exists immediately therebefore. Therefore, synchronization offset between the data of the recorded area before recording and the data after recording arises. Accordingly, when it is recorded in this way, a phase shift arises between the data before and after a boundary which is the recording head position, and bit shift errors easily occur. Therefore, when data is newly recorded, the "border-out" area is arranged after the recorded area before recording, and at the recording position, due to the "border-in" area being arranged before recording user data, the physical distance between the user data before and after the boundary which is the recording head position increases. By carrying out synchronizing of the information reproduction apparatus again in the "border-in" area, the accuracy of the synchronizing at the user data positions before and after the boundary which is the recording head position is ensured.

[0068] (B) DVD-RW exists as re-recordable information storage medium.

[0069] There is a recording method called "restricted overwrite" as an information re-recording method at DVD-RW. This method is a recording method in which the next

data can be recorded or re-recorded from after the previously recorded data without recording the above-described "border-in/border-out" area.

[0070] However, because the recording method by "restricted overwrite" destroys one part of the previously recorded data and carries out re-recording of new data, the reliability of the recorded data markedly deteriorates. When the recording method by "restricted overwrite" is used in this way, the reason (problem) for destruction of one part of the recorded data is as follows.

[0071] Reason (B1): In a DVD-ROM, there is no synchronizing preparation area which is necessary for reproducing recorded or re-recorded information.

[0072] Namely, in current DVD-ROM, since reproduction of AV (Audio & Video) information or installing of a program is the main object, the demands for high speed access and the demands for shortening the time until the reproduction starting time are not that strong. Accordingly, as the data structure of the data recorded in a current DVD-ROM, a data structure, in which there is no recorded area of a VFO (Variable Frequency Oscillator) used as information for specific synchronizing and the user data is continuously recorded, is adopted.

[0073] When an information reproduction apparatus reproduces information from a DVD-ROM disk, the optical head accesses an appropriate position, and synchronizing is carried out by using a reproduction signal from the user data already recorded. Accordingly, since the synchronizing is not completed for the reproduction data immediately after accessing in this method, decoding for the user data cannot be carried out. After completing accessing, after a while, the reproduction/decoding of the user data becomes possible from the point where the synchronizing is completed. If recording or re-recording of the data in a unit of sector is attempted in a state corresponding to the data structure of the DVD-ROM, as described in aforementioned reason (A2), synchronization offset occurs between the data of the recorded sector and the sector data recorded or re-recorded immediately thereafter that, and it is impossible to continuously and steadily reproduction before and after that.

[0074] As a provisional, proposed solution for the above-described problem, a method as follows is adopted. Namely, in the "restricted overwrite" mode in the DVD-RW, a VFO for synchronizing at the DVD-ROM does not exist. Instead, as the synchronizing preparation area (running period), one part of the recorded sector data immediately before the recording head position is crushed. The synchronizing preparation area is detected, and the recording head position is determined, and it is possible to accurately reproduce from the recording head position.

[0075] The "restricted overwrite" method is a method in which an advance synchronizing is completed such that it is possible to reproduce/decode data from the recording head position of the part at which newly recording or re-recording is carried out.

[0076] However, in this method, the recorded data immediately before newly starting recording or re-recording is destroyed (in order to prepare the preparation area for synchronizing), and the reliability of the reproduction operation at the broken part is greatly lacking.

[0077] (C) DVD-ROM exist as read only information storage media.

[0078] (C1) In a DVD-ROM, data is recorded in a unit of sector, and when a desired point is accessed, information of identification data (which corresponds to data ID **1** of the present embodiment) recorded at the head position of each sector is reproduced. Thus, it becomes a mechanism by which the position (address) information of each sector can be identified. However, because 16 sectors together structure one ECC block (Error Correction Code) in a current DVD-ROM, there is need to reproduce the information successively from the sector positioned at the head of the ECC block. Currently, there is no method which directly find the head position of the ECC block, and there is no way except carrying out reproduction successively for each sector while successively decoding the identification data of the sectors, and it takes much time to access to the head position of the ECC block.

[0079] Thus, an object of an embodiment of the present invention is to enable recording of data in a unit of segment without destroying recorded user data in a next-generation DVD-R, while ensuring the compatibility of next-generation DVD-ROM and the next-generation DVD-R.

[0080] Namely, if the above-description are expressed in more detailed words, the object is to provide a read only information storage medium ensuring the compatibility with information storage media which can record or re-record information in a unit of segment. Further, even if recording or re-recording in a unit of segment is carried out in the above-described recordable or re-recordable information storage medium, high reliability for the recorded data can be ensured without destroying the data in recorded areas.

[0081] The embodiment of the present invention provides a data structure of the information storage medium (recording format), or a method of recording information onto the information storage medium, a method of reproducing information from the information storage medium, an information recording and reproduction apparatus, and an information reproduction apparatus.

[0082] Further, an object of an embodiment of the present invention is to provide a data structure of a information storage medium (recording format), a method of recording information onto the information storage medium and a method of reproducing information from the information storage medium suitable for the data structure, or an information recording and reproduction apparatus and information reproduction apparatus, in which it is possible to make accessing of the head position of the ECC block high speed even for next-generation DVD-ROM.

[Description of Outline Shown in the Respective Drawings]

[0083] Contents shown in the respective drawings will be described.

[0084] FIGS. **1**A to **1**D, and **2**A to **2**D explain the basic way of thinking of the embodiment of the present invention. FIG. **3** explains one segment area (one recording unit of continuous data) in the read only information storage medium or the read only area of the information storage medium according to the embodiment of the present invention.

[0085] FIGS. **4** and **5** explain the advantage in accordance with the data arranging method on the information storage medium according to the embodiment of the present invention. FIG. **6** explains one segment area (one recording unit of continuous data) in the recording area (recordable area or re-recordable area) of the recordable information storage medium according to the embodiment of the present invention. FIG. **7** shows a first example of a user data recording method in the recording area (recordable area or re-recordable area) of the recordable information storage medium according to the embodiment of the present invention. FIGS. **8** and **9** explain a structure on the recordable information storage medium and the user data recording method shown in FIG. **7**. In FIGS. **8** and **9**, an example in which a wobble modulation pattern is changed at a starting position and a non-starting position of an ECC block is shown. However, in a mark for determining a recording starting point, information (for example, segment ID information or the like) showing an existing position showing where this mark (or segment) is positioned in the ECC block may be recorded in advance.

[0086] FIGS. **10**A and **10**B explain the necessity of an interval area shown in FIGS. **8** and **9**. Moreover, FIGS. **11**A to **11**D, and **12**A to **12**E show second and third examples of the user data recording method in the recording area (recordable area or re-recordable area) of the recordable information storage medium according to the embodiment of the present invention.

[0087] FIGS. **13**A to **13**E, **14**A to **14**E, **15**A to **15**D, and **16**A to **16**C explain the ECC block in the embodiment of the present invention. FIGS. **17**A to **17**D, **18**A to **18**C, and **19**A to **19**D explain a synchronous frame structure in one physical sector data. FIGS. **20**A to **20**C explain a synchronous code according to the embodiment of the present invention. In FIGS. **20**A to **20**C, a pattern of a synchronous position detecting code **121** is determined as follows: (i) the space between "1" and "1" is longer than a maximum length which can be generated by a modulation rule (in the example of the figure, k+3 "0"s are continuous), and (ii) the space between "1" and "1" does not include the most dense (shortest) length which can be generated by the modulation rule.

[0088] FIGS. **21**A to **21**C show an arrangement example of the synchronous codes in one physical sector. As this arrangement structure, the same arrangement structure is adopted in the read only area and the recording area. FIGS. **22** and **23** explain a method for indexing a synchronous frame position in one physical sector data from the order of alignment of the synchronous frame position identification codes in the synchronous code.

[0089] FIGS. **24** to **27** explain another example of a common data structure recorded on the information storage medium of the embodiment of the present invention.

[0090] FIG. **28** shows a structure of a recording system of the information recording and reproduction apparatus. FIG. **29** shows a structure of a reproduction system of the information recording and reproduction apparatus. FIG. **30** shows an internal structure of a scrambling circuit. FIG. **31** shows an internal structure of a descrambling circuit.

[0091] FIGS. **32** to **37** show a flowchart showing a controlling method when the information recording and reproduction apparatus accesses a predetermined position on the information storage medium. FIGS. **38** and **39** show a flowchart of a recording method or a re-recording method in the information recording and reproduction apparatus.

[Description of Main Points]

[0092] Next, concretely, main portions of the embodiment will be compactly described.

[0093] First, with regard to the topic of ensuring tracking stability at the time of accessing of reason (A1), among read only information storage media (next-generation DVD-ROM) and recordable information storage media, a physical shape of a "lead-in" area and a data structure of the "lead-in" area are made to have similar shapes (made to be in common), and the track offset detecting method in the "lead-in" area is made to be in common for information storage media which can record only one time (next-generation DVD-R) and re-recordable information storage media (next-generation DVD-RW or next-generation DVD-RAM).

[0094] In accordance therewith, regardless of the type of the information storage medium, in the "lead-in" area, a method in which the track offset correction is stably carried out (for example, a DPD (Differential Phase Detection) method is used for track offset detection) and an extremely high reliability reproduction signal and identifying information thereof can be obtained. Moreover, media identifying information showing the type of the above-described information storage medium is recorded in the "lead-in" area.

[0095] In this way, the type of the information storage medium is stably detected, an optimal track offset detecting method in the user data area (for example, the DPD method is used for a read only information storage medium and a DPP (differential Push-Pull) method is used for a recordable information storage medium) is selected at the information reproduction apparatus side in accordance with the type of the information storage medium, and tracking can be stably carried out for the user data area.

[0096] Further, the measures as follows are carried out with respect to the topic of eliminating synchronization offset between data in a recorded area before recording and data after recording of the above-described reason (A2) and a countermeasure for the point that a synchronizing preparation area necessary for reproducing the recorded or re-recorded information does not exist a DVD-ROM of the above-described reason (B1).

[0097] An intermediate area is arranged between the user data recording area and the next user data recording area which is configured in a unit of segment, and data used for synchronizing (VFO data) is recorded in the intermediate area, and the intermediate area is utilized as a synchronizing preparation area for the user data recording area to be recorded next.

[0098] As a result, in the embodiment of the present invention, it is possible to record or re-record information in a unit of segment without destroying the recorded user data. Further, the embodiment of the present invention can provide an information storage medium and a data structure thereof or an information recording method and an information recording and reproduction method, and provide an information reproduction method and an information reproduction apparatus for an information storage medium

recorded in the data structure, in which this structure is commonly used for a recordable information storage medium and a read only information storage medium, and even a recordable information storage medium having the same data structure as a read only information storage medium is not affected by synchronization offset between segments (a countermeasure to the topic of reason (A1)), and the data of other segments in a recorded state is not destroyed (a countermeasure to the topic of reason (B1)).

[0099] With respect to the problem of the above-described reason (C1) that time is required to access the head position of the ECC block in the read only information storage medium, the following measure is taken. A segment comprises collecting a plurality of sectors together in one ECC block, and information (a PA/PS area) detecting the intermediate position is arranged in an intermediate area **301** in each segment. In accordance therewith, the place of the intermediate position **301** can be detected, thereby access to the head position of the ECC block is easier than in the current method.

[0100] As the method of accessing the head position of the ECC block, an access control is easier by grouping a plurality of sectors together and detecting in a unit of segment, than successively reproduction identification data at the head of the sectors as in the current way.

[Effective Points, Functions, Effects and the Like in the Embodiment]

[0101] Next, particularly effective points and functional effects in the present embodiment will be first described.

[0102] [1] The user data recording area and the intermediate area are alternately arranged in the read only information storage medium or the read only area (the "lead-in" area **320** in FIG. **1** or the like) in the recordable information storage medium, and at least data used for synchronizing is recorded in the intermediate area [corresponding to the contents described in FIGS. **1**A to **2**D].

[0103] Effective point: Because detecting of the boundary position of the ECC block is easy and processings up to the start of error correction processing using the ECC block are simplified, it is possible to make the control high-speed, and to lower the frequency of occurrence of bugs, and to make the apparatus low-cost.

[0104] Namely, detection of the position of the ECC block boundary is first possible when information of the synchronous code **110** arranged at **26** places in one physical sector **105** (FIG. **21**A) is decoded and the head position of one physical sector **103** is searched for, and the information of the data ID **1** recorded at the head position of the physical sector **103** is reproduced (the method shown in FIG. **4**). As compared with this, in the embodiment of the present invention (which corresponds to the contents described by FIG. **5**), when the position of the intermediate area is detected, the position of the data ID **1**, in which is described address information which is arranged behind the intermediate area and is discrete at a segment interval (has jumped by the number of the sectors existing in one segment), is immediately known. Accordingly, in the present embodiment, the boundary position of the ECC block can be easily detected.

[0105] In particular, in the present embodiment, as shown in FIGS. **24**, **25**, **26**, and **27**, in order to increase the number of re-recordings, the data ID **1** portion is also scrambled. Accordingly, it takes much time to reproduce the data ID **1**. Namely, in the data structure of the present embodiment, if the data ID **1** in the physical sector data is reproduced/decoded one by one, it takes more time to access data than in a current system.

[0106] Accordingly, when a method of scrambling such as the present embodiment is adopted, firstly, detecting of the position of the intermediate area **301** is carried out, and data accessing has a better effect for shortening the accessing time.

[0107] [1a] The data size of the intermediate area described in [1] is made to match an integer multiple of the size of one synchronous frame (which corresponds to the description of FIGS. **1**A to **1**D).

[0108] As shown in FIGS. **18**A to **18**C, the synchronous code **110** is arranged at the head position of the fixed length synchronous frame **308**. Similar, the size of the intermediate area **301** coincides with the synchronous frame **308** as shown in FIGS. **2**C and **2**D, and a PA (postamble) area **311** having a structure similar to the synchronous code **110** is arranged in the same synchronous frame **308**, as shown in FIG. **2**B. Effective point

[0109] (1a-1) Because a synchronous frame interval in the user data recording area is held in the intermediate area as well, detection of the position of the synchronous code is easy.

[0110] Namely, as shown in FIGS. **2**A to **2**D, in the physical sector data **5**, the synchronous code **110** is arranged at the head position of the fixed length synchronous frame **308**, and the PA area **311** is arranged at the head position of the intermediate area **301** having a size matching the synchronous frame **308**. Thus, the arrangement intervals of the PA area **311** and the synchronous code **110** always coincident over the entire area in the information storage medium **9** (regardless of any of the read only area and the recordable area).

[0111] As a result, if the synchronous code **110** or the PA area **311** is detected once, it is possible to estimate the timing in which the synchronous code **110** or the PA area **311** will be detected since the synchronous code **110** or the PA area **311** is arranged at a uniform interval.

[0112] Therefore, not only is the detection of the synchronous code **110** or the PA area **311** easy, but also, the detecting accuracy of the synchronous code **110** or the PA area **311** is improved.

[0113] (1a-2) Continuity of the wobble group can be ensured.

[0114] Namely, a wobble continuous groove (pregroove) is formed as shown in FIGS. **8** and **9** in the user data recording area of the recordable information storage medium. As shown in FIG. **7**D, FIG. **1**D, and FIG. **12**D, the physical length of one synchronous frame is an integer multiple of a wobble period of the above-described continuous groove.

[0115] Therefore, since the data size of the intermediate area is made to match an integer multiple of one synchronous frame size, it is possible for the physical length of the intermediate area to match an integer multiple of a wobble

period. This means that it is possible for the wobble phases at the starting position and the ending position of the user data recording area to be always made to coincide.

[0116] [1b] Relative address information (in-ECC position information **314/315** shown in FIG. **2**A) is recorded in the intermediate area described in [1].

Effective Point

[0117] As a result, the position of each segment in the ECC block is known. At the time of reproduction, the head position of the ECC block is always searched for, and error correction processing is carried out in a unit of ECC block from the head position of the ECC block. Accordingly, as the present embodiment, by using a structure in which relative address information is recorded in the intermediate area and the position of each segment in the ECC block is known, the head position of the ECC block is quickly found, and an attempt can be made to shorten the processing time up to the error correction processing.

[0118] [1c] At least one part (the PA area **311** and SY**0** or SY**5** in the PS area) among the synchronous code **110** in the user data recording area is used for (at least one part of) the synchronous code in the intermediate area (which corresponds to SY**0**, SY**4**, SY**5** of the synchronous frame position number **115** shown in FIG. **20**).

Effective Point

[0119] As shown in FIG. **20**, a specific synchronous code **110** pattern is arranged in accordance with the position in the physical sector data **5**. Therefore, in a sync code position extracting section **45** shown in FIG. **29**, the position in the physical sector data **5** can be detected by using the connection of the synchronous codes **110** detected as shown in FIGS. **21**A to **21**C and **22** to **23**. By determining whether it is SY**0** or SY**5** in the PA area **311** or PS (pre-synchronous) area, the same structure/function as the synchronous code **110** can be realized. In accordance therewith, in the sync code position extracting section **45** of FIG. **29**, two types of position extractions, which are the position extraction of the intermediate area **301** and the position extraction of the intermediate-area **301** in the ECC block **304**, are carried out. Therefore, the circuit structure of the information recording and reproduction apparatus or the information reproduction apparatus can be simplified, and it is possible to simplify the processings as described in FIGS. **32** to **37**.

[0120] [1d] The pattern content is changed between the synchronous code **110** in the user data recording area and the synchronous code in the intermediate area (corresponding to the description of FIGS. **20**A to **20**C and **2**A to **2**D).

Effective Point

[0121] The pattern content is changed between the synchronous code **110** in the user data recording area and the synchronous code in the intermediate area, thereby it is possible to quickly detect whether the detecting information is a position information in the physical sector data **5** or a position information of the intermediate area **301**, in the sync code position extracting section **45** in FIG. **29**.

[0122] [2] The recording position of the intermediate area is detected by using the data pattern recorded in the intermediate area described in [1]. Namely, the recording position of the intermediate area is detected by detecting the synchronous code recorded in the intermediate area.

Effective Point

[0123] Because ECC block boundary position detection is easy, and the processings up to the start of error correction processing by using the ECC block are simplified, it is possible to make the control high-speed, to decrease the frequency of occurrence of bugs, and to make the apparatus low-cost.

[0124] In current DVDs, it is possible to first detect the ECC block boundary position when the head position of one physical sector **103** is searched for by decrypting the information of the synchronous code **110** arranged at **26** places in one physical sector **103**, and the information of the data ID **1** recorded at the head position of the physical sector **103** is reproduced (the method shown in FIG. **4**).

[0125] As compared with thus, in the embodiment of the present invention (the description shown in FIG. **5**), when the position of the intermediate area is detected, the position of the data ID **1** which is arranged behind the intermediate area and has described therein an address information discrete at a segment interval (has jumped by the number of the sectors existing in one segment), is immediately known. Therefore, detection of the position of the ECC block boundary is easy.

[0126] [3] In a recordable information storage medium and a read only area of a read only information storage medium (or recordable information storage medium), the arrangement intervals of the user data recording areas and the intermediate areas from the standpoint of the arranged states or the number of data bits are made to coincide.

[0127] Namely, as is clear in comparison with FIGS. **3** and **6**, the arrangement states or the numbers of data bits in the user data recording area and the intermediate area substantially coincide in the re-recordable information storage medium and the read only area in the read only information storage medium (or recordable information storage medium), and only the size of the VFO area is different.

Effective Point

[0128] (a) Compatibility between the read only storage medium and the recordable information storage medium can be maintained. Because a processing circuit for reproducing can be used for both a read only information reproduction apparatus and a recordable information recording and reproduction apparatus, it is possible to make the apparatus low-cost.

[0129] (b) There is no need to form the current "border-out" area, and it is possible to record or re-record in a unit of segment without carrying out "restricted overwrite". Therefore, recording and re-recording at small units (segment units) in the recordable or re-recordable information storage medium can be carried out (because the areas in which unnecessary "border-out/border-in" information are recorded become unnecessary), the usage efficiency at the time of recording onto an information storage medium is improved.

[0130] [4] The user data recording area and the intermediate area, which are continuous in a unit of segment, are alternately arranged for the recordable information storage

medium. The recording or re-recording of the user data is carried out in a unit of segment, and the recording start is carried out from a midway position of the above-described intermediate area at the time of recording/re-recording. The recording end processing is carried out at a midway position of the intermediate area (which corresponds to the description shown in FIGS. **1**D, **7**B, **7**C, **11**B, **11**C, **12**B, and **12**D).

Effective Points

[**0131**] The recording head position which is the leading end of the continuous data recording unit **110** and the recording end position which is the trailing end of the continuous data recording unit **110** are within the VFO areas **312**, and **331** to **335**. The VFO areas exist outside of the user data recording field **303** at which the physical sector data **5** is arranged. Thus, the destruction of user data in a case where the recording method in accordance with "restricted overwrite" is used as described in (B), does not occur, and even if overwrite recording is carried out many times, high reliability of the information within the user data recording field **303** can be maintained.

[**0132**] [5] Address information, which is arranged discretely (dispersedly inserted) into one data recording unit (segment) with respect to the recordable information storage medium, is recorded at plural places (corresponding to the description shown in FIGS. **1**A to **2**D).

[**0133**] In other words, a plurality of sectors, which contain one or more data ID **1** including the address information, are collected, so as to form one data recording unit (segment).

Effective Points

[**0134**] (a) The recording efficiency improves.

[**0135**] (b) High speed of access is obtained.

[**0136**] Namely, even when reproduction starts from midway in the recording unit (one segment) for data recorded in recording units (segment units), the place which is currently being reproduced can be detected by identifying the data ID information reproduced immediately after start of reproduction. This enables a shortening of the total access time, because the time until the re-access processing is shortened.

[**0137**] [**6**] The recordable information storage medium has a structure in which a recordable recording area and an emboss area, such as a "lead-in" area at which information is recorded in advance by minute convex and concave configurations, exist within the same plane. The recordable data structure in the recording area and the data structure of the data recorded in advance in the emboss area have a data structure in which the user data recording areas and intermediate areas are arranged alternately (the description shown in FIGS. **1**A to **2**D).

Effective Points

[**0138**] (a) In a recordable (including both a one time only recordable and a re-recordable) information storage medium, the recorded data structure coincides at the recordable recording area and the emboss area. Thus, the reproduction circuit which reproduces information from the recording area and the reproduction circuit which reproduces information from the emboss area can be used in common, and the reproduction circuit can be simplified and made lower cost.

[**0139**] (b) In a read only information storage medium, in the same way as with a recordable information storage medium, there are many cases in which a "lead-in" area is provided. By combining this point and the point of [3], the data structure at the "lead-in" area can be used in common for read only information storage media and recordable information storage media. As a result,

[**0140**] (a1) At an information reproduction apparatus which can reproduce data from both read only information storage media and recordable information storage media, the reproduction processing circuit for the "lead-in" area can be used in common for both information storage media. The information reproduction apparatus can be simplified and made lower cost.

[**0141**] (b1) The structure of the "lead-in" area can be made the same for the read only information storage medium and the recordable information storage medium. Thus, not only the reproduction signal processing circuit in the "lead-in" area, but also the track offset detecting method can be used in common. The media information is recorded in the "lead-in" area for a read only information storage medium (ROM disk), and an R disk which is a recordable information storage medium and can be recorded only one time, and a re-recordable RAM disk. Thus, the data from the "lead-in" area is reproduced at a reproduction signal processing circuit common to a track offset detecting method common to a different type of information storage medium, and the media identification information can be reproduced easily and reliably.

[Specific Explanation of the Embodiment]

[**0142**] Next, more specific explanation will be given with reference to the drawings.

[**0143**] FIG. **1**D shows an outline of the information storage medium **9**.

[**0144**] In the recordable or re-recordable information storage medium **9**, the recordable recording area and the emboss area such as a "lead-in" area **320** or the like in which information is recorded in advance by minute convex and concave configurations, exist within the same plane. Identification information showing the type of the information storage medium (e.g., a next-generation DVD-ROM, a next-generation DVD-R, a next-generation DVD-RW, a next-generation DVD-RAM) is recorded in the "lead-in" area **320**.

[**0145**] The data structure for recording the data to the recording area and the data structure of the data recorded in advance in the emboss area both have a data structure in which the user data recording areas and the intermediate areas are alternately arranged.

[**0146**] Thirty-two items of physical sector data **5** (FIG. **1**B) are collected to form one ECC block **304** (FIG. **1**A). The arrangement within the ECC block is shown in FIGS. **13**A to **13**E, **14**A to **14**E, **15**A to **15**D, and **16**A to **16**C, as described later.

[**0147**] Here, four items of physical sector data are arranged within one segment area **305**, and form a user data recording field **303** (FIG. **1**C).

[**0148**] Further, the intermediate area **301** exists in one segment area **305**.

[0149] The size of the intermediate area **301** is an integer multiple (FIG. **2**C) of a synchronous frame **308**. A PA (Postamble) area **311**, a VFO (Variable Frequency Oscillator) area **312**, and a PS (Pre-Synchronous code) area **313** exist within the intermediate area **301**, as shown in FIG. **2**B.

[0150] Information of SY**0** or SY**4** to be described later is recorded in the PA area **311**, as shown in FIG. **2**A. Information of SY**0** or SY**5**, in-ECC position information **314** or **315**, and the error detection code **316** or **317** thereof are recorded in the PS area **313**, as shown in FIG. **2**A.

[0151] FIGS. **1**A to **2**D show the structure of the read only information storage medium or the read only area within the recording medium. The structure is made to substantially coincide with the data structure of the recording area at a recordable or re-recordable information storage medium.

[0152] As the data structure of the recording area, data recording or re-recording in a unit of segment area **305** is possible. As shown in FIG. **2**D, recording can start from a midway position of the intermediate area **301***a*, and recording can end at a midway position of the intermediate area **301***b*.

[0153] FIG. **3** is a diagram in which the data structure within the segment area **305** shown in FIG. **1**C is redrawn so as to be easily understood.

[0154] In a next-generation DVD-ROM, VFO area **312**, PS area **313**, and PA area **311** are arranged in one segment of data **305** such that the total of the synchronous frames within one segment area **305** becomes one synchronous frame size (a fixed length). Four items of continuous information (data size of one sector **5** is 2048 bytes) are in the data field **303** of FIG. **3**, and form one segment of data **305**. For each segment of the data, VFO area **312** and PS area **313** are arranged immediately therebefore, and PA area **311** is arranged immediately thereafter.

[0155] The functions or effects of the data structure of the present embodiment shown in FIGS. **1**A to **3** will be explained by using FIGS. **4** and **5**.

[0156] In the data structure of current DVD-ROM, DVD-R, and DVD-RW, there is no intermediate area **301** as in the present embodiment. In the data structure of current DVD-ROM, DVD-R, and DVD-RW, one ECC block comprises **16** items of physical sector data **5**. One ECC block occupies a position **321** on the information storage medium at which data is arranged.

[0157] Further, the position within one physical sector data **5** is detected from the information contents of the synchronous code **110**, and the position is detected from the ID information recorded at the head position of the physical sector data **5**. Data access control is thereby possible.

[0158] An access control method for current DVD-ROM and DVD-R/RW is shown in FIG. **4**.

[0159] (a-1) First, rough access to an estimated position on the information storage medium **9** is carried out, and data reproduction at the accessed position started by an information recording and reproduction section **41** (FIG. **28**).

[0160] (a-2) The position of the synchronous code **110** is detected, and the head position of the physical sector data is detected.

[0161] (a-3) The in-ECC block position **321** is indexed from the data ID **1** (or ID) information within the physical sector data **5**.

[0162] (a-4) The position of the next synchronous code **110** is detected, and the data ID **1** (or ID) information is read, and thereafter,

[0163] (a-5) the operation of (a-4) is repeated until the next ECC block head position.

[0164] As a result, (a-6) the information recording and reproduction section **41** accesses the next ECC block head position on the information storage medium **9**, and information reproduction and error correction are started therefrom. In this sway, currently, there is the need to always reproduce the physical sector data information (data ID **1**) until the head position of the ECC block, which starts information reproduction/error correction, is accessed.

[0165] As in the present embodiment, as explained in FIGS. **24** to **31**, when the data ID **1** (or ID) information is scrambled, the following problem occurs. Namely, at the time of reproduction, if the scrambled data ID **1** (or ID) information is descrambled, even more time is required until the head position of the ECC block is accessed. Namely, the problem arises that the access time becomes even slower.

[0166] In contrast, in the method of the present embodiment, plural items of physical sector data **5** are gathered to form the segment area **305**, and access control is carried out by using the segment area **305** as a unit. Thus, access processing is easy, and the access time is shortened.

[0167] The structure of the information recording and reproduction apparatus or information reproduction apparatus in the present embodiment is shown in FIGS. **28** and **29**. Details of the information reproduction apparatus will be described later.

[0168] The access processing method for the data structure of the present embodiment shown in FIG. **5** is shown in FIGS. **32** to **37**.

[0169] When an instruction of a data range to be reproduced is received from the interface section **42** (ST**31**), the value of the data ID **1** within the physical sector data **5** having the reproduction head position of the ECC block **304** is calculated (ST**32**). At the information recording and reproduction section **41**, reproduction is started from the roughly-accessed position (ST**33**).

[0170] At the information recording and reproduction section **41**, data in which is mixed in the intermediate area **301** having the PA area **311** at the head (FIG. **2**B), is reproduced. The reproduced data is supplied as is to a sync code position extracting section **45** (ST**34**). At the sync code position extracting section **45**, the order of alignment of the codes for identifying the synchronous frame position, or the pattern of SY**4** is directly detected, and the position of the PA area **311** is detected. The place of the intermediate area **301** is detected from the results thereof (ST**35**).

[0171] FIGS. **32** to **34** show a method for accessing by using only information of the PA area **311**. FIGS. **35** to **37** show a method of accessing using also the in-ECC position information **314** or **315** within the PS area **313**.

[0172] As shown in FIGS. **32** to **34**, when accessing by using only the information of the PA area **311**, the data of the

physical sector data **45-28** (FIG. **5**), which is a scrambled state and arranged immediately after the intermediate area **301**, is given to a demodulation circuit **52**. The demodulated data is supplied to a descrambling circuit **58** (ST**36**).

[**0173**] The physical sector data **45-28** is descrambled within the descrambling circuit **58**. The data ID **1-0** existing at the head position, and the data IED **2-0** (FIG. **14**C) information (information after descrambling) are supplied to the ID and IDE extracting section **71** (ST**37**). At the error checking section **72** of the data ID, by using the information of the IDE**2**, it is checked whether or not there is an error in the detected data ID **1** (ST**38**, ST**39**).

[**0174**] When there is an error, at the ECC decoding circuit **162**, the data ID **1** after error correction processing is extracted (ST**40***a*). Within the control section **43**, the amount of difference with the address at which it is desired to start reproduction is calculated by using the data ID **1**. This difference amount determines whether the current track position is greatly deviated from the desired track position (ST**40***b*). When there is no error in step ST**39**, the routine moves directly to step ST**40***b*.

[**0175**] If the above-described difference amount is large, a difference between the value of data ID **1** of the results of reproduction and the value of data ID **1** of the sector at which start of reproduction is planned, is obtained. The track offset amount on the information storage medium **9** is calculated within the control section **143**, and dense access is carried out on the basis of the results thereof (ST**41**).

[**0176**] Namely, the data ID **1** information of the physical sector data **45-28** is detected, and the position within the ECC block is detected. Namely, at the descrambling circuit **58**, the data ID **1** portion within the physical sector data **45-28** in a scrambled state is descrambled, and the position within the ECC block is indexed (ST**36**). At this time, when the difference between the detected value of data ID **1** and the value, which is desired to be accessed and is indexed in ST**32**, is great (ST**40***b*), dense access is carried out again (ST**41**).

[**0177**] In step ST**40***b*, when it is clear that there is no great track offset, the routine moves on to step ST**42**. Immediately after the detected value of data ID **1**, the control section **43** calculates how many segments the value indexed in step ST**32** (showing the place desired to be reached) is after the current position. This after position corresponds to the physical sector data **45-32** of the head of the next ECC block **322***b* (ST**42**). Next, the control section **43** confirms (ST**43**) that the segment has passed by the number of segments **305** calculated in step ST**42**, while the information recording and reproduction section **41** always monitors the intermediate area within the passing information storage medium **9** by the methods of steps ST**34** and ST**35**. Namely, the information recording and reproduction section **41** passes by a number of segments, which number is the calculated number (or ST**43**).

[**0178**] When the information recording and reproduction section **41** reaches the head position of the desired ECC block **322***b*, in the reproduction data, the intermediate area **301** is deleted, and only the data within the user data recording field **303** is successively supplied to the demodulation circuit **52**, the ECC decoding circuit **62**, and the descrambling circuit **59**. At a main data extracting section **73**, the user data is extracted and is supplied to the exterior via the interface section **42** (ST**44**).

[**0179**] FIGS. **35** to **37** show the processes in a case of accessing a desired position by using the in-ECC position information **314** and **315** of the PS area **313**. Processes from step ST**31** to step ST**35** are the same as in the case of FIGS. **32** to **34**.

[**0180**] Namely, as shown in FIG. **35** or FIG. **5**, when access is carried out by using the in-ECC position information **314** or **315** of the PS area **313** within the ECC block, the position of the PA area **311** is indexed, and the place of the intermediate area **301** is detected from the results thereof (ST**35**). Next, the position information **314** or **315** of the PS area **313** within the ECC block is read, and the current position of the intermediate area within the ECC block **304** is searched for (ST**51**).

[**0181**] Next, it is determined whether or not the corresponding intermediate area **301** is the head position of the ECC block (ST**52**). As this method, the information of the PS area **313** positioned at the rear portion is detected. It is determined whether the head information of the PS area **313** is SY**0** or SY**5** (ST**52**).

[**0182**] As shown in FIGS. **2**A to **2**D, when the head information is SY**5**, it is known that the intermediate area **301** exists at the head of the ECC block. Further, if the head information is SY**0**, the in-ECC position information **315** immediately thereafter is detected, and it is determined which position within the ECC block **304** the corresponding segment is at.

[**0183**] When the corresponding intermediate area **301** is not at the head position of the ECC block, by the processings of steps ST**34** to ST**51**, it waits until the intermediate area **301** arranged at the head position of the ECC block **304** is reproduced (ST**53**).

[**0184**] In actuality, what segments must be passed until the head position of the next ECC block **322***b* is calculated, and the information recording and reproduction section **41** is made to pass in the tracking direction by the calculated segment number (ST**53**). This portion is a different point of the processings shown in FIGS. **32** to **34**, and in FIGS. **35** to **37**.

[**0185**] When the corresponding intermediate area **301** is at the head position of the ECC block, the data of the physical sector data **45-32** in the scrambled state at the head position of the ECC block **322***b* is supplied to the demodulation circuit **52** and demodulated. The demodulated data is supplied to the descrambling circuit **58**. This processing is obtained on the basis of control of the control section **43** (ST**54**).

[**0186**] From steps ST**37** to ST**41**, the processes are the same as the processes shown in FIGS. **32** to **34**. In step ST**55** which is executed after step ST**40***b*, the processings from step ST**33** to step ST**40***b* are executed, and the access position reaches the position of the physical sector data **45-32** which is the head position of the ECC block **304** determined in step ST**32**. After the access position has reached the desired position, the routine moves on to step ST**44**.

[**0187**] The data arrangement structure of the one segment area of FIG. **3** which is described previously is a structure of a read only area. In contrast, FIG. **6** shows the data arrangement structure of one segment area in a recordable area or a re-recordable area.

[0188] The data structure of a recordable next-generation DVD-R or a re-recordable next-generation DVD-RAM basically follows the structure of FIG. **3**. Accordingly, in the same way as the example shown in FIG. **3**, the VFO area **312**, the PS area **313**, the user data recording field **303**, and the PA area **311** are included in one segment area. However, at the one segment area of FIG. **6**, the size of the VOF area differs due to the embodiment. Namely, the size of the VFO area differs due to the embodiment.

[0189] For example, FIGS. **7**A to **7**D and **11**A to **11**D show an example of a method of recording user data on a recordable area or a re-recordable area. Here, in the embodiment shown in FIGS. **7**A to **7**D, a gap **111** (Mirror Field) exists between the VFO areas **331** and **332**. Further, in the embodiment shown in FIGS. **11**A to **11**D, the gap **111** (Mirror Field) exists immediately before the VFO area **333**. Namely, in the embodiment of FIGS. **11**A to **11**D, it means that the VFO area size immediately after the PA area **311** is "0", and the gap **111** is arranged immediately after the PA area **311**. The gap **111** is provided, and the effects of fluctuations in the recording end position due to irregular rotation of the spindle motor can be removed.

[0190] FIGS. **8** and **9** shows the method of recording the user data shown in FIGS. **7**A to **7**D, and the relationship with the physical structure of the information storage medium. As shown in FIGS. **8** and **9**, the recording area is a structure in which a meandering (wobbling) continuous groove (pregroove) is provided in a spiral shape, and recording marks **127** are formed on the continuous groove (pregroove).

[0191] At the recordable information storage medium or the re-recordable information storage medium **9**, there is formed a mark **141** for showing the recording head position of the continuous recording unit **110** which is the unit of the segment area **305** along the continuous groove (pregroove). A wobbling pattern different than that of a general wobble groove area **143** is formed in advance for the mark **141**. Further, in the present embodiment, the pattern differs due to the position within the ECC block. Namely, the pattern at the head position and at the non-head position of the ECC block changes, and therefore, it is a structure in which the ECC block head position can be detected at an even higher speed. Further, a recording preparation area **142** of a length of a wobble period determined in advance, exists adjacent to the mark **141** for recording head positioning.

[0192] When recording starts at the continuous data recording unit **110**, first, after the mark **141** for recording head positioning is detected, recording is started after a wobble detection signal is counted for the length of the recording preparation area **142**.

[0193] As shown in FIGS. **8** and **9**, in a next-generation recordable DVD-R or a next-generation re-recordable DVD-RAM, recording of the segment unit is possible from immediately after the gap **111**. The gap **111** divides the phase offset between the phase of recorded data and subsequent recording data to be recorded by recording processing to be carried out thereafter, and functions to eliminate the effects of phase offset between the before and after data processings. As a result, recording in a unit of segment is possible without recording "border-in" and "border-out" data at the next-generation DVD-R.

[0194] In the above-described method, the recording head position of the continuous data recording unit **110** is fixed. However, as shown in FIGS. **10**A and **10**B, there are cases when the actual length of a continuous data recording unit **110***a* changes due to irregular rotation of the spindle motor rotating the information storage medium **9**, and crosses over the gap **111** and a data overlap portion **116** is generated. Even when the data overlap portion **116** (FIG. **10**B) is generated in this way, in the present embodiment, the data of the user data area **303** is not destroyed. This is because, as shown in FIG. **6**, the VFO area **312** is always arranged at the head of the segment area **305** (the overlap area **116** is set so as to always be contained within the VFO area **312**).

[0195] Another embodiment of the present invention which permits the data overlap portion **116** in the worst case as shown in FIG. **10**B, is shown in FIGS. **12**A to **12**E.

[0196] As shown in FIG. **12**B, the sizes of the VFO areas **334** and **335** are set to be large in advance, and a VFO overlap area **338** (FIG. **12**C) is arranged so as to exist even when there is no irregular rotation of the spindle motor. FIG. **12**B shows the positional relationship of the time axis direction between data already recorded and data to be newly recorded or re-recorded. Data is newly recorded or re-recorded in this way, and a portion of the VFO area is overlappingly recorded. In this way, the data structure of the present embodiment can be made to coincide with the data structure of a read only area which dose not have the gap **111**. This means that the data of the read only area and the recordable or re-recordable area can be reproduced by the same reproduction circuit.

[0197] FIGS. **38** and **39** show the method of recording or re-recording in a unit of segment on the recording-type or re-recording-type information storage medium **9**.

[0198] The recording-type or re-recording-type information storage medium **9** in the present embodiment employs a CLV (Constant Linear Velocity) method. Thus, the angle of the recording position at the segment unit differs in the radial direction of the information storage medium **9**.

[0199] Accordingly, when a designation of the recording position is received (ST**11**), the angular position in the rotation direction of the mark **141** for recording head positioning shown in FIGS. **8** and **9** must be estimated (ST**12**). Further, since information of the PS area **313** and the PA area **311** shown in FIG. **6** is not included in the information inputted from the interface section **42**, this data is prepared in a sync code selecting section **47** (ST**14**).

[0200] After rough access, it is determined whether or not the mark **141** for recording head positioning is detected at the estimated angular position on the information storage medium **9** (ST**16**). On the basis of these results, it is determined whether or not the information reproduction position of the reproduction apparatus has reached the estimated track.

[0201] As shown in FIG. **9**, the wobble pattern of the pregroove differs due to the position within the ECC block. Thus, the difference in the wobble pattern is detected, and the head position of the ECC block is determined (ST**21**), and preparations for recording processing are carried out. After the information recording and reproduction section **41** has passed the final end portion of the mark **141** for recording head positioning on the information storage medium **9**, the number of wobbles within the recording preparation area **142** is counted, and preparations for record-

ing processing are carried out (ST17). Here, when it has passed the wobble by a predetermined count number, immediately thereafter, recording is carried out for each segment unit (ST18).

[0202] It is determined whether or not recording is completed (ST19), and when recording is not completed, the routine returns to step ST16. If recording is completed, the routine moves on to step ST20.

[0203] As shown in FIGS. 20A to 20C, the patterns of the PA area 311 and the PS area 313 within the intermediate area 301 are set by a synchronous pattern different than the synchronous code 110 within the physical sector data 5 (see FIGS. 13A to 13E, 14A to 14E, and 15A to 15C). As shown in FIG. 20C, as the synchronous frame position number 115, SY0 to SY3 are used as the synchronous code 110 within the physical sector data 5.

[0204] As shown FIG. 2A, SY0 or SY4 is used as the pattern of the PA area 311. Further, when the segment is at the head position of the ECC block, the pattern of SY5 is used as the pattern of the head position of the PS area 313, and when the segment is at a non-head position, the pattern of SY0 is used.

[0205] Moreover, in the present embodiment, as shown in FIG. 21B, the specific pattern contents of SY0 to SY3, coincide with the contents shown in FIG. 20C. In the synchronous code arranging method shown in FIGS. 21A to 21C, SY0 is arranged only at one place within one physical sector data 5, and is arranged at the head position of the same physical sector data 5. In this way, there is the effect that the head position of the physical sector data 5 can be easily known merely by detecting SY0. Further, as compared with a conventional DVD-ROM, DVD-R, DVD-RW, and DVD-RAM, the number of synchronous patterns can be reduced to four types which are SY0 to SY3, and the position detecting processing within the physical sector data 5 using the pattern of the synchronous code is simplified.

[0206] Further, as shown in FIG. 21C, the synchronous frame 308, which is a data size combining the synchronous code 110 and the synchronous frame data 106 after modulation, is always constant and is 116 channel bits. The fixed-length synchronous frame 308 and the data size of the intermediate area 301 coincide with each other.

[0207] In the present embodiment, as shown in FIGS. 22 and 23, combinations of three continuous synchronous codes 110 arbitrarily extracted in FIG. 21A all differ in accordance with the position within the same physical sector data. By using this technique, it is possible to extract not only the position within the same physical sector data 5 using the order of alignment of each synchronous code 110 including the PA area 311, but also the position of the intermediate area 301.

[0208] An example of the position detecting method is shown in FIGS. 22 and 23. For example, as shown in FIG. 23, when the order of alignment of SY1→SY3→SY1 is detected, it can be found, from the order of alignment shown in FIG. 21B, that the modulated synchronous frame data immediately after SY1 is 106-6. Further, when SY0→SY0→SY1, i.e., SY0 continue continuously two times, it is found, from FIG. 2A or FIGS. 20A to 20C, that the initial SY0 belongs to the intermediate area 301. Further, when SY4→SYD→SY1, i.e., the pattern SY4 which cannot exist within the physical sector data 5 are detected, without investigating the connection of the three patterns, it can immediately be determined that SY4 shows the pattern of the PA area 311 within the intermediate area 301.

[0209] Next, with reference to FIGS. 13A to 13E, FIGS. 14A to 14E, and FIGS. 15A to FIG. 31, explanation will be given of the ECC block (FIGS. 13A to 16C), the synchronous frame structure within one physical sector data (FIGS. 17A to 19D), the synchronous code 110 (FIG. 20A), the arrangement example of the synchronous codes within one physical sector (FIG. 21A), and the method of indexing the synchronous frame position within one physical sector data, from the order of alignment of the synchronous frame position identifying code within the synchronous code (FIGS. 22 and 23).

[0210] Further, another example of a common data structure recorded on the information storage medium (FIGS. 24, 25, 26, and 27), the structure of a recording system of the information recording and reproduction apparatus (FIG. 28), the structure of a reproduction system of the information recording and reproduction apparatus (FIG. 29), the internal structure of the scrambling circuit (FIG. 30), and the internal structure of the descrambling circuit (FIG. 31) will be described.

[0211] The array of the physical sector data 5-0, 5-1, . . . of the information storage medium 9 shown in FIG. 1C is shown in FIG. 13D. One physical sector data includes data 0-0-0, 0-0-1, 0-0-2, . . . as a plurality of rows, and inner-code parities PI 0-0-0, PI 0-0-1, PI 0-0-2, . . . added to the respective rows, and an outer-code parity PO 0-0 added to the next one row after the twelve rows. The other physical sector data have similar data structures. Here, the above-described respective physical sectors are defined as sectors corresponding to logical sector information 103-0, 103-1, 103-3, . . . as shown in FIGS. 13B to 13D. Moreover, the logical sector information is defined as information corresponding to one video pack or audio pack, as shown in FIGS. 13A to 13C. FIG. 13A shows a pack array of video pack 101*a*, audio pack 102*a*, . . . , and the like. FIG. 13B shows logical sector information 103-0, 103*a*-1, 103-2, . . . corresponding to the respective packs.

[0212] The contents of the data shown in FIG. 13C is described more detail in FIGS. 14A to 14E. The data 0-0-0 is data corresponding to the first row. The data 0-0-1 corresponds to the next row.

[0213] FIG. 14C shows the state in which one logical sector information 103-0 is scrambled, and the scrambled logical sector information is divided into information of 12 rows, and PI information is added to each row (12 rows in this example). Data ID, IED, CPR_MAI are added to the first row. Further, the final row (the 13^{th} row) of the logical sector is PO information.

[0214] FIGS. 15A to 15C and 16A to 16C show the relationship between the physical sector data and the ECC blocks. The ECC block is a unit to which an error correction code is added when data is recorded at the information storage medium 9, and is a unit used when data is reproduced from the information storage medium 9 and error correction is carried out.

[0215] The data array shown in FIG. 15A (corresponding to FIG. 14E and FIG. 1B) shows a state in which it is

organized as an ECC block. Every other physical sector data is selected, and is allocated to a first small ECC block **7-0** and a second small ECC block **7-1** (see FIGS. **16**A to **16**C).

[**0216**] With this example, one physical sector data is formed from 13 rows. Among these, one row is the portion of the PO information. The respective rows of the ECC block are-recorded as data **0-0-0**, **0-0-1**, **0-0-2**, . . . One small ECC block is formed from 31 physical sector data. The 62 physical sector data (the two small ECC blocks) are, for example, divided into even-numbered sector data and odd-numbered sector data. PO information is prepared for each of the blocks by the even-numbered sector data and the blocks by the odd-numbered sector data. The PO information is prepared in units of 1 ECC block organized by a plurality of physical data, and are dispersed one row by one row at the respective physical sectors. Namely, the PO information of 31 rows is prepared in small ECC block units, and the PO information is dispersed one row by one row at the 31 data blocks. One data block contains data of 12 rows.

[**0217**] FIGS. **17**A to **17**D, **18**A to **18**C, and **19**A to **19**D are diagrams explaining the structure of a synchronous frame within one physical sector data.

[**0218**] The sector block (corresponding to data of 13 rows (including the one row of PO information) shown in FIG. **17**C is divided into synchronous frame data **105-0**, **105-1**, . . . (there are 26 (13×2) altogether), as shown in FIG. **17**D. A synchronous code to be described later is added between the synchronous frame data. Namely, a synchronous code is added to the head of each synchronous frame data.

[**0219**] Namely, as shown FIGS. **18**A and **18**B, a synchronous code **110** is inserted between the synchronous frame data **106**. As shown in FIG. **19**C, the synchronous code **110** is formed from, for example, a variable code area **112**, a fixed code area **111**, and a variable code area **113**. Each area has contents such as shown in FIG. **19**D.

[**0220**] A description of the data structure is as follows.

[**0221**] As shown in FIG. **17**A, image data is recorded on the information storage medium **9** in the form of video pack **101** and audio pack **102** in 2048-byte units. The 2048-byte recording unit is treated as logical sector information **103**, as shown in FIG. **17**B.

[**0222**] In current DVD specifications, data ID **1-0**, IED **2-0**, CPR_MAI **8-0** are added to this data. Data, to which is added PI (Parity of Inner-code) information and PO (Parity of Outer-code) information corresponding to the ECC structure shown in FIGS. **16**A to **16**C, is equally divided into **26** portions, so as to form synchronous frame data **105-0** to **105-25**, as shown in FIG. **17**D. In this case, the PO information also is divided in two. As shown in FIG. **17**C, the PO information is divided in two and shows as PO **0-0-0** and PO **0-0-1**.

[**0223**] Each synchronous frame data **105** is modulated, and as shown in FIG. **19**A, synchronization codes **110** are inserted between the modulated synchronous frame data **106**. The method of modulation is generally expressed by (d,k; m,n). These letters mean that original data of m bits is converted into n channel bits, and the number of continuous "0"s is d (at minimum) and k (at maximum).

[**0224**] The present embodiment shows a case where the modulation method shown in U.S. Pat. No. 6,300,886 is employed. In this modulation method,

[**0225**] d=1, k=9, m=4, and n=6.

[**0226**] The synchronization code **110** is divided into the fixed code area **111** and the variable code areas **112** and **113**, and the variable code areas **112** and **113** are structured so as to be more finely divided into a recording position of a conversion table selection code **122** at modulation, a recording position of a synchronous frame position identifying code **123**, and a recording position of a DC suppressing polarity reversing pattern **124** (partially including combination/sharing of recording positions), as shown in FIG. **19**D.

[**0227**] Modulation here means converting input data into modulation data in accordance with the above-described modulation rule. In this case, for the conversion processing, a method is used of selecting modulation data corresponding to the input data, from among the large number of modulation data recorded in the conversion table. Here, a plurality of conversion tables are prepared. Accordingly, information, expressing that the modulation data is modulation data converted by using which table at the time of modulation, is needed. This information is the conversion table selection code **122** at modulation. This shows the conversion table which generates the modulation data which will come next of the modulation data immediately before the synchronization code.

[**0228**] The synchronous frame position identifying code **123** is a code for identifying the frame of which position within the physical sector is the synchronous frame. In order to identify the frame, the frame can be identified by an arrangement pattern of a plurality of synchronous frame position identifying codes before and after.

[**0229**] An example of specific contents of the synchronous position detecting code **121** is shown in FIGS. **20**A to **20**C.

[**0230**] A code, which cannot exist within the synchronous frame data **106** after modulation, is arranged within the synchronous position detecting code **121** in order to facilitate detection of the position of the synchronous code **110**. Because the modulated synchronous frame data **106** is modulated in accordance with the (d,k; m,n) modulation rule, it is not possible that k+1 "0"s are continuous within the modulated data. Accordingly, it is preferable to provide a pattern, in which k+1 or more "0"s are continuous, as the pattern within the synchronous position detecting code **121**.

[**0231**] However, if a pattern, in which k+1 or more "0"s are continuous, is provided as the pattern within the synchronous position detecting code **121**, at the time of reproduction of the modulated synchronous frame data **106**, when one bit shift error arises, there is the fear that it will be misdetected as the synchronous position detecting code **121**. Accordingly, it is preferable to provide a pattern, in which k+2 "0"s are continuous, as the pattern within the synchronous position detecting code **121**. However, if the pattern in which the "0"s are continuous continues for too long, a phase offset at the PLL circuit **174** easily arises.

[**0232**] In current DVDs, a pattern in which k+3 "0"s are continuous is utilized (the modulation rule for current DVDs is (2,10; 8,16). Accordingly, in order to suppress the occurrence of bit shift errors and ensure the reliability of syn-

chronous code position detection and information reproduction more than in current DVDs, the length by which "0"s are continuous in the present embodiment must be k+3 or less, and preferably k+2.

[0233] As is shown in FIG. **8** of U.S. Pat. No. 6,229,459 and the explanatory description thereof, the DSV (Digital Sum Value) value changes due to the modulated bit pattern. If the DSV value is greatly offset from 0, the DSV value can be made to approach 0 by changing the bit from "0" to "1" at the optimal bit pattern position.

[0234] Accordingly, the DC suppressing polarity reversing pattern **124**, having a specific pattern for making the DSV value approach 0, is provided within the synchronous code **110**.

[0235] Further, when the modulation method shown in U.S. Pat. No. 6,300,886 is used, the following must be considered. Namely, demodulation of the 6 channel bits which are the object of demodulation must be carried out by using the "selection information of the conversion table used when modulating the 6-channel bit modulated data" existing immediately after the 6-channel bit modulated data which is the object of demodulation.

[0236] Accordingly, the selection information of the conversion table of the 6 channel bits which should come after the final 6 channel bits of the modulated synchronous frame data **106** arranged immediately before the synchronous code **110**, are recorded within the "conversion table selection code **122** at modulation" of the head within the synchronous code **110**. Namely, the conversion table selection code **122** at modulation exists within the synchronous code **110**.

[0237] This conversion table selection code **122** at modulation is conversion table selection information for the 6 channel bits which should come after the final 6 channel bits of the immediately previous modulated synchronous frame data **106**. By referring to this conversion table information, the conversion table which should be used can be determined at the time of demodulating the next data.

[0238] Next, a specific example of the synchronous code **110** will be described.

[0239] FIGS. **20**A to **20**C show a specific example of the synchronous code **110**. The synchronous code **110** has the variable code area **112** and the fixed code area **111**. In the variable code area **112** is arranged the data structure shown in FIGS. **19**A to **19**D in which the conversion table selection code **122** at modulation, the synchronous frame position identifying code **123**, and the DC suppressing polarity reversing pattern **124** are integral.

[0240] For example, 0 to 5 are prepared as numbers for synchronous frame position identification. The numbers 0 to 5 correspond to the syncs YS**0** to YS**5**. In order to express the modulation table selection code at the time of modulation, a conversion table number **116** is prepared. For the pattern when the conversion table number=1 and the pattern when the conversion table number=0, the respective cases are broadly classified and patterns A and B for DC suppression are prepared.

[0241] For example, with this example, when 8 channel bits are allotted and the synchronous frame expresses synchronous frame SY**0**, "10000000", or "10000000", or "00010000", or "00010010" exists as the synchronous code. This means that, when it is "10000000", conversion table number=0 is used, and when it is "00010000" or "00010010", conversion table number=1 is used. This synchronization pattern is selected and used in accordance with the DSV.

[0242] For example, 16 channel bits are allotted, and the synchronous position detecting code **121** is "1000000000000100".

[0243] The mode of selection of the synchronization pattern used in the intermediate area **301** is explained with reference to FIG. **1**C.

[0244] Namely, according to the present embodiment, a synchronous pattern, which is different from the synchronous code **110** within the physical sector data **5**, is set as the synchronous pattern of the PA area **311** and the PS area **313** within the intermediate area **301**. As shown in FIG. **20**C, as the synchronous frame position number **115**, SY**0** to SY**3** are used as the synchronous code **110** within the physical sector data **5**.

[0245] As shown in FIG. **2**A, SY**0** or SY**4** is used as the synchronous pattern of the PA area **311**. Further, as the head pattern of the PS area **313**, the pattern of SY**5** is used when the corresponding segment is the head position of the ECC block, and the pattern of SY**0** is used when it is not the head position.

[0246] FIGS. **21**A to **21**C show an arrangement example of the synchronous code within one physical sector data.

[0247] The synchronous code is 24 channel bits as the total of the synchronous pattern of the 8 channel bits and the synchronous position detecting code **121** of 6 channel bits, as described previously. One row of the modulated synchronous frame data is 1092 channel bits. FIG. **21**B makes it easy to see the synchronous code position, by rearranging the modulated frame data **106-0**, **106-1**, . . . in a matrix form, within the data array of FIG. **21**A (the same as the data array of FIG. **19**A). The channel bit length of the synchronous code and modulated synchronous frame data is synchronous frame **308** (a fixed length of 116 channel bits) (this state is shown in FIG. **2**C as well).

[0248] The specific pattern contents of SY**0** to SY**3** shown in FIG. **21**B are selected from the pattern shown in FIG. **20**C. According to the synchronous code arranging method shown in FIG. **21**B, SY**0** is arranged only at one place within 1 physical sector data **5**, and is arranged at the head position of the same physical sector data **5**.

[0249] In this way, there is the effect that, by merely detecting SY**0**, the head position of the physical sector data **5** can easily be known. Further, the number of the synchronous pattern is reduced to the four types which are SY**0** to SY**3**, as compared with a current DVD-ROM, DVD-R, DVD-RW, and DVD-RAM, and position detection processing within the physical sector data **5** can be carried out by using the pattern of the synchronous code. Thus, the position detecting processing is simplified.

[0250] Further, as shown in FIG. **21**C, the synchronous frame **308**, which is a data size combining the synchronous code **110** and the modulated synchronous frame data **106**, is always constant and is 1116 channel bits. Further, the fixed-length synchronous frame **308** and the data size of the intermediate area **301** coincide with each other.

[0251] Next, with reference to FIGS. **22** and **23**, explanation will be given of the method of detecting the synchronous code and determining at what position within the physical sector the currently reproduced data is at.

[0252] As shown in FIG. **22**, the modulated synchronous data reproduced by the information recording and reproduction section **41** from the information storage medium is supplied to the synchronous code position extracting section **45**, and is made to be the object of synchronous code position detection. At the synchronous position extracting section **45**, the position of the synchronous position detecting code **121** (the code of the fixed code area in FIG. **20**A) is detected by, for example, a pattern matching method.

[0253] In this way, the synchronous code position can be detected, and the synchronous code can be extracted. The information of the detected synchronous code **110** is, via the control section **43**, successively held in a memory section **137** as shown in FIGS. **22** and **23**. When the position of the synchronous code **110** is known, the position of the modulated synchronous frame data is also known. Therefore, the synchronous frame data is successively stored in the shift register circuit **170** as shown in FIG. **22**.

[0254] By inspecting the order of alignment of the synchronous code, it can be determined at what position of the matrix system of FIG. **21**B the modulated synchronous frame data is at. This is because the synchronous code is arranged in the pattern shown in FIG. **21**B (SY**0**→SY**1**→SY**1**→SY**1**→SY**2**→SY**1**→SY**1**→SY**3**→SY**1**→SY**2**→SY**2**→SY**1**→SY**3**→SY**2**→SY**1**→SY**2**→SY**3**→SY**3**→SY**3**→SY**2**→SY**2**→SY**2**→SY**3**→SY**2**→SY**3**→SY**1**).

[0255] Combinations of three continuous synchronous codes **110** arbitrarily extracted in FIG. **23** all differ in accordance with the position within the same physical sector data. By using this feature, it is possible to extract not only the data position within the same physical sector data **5** using the order of alignment of each synchronous code **110** including the PA area **311**, but also the data position within the intermediate area **301**.

[0256] An example of the position detecting method is shown in FIG. **22**. For example, as shown in FIG. **23**, when the order of alignment of SY**1**→SY**3**→SY**1** is detected, it can be known, from the order of alignment shown in FIG. **21**B, that the modulated synchronous frame data immediately after SY**1** is **106-6**.

[0257] Further, when SY**0**→SY**0**→SY**1** is detected, i.e., SY**0** continue continuously two times, it is known that the agreement shown in FIG. **2**A, or the initial SY**0** from the information of FIG. **20**C, belongs to the intermediate area **301**. Further, when SY**4**→SY**0**→SY**1** is detected, i.e., SY**4** which cannot exist within the physical sector data **5** is detected, without investigating the connection of the three patterns, it can immediately be determined that SY**4** shows the pattern of the PA area **311** within the intermediate area **301**.

[0258] Further, when the order of alignment of SY**0**→SY**1**→SY**1** is detected, it is known, from the order of alignment shown in FIG. **21**B, that the modulated synchronous frame data immediately after SY**0** is **106-1**.

[0259] Next, another example of the pre-modulation sector data being scrambled will be shown.

[0260] Description will be given with the physical sector data being scrambled as shown in FIGS. **13**A to **13**E and **14**A to **14**E. In the example shown in FIG. **14**C, data ID, IDE, CPR_MAI of the head of the physical sector data are shown as not being scrambled.

[0261] However, as shown in FIG. **24**, all of data ID **1**, IED **2**, specific data (e.g., data type **3**, preset data **4**), and main data (including EDC) may be subjected to scrambling processing.

[0262] In the example of FIG. **24**, specific data (e.g., data type **3**, preset data **4**) is used as the initial data for executing the scrambling. The specific data is extracted from the main data (sector data). The extracted specific data is used as is as the initial value (or trigger) of the scrambling circuit, and scrambling processing is carried out, and all of the main data (sector data) are scrambled. The scrambled data is modulated in accordance with a predetermined modulation rule, and then, the above-described synchronous code is added. Data, for which this processing is carried out, is recorded onto the re-recordable information storage medium **21**.

[0263] FIG. **25** is an example in which the aforementioned specific data is replaced by CPR_MAI (copyright managing information) **8***a*. This is because, at a DVD-ROM, this CPR_MAI is used at the portion of the specific data. Other processings are the same as the example of FIG. **24**.

[0264] FIG. **26** is for explanation of the processes in the reproduction processing corresponding to the recording processing of FIG. **24**. The data reproduced from the re-recordable information storage medium **21** is formed from the synchronous codes **19***a*, **19***b*, **19***c*, . . . and pre-demodulated data **15***a*, **15***b*, **15***c*, . . . As described previously, the synchronous codes and the pre-modulated data are separated, and the pre-modulated data is collected. The collected pre-modulated data is demodulated in accordance with a predetermined demodulation rule, and is collected as data **17** which is scrambled as is. As explained in FIG. **24**, the specific data is scrambled and contained in the data **17**. This scrambled specific data is extracted from a predetermined position arranged in advance. The descrambling section uses the specific data scrambled as is, and descrambles the data **17** scrambled as is as shown in FIG. **26**. Due to the descrambling processing, it is made to be data which is the same as the data shown in FIG. **24** (the original data is reproduced).

[0265] FIG. **27** is for explanation of the processings in the reproduction processing corresponding to the recording processing of FIG. **25**. In this example, the aforementioned specific data is merely replaced by CPR_MAI (copyright managing information) **8***a*. This is because, at a DVD-ROM, this CPR_MAI is used at the portion of the specific data. Other processings are the same as the example of FIG. **26**.

[0266] FIG. **28** shows blocks relating to the recording system in particular, in an information recording and reproduction apparatus. This is a block diagram explaining the structure of an information recording system with respect to a re-recordable information storage medium or a read only information storage medium.

[0267] Main data for recording (source data or user data) is supplied to a predetermined information adding section **68** via the interface section **42**. At the predetermined information adding section **68**, the source data is finely divided in a

unit of sector, and the finely divided source data is array-stored in the main data **6** portion of FIG. **24** or FIG. **25**.

[**0268**] When the medium used in recording is the re-recordable information medium **21**, at the predetermined information adding section **68**, the ID **1**, IED **2**, data type **3**, present data **4**, and reserve area **5** of that sector are added before the main data **6** portion, and the EDC **7** is added after the main data **6** portion. The ID **1** added at this time is obtained from a data ID generating section **65**, and the preset data **4** is obtained form a preset data generating section **66**. The preset data generating section **66** has a "random number generating function", and can always generate a time-varying random number as the preset data **4**. Note that the preset data generating section **66** can also separately generate the lower n bits of the preset data, and sends them to the synchronous code selecting section **46** as one portion of the generated lower n bit synchronous code selection key.

[**0269**] On the other hand, when the medium used in recording is the read only information medium **22**, at the predetermined information adding section **68**, the ID **1**, the IED **2**, and the copyright managing information **8** (**8***a* and **8***b*) of that sector are added before the main data **6** portion, and the EDC **7** is added after the main data **6** portion. The ID **1** added at this time is obtained from the data ID generating section **65**, and the copyright managing information **8** (**8***a* and **8***b*) is obtained from a copyright managing information data generating section **67**. Note that the copyright managing information data generating section **67** can also separately generate the lower n bits of the copyright managing information, and sends them to the synchronous code selecting section **46** as one portion of the generated lower n bit synchronous code selection key.

[**0270**] Note that, in the present embodiment, the "n" of the lower n bits is selected from the range of 1 to 8 bits.

[**0271**] The sector data of the data structured shown in FIG. **24** generated at the predetermined information adding section **68** is supplied to a data arrangement portion exchanging section (or data extracting section) **63**. The data arrangement portion exchanging section **63** extracts the specific data form the sector data which is supplied in.

[**0272**] The extracted specific data and the entire sector data are supplied to a scrambling circuit **57**. The scrambling circuit **57** carries out sampling processing on the entire sector data from the sector head to the sector tail.

[**0273**] The sector data subjected to scrambling processing in this way is successively supplied to an ECC encoding circuit **61**. The ECC encoding circuit **61** ECC encodes a predetermined number of the input sector data (e.g., sector data of from 16 sectors to 32 sectors).

[**0274**] The ECC-encoded data is supplied to a modulation circuit **51**. The modulation circuit **51**, while obtaining necessary information from the conversion table for modulation **53**, carries out a predetermined modulation (e.g., 8/16 modulation or the like, although the modulation is not limited to this method) on the data which is supplied to. The modulated data is supplied to a data synthesizing section **44**.

[**0275**] The value of the digital sum value (DSV) therefor is calculated at a DSV value calculating section **48** for the modulated data (e.g., 6 channel bits) of the end portion of each sector among the modulated data supplied to the data synthesizing section **44**. The calculated DSV value is supplied to a synchronous code selecting section **46**.

[**0276**] The synchronous code selecting section **46** selects a specific (optimal) synchronous code from the plural types of synchronous code tables recorded in the synchronous code selection table recording section **47**, on the basis of the DSV value calculated at the DSV value calculating section **48**, and either the lower n bit data from the preset data generating section or the lower n bit data from the data generating section **67** of the copyright managing information.

[**0277**] Note that, in the present embodiment, four or more types (e.g., eight types) of synchronous code tables for the synchronous code (**19***a* or **19***e*) at the same place within the sector (e.g., the head position) may be prepared. In this way, a plurality of types (e.g., eight types) of the bit pattern of the synchronous code coming to the head position of each sector (**33** or **34**) can be used.

[**0278**] The synchronous code within the synchronous code table selected from the synchronous code table recording section **47** by the synchronous code selecting section **46**, is, at the data synthesizing section **44**, arranged alternately with the modulation data from the modulation circuit **51**.

[**0279**] The data which is structured in this way is recorded to a re-recordable information medium **21** (a RAM disk, a RW disk or the like using a change of phase recording method).

[**0280**] On the other hand, when the synthesized data is for a read only information medium, the data is

[**0281**] (a) cut at an original plate for ROM disk copying by an original plate recording section of a ROM disk, or

[**0282**] (b) printed onto an R disk (a disk using pigment whose reflectance of the recording laser irradiated portions permanently changes) for exclusive use for reproducing after once being recorded, by the information recording and reproduction section **41**.

[**0283**] The operation of each block element of the above-described apparatus is controlled in accordance with a control program recording in the ROM within the control section **43**, by using the ROM therein as a work area, by an MPU therein.

[**0284**] FIG. **29** is a block diagram for explanation of the structure of an information reproduction system for a re-recordable information storage medium or a read only information storage medium.

[**0285**] In the data structure immediately after reproduction from the information storage medium (**21** or **22**) from the information recording and reproduction section (or reproduction section not having a recording function) **41**, in the case of the example of FIG. **26** for example, pre-modulated data **15***a*, **15***b*, . . . and synchronous codes **19***a*, **19***b*, **19***c*, . . . are arranged so as to be mixed together. The reproduced data immediately-after reproduction by the reproduction section **41** is supplied to a synchronous code position detecting/extracting section **45** and a demodulation circuit **52**.

[**0286**] The synchronous code position detecting/extracting section **45** uses a pattern matching method, and searches for and detects the synchronous code at the head position of

each sector from the reproduced data immediately-after reproduction. After the synchronous code of the head position is detected, the following synchronous code within that sector is also detected and extracted.

[0287] The information of the extracted synchronous code is supplied to the demodulation circuit **52**. Due to the information of the synchronous code from the synchronous code position detecting/extracting section **45**, the demodulation circuit **52** knows the sector head position of the reproduction data from the reproduction section **41**, and can also know the synchronous code position within that sector.

[0288] Within the demodulation circuit **52**, the synchronous code included in the sector is deleted by the synchronous code information from the synchronous code position detecting/extracting section **45**. After deletion, the post-modulated data (this is 8/16 modulated) remaining within the sector is demodulated on the basis of demodulation information from a conversion table for modulation **54**.

[0289] The data demodulated at the demodulation circuit **52** is supplied to the descrambling circuit **58** and the ECC decoding circuit **62**. The descrambling processing is explained in FIGS. **26** and **27**.

[0290] Namely, information of specific data is within a predetermined range of descrambled data. The descrambling circuit **58** first descrambles the data ID, IED portions by using the specific data which is scrambled. The descrambled data ID, IED are extracted at a data ID portion & IED portion extracting section **71**. The data ID portion & IED portion extracting section **71** sends the data ID, IED to the control section **43**. The control section **43** monitors the successively obtained data IDs.

[0291] The MPU of the control section **43** can carry out detection of off-track by the information contents of descrambled ID **1**.

[0292] When it is detected that there is off-track, reading of information is carried out again within a short period.

[0293] The data demodulated at the demodulation circuit **52** is supplied to the ECC decoding circuit **62** as well. The ECC decoding circuit **62** groups together a predetermined number (16 or 32) of sectors into one ECC block, ECC decodes the ECC encoded data, and thereafter, sends it to the descrambling circuits **58** and **59**.

[0294] At the descrambling circuit **59**, descrambling of the entire main data portion is carried out. At this time, the specific data extracted before is used scrambled as is. This processing is carried out when it is detected that there is no off-track.

[0295] Note that the identification as to whether the used medium is the re-recordable information medium **21** or the read only information storage medium **22** can be carried out by using medium identifying information (not shown) recorded on a specific portion of the medium (the inner peripheral portion at a disk medium).

[0296] The data after descrambling processing is supplied to a data arrangement portion exchanging section **64**. The data arrangement portion exchanging section **64** sends, to the data ID portion & IED portion extracting section **71**, the specific data within the data after descrambling processing which has been sent in.

[0297] The data ID, IED in the descrambled-processed data are detected by the data ID portion & IED portion extracting section **71**, and the data ID after error checking is extracted. The main data **6** of a fixed length is extracted by the main data extracting section **73** from the head position of each obtained sector data, and is supplied to the exterior via an interface section **42**.

[0298] The operations of the respective block elements of the apparatus of FIG. **29** are controlled in accordance with a control program recorded into the ROM inside the control section **43**, and by using the RAM therein as a work area, by the MPU therein. Further, the data processing explained in FIGS. **32** to **39** is also carried out in accordance with a control program.

[0299] Next, specific examples of the scrambling circuit and the descrambling circuit will be described.

[0300] FIG. **30** shows the scrambling circuit **57**, and FIG. **31** shows the descrambling circuit **58**.

[0301] The bit array which is the object of scrambling is processed bit-by-bit in units of 8 bits (1 byte).

[0302] The scrambling circuit **57** comprises an 8-bit shift register circuit **91**, an 8-bit switch array **93** having a predetermined on/off pattern, and an adding circuit array **95** selectively connected to respective bits r**0** to r**7** of the shift register circuit **91** via the switch array **93**.

[0303] The shift register circuit **91** is initially cleared (CLR), and in a state in which there is no input A to the data port (DATA), all of the bits r**0** to r**7** become "0". The shift register circuit **91** receives, bit-by-bit, the input to the data port DATA at a clock timing of a predetermined clock (CK), and fetches the received bit data while successively bit shifting from bit r**0** to r**7**.

[0304] The adding circuit array **95** has seven serially connected 1-bit address connected selectively to the bits r**0** to r**7** of the shift register circuit **91**, and a final-stage 1-bit address (the right end of the array **95**) which 1-bit-adds the cumulative added results of the one-bit-adders and the scramble input A, and outputs them. Scramble results (scramble data **11***a*) is outputted from this final-stage 1-bit-adder.

[0305] Note that the on/off pattern of the switch array **93** is the same as the on/off pattern of the switch array **93** of the scramble circuit **59** shown in FIG. **31**. This on/off pattern becomes one type of key information for the scrambling/descrambling processing.

[0306] The scramble circuit **57** works as follows with respect to input data shown in FIG. **24** or FIG. **25**.

<Case of Input Data Shown in FIG. **24**>

[0307] First, from the head of the specific data (the initial 8 bits of the data type **3** and the preset data **4**) extracted from the sector data which is to be scrambled, it is supplied to the data port DATA of the shift register circuit **91** via the final-stage 1-bit-adder (right end of the array **95**). This specific data SD-A (a 0/1 bit array of 8 bits) is, bit-by-bit from the head thereof, synchronized with the timing of the clock CK, and fetched successively to bits r**0** to r**7** of the shift register circuit **91**.

[0308] The respective bits r0 to r7 of the shift register circuit **91** are connected to the adding circuit array **95**, which is formed from eight serially connected 1-bit-adders, via the 8-bit switch array **93** having a predetermined on/off pattern. The adding circuit array **95** 1-bit-adds (binarily adds), in real time and cumulatively, the 1-bit data ("0" or "1") which is set (cleared if before setting) at the shift register bits of positions which are on (e.g., bits r7, r5, r3, r1) among the switch array **93**, and inputs the added results ("0" or "1" of 1 bit) to the final-stage 1-bit adder (1-bit adder to which the input A is given). The output of the final-stage 1-bit adder (1-bit added result) is the bit of the initial scrambling result with respect to the input A, and is the head of the specific data of scrambled data **11***a*.

[0309] Similarly, synchronously with the timing of the clock CK, the data bits before scrambling are, serially and bit-by-bit, fetched at the shift register **91**. Synchronously therewith and in parallel thereto, the scrambled data bits are, serially and bit-by-bit, outputted from the final-stage 1-bit adder of the adding circuit array **95**. When output of the initial 8-bit scrambled data is completed in this way, immediately without a break, the next 8 bits are similarly scrambled, and the scrambled data bits are outputted from the final-stage 1-bit adder of the adding circuit array **95**. Thereafter, similarly, the following data (ID **1** and thereafter) is scrambled in predetermined units (8 bits, i.e., 1 byte), and is supplied to the ECC encoding circuit **61** as scrambled data **11***a*.

[0310] Among the 0/1 bit array of the 8-bit (1-byte) unit obtained serially in this way, the portion corresponding to the specific data structured by the initial, predetermined number of bytes (e.g., 1 byte) is used as the trigger of the scrambling. Because this is not needed as recording information, it is discarded (or ignored) in the recording processing after. Because contents which are the same as the discarded portion corresponding to the specific data are included in the scrambled data thereafter as well, they can be discarded.

<Case of Input Data Shown in FIG. **25**>

[0311] The circuit operations themselves of the scrambling circuit **57** are the same as in the case of input data shown in FIG. **24**. However, in the case of input data shown in FIG. **24**, the trigger for scrambling is included in the time-variable data (the preset data **4**), whereas, the case of input data shown in FIG. **25** differs in that the trigger for scrambling is fixed data (copyright managing information CPR_MAI). Because the triggers for scrambling are different for input data shown in FIG. **24** and input data shown in FIG. **25**, even if the same scrambling circuit is used, the scrambled data **11***a* with respect to the input data shown in FIG. **24** and the scrambled data **11***b* with respect to the input data shown in FIG. **25** are different bit arrays.

[0312] In the scrambling circuit **57** of FIG. **30**, the adding circuit array **95** does not form a processing loop (the added result of the final-stage 1-bit adder is not fed-back to another adder input). Thus, even if an error arises for some reason in the scrambling processing, that error does not extend to more than 8 bits. Namely, because the error propagation distance is limited to 8 bits, the reliability in the scrambling circuit operation improves.

[0313] FIG. **31** is a circuit diagram showing an example of the descrambling circuit **58**. Here, in the same way as the scrambling circuit **57**, the bit array which is the object of descrambling is processed bit-by-bit in units of 8 bits (1 byte).

[0314] The descrambling circuit **58** comprises the 8-bit shift register circuit **91**, the 8-bit switch array **93** having a predetermined on/off pattern (the same as the on/off pattern of the switch array **93** of FIG. **30**), and the adding circuit array **95** selectively connected to the respective bits r0 to r7 of the shift register circuit **91** via the switch array **93**.

[0315] The shift register circuit **91** is initially cleared CLR, and in a state in which there is no input to the data port DATA, all of the bits r0 to r7 become "0". The shift register circuit **91** receives, bit-by-bit, the input to the data port DATA at the clock timing of the predetermined clock CK, and fetches the received bit data while successively bit shifting from bit r0 to r7.

[0316] The adding circuit array **95** has eight serially connected 1-bit adders connected selectively to the bits r0 to r7 of the shift register circuit **91**. The descrambled bit array is inputted bit-by-bit from the head thereof to an initial-stage 1-bit adder (right end of the array **95**) selectively connected to bit r0. Cumulative added results of the 1-bit adders of the adding circuit array **95** are outputted from the initial-end 1-bit adder (the left end of array **95**). The bit array of the descrambled results formed of ID **1**, IED **2**, CPR_MAIb **8***b*, and main data **6***a* or ID **1**, IED **2**, reserve area **35**, and main data **6***a* is obtained from the final-stage 1-bit adder.

<Case of the Data **17** Shown in FIG. **26** Being Descrambled>

[0317] The descrambling circuit **58** of FIG. **31** operates as follows with respect to scrambled data **17**.

[0318] The scrambled data type and the data **23** of the position of the preset data, and the scrambled data **17** are input to the data port DATA of the shift register circuit **91** successively. This data (a 0/1 bit array of 8 bits) is, synchronously with the timing of the clock CK, fetched successively and bit-by-bit from the head thereof at the bits r0 to r7 of the shift register circuit **91**.

[0319] The bits r0 to r7 of the shift register circuit **91** are connected to the adding circuit array **95**, which comprises 8 serially-connected 1-bit adders, via the 8-bit switch array **93** having the same on/off pattern as the switch array **93** of FIG. **30**. The adding circuit array **95** 1-bit-adds (binarily adds), cumulatively and in real time, the 1-bit data ("0" or "1") set at the shift register bit of the position which is on among the switch array **93**, and outputs the added results ("0" or "1" of 1 bit) from the final-stage 1-bit adder (the 1-bit adder of the left end to which the register r7 is connected). The output of the final-stage 1-bit adder (1-bit added results) is the descrambled data.

[0320] Similarly, synchronously with the timing of the clock CK, the data bits before descrambling are, serially and bit-by-bit, fetched at the shift register **91**, and input to the initial-stage 1-bit adder at the right end of the adding circuit array **95**. Synchronously with the timing of the clock CK, the descrambled data bits are, serially and bit-by-bit, outputted from the final-stage 1-bit adder of the adding circuit array **95**. When output of the initial 8-bit descrambled data is completed in this way, immediately without a break, the next 8 bits are similarly scrambled, and the scrambled data bits

are outputted from the final-stage 1-bit adder of the adding circuit array **95**. Thereafter, similarly, the following data is descrambled in predetermined units (8 bits, i.e., 1 byte), and the descrambled output A is obtained.

[**0321**] Among the 0/1 bit array of the 8-bit (1-byte) unit obtained serially in this way, the portion corresponding to the specific data structured by the initial, predetermined number of bytes (e.g., 1 byte) is used as the cue for starting descrambling processing. Because this is not needed as reproduction information, it is discarded (or ignored) in the recording processing after. Because contents which are the same as the discarded portion corresponding to the specific data (SD-A) are included in the scrambled data thereafter as well, they can be discarded.

<Case of the Data **18** Shown in FIG. **27** Being Descrambled>

[**0322**] The circuit operations themselves of the descrambling circuit are the same as in the case of data **17**. However, in the case of data **17**, the trigger for the descrambling is included in the time-varying data (preset data **4**), whereas the case of data **18** differs in that the trigger for descrambling is fixed data (copyright managing information CPR_MAI).

[**0323**] In this descrambling circuit as well, the adding circuit array **95** does not form a processing loop (the added result of the final-stage 1-bit adder is not fed-back to another adder input). Thus, even if an error arises for some reason in the descrambling processing, that error does not extend to 8 bits or more. Namely, because the error propagation distance is limited to 8 bits, the reliability in the descrambling circuit operation improves.

<Feature of the Embodiment of FIG. **31**>

[**0324**] If the descrambling circuit **58** has a feedback loop with respect to the input data, when an error arises in the input data for some reason (effects such defects in the information storage medium **21**/**22** and/or as dust or scratches at the medium surface), the error is propagated in processing thereafter by the circulating processing operation of the feedback loop. However, if no feedback loop is provided, even if an error is included in the input data, the place of the error is not fed-back (circulated), and will extinguish as is from the shift register circuit **91** after passing through the shift register circuit **91**. Namely, by using a circuit structure not having a feedback loop, the characteristic that an error does not propagate for greater than or equal to the number of bits of the shift register circuit **91** (an error propagation suppressing characteristic) is obtained.

[**0325**] As described above, in accordance with the embodiment of the present invention, an improvement in the data format (recording data format) recorded on an information storage medium, or an improvement in the recording method or the reproduction method recording information onto an information storage medium, and an improvement in an information reproduction apparatus or an information recording and reproduction apparatus, are achieved, and simplification relating to positional detection of a synchronization code is aimed for, and reliability of detection of a synchronization code can be improved.

[**0326**] As examples in which the present invention is effective, the present invention is effective as a technique for ensuring compatibility between next-generation DVD formats, next-generation DVD-ROM recording formats, next-generation DVD-R, DVD-RW formats, next-generation DVD-ROM and DVD-R, DVD-RW or DVD-RAM. Further, the present invention can also be applied to communications equipment using the above-described data structure.

What is claimed is:

1. A read only storage medium comprising:

user data recording areas and intermediate areas which are alternately arranged, the intermediate areas recording at least information for synchronization.

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