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An agency of Industry Canada

CA 2162795 C 2006/01/10

(11)(21) 2 162 795

(12) BREVET CANADIEN
CANADIAN PATENT

(13) C

(22) Date de dépôt/Filing Date: 1995/11/14

(41) Mise à la disp. pub./Open to Public Insp.: 1996/05/18

(45) Date de délivrance/Issue Date: 2006/01/10

(30) Priorité/Priority: 1994/11/17 (307117/1994) JP

(51) Cl.Int.^{7}/Int.Cl.^{7} G09G 3/00

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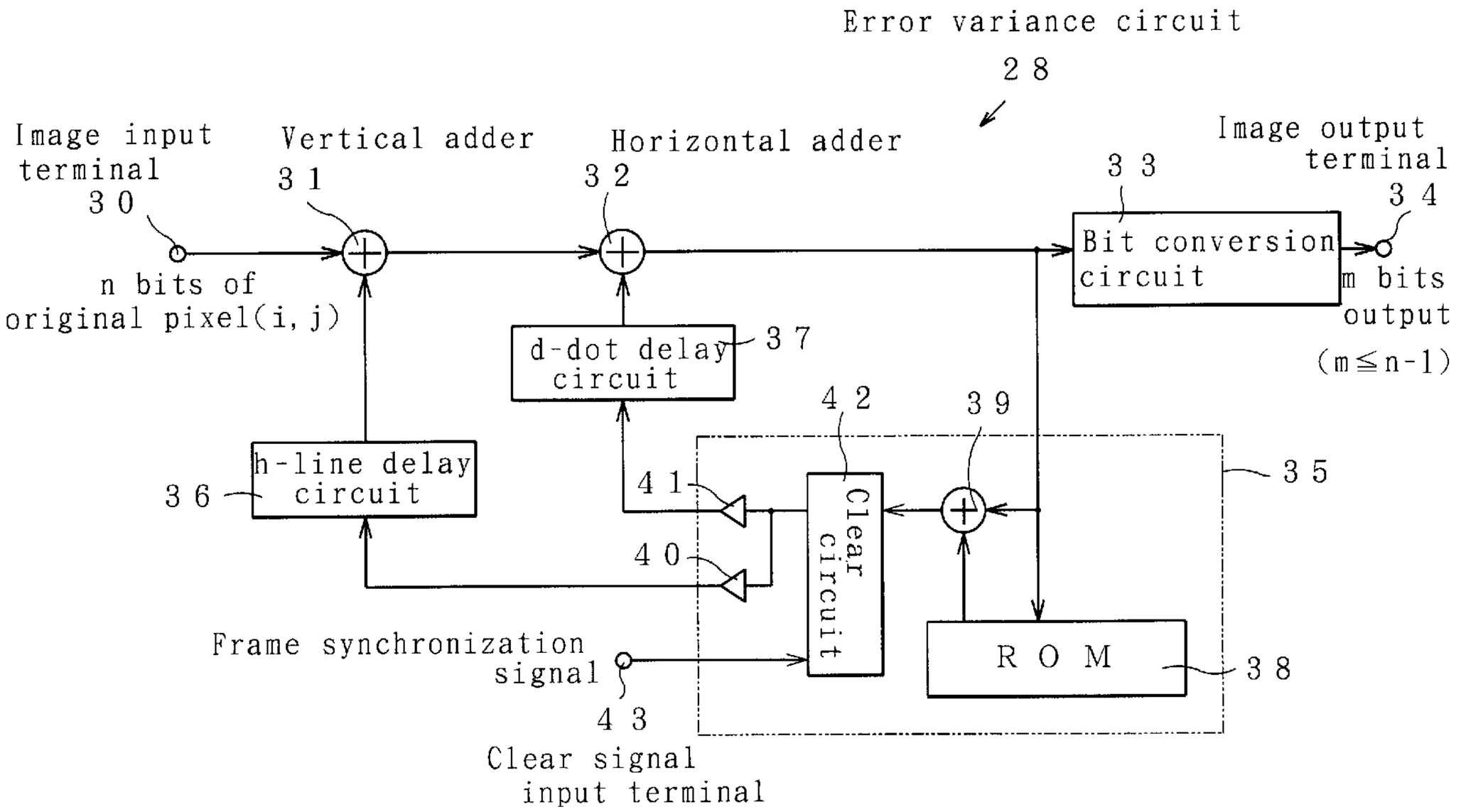
(54) Titre : CIRCUIT DE MESURE DE VARIANCE DES ECARTS
(54) Title: ERROR VARIANCE CIRCUIT



(57) Abrégé/Abstract:
In a circuit in which the reproduced error as detected at an error detect circuit 35 is added to the image signal of the input signal picture element of n bits, and further the variance output signal is converted into a signal of m (≦n-1) bits to output on the display panel, the error detect circuit 35 having a clear circuit 42 that clear the error at every frame may reduce forcible to zero the prior error for every frame thus preventing excessive noise from preceding frames and non-image duration to avoid flickering of picture.

AN ERROR VARIANCE CIRCUIT

ABSTRACT OF THE DISCLOSURE

In a circuit in which the reproduced error as detected at an error detect circuit 35 is added to the image signal of the input signal picture element of n bits, and further the variance output signal is converted into a signal of m (≦n-1) bits to output on the display panel, the error detect circuit 35 having a clear circuit 42 that clear the error at every frame may reduce forcible to zero the prior error for every frame thus preventing excessive noise from preceding frames and non-image duration to avoid flickering of picture.

SPECIFICATION

TITLE OF THE INVENTION

AN ERROR VARIANCE CIRCUIT

BACKGROUND OF THE INVENTION

(1) Field of the Invention

This invention relates to an error variance circuit that annihilates the flickering of image due to the error transmission from preceding frames or to the influence of non-image duration in such a display device as plasma display panel (PDP) and liquid crystal panel.

(2) Description of the Prior Art

Recently PDP (Plasma Display has been attracting a great deal of public attention as a thin, light-weighted display device. Totally different from the conventional CRT drive system, the drive method of this PDP is a direct drive by means of digitalized image input signal. Consequently, the luminance and tone of the light emitted from the panel face depends on the bit number of the signal to be processed.

PDP may be classified into two types: AC and DC types whose basic characteristics are different from each other.

AC type features satisfactory characteristics as far as is concerned the luminance and durability. As for the tonal display, maximum 64 tones only have reportedly been displayed at the level of trial production.

It is however proposed to adopt in future a technique for 256 tones by address/display separate type drive method (ADS subfield method).

In such an AC device method, the more the number of tones, the more the number of bits of the address duration increase as the preparation time for lighting up and making the panel luminescent within one frame of duration. The sustaining duration as light emitting duration becomes thus relatively short reducing the maximum luminance.

Because the luminance and tone of the light emitted from the panel face depend upon the number of bits of the signal to be processed, increased number of the bits of the signal improves the picture quality, but decreases the emission luminance.

If, conversely, the number of bits of the signal to be processed is decreased, the emission luminance increases, but it decreases the tone to be displayed thereby causing the degradation of the picture quality.

The applicant proposes therefore such an error variance circuit 28 of false half tone display device as shown in FIGURE 1 which can minimize the color depth difference between the input signal and emission luminance rendering the number of bits of the output drive signal smaller than that of the input signal, and at the same time prevent any false patterns even when the image signal of same level inputs continuously.

In FIGURE 1, the numeral 30 represents the image signal

input terminal of the original picture element A(i,j) of n bits, which is connected to the vertical adder 31 and horizontal adder 32, reduces the number of bits at the bit conversion circuit 33 and then connected to the image output terminal 34.

Connected to the output side of the horizontal adder 32 is the error detect circuit 35. The error detect circuit 35 is made of the ROM 38 that sets and stores the data of corrected luminance level for correction of luminance and tone, the adder 39 that operates the sum of the corrected luminance level as set in the ROM 38, and the variance output signal as output from the horizontal adder 32 to output the error detect signal and the weighting circuits 40 and 41 that weight the error detect signal output from the adder 39 and output it as error weighted signal.

Connected to the outside of the weighting circuits 40 and 41 of said error detect circuit 35 are the vertical adder 31 and horizontal adder 32 through the intermediary of h-line delay circuit 36 and d-dot delay circuit 37 respectively.

Said h-line delay circuit 36 "h-line" delays the error weighted output signal as output from said weighting circuit 40 and outputs, as shown in FIGURE 3, reproduced error of the picture element (pixel), by h-line prior to the original pixel A(i,j), for instance, the reproduced error E(i,j-1), one line prior, if h=1. Said d-dot delay circuit 37 "d-dot" delays the error weighted output signal as output from said weighting circuit 41 and outputs the reproduced error at the

pixel, by d dots before the original pixel A(i,j), for instance, the reproduced error E(i-1,j) generated by 1 dot prior if d=1.

In FIGURE 1, the errors of h-line delay circuit 36 and d-dot delay circuit 37 are incorporated and diffused into variance output signal by the vertical adder 31 and horizontal adder 32. The variance output signal is then sent to the bit conversion circuit 33, where the quantized variance output signal is converted into m ($\leqq$n-1) bits to be output as drive signal from the image output terminal 34 into PDP.

This prior art was problematical in that if the errors are continuously transferred, the errors from the preceding frames are taken over and an influence is exerted from non-image duration, causing thus the flickering of the picture.

BRIEF SUMMARY OF THE INVENTION

The purpose of this invention is to annihilate the flickering of the picture eliminating any excessive error transfer from the preceding frames and non-image duration.

In order to achieve the objective, this invention comprises a reproduced error adder, a bit conversion circuit 33, an error detect circuits 36 and 37. Said error detect circuit 35 is provided with a clear circuit 42. This configuration allows to obtain smooth responses without reducing the emission luminance despite the fact that the number of bits of the output signal is lower than that of the

original image input signal, forcibly reduces to zero the previous error for every frame unit. The error is thus not transferred to the subsequent frames, thereby eradicating the flickering of the picture.

Since moreover the frame synchronization signal is sent during the non-image duration, the error can be cleared without exerting any influence on the image.

Other and further objects of this invention will become obvious upon understanding of the illustrative embodiments about to be described.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a block diagram of such an error variance circuit of false half tone display device as has been already proposed by the applicant.

FIGURE 2 is another block diagram representing an embodiment of the error variance circuit by this invention.

FIGURE 3 is an explicative drawing that depicts the error variance processing among respective picture elements.

DETAILED DESCRIPTION

Referring now in particular to FIGURE 2, there is illustrated an embodiment of the error variance circuit by this invention, in which like reference characters denote like parts in FIGURE 1.

This invention features the characteristics that inserted on the outside of the adder 39 of the error detect

circuit 35 is the clear circuit 42 to which a clear signal input terminal 43 is connected.

More specifically, the numeral 30 represents the image signal input terminal of original n-bit picture element A(i,j) , which is connected to the vertical adder 31 and horizontal adder 32. After it reduces the number of bits at the bit conversion circuit 33, it is connected to the image output terminal 34. Said vertical adder 31 and horizontal adder 32 build up a reproduced error adder.

Connected to the output side of said horizontal adder 32 is the error detect circuit 35. The error detect circuit 35 is made of the ROM 38 that sets and stores the data of corrected luminance level for correction of luminance and tone, the adder 39 that operates the sum of the corrected luminance level as set in the ROM 38 and the variance output signal as output from the horizontal adder 32 to output the error detect signal, the clear circuit 42 that inserted at output side of said adder 39, and the weighting circuits 40 and 41 that connected to said clear circuit 42 and weight the error detect signal output from the adder 39 and output it as error weighted signal.

Connected to the clear circuit 42 is the clear signal input terminal 43 that inputted the synchronization signal in order to clear the error value by frame unit.

Connected to the outside of the weighting circuits 40 and 41 of said error detect circuit 35 are the vertical adder 31 and horizontal adder 32 through the intermediary of h-line

delay circuit 36 and d-dot delay circuit 37 respectively.

Said h-line delay circuit 36 "h-line" delays the error weighted output signal as output from said weighting circuit 40 and outputs, as shown i FIGURE 3, reproduced error of the picture element (pixel), by h-line prior to the original pixel A(i,j), for instance, the reproduced error E(i,j-1), one line prior, if h=1. Said d-dot delay circuit 37 "d-dot" delays the error weighted output signal as output from said weighting circuit 41 and outputs the reproduced error at the pixel, by d dots prior to the original pixel A(i,j), for instance, the reproduced error E(i-1,j) generated by 1 dot prior if d=1.

Referring now to the embodiment illustrated in FIGURE 2, we will describe the action of this embodiment.

In this embodiment a density is modulated by two luminances and tones to produce a visually false tone within a small area spreading to a certain extent to obtain multiple tone.

Assuming,

A(i,j): input pixel value of the object now under processing,

A(i,j-1): input pixel value, by one line prior (when h=1),

A(i-1,j): input pixel value, by one line prior (when d=1),

δv: error weighted value of the variance output pixel from by 1 line prior

δh: error weighted value of the variance output pixel from by 1 dot,

the adder 39 sums up the variance output signal as input into the error detect circuit 35 and the date from ROM38 to give the error output signal.

The weighting circuits 40 and 41 weight this error output signal into error weighted output signals δv and δh that weighted by Kv(<1) and Kh(=1-Kv) respectively, which will then be input into 1-line delay circuit 36 (h=1) and 1-dot delay circuit 37 (d=1) and incorporated into the original pixel A(i, j) by horizontal adder 32 to be

$$C(i, j)=A(i, j)+\delta v+\delta h$$

where, C(i, j): variance output pixel value of the object now under processing.

$$\delta v=Kv\times[f\{C(i, j-1)\}-Br]$$

$$\delta h=Kh\times[f\{C(i-1, j)\}-Br]$$

f{C(i, j)}: corrected luminance for C(i, j)

Br: emission luminance level.

When the frame synchronization signal is sent for every frame from the clear signal input terminal 43 to the clear circuit 42, the error output signal from the adder 39 is cleared by the clear circuit 42. That is, the prior error is forcibly reduced to zero for every frame. Therefore, it is not transferred to the subsequent frames any more. Since the frame synchronization signal is sent while the non-image duration, the error value can be cleared without having any influence on the image. The frame synchronization signal can be sent to the clear circuit 42 for every two or more frames with more or less effect.

Thus, the error from preceding frames and any excessive error from the non-image duration can be eliminated. the new errors are incorporated and varied for every frame into the variance output signal, which is then forwarded to the bit conversion circuit 33, where the variance output signal as quantized by n bits is converted into m ($\leqq$n-1) bits to be output from the image output terminal 34. The signal fewer in bit number than the original image input signal thus gives smoother response without reducing the emission luminance.

Though in the foregoing embodiment the reproduced error adder has been made up of the vertical adder 31 and horizontal adder 32, this example is intended to illustrate the invention and is not to be construed to limit the scope of this invention. For example we can add such a circuit that will add the error in diagonal direction. The adder may further be built up with the combination with one or more of the vertical adder 31, horizontal adder 32 and diagonal adder.

Although the foregoing embodiment illustrates a case where the display panel is PDP, this invention is not limited thereto; it can make use of any such display panels as liquid crystal display.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. An error variance circuit comprising:

a reproduced error adder that adds a reproduced error generated prior to the original pixel, to an output image signal including n-bit original pixels,

a bit conversion circuit that converts a variance output signal output from said reproduced error adder into a signal of m ≤(n-l) bits and outputs it to a display panel,

an error detect circuit that detects a difference between (a) a previously set corrected luminance level for correcting a luminance and a tone of an image produced on the display panel, and (b) the variance output signal, as output from said reproduced error adder and outputs this difference through a weighting circuit, and

a delay circuit that delays, for a predetermined number of pixels, the error weighted output signal from the weighting circuit and outputs it to said reproduced error adder as a reproduced error, said error detect circuit including a clear circuit that clears the error every frame.

2. The error variance circuit as claimed in claim 1 wherein the clear circuit clears the errors of preceding frames and those in a non-image duration in response to a frame synchronization signal from a clear signal input terminal.

3. The error variance circuit as claimed in any one of claims 1 or 2 wherein the reproduced error adder comprises at least one or more of a vertical adder, a horizontal adder, and a diagonal adder.

4. The error variance circuit as claimed in any one of claims 1 or 2 in which the display panel is one of a PDP and a liquid crystal display panel.

5. An error variance circuit having an error diffusion arrangement comprising:

a first adder for receiving n-bit original pixels;

a second adder, said second adder being serially connected between said first adder and a bit conversion circuit said conversion circuit for converting a variance output signal into a m-bit output (m≤n-1);

a first delay circuit connected with said first adder;

a second delay circuit connected with said second adder; and

an error detection circuit including:

means for detecting a difference between a previously corrected luminance level and said variance output signal and to output an error detect signal;

a clear circuit connected with an output of said second adder;

a first weighting circuit connected between said first delay circuit and said clear circuit for weighting an output of the clear circuit; and

a second weighting circuit connected between said second delay circuit and said clear circuit for weighting the output of the clear circuit,

wherein said clear circuit for receiving said error detect signal and clearing errors diffused into said variance output signal on a frame-by-frame basis.

6. The error variance circuit as claimed in claim 5, wherein said error detection circuit further comprises:

a ROM which is responsive to the output of said second adder; and

a third adder which adds the output of the second adder to an output from said ROM and supplies an output to said clear circuit.

7. The error variance circuit as claimed in claim 5, wherein said clear circuit has a clear circuit input terminal which receives a frame synchronization signal.

8. The error variance circuit as claimed in claim 5, wherein said first delay circuit is a horizontal line delay circuit.

9. The error variance circuit as claimed in claim 5, wherein said second delay circuit is a d-dot delay circuit.

Fig. 1 (prior art)

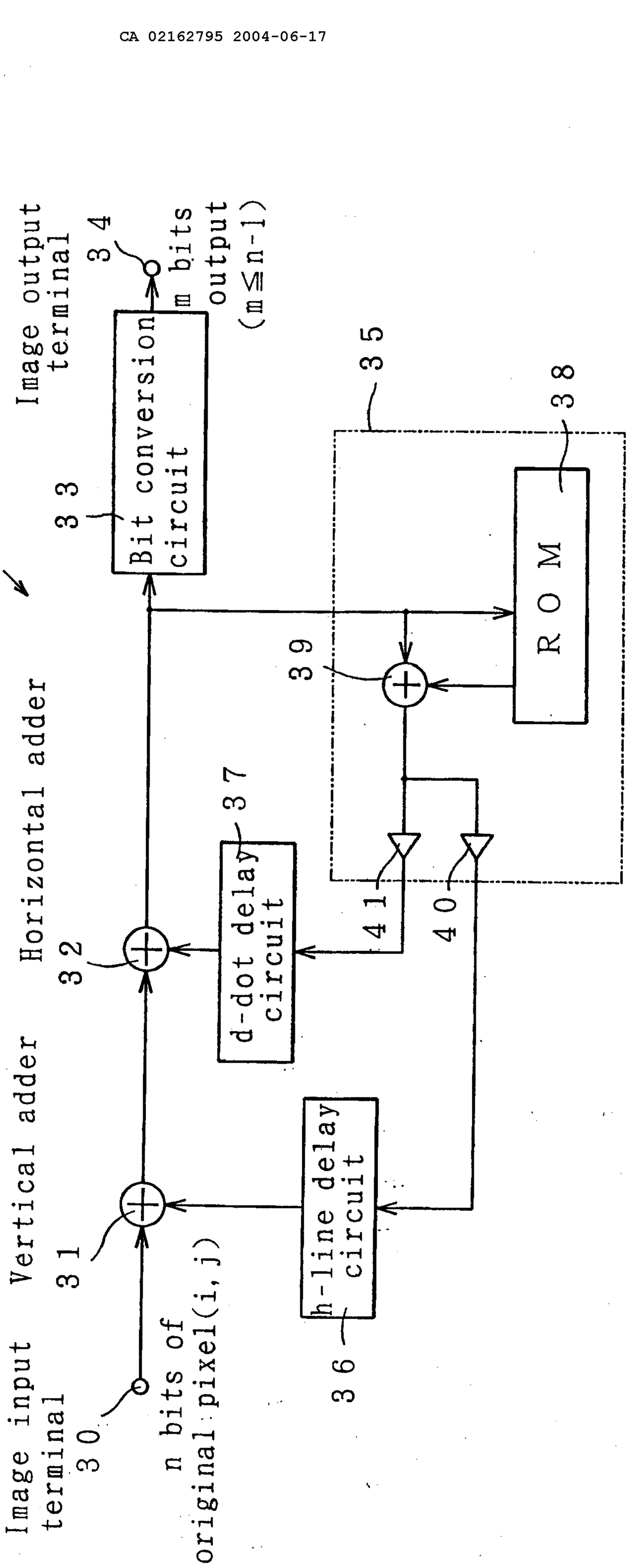


Fig. 2

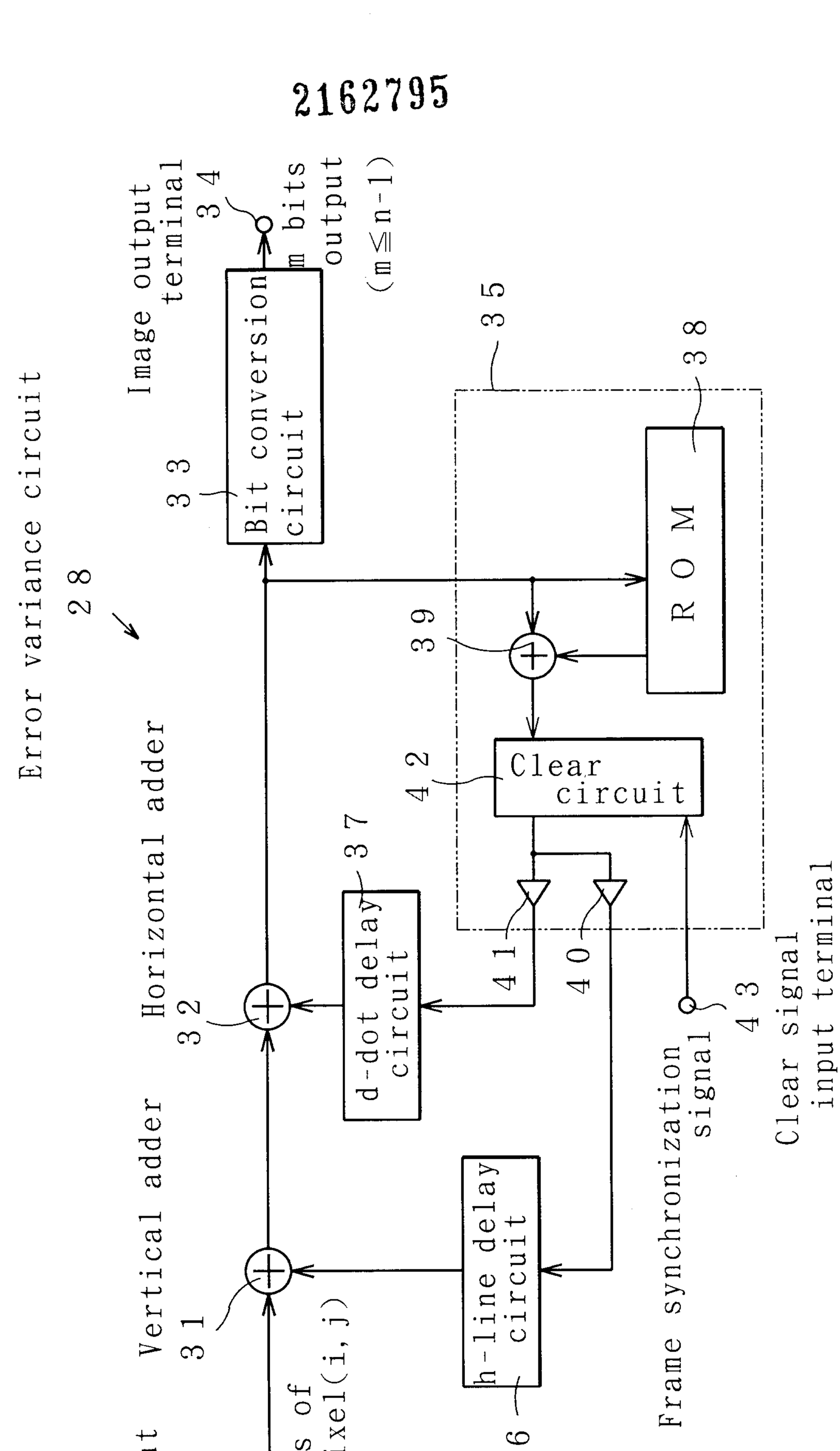


Image input terminal
30
n bits original pixel data of pixel(i, j)
Vertical adder
31
Horizontal adder
32
Bit conversion circuit
33
m bits output
(m≦n-1)
Image output terminal
34
h-line delay circuit
36
d-dot delay circuit
37
Error variance circuit
28
35
38
ROM
39
Clear circuit
42
41
40
Frame synchronization signal
43
Clear signal input terminal

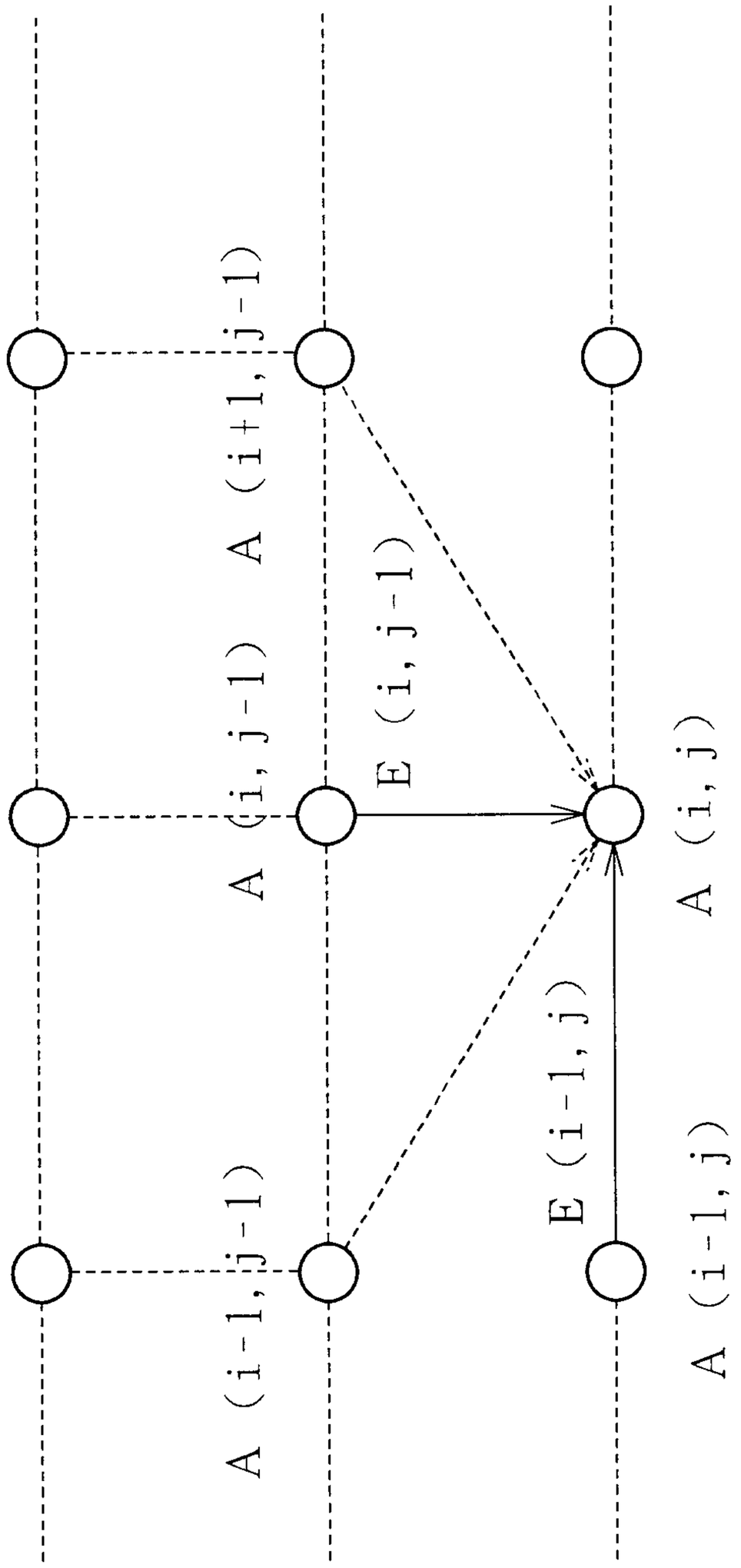
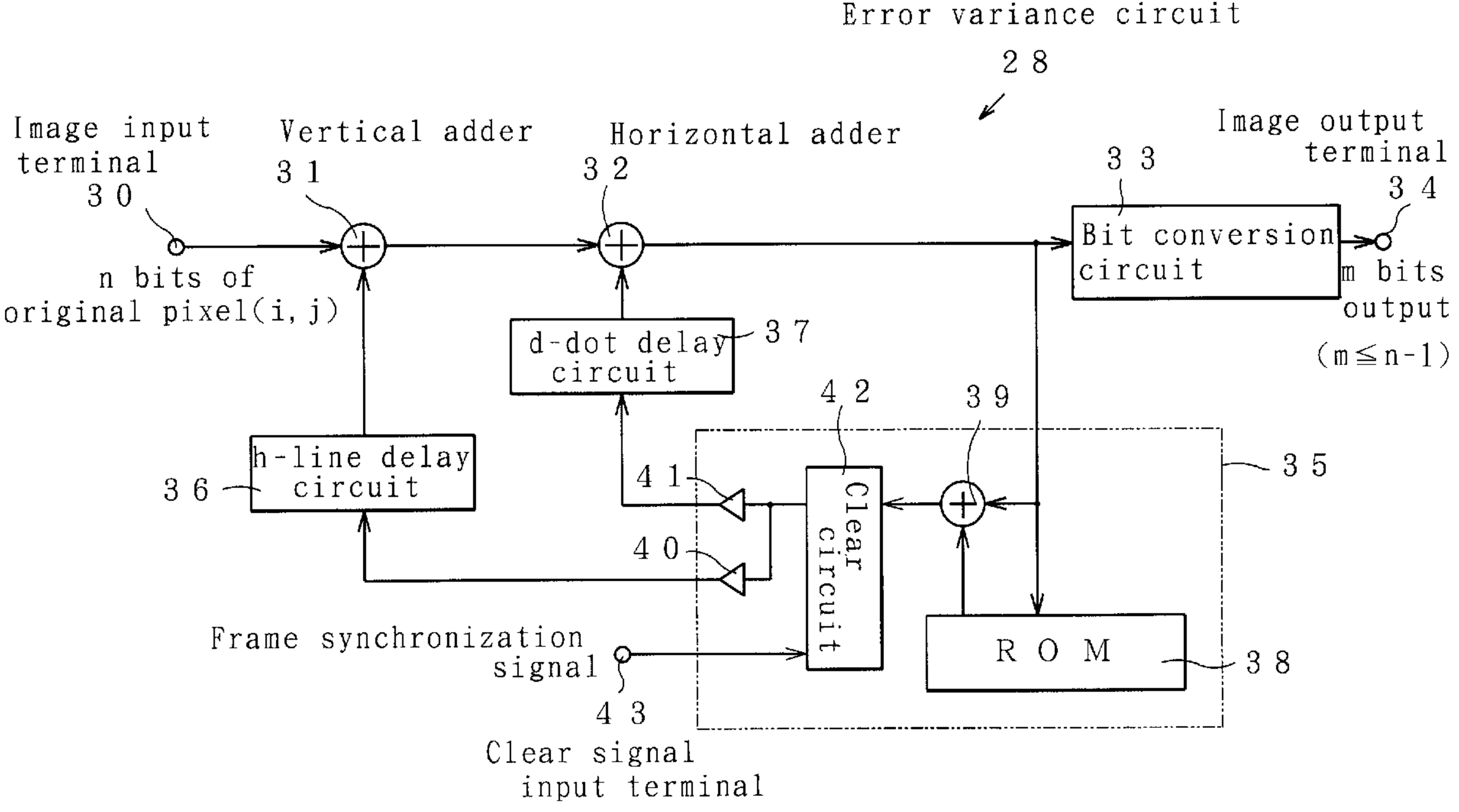


Fig. 3


Error variance circuit
28
Image input terminal
30
Vertical adder
31
Horizontal adder
32
33
Image output terminal
34
n bits of original pixel(i, j)
Bit conversion circuit
m bits output
(m≦n-1)
d-dot delay circuit
37
42
39
h-line delay circuit
36
41
40
35
Clear circuit
ROM
38
Frame synchronization signal
43
Clear signal input terminal