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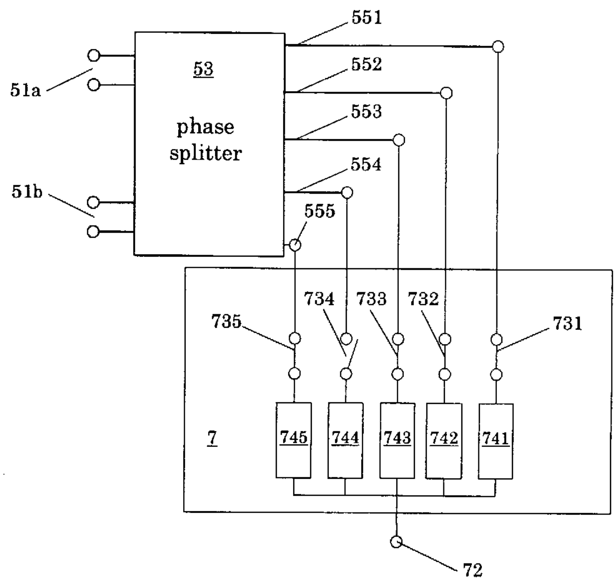
[Continued on next page]

(54) Title: A SIGNAL GENERATOR DEVICE, METHOD FOR GENERATING A SIGNAL AND DEVICES INCLUDING SUCH A SIGNAL GENERATOR DEVICE



(57) Abstract: A signal generator device which includes a generator input (51a, 51b) for receiving input signals; a frequency multiplication section (7) including: at least two frequency multiplication inputs (551-555) communicatively connected to the generator input (51a, 51b), for receiving each at least one phase shifted signal having a phase difference with respect to the other phase shifted signal; pulse generator sections (741-745) connected to at least one of said frequency multiplication inputs for generating an output signal if said phase shifted signals has a transition from a first state to a second state. The signal generator device further includes at least one generator output (72) connected to at least one of said at least one pulse generator sections for transmitting said output signal.

WO 03/005585 A1

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Title: A signal generator device, method for generating a signal and devices including such a signal generator device

The invention relates to a signal generator device and a method for generating signal of a harmonic frequency. The invention further relates to electronic devices, e.g. a receiver device, a transmitter device, a transceiver device including a signal generator device according to the invention.

From the United States patent 5 990 712 a harmonic generator is known. This publication describes a harmonic generator which converts an input signal at a fundamental frequency into an output signal at a harmonic frequency. A non-linear device converts the input signal into an intermediate signal in which the harmonic frequency has a maximized amplitude determined by a conduction angle. A harmonic filter produces a filtered signal proportional to the amplitude of the harmonic frequency within the intermediate signal. A detector produces a control signal proportional to the amplitude of the filtered signal. A control circuit produces a variable bias signal for the non-linear device, the bias signal being proportional to the amplitude of the control signal and determining the conduction angle. An output filter converts the intermediate signal into an output signal at the harmonic frequency.

However, the known signal generator is complex of design because of the large number of components. Furthermore, the harmonic filter, the detector and the control circuit form a feedback loop, which makes the signal generator even more complex. The invention seeks to overcome this disadvantage. It is therefore a goal of the invention to provide a less complex signal generator device.

The invention seeks to achieve said goal by providing a signal generator device, at least including a generator input for receiving at least one input signal having an input frequency; a frequency multiplication section at least including: at least two frequency multiplication inputs, each communicatively connected to the generator input for receiving each at least one phase shifted signal having a phase difference with respect to the other phase shifted signal; at least one pulse generator section connected to at least one of said frequency multiplication inputs for generating an output signal if said phase shifted signals has a transition from a first state to a second state, said signal generator device further including at least one generator output connected to at least one of said at least one pulse generator sections for transmitting said output signal.

Such a signal generator device is simple of design, because of the small number of simple components used in the device. Furthermore, the design of device may easily be adapted, for example by connecting of disconnecting pulse generator sections. Also, a signal generator according to the invention is especially suited for implementation in an integrated circuit, because the device may be implemented using components used in logical circuits, such as AND-ports and transistors

Furthermore, the invention provides a method for generating a signal of a predetermined frequency at least including receiving at least two input signals having a phase difference with respect to each other; generating an output signal if one of said input signals has a transition from a first state to a second state.

Such a method is simple and may be performed with a device for generating a frequency according to the invention.

Particular embodiments of the invention are set out in the dependent claims

Further details, aspects and embodiments of the invention will be described with reference to the figures in the attached drawing.

Fig. 1 shows a block diagram of an example of an embodiment of a signal generator device according to the invention.

Fig. 2 shows a flow-chart of an example of an embodiment of a method according to the invention.

Fig. 3 shows the development in time of phase splitter output signals and signals in successive steps of a signal generation method according to the invention.

Fig. 4 shows a block diagram of a first example of an embodiment of a phase splitter section for a signal generator device of the present invention.

Fig. 5 shows a circuit diagram of a second example of an embodiment of a phase splitter section for a signal generator device of the present invention.

Fig. 6 shows a circuit diagram of a third example of an embodiment of a phase splitter section for a signal generator device of the present invention.

Fig. 7 shows a block diagram of an example of an embodiment of a phase shifter section for a signal generator device of the present invention.

Fig. 8 shows a block diagram of an example of an embodiment of a signal generator device according to the invention in which a phase shifter section as shown in fig. 7 is implemented.

Fig. 9 shows a flow chart of a second example of a frequency multiplication method according to the invention.

Fig. 10 shows the development in time of phase splitter output signals and a generator output signal in a signal generation method according to the invention, as may be performed by the device of fig. 8.

Fig. 11 shows a block diagram of an example of a pulse generator device for a signal generator device as shown in figs. 1 and 8.

Fig. 12 shows a block diagram of an example of an embodiment of a signal generator device according to the invention combined with a frequency generator device.

A block diagram of a signal generator device according to the invention, is shown in fig. 1. The shown signal generator device has a phase shifter or phase splitter section 53 and a frequency multiplication section 7. The phase splitter section 53 has two generator inputs 51a,51b and a plurality of shifter outputs 551-555. The frequency multiplication section 7 has a plurality of frequency multiplication inputs communicatively connected to the shifter outputs and depicted in fig. 1 as coinciding with the shifter outputs 551-555.

The frequency multiplication device 7 further includes a plurality of switches 731-735 each connected to one of the frequency multiplication inputs 551-555 and connected to a pulse generator device 741-745. The pulse generator devices 741-745 are further connected to a generator output 72.

Input signals having a phase difference with respect to each other may be received at the generator inputs 51a,51b. At the shifter outputs 551-555 shifter output signals derived from the input signals may be presented. In fig. 1, a first balanced input signal is applied to the phase splitter section 53 at one of the generator inputs 51a-51b and at the other input a second balanced input signal is applied to the phase splitter section 53. The second balanced signal differs in phase with respect to the first balanced input signal. In the shown example, it is assumed that the second balanced signal is 90 degrees shifted in phase with respect to the first balanced input signal. Both signals are usually already available in many types of devices, like for instance complex transceivers with image rejection.

Based on the signals presented at the generator inputs 51a,51b the phase splitter section 53 generates phase shifted output signals and transmits the phase splitted output signals via phase splitter output connections 551-555 to the frequency multiplication section 7. In the example shown in fig. 1, the phase of the signals at each of the shifter output connections 551-555 differs with respect to the signal at all the other shifter output connections. The respective phase differences are listed in table 1, wherein the phase at output 551 is assumed to be 0 degrees.

Table 1

output	phase (degrees)
551	0

552	45
553	90
554	135
555	180

The shifter output signals are used for generating signals of harmonic or other frequencies based on the frequency of the input signal. The frequency multiplication section 7 of fig. 1 may perform a method as represented by the flow-chart in fig. 2. First, in selecting step I, the desired frequency multiplication inputs are selected, which in the example of fig. 1 are inputs 731-733 and 735. In the next step II, an upgoing transition is detected at one of the inputs and in step III a pulse is generated. Thereafter, steps II and III are repeated as long as desired.

The development in time of the shifter output signals is shown in fig. 3 for each of the shifter outputs 551-555. In fig. 3 the development in time of signals at the output of pulse generators 741-745 and the frequency multiplication output 72 is also depicted. Thus, fig. 3 signals in successive stages of a signal generation according to the invention are shown. If one of the phase shifted output signals at the shifter outputs has an upgoing transition, the pulse generator connected to the specific output generates a small pulse. For example, at the moment indicated with dotted line A the signal at shifter output 551 has an upgoing transition and the pulse generator 741 connected to this shifter output generates a pulse. Likewise, at the moment indicated with dotted line B the signal at shifter output 555 has an upgoing transition and the pulse generator 745 generates a pulse. The outputs of the pulse generators are added to each other. This addition results in a generated signal at the signal generator output 72. In fig. 1, the pulses are combined in a relatively simple manner by connecting the outputs of the pulse generators to each other, however other ways of combining the pulses may likewise be applied. For example,.by adding currents, using (N)AND-, or (N)OR-gates

In the device of fig. 1, the switches 731-735 communicatively connect the pulse generator devices 741-745 and the shifter outputs 551-555 in a conducting state of the switches. In a non-conducting state of the switch devices 731-735 the pulse generator devices are not communicatively connected to the shifter outputs.

In fig. 1, the switch 734 is in the non-conducting state and the switches 731-733,735 are in the conducting state. By combining the appropriate shifter outputs with the switches, the required frequency will be available at the output 72 of the generator 7. In general, every higher order frequency or combination of higher order frequencies of the frequency of the phase splitter input signal may be generated. For example, if all switches 731-735 are closed, the 4^{th} harmonic of the signal will be generated and if only switches 731,733 and 735 are closed, the second harmonic will be generated.

If, in use, only a single frequency has to be generated, the pulse generator device may be connected directly to the frequency multiplication inputs, instead of via the switch devices. Thereby, the signal generator will be even less complex, however the frequency of the output signal is not adjustable anymore.

A signal generator device according to the invention is of a simple design and may be adapted easily to different requirements by connecting or disconnecting one or more of the pulse generator devices to or from one or more of the shifter outputs, for example by switching one or more of the switches to either the conducting or the non-conducting state. Furthermore,.digital control of the signal generator device is possible such that digital programming is very easy.

In the example of fig. 1 a phase splitter device as shown in fig. 4 may be used. The inputs 51a,51b of the phase splitter section 53 of fig. 4 are connected to a phase calibration section 55. The phase calibration section 55 ensures the required phase difference between the input signals of the section 53, i.e. in the example given 90 degrees. The phase calibration section 55 includes a phase detector circuit 550 which detects the phase difference of its input signals. The phase detector circuit 550 controls a phase shifter circuit 559 which shifts the phase of the signal to the required phase difference. If the phases of the respective signals are known to be sufficiently accurate, the phase calibration section may be omitted in the signal generator device.

The phase splitter section 53 may be implemented as shown in fig.5. The phase splitter section of fig. 5 is a phase splitter section 53 which generates a signal with a phase of 45 degrees at an output out_45. At an input in_0 an input signal is provided. The same input signal shifted 90 degrees in phase is provided at an input in_90. As explained, a +90 or -90 degrees phase shifted signal is usually available in image reject devices and other devices. The inputs in_0, in_90 are connected via resistors R1 and R2. At the node between the resistors R1, R2, the output out_45 is connected. The signal s_45 at output out_45 has a phase shifted over 45 degrees with respect to the signal at input in_0, because:

$$\begin{aligned} s\_45 &= \sin(wt) + \sin(wt + 90°) \\ &= 2\sin(\frac{wt - wt - 90°}{2})\sin(\frac{wt + wt + 90°}{2}) \\ &= 2\sin(45°)\sin(wt + 45°) \\ &= \sqrt{2}\sin(wt + 45°) \end{aligned}$$

The type of phase-splitter shown in fig. 5 may be extended with more resistors and output contacts. For example in fig. 6, a phase splitter is shown wherein signals with a 10 degree phase resolution between 0 and 90 degrees are available at outputs out_0-out_90. The outputs out_0-out_90 are connected with resistors R1-R9. The resistance of the resistors R1 and R2 and R1-R9 resp. in figs. 3 and 4 may be selected such that the contribution of the two input signals is equal. For the splitter shown in fig. 6 this criterion results in the values listed in table 2.

Table 2

resistor	resistance (kOhm)
R1	1.5
R2	1.17
R3	0.99
R4	0.90
R5	0.874
R6	0.90
R7	0.99
R8	1.17
R9	1.5

Apart from purely resistive splitters as shown in fig. 5 and 6, capacitive splitters, inductive splitters or a combination of such splitters may be used. Furthermore, the phase-splitter section may be implemented as a ring oscillator section. In general a ring oscillator includes a circular chain consisting of an odd number of inverters.

In the example of the generator device of fig. 1, each phase shifted signal has its own frequency multiplication input. In fig. 8, an example of a signal generator device is shown with only two frequency multiplication inputs 551-552, which are depicted as the same as the phase shifter ouputs. The frequency multiplication section 7 includes a switch section 73 which switches between two shifter outputs 551 and 552. The switch 73 is connected to a pulse detector 74. Connected to the pulse detector 74 are two phase shift adjusters 751 and 752 for adjusting the phase shift of the signals presented at the phase shifter outputs 551-552.

In the embodiment in fig. 8 not all the different phase-shifted signals are available to the frequency multiplication section 7 at the same time. The signal generation is performed using a phase shifter 53 with an adjustable phase shift and using each of the shifter outputs 551-552 for a multiple of signals with different phase shifts.

In the example of fig. 8, the frequency multiplication section 7 sets the phase shift of the shifter section 53 to a predetermined value with phase shift adjuster sections 751 and 752, as is described below. The switch section 73 in the frequency multiplication section 7 selects one of the frequency multiplication inputs 551-552 and the pulse generator 74 generates a pulse if the signal from the selected input has an upgoing transition. In fig. 8, a first frequency multiplication input 551 is selected. After the signal from the input 551 has had an upgoing transition, a second shifter output 552 is selected by switching the switch 73. The second shifter output 552 is set to a different phase shift and the operation is performed again with the second shifter output. Hereby, for each repetition of the signal generation method the phase shift is different but not all the shifted signals need to be available at the same time and the number of shifter outputs is reduced.

In the signal generator device shown in fig. 8, the frequency multiplication section 7 may perform an operation according to the flow-chart shown in fig. 9. Of the shifter outputs 551-552 only one at the time is actually used as input to the frequency multiplication section 7. The development in time of the signals at the phase shifter outputs 551, 552 and the generator output 72 is shown in fig. 10. At the start in step I the phase shift of the signal of a selected one of the shifter outputs 551-552 is set to a phase shift phi by one of phase shift adjusters 751,752.

If the signal from the selected shifter input has an upward transition, as is indicated with arrow dotted line A in fig. 9, the criterion of step II is satisfied and a pulse is generated by the generator device 74 in step III. In step IV the next frequency multiplication input is selected and the phase shift of the signal presented at the first shifter output 551 is adjusted to a new value and the whole process is repeated.

In the example of an embodiment of a signal generator device as shown in fig. 8, the phase shifter section 53 differs from the phase splitter devices shown in figs. 5 and 6. The phase shifter 53 of fig. 8 includes two filter sections 531 and 532 each connected to one of the phase shifter outputs 551,552. An example of suitable filter sections 531 (or 532) is schematically shown in fig. 7. The filter 531 in fig. 7 is an all-pass filter section. The amplitude of the filter output signal is flat in the frequency domain. The filter section includes two balanced substantially similar filters. A first filter is formed by a resistor R10 and a capacitor C1 and a second filter is formed by resistance R11 and capacitor C2. The phase shift *phi* of the output signal of each of the filters with respect to the input signal depends directly on the time-constant of the filter. The time constant is equal to the product of the resistance and capacitance. The phase shift *phi* is substantially equal to:

$$phi = 2\arctan(wRC),$$

wherein w is the frequency of the signal; R is the resistance of the resistor and C is the capacitance of the capacitor. The time constant of the filter sections 531-532 is adjustable if the resistance and/or the capacity of one or more of the resistors and/or capacitors is adjustable. Thus the phase adjuster sections 751 and 752 set the resistances and/or capacitances in the filter section connected to the selected one of the shifter outputs 551-552 to a predetermined value to obtain the desired time constant and corresponding phase shift. The adjustable resistors R10,R11 may for example be implemented as field effect transitors connected with source or drain to the capacitors The resistance from source to drain may then be controlled by the voltage applied at the gate of the transistor. The capacitor may for example be implemented with a varactor diode, a Gate-Source capacitance in a MOS device, or by switching-in extra capacitors.

If an adjustable phase shifter section is used, the shifter section may also have only one shifter output and the phase shift of the this single output may after each repetition of the division operation be set to a new phase shift.

The phase shift may also be adjusted continuously, such that an infinite frequency resolution is realised. Continuously adjustable phases may be realised by e.g. continuously adjusting the resistance in the filter sections (e.g. using Metal Oxide Semiconductor Field Effect Transistors (MOS FETs) operating in the triode region) and/or by using varactors as capacitance and/or using adjustable inductances. The shown filter is an all-pass filter, it is likewise possible to use one or more low-pass filters, one or more high-pass filters or one or more poly-phase filters or a combination thereof.

In the shown examples the phase shifter is in the proximity of the frequency multiplication section. As an alternative, the phase shifter section may be at a different physical location. In devices wherein a number of phase shifted signals is already available, the phase shifter section may logically be implemented in several sections of the entire device and thus not be physically present. For example in balanced image reject receiver front-ends, transmitters and transceivers, signals with 180 degrees and +90 and -90 degrees phase difference are already available and therefore a separate shifter section may not be necessary. Furthermore, the phase-splitter section may be implemented as a ring oscillator section. In general a ring oscillator includes a circular chain consisting of an odd number of inverters.

The pulse generator may be implemented with combinatorial logic, such as AND,NAND,OR or NOR devices. Fig. 11 shows an embodiment of a pulse generator 74, which may be used in the frequency multiplication sections shown in the figs. In the device 74 shown in fig. 11, the input signal is supplied to an NAND-circuit 742 and to an inverter 741. The inverter 741 inverts and delays the input signal. The NAND-circuit output signal is then a small pulse. By optimising the delay in the inverter 741, or by using multiple inverters, the duty-cycle of the output signal can be made equal to 50%.

It should be noted that in all of the above mentioned implementations it is possible to add a (relatively slowly varying) signal to the phase-shifted signals such that the output signal contains phase and/or frequency modulation. In the examples presented above, the basis used for the phase-splitter is 90 degrees. Other bases can be used as well: e.g. 0 degrees and 135 degrees can also be used.

Furthermore, the 0 and 90 degrees phase-shifter signals may be used as a radio frequency (rf) input in an image reject mixer. In such a mixer the rf input may be combined with Local Oscillator signals. The mixer may be implemented in receiver, transmitter or transceiver devices.

Furthermore, a signal generator device according to the invention may be connected to other signal generator devices for example to provide means to compensate for the spurious frequencies generated by the fractional generator. Also, the frequency of the generated signal may be (continuously) adjusted in order to obtain a frequency or phase modulation, for example by continuously switching the switch devices in fig. 1 from the conducting state to the non-conducting state or vice versa.

A signal generator device according to the invention may also comprise a frequency divider device. An example of such a signal generator device is shown in fig. 12. Besides a phase shifter device 53 and a frequency multiplication device 7, the shown signal generator device has a count and select section 54, as is known from the applicants co-pending international patent application PCT/NL01/00514, to which reference is made

Claims

1. A signal generator device, at least including:
a generator input (51a,51b) for receiving at least one input signal having an input frequency;
a frequency multiplication section (7) at least including:
at least two frequency multiplication inputs (551-555), each communicatively connected to the generator input (51a,51b), for receiving each at least one phase shifted signal having a phase difference with respect to the other phase shifted signal; and
at least one pulse generator section (741-745) each connected to at least one of said frequency multiplication inputs for generating an output signal if said phase shifted signal has a transition from a first state to a second state,
said signal generator device further including at least one generator output (72) connected to at least one of said at least one pulse generator sections for transmitting said output signal.

2. A signal generator device as claimed in claim 1, further including:
at least one switch device (731-735) each having:
at least one switch input connected to at least one of said frequency multiplication inputs (551-555), said switch device further having at least one switch output;
said switch device (731-735) in a conducting state having its input electrically connected to it outputs and electrically disconnected from its output in a non-conducting state of said switch device (731-735),

3. A signal generator device as claimed claim 1 or 2, further including:

a phase shifter section (53) for generating at least one phase shifted signal having a phase difference with respect to said input signal, said phase shifter section (53) at least including:

at least one shifter input communicatively connected to said generator input (51a,51b) and

at least one shifter output for outputting at least one of said phase shifted signals, said shifter output being communicatively connected to said frequency multiplication section (7).

4. A signal generator device as claimed in any one of the preceding claims, wherein

said phase shifter section (53) has first input (51a) for receiving a first input signal and a second input for receiving a second input signal (51b) having a phase difference with respect to said first input signal and

wherein said shifter output has at least one intermediate phase output for outputting at least one phase shifted signal with a phase between said first input signal and said second input signal.

5. A signal generator device as claimed in claim 4, wherein said phase shifter section is a phase splitter section (53) at least including:

a chain of splitter components (R1-R9), said chain having a first end connected to said first input and a second end connected to said second input, said chain including at least two splitter components (R1-R9) being connected to each other at a splitter output (out_0,out_90).

6. A signal generator device as claimed in any one of the preceding claims, wherein said phase shifter section (53) includes at least one filter section (531,532) having an adjustable time constant and said frequency multiplication section includes at least one phase shift adjuster device

(751,752) for adjusting said adjustable time constant after a predetermined number of periods of said phase shifted signal.

7. A signal generator device as claimed in claim 6, wherein said filter section (531,532) includes a low-pass filter.

8. A signal generator device as claimed in claims 6 or 7, wherein said filter section (531,532) includes a high-pass filter.

9. A signal generator device as claimed in any one of claims 6-8, wherein said filter section (531,532) includes an all-pass filter.

10. A signal generator device as claimed in any one of claims 6-9, wherein said filter section (531,532) includes a poly-phase filter.

11. A signal generator device as claimed in any one of claims 6-10, wherein said filter section (531,532) includes at least one variable resistor (R10,R11)

12. A signal generator device as claimed in any one of claims 6-11, wherein said filter section (531,532) includes at least one variable capacitor (C1,C2).

13. A signal generator device as claimed in any one of claim 6-12, wherein said filter section (531,532) includes at least one variable inductor.

14. A signal generator device as claimed in any one of the preceding claims, further including a frequency divider section communicatively connected to at least one of said generator inputs.

15. A signal generator device as claimed in claim, wherein the phase splitter section is a ring-oscillator section.

16. A signal generator device as claimed in any one of the preceding claims, further including at least one phase calibration section (55) for calibrating said at least one phase shifted signal to minimise spurious frequency components in said output signal.

17. An electronic device at least including a signal generator device as claimed in any one of claims 1-16.

18. An electronic device as claimed in claim 17, wherein said electronic device is selected from a group including a receiver device, a transmitter device, a transceiver device.

19. A method for generating a signal of a predetermined frequency, at least including

receiving at least two input signals having a phase difference with respect to each other;

generating an output signal if one of said input signals has a transition from a first state to a second state.

20. A method as claimed in claim 19, wherein said receiving at least two signals having a phase difference includes:

receiving at least one input signal;

generating from said input signal at least one phase shifted signal having a phase difference with respect to said input signal.

21. A method as claimed in claim 20, wherein said step of receiving said at least one input signal includes:

receiving a first input signal;
receiving a second input signal having a phase difference with respect to said first input signal; and said generating at least one phase shifted signal includes:
generating at least one intermediate phase signal having a phase between said first input signal and said second input signal.

22. A method as claimed in claim 21, wherein said generating said at least one intermediate phase signal is performed by superimposing a first signal based on said first input signal and a second signal based on said second input signal.

23. A method as claimed in claim 22, including:
receiving an input signal;
generating an output signal;
generating at least one phase shifted signal by shifting the phase of said input signal with a first predetermined phase shift;
if said phase shifted signal has a transition from a first state to a second state:
switching said output signal from a current state to a substantially inverse state;
and after a predetermined number of periods of said selected signal:
performing said step of generating at least one phase shifted signal with a phase shift different from said first predetermined phase shift; and
performing said switching.

24. A method as claimed in claim 23, wherein said generating at least one phase shifted signal includes filtering at least one of said input signals.

25. A method as claimed in claim 24, wherein said filtering includes low pass filtering.

26. A method as claimed in claim 24 or 25, wherein said filtering includes all-pass filtering.

27. A method as claimed in any one of claims 24-26, wherein said filtering includes high pass filtering.

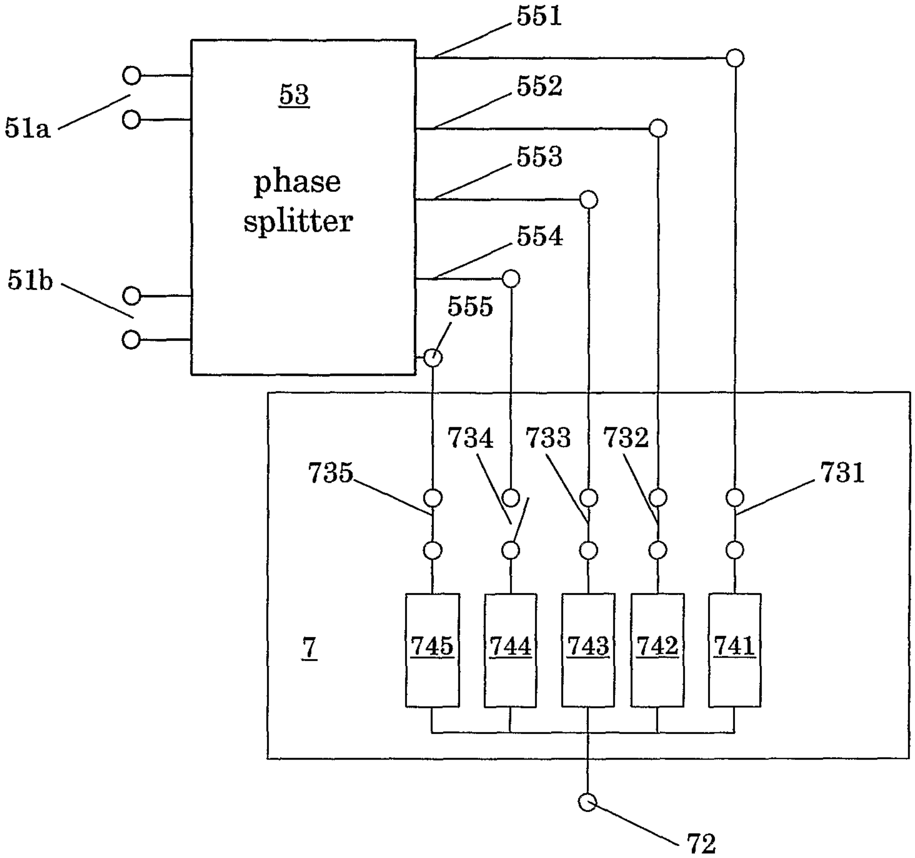
28. A method as claimed in any one of claims 24-27, wherein said filtering includes poly-phase filtering.

29. A method as claimed in any one of claims 23-28, wherein said performing said step of generating at least one phase shifted signal with a different predetermined phase shift is performed by adjusting the resistance of an adjustable resistor.

30. A method as claimed in any one of claims 23-28, wherein said performing said step of generating at least one phase shifted signal with a different predetermined phase shift is performed by changing the capacitance of a variable capacitor.

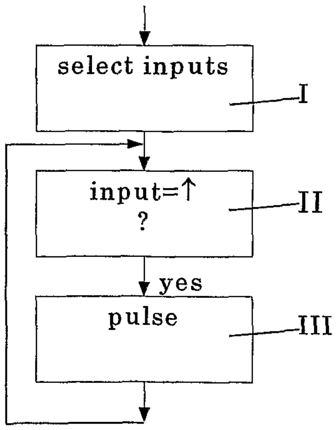
31. A method as claimed in any one of claims 23-28, wherein said performing said step of generating at least one phase shifted signal with a different predetermined phase shift is performed by changing the inductance of an adjustable inductance.

Fig. 1



551
552
553
554
555
53
phase splitter
51a
51b
734
733
732
735
731
745
744
743
742
741
7
72

Fig. 2



select inputs
I
input=↑ ?
II
yes
pulse
III

Fig. 3

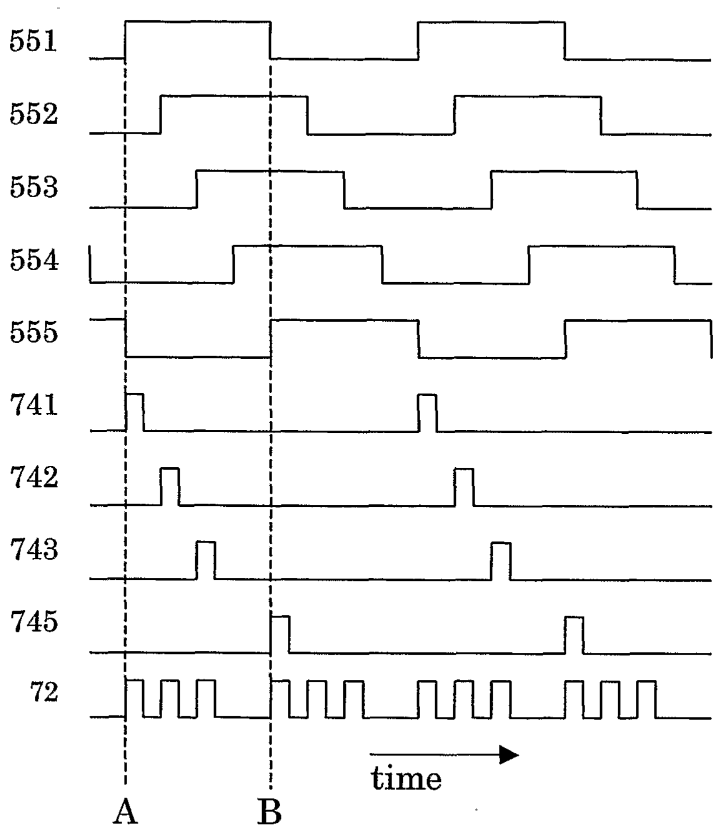

551
552
553
554
555
741
742
743
745
72
time
A
B

Fig. 4

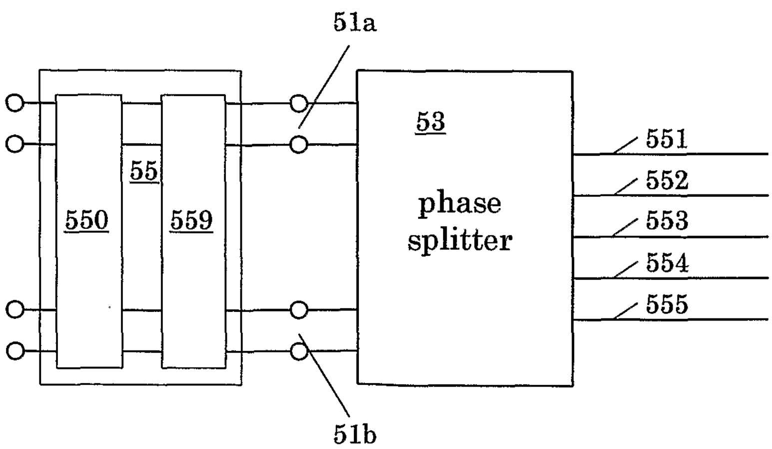

51a
53
phase
splitter
55
550
559
551
552
553
554
555
51b

Fig. 5

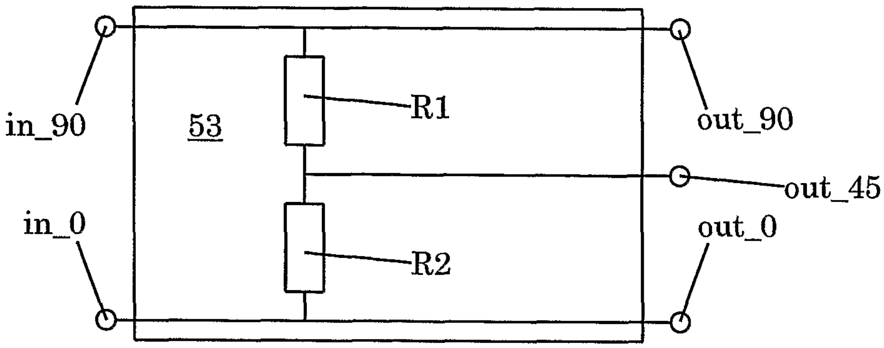

in_90
in_0
53
R1
R2
out_90
out_45
out_0

Fig. 7

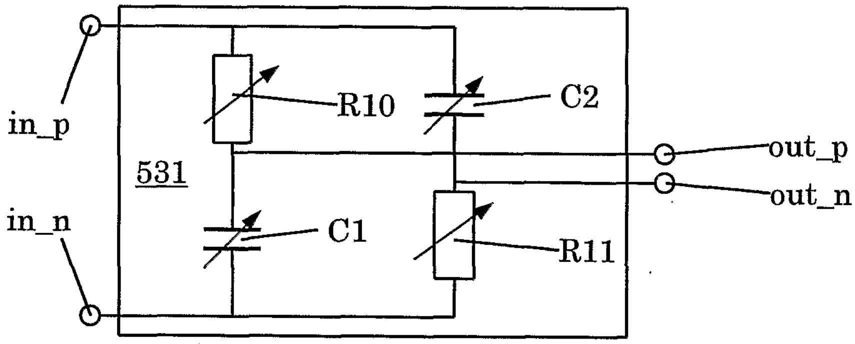

in_p
in_n
531
R10
C2
C1
R11
out_p
out_n

Fig. 6

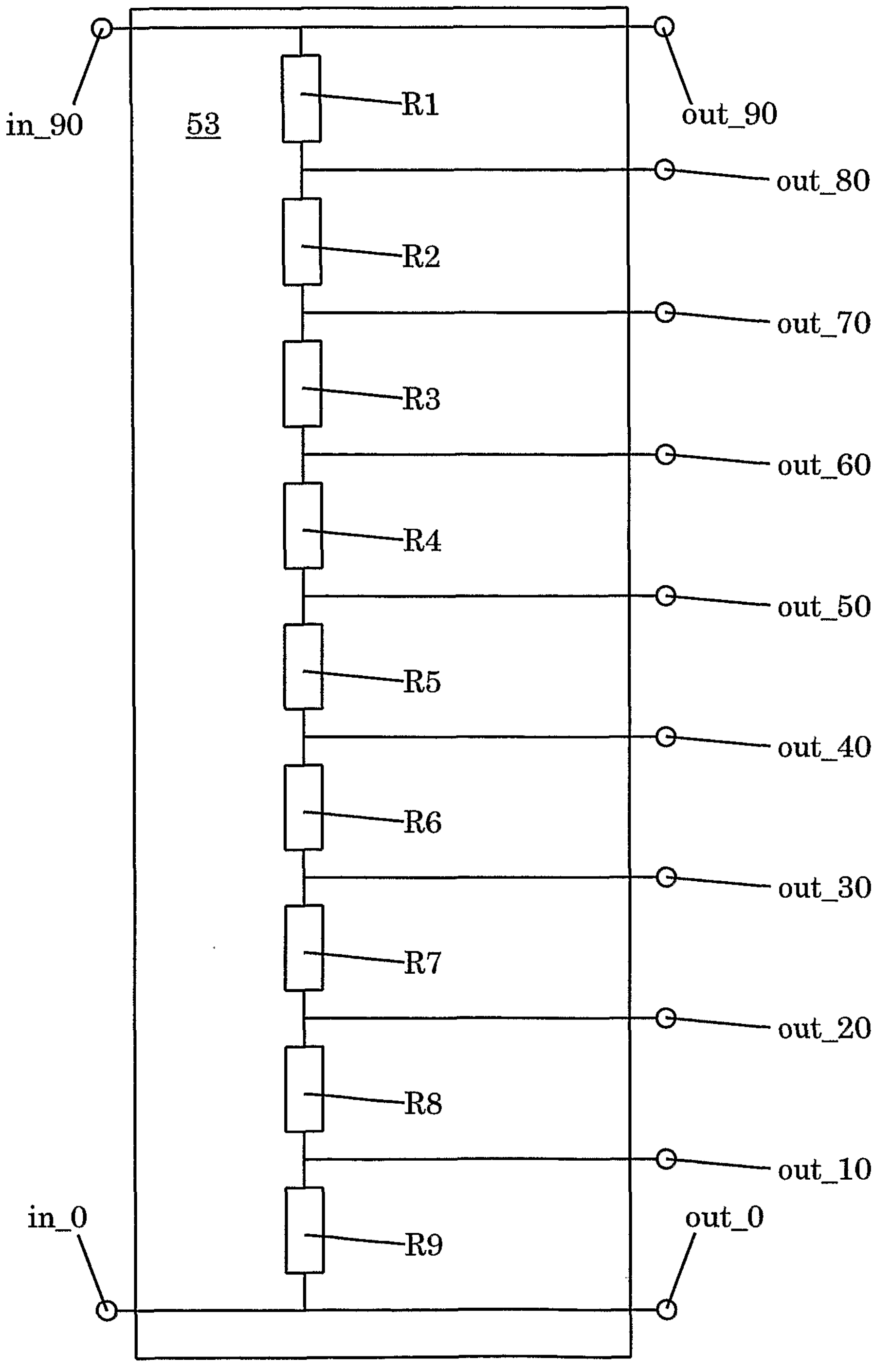

in_90
53
R1
out_90
out_80
R2
out_70
R3
out_60
R4
out_50
R5
out_40
R6
out_30
R7
out_20
R8
out_10
in_0
R9
out_0

Fig. 8

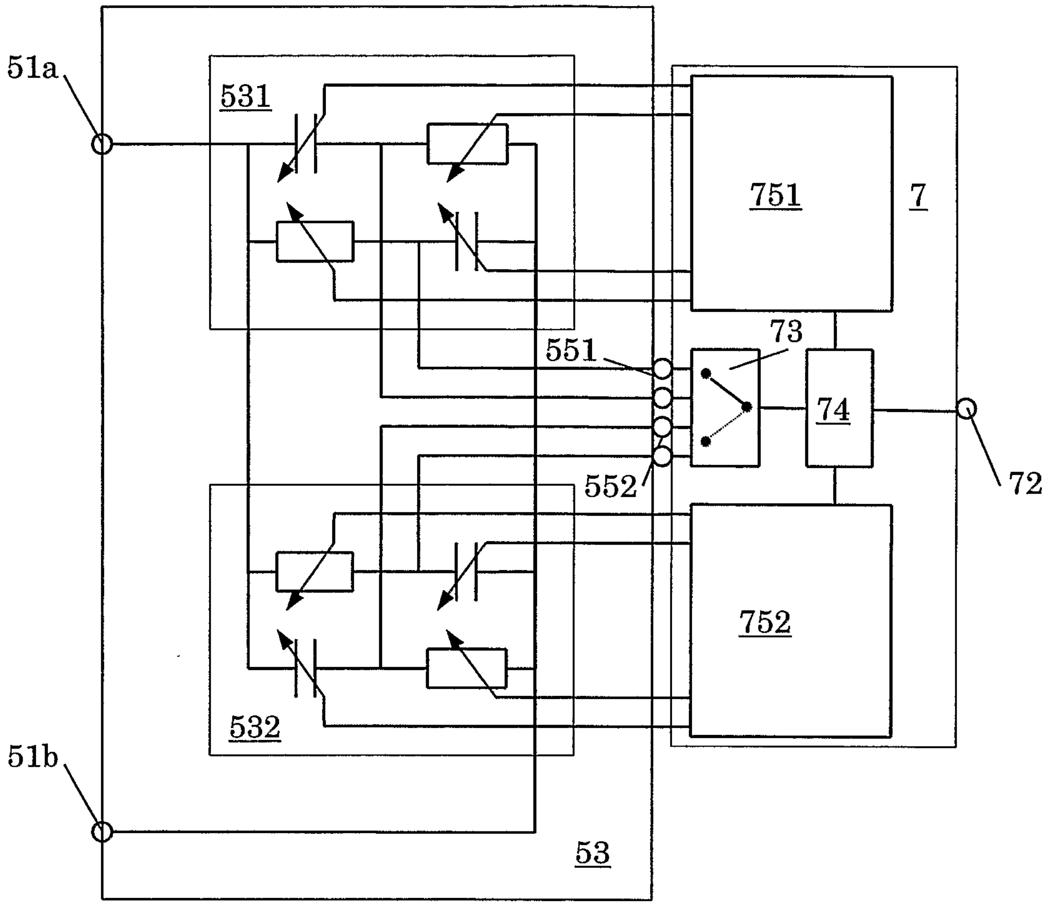

51a
531
751
7
73
551
74
72
552
752
532
51b
53

Fig. 9

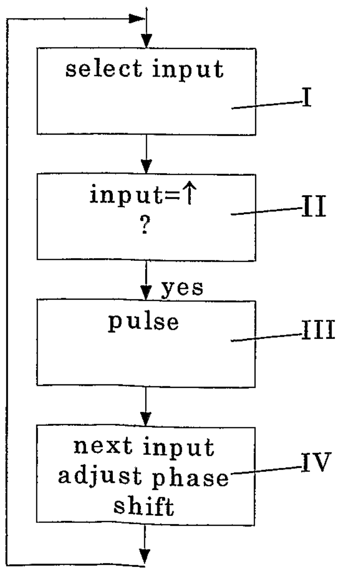

select input
I
input=↑
?
II
yes
pulse
III
next input
adjust phase
shift
IV

Fig. 10

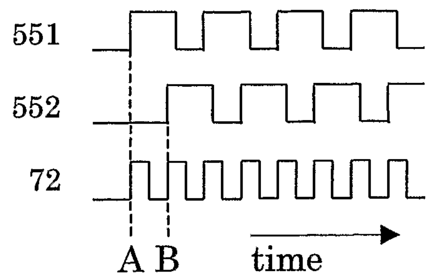


Fig. 11

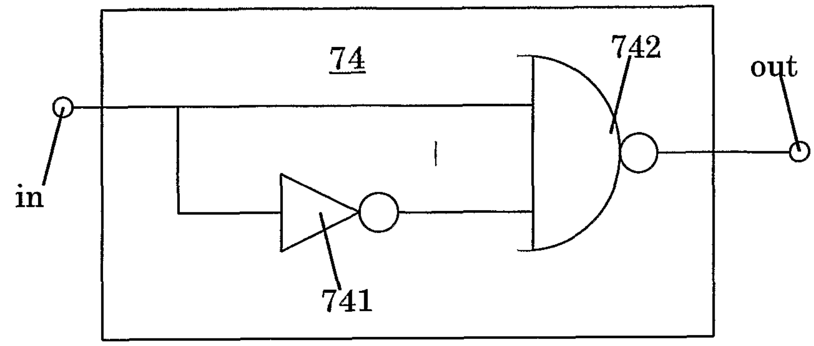
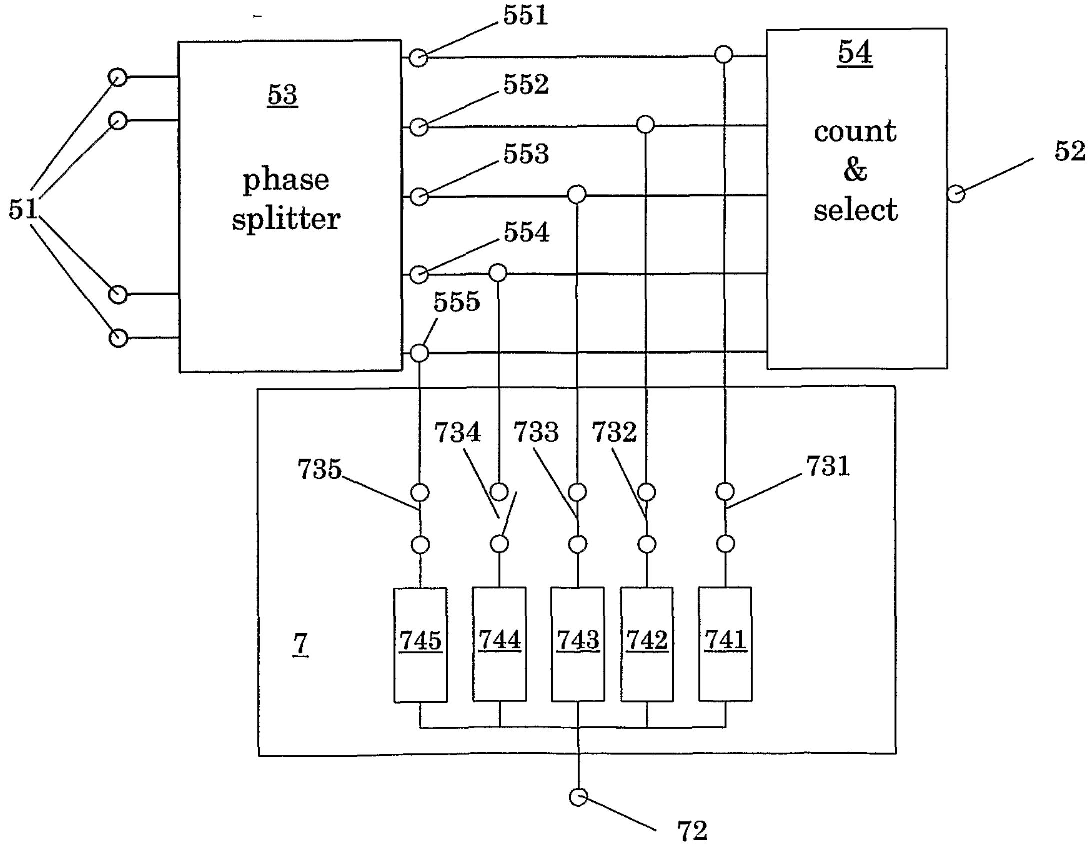


Fig. 12



INTERNATIONAL SEARCH REPORT

Int nal Application No
PCT/EP 02/00268

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K5/00 H03K5/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 864 246 A (ANDERSON MICHAEL B) 26 January 1999 (1999-01-26) column 2, line 9-45; figures 2-4	1,3,4, 17-22
X	US 5 963 071 A (DOWLATABADI AHMAD) 5 October 1999 (1999-10-05)	1,3,6,7, 11,12, 14,16-20
	column 4, line 26 -column 6, line 5; figure 4A column 8, line 65 -column 9, line 34; figures 9,10 column 8, line 53-57; figures 8A,8B column 7, line 31-34; figure 6	
A		24,25, 29,30

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
31 October 2002	12/11/2002

Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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