

(19)  
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2004 01 24

(21) 10-2002-0040651  
(22) 2002 07 12

(71) 136-1

(72) 108-312

2 295-50

(74)

:

(54)

가

1

1

2

(Shared)

(Isolation)

Vpp

Vss

Vext

tDPL(data-in to precharge time)  
가

(inline)

(Leakage)

V( )가

tRAS

가

tRP( )

가

1

1

2

1, 2

가

가

1

S N1,N2 N3~N5 bish (10) (20) BL,/BL blp (30) BL,/BL NMOS NMO

bisl (40) PMOS P1,P2 BL,/BL NMOS (30) RTO,/S N6,N7 BL,/BL NMOS (30) N8,N9

tage) 가 (10,40) NMOS N1,N2,N8,N9 NMOS N1,N2,N8,N9 (Substrate vol) 가

bish,bisl가 가 (Negative bias)

(Equalizing) NMOS N3~N5 가  
blp가 가

2

(1) (x-address) bish bisl 가  
Vpp

MOS OS Vbb N8,N9( N8,N9( bish( N1,N2) bisl) NMOS N1,N2( N8,N9) , N NM  
N8,N9( N1,N2) 가 bish( bisl) 가

(20) NMOS N3~N5 가

(2) (30)

(3) (4) (30)  
BL /BL bish bisl가 NMOS N1,N2,N8,N9가 ,  
Vblp(half Vcc) N1,N2,N8,N9 가  
Vbb 가

3

3 OS N10 NMOS bleq BL /BL NM (60)  
N13,N14 BL,/BL N19 , N11,N12 bish /BL BL,/BL CSP,CSN  
PMOS (50) P3,P4 NMOS

(60)

(70) (80) bleq BL,/BL NMOS (60) N15,N16 N  
MOS N17,N18 bisl (80) BL,/BL

/ 가 NMOS N10,N19 bleq , BL  
/BL (Direct) tRP

, NMOS N10,N19 가 bleq가 가  
(Negative bias)

, NMOS N10,N19 BL  
/BL

tRP

, tRAS가

(lcc curr

ent)

(57)

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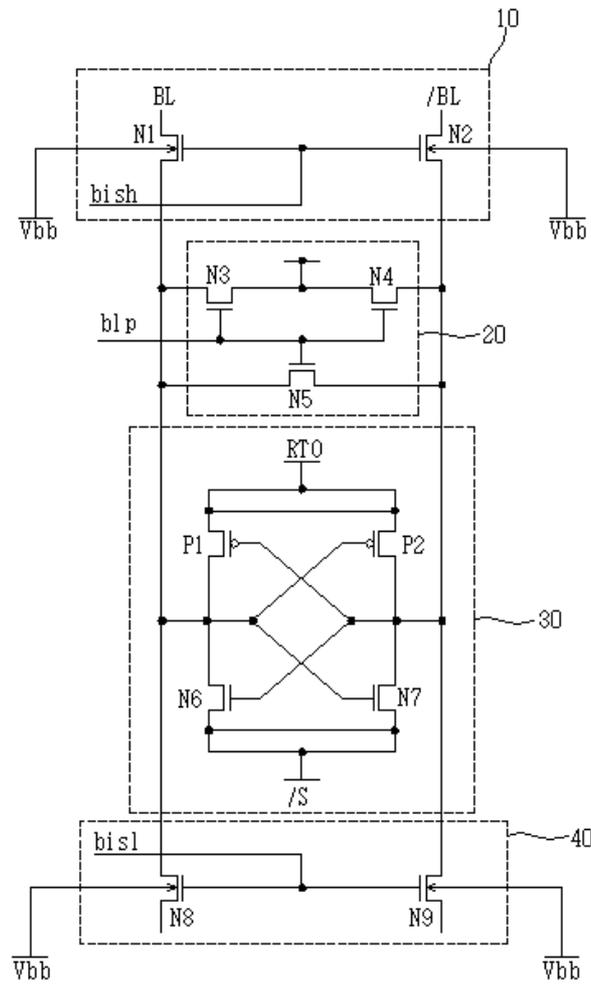
가

5.

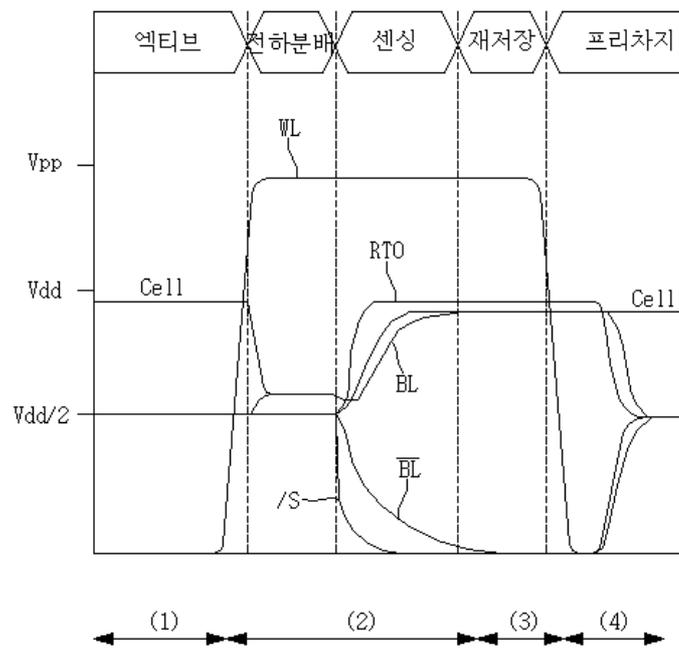
4

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1



2



3

