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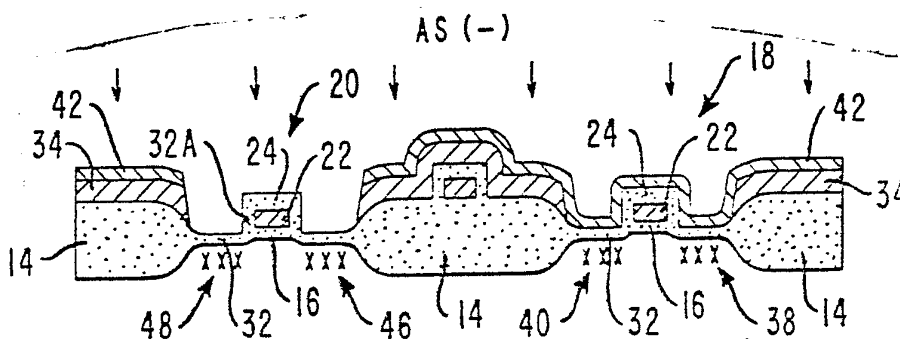

(57) Abstract

In a process for fabricating CMOS devices having polysilicon gate electrodes on a semiconductor substrate (10), a gate oxide layer (16) is provided on the substrate, and doped polysilicon gate electrodes (22) are defined on the gate oxide layer (16) which is then removed from the source and drain regions. A protective layer (32) of silicon dioxide is then applied over the source and drain regions and over the sidewalls (28) of the gate electrodes (22). A first silicon nitride mask (34) is formed leaving exposed a first region (18) which is then subjected to a boron implant to form the sources and drains of the p-channel devices. A second silicon nitride mask (42) is formed over the substrate (10), and a second region (20) of the substrate is then subject of an arsenic implant to form the sources and drains of the n-channel devices. The remaining silicon nitride is removed using a phosphoric acid etchant, the substrate surface being protected during the etching by the silicon oxide protective layer (32).

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PROCESS FOR MANUFACTURING CMOS SEMICONDUCTOR DEVICES

Technical Field

This invention relates to processes of the kind for selectively doping areas in a semiconductor substrate with different impurity type dopants, including the step of defining first and second regions to be subjected to the application of respective first and second impurity type dopants.

The invention has a particular application to the manufacture of CMOS semiconductor devices.

Background Art

By definition, CMOS integrated circuits (ICs) require both p-channel and n-channel FETs on the same semiconductor chip. To account for the opposite resistivity type in the two channels, islands or wells are formed in the semiconductor substrate and are doped to have a conductivity opposite that of the substrate. Contemporary preference is to utilize an n-type substrate, for the p-channel FETs, and diffused p-type wells for the n-channel FETs, though substrates and wells of the opposite dopant are being considered for the future. Undoubtedly, one recognizes that the present invention, though embodied in one form, is amenable to fabrication having either configuration.

In the pursuit of higher component densities in CMOS ICs, scaling techniques and processing steps have been conceived and refined to produce active circuit devices with exceptionally small dimensions. The coplanar process, often referred to as the LOCOS process, is particularly suited for fabricating ICs with high component density levels by utilizing self-aligned gate electrodes and field guard rings to suppress parasitic devices. The field guard rings are the regions of greater impurity density underlying the field oxide. As

the vertical dimensions of such IC devices decrease further, the source and drain regions of the individual FETs must also shrink. This reduction of the S/D (source and drain) regions is generally accomplished by using
5 refined ion implant techniques to dope the S/D regions with p^+ and n^+ impurities. With a judicious choice of impurity types and annealing conditions, relatively small and shallow, but heavily doped, S/D regions can be formed in the chip.

10 The demand for higher dopant concentrations at shallow depths are not limited to the S/D regions of the CMOS ICs, since the increase in density also dictates that the electrical interconnects be formed with diffusion lines in the substrate. Like the S/D regions,
15 the diffusion lines must be shallow, yet low in resistivity.

Given the pervasive need for higher dopant concentrations with relatively shallow penetration depths, one is confronted by the inherent limitations of
20 conventional processes. Generally, contemporary manufacturing processes prescribe ion implanting as the method for selectively doping substrate regions. If low or medium ion energy and implant dose rates are used, the concentration and depth requirements for shallow S/D
25 regions cannot be satisfied. Furthermore, high doses, for instance, 10^{15}-10^{16} ion/centimeters squared implanted with energy levels of 20-200 KeV, still require high ion implant beam currents if the processes are to be completed within a reasonable period of fabrication
30 time. Note, however, that combinations of high currents and energy levels inherently raise the wafers to temperatures significantly greater than normally experienced during fabrication. The implications of such elevated temperatures will be described hereinafter.

35 Generally, during the fabrication of the S/D regions of the p-channel FETs and p-type interconnects,

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the S/D regions and interconnects of the n-type areas are somehow protected from the p-type boron implant ions. Conversely, the n-type areas are implanted with phosphorus, arsenic or antimony ions while the p-type
5 areas are protected. In the general practice of the prior art, photoresist materials served adequately as the ion barrier. However, photoresist masks are suited only for moderate temperature environments, represented by processes in which the ion implant dose rates and
10 energy levels are low or medium in relative amplitude. Photoresist masks may remain viable at high implant rates, but only if extraordinary measures are taken to cool the wafer during the implant process. If such precautions are not incorporated into the process, and
15 high dose rates and energy levels are implemented, the photoresist burns or flows, with a consequential deformation of the photolithographic pattern, non-uniform implant resistivity and likely contamination of the implant chamber. With conventional photoresist materials
20 and implant apparatus, process integrity limits the wafer temperature to about 160°C. Consequently, one now recognizes the need for specialized cooling or process refinements if high ion implant dose rates and energy levels are to be utilized with masks of photoresist
25 material.

Disclosure of the Invention

According to the present invention, there is provided a process of the kind specified, characterized by the steps of: covering said first and second regions
30 with a layer of a protective material having a thickness substantially permeable to implants of said first and second impurity type dopants; depositing a first implant mask substantially impermeable to an implant of said impurity type dopant, leaving exposed said first region;
35 exposing the masked substrate to an implant of said first impurity type dopant; depositing a second implant

mask substantially impermeable to an implant of said second impurity type dopant, leaving exposed said second region; exposing the masked substrate to an implant of said second impurity type dopant; and removing said first and second implant masks from the substrate with an etchant which etches the first and second implant mask materials at a greater rate than said protective material.

A process according to the invention has the capability of alleviating the problems arising in using photoresist masks for ion implantation at high ion implant beam currents and energy levels.

Preferably, the first and second implant masks are formed of silicon nitride, a material having a high thermal stability at temperatures produced in the semiconductor substrate when using high ion implant currents and energy levels. In this connection it is to be noted that the use of silicon nitride ion implant masks in the manufacture of CMOS devices is known per se from German Offenlegungsschrift No. 2,930, 630.

Where the first and second regions have gate structures projecting above said substrate, including gate oxides and electrodes, a further feature of the process according to the invention resides in the step of covering the sidewalls of the electrodes with the layer of protective material. This has the advantage of protecting the exposed vertical walls of the electrodes from process ambients.

In summary, the present invention is generally directed to a process for fabricating semiconductor devices having p-type and n-type doped regions in a common substrate. In a preferred form, it relates to a refined process for forming complementary metal oxide semiconductor (CMOS) type field effect transistors (FETs) by altering the generally-known coplanar process. In the manner practiced, the process lends itself to structures characterized by single dopant type polycrystalline silicon electrodes and self-aligned gates.

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The ion implants of the source-drain (S/D) regions are performed at relatively high implant energy levels and beam currents. Consequently, shallow, but high impurity density, S/D junctions are formed in CMOS structures having self-aligned gates and doped polycrystalline silicon electrodes.

With more particularity, the process departs from the convention at a step in the process after the field oxides are formed and the doped polycrystalline silicon electrodes are deposited and photolithographically defined. During the plasma etch associated with the electrode definition, only the gate and interconnect electrodes areas, each covered by silicon dioxide, are not etched away. The S/D regions of the substrate are exposed. Thereafter, a nominal thickness of silicon dioxide is grown on the sidewall of each polycrystalline silicon electrode, while a thinner layer of silicon dioxide is simultaneously formed on the exposed substrate in each of the S/D regions. The silicon dioxide formed over each S/D region is by selection sufficiently thin to be substantially permeable to impurity ions during the succeeding implant step, yet adequately thick to protect the underlying substrate from silicon nitride etchants used subsequently in the process.

The wafer is then covered by a deposition of silicon nitride, which is in succession photolithographically defined and dry plasma etched to expose the p-channel FET S/D regions. The regions, however, retain a thin covering of silicon dioxide. The silicon nitride layer covering the n-channel FETs serves as an ion implant mask, readily withstanding the high wafer temperatures encountered during the boron implant into the p-channel S/D regions. Since the silicon nitride is a protective barrier for the n-channel S/D regions, it must be sufficiently thick to be substantially impermeable to boron ions.

After the first ion implant is completed, another silicon nitride layer is deposited over the

surface of the wafer. In this case, the succeeding steps photolithographically expose the S/D regions of the n-channel FETs for arsenic ion implanting. As was true for the previous silicon nitride layer, the depth of the new layer is by selection just sufficient to protect the complementary FETs during the S/D implant of the n-channel FETs.

At the conclusion of the n-channel implant, all remaining silicon nitride is removed using an etchant having a very high preferential etch ratio between silicon nitride and silicon dioxide. Thereby, the thin silicon dioxide layers covering the various exposed surfaces protect the underlying polycrystalline silicon electrodes and monocrystalline silicon S/D regions of the substrate.

Thus, it will be appreciated that the beneficial aspects of coplanar processing, with polycrystalline silicon and self-aligned gates, single impurity type polycrystalline interconnects, minimal mask alignment constraints and few process masks, are retained, while gaining the ability to create shallow regions with high dopant concentrations.

Brief Description of the Drawings

One embodiment of the invention will now be described by way of example with reference to the accompanying drawings in which:

Figs. 1-13 depict sequential stages in the processing of a complementary pair of CMOS FETs, shown in cross-section.

Best Mode for Carrying Out the Invention

Fig. 1 represents an IC (integrated circuit) at a recognized step in the coplanar process, and shows an n-type substrate 10, a p-type well 12, thick field oxides 14, thin gate oxides 16, and regions 18, 20 for the provision of p-channel and n-channel FETs. Channel stopper implants (not shown) under the field oxides 14

are normally introduced in a prior step. Since the substrate and well designations are well-known, their repeated delineation and dopant marking is dispensed with after Fig. 1.

5 Figs. 2 illustrates the relative organization of the IC after a deposition of phosphorus (n-type impurity) doped polycrystalline silicon 22 followed by a covering of chemical vapor deposition (CVD), or thermally grown, silicon dioxide 24 in the manner of the known

10 art. In a similarly-known manner of the art, a photoresist (PR) mask 26 is deposited and photolithographically delineated in Fig. 3. The CVD silicon dioxide 24 is then selectively removed with a wet etch, and followed in sequence by a dry plasma etch through the polycrystal-

15 line silicon layer 22, using the photoresist 26 as a mask.

Fig. 4 depicts the general structure which results from the steps in the preceding figures, including an n-channel gate area, 1, a p-channel gate

20 area, 2, and a doped polycrystalline silicon interconnect area, 3. Given the structural organization depicted, and the intended utilization of the gate electrodes as the implant masks, the depth of the CVD silicon dioxide covering the polycrystalline silicon is preferably about

25 3,000 Angstroms. This depth is suited to a boron implant performed at an energy of approximately 30 KeV. Though thinner layers of silicon dioxide are feasible when the polycrystalline silicon is heavily doped with an impurity of phosphorus (n-type dopant), care must still

30 be exercised to prevent significant boron accumulation in the polycrystalline silicon lest it subsequently migrate through the gate oxide to contaminate the channel region in the substrate layer.

It is with Fig. 4 that the present process

35 departs significantly from the general prior art and embarks upon procedural steps unique to the invention. In one form of practicing the invention, a brief wet

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etch step is first used to remove the exposed areas of the gate oxides 16. The field oxides 14 and CVD oxides 24 over the polycrystalline silicon electrodes 22 remain by virtue of their significantly greater thickness.
5 Thereafter the bare sidewalls 28 of the polycrystalline silicon electrodes 22 and monocrystalline silicon S/D regions 30 of the substrate, as shown in Fig. 5, are thermally oxidized to form a covering 32, 32A of silicon dioxide. Refer to Fig. 6. This step protects the
10 exposed vertical walls 28 of the polycrystalline silicon 22 from process ambients, for example the potential sources of auto-doping, while providing a better match in terms of thermal coefficient of expansion with the succeeding layer of silicon nitride. The oxidation
15 conditions and dopant levels in the polycrystalline silicon gate 22 are selected so that the sidewall oxides 32A are grown to a thickness in the range of 1,500-2,500 Angstroms, while the S/D region silicon dioxide 32 levels reach approximately 500 Angstroms. The significant
20 differences in growth rate are primarily due to the differences in dopant levels, but are, nevertheless, influenced to some degree by the polycrystalline character of the gate electrode 22 in contrast to the monocrystalline character of the S/D region in the
25 substrate 10. It should not be overlooked that the top surface of the electrode, covered by the CVD oxide 24, also experiences a growth in oxide depth. The increase in depth is not nearly to the same extent as the sidewalls 32A, reaching a level of about 3500 Angstroms for
30 the conditions described above.

Given that silicon nitride is to be utilized in this embodiment as the implant barrier, attention must be redirected briefly to consider some constraints intrinsic to the materials and energy levels. Undoubtedly,
35 any silicon nitride layer used as implant barrier must be thick enough to prevent penetration of the impurity ion utilized. In this context, if one plots

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the concentration of the implant species versus depth of penetration, the plot obtained is approximately Gaussian in its distribution. Use R_p to represent the range, defined as the depth at which the concentration reaches its Gaussian peak. Reference to empirical and statistical data will show that both R_p and the standard deviation ( ) for the Gaussian distribution are functions of the implant energy, the implant species, and the material into which the species are implanted. For silicon nitride as the implant recipient, Table 1 represents the approximate statistical penetration for boron and arsenic with respective energy levels of 30 KeV and 80 KeV.

TABLE 1

	30 KeV Boron Implant		80 KeV Arsenic Implant	
	Si_3N_4	SiO_2	Si_3N_4	SiO_2
R_p	740 A	950 A	300 A	390 A
	270	370	100	130
5	1350	1710	490	630
R_p+5	2070	2260	790	1010

A conservative description of a process relying on the data in the Table would establish that the implant is sufficiently blocked if only an extreme tail of the Gaussian distribution, at least 5 from the peak, penetrates the blocking layer. With this barrier depth, the implanted impurity concentration penetrating is approximately 10^{-5} lower than the peak concentration in the barrier. Referring to the Table for a depth of R_p + 5 , one extracts that a silicon nitride layer of 2,100 Angstroms is suitable during the 30 KeV boron implant, and 800 Angstroms during the 80 KeV arsenic implant. It should not be overlooked that these silicon nitride masking layers are exemplary for the impurity

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species and energy levels of the present embodiment. Accordingly, refinements will be necessary as materials, energy levels and process tolerances dictate.

With an understanding of some of the underlying constraints at hand, attention is again drawn to the figures illustrating the process steps. The oxidized surface shown in Fig. 6 is now coated with a 2,000 Angstrom layer 34 of silicon nitride in Fig. 7. As embodied, a photoresist layer 36 is applied over the deposited silicon nitride and delineated to expose the p-channel active area 18. Fig. 8 shows the silicon nitride 34 exposed through the photoresist 36 undergoing a dry plasma etch to remove the region covering the p-channel device. Though the invention was practiced with a plasma containing CF_4 and oxygen in a barrel etcher, a planar etcher with gases having better selectivity is preferred. One reason for the sidewall oxide 32A is now recognized. The CF_4 plasma used to etch the silicon nitride 34 also attacks the polycrystalline silicon and the monocrystalline substrate, both at a rate many times greater than the silicon nitride etch rate. In contrast, the etch rate of silicon dioxide is relatively low, allowing the silicon dioxide to serve as a protective buffer.

The illustration in Fig. 9 shows that the low temperature photoresist is removed before undertaking the boron ion implant to form the p^+ doped S/D region 38, 40 of the p-channel FET. During the implant, the n-channel FET region is masked by the combination of the 2,000 Angstrom silicon nitride layer 34 and approximately 500 Angstroms of silicon dioxide 32 grown over the S/D regions. The self-aligned channel area of the p-channel FET is protected from boron doping by the covering 24 of 3500 Angstroms of silicon dioxide. In contrast, the S/D regions 38, 40 of the p-channel FET are readily doped through the 500 Angstroms of silicon dioxide 32 when the implant is performed with an energy of 30 KeV. Refer to Table 1.

Figs. 10 and 11 show the deposition of another silicon nitride layer 42, to a depth of approximately 800 Angstroms, followed by a photolithographic definition in a photoresist layer 44 and a dry plasma etch. CF_4 again serves as the etchant material, removing the 2800 Angstrom cumulative thickness of silicon nitride over the region 20 of the n-channel FET. Following the removal of the photoresist 44, arsenic ions (n-type dopant) are implanted, as schematically depicted in Fig. 12, by penetration through the approximately 500 Angstroms of oxide over the S/D regions 46, 48. Again, referring back to Table 1, it is evident that the 800 Angstroms of silicon nitride 42 prevents arsenic ion penetration into the p-channel FET when the arsenic implant energy is 80 KeV. Likewise, the 3500 Angstroms of silicon dioxide 24 protects and self-aligns the n-type channel.

It now becomes apparent why the thickness of the silicon dioxide 32 over the S/D regions was limited to approximately 500 Angstroms or less. Were the gate oxide 16 of approximately 600 Angstroms not removed prior to the growth of the sidewall oxide 32A and the S/D oxide 32 of 500 Angstroms, the combined thickness of the oxide covering the S/D region, approximately 1,100 Angstroms, would exceed the nominal penetration of the proposed arsenic implant. From the foregoing, it is clear that the various steps are closely related in accomplishing the final objective.

The final step in the process, removing the residual silicon nitride 34, 42, leads to the IC configuration depicted in Fig. 13. Note that it is necessary to remove a total of 2800 Angstroms of silicon nitride in the field oxide regions, while the p-channel FET is covered by only 800 Angstroms and the n-channel FET lacks any silicon nitride covering. Care must be exercised to avoid etching into the S/D regions and laterally into the polycrystalline silicon electrode walls, while reliably removing the thickest silicon

nitride layer. Residuals of silicon nitride have been linked to instabilities during the operation of IC FETs.

The present embodiment relies upon the preferential etch ratio of hot phosphoric acid (H_3PO_4). The
5 50:1 etch ratio, nitride to oxide, exhibited by hot phosphoric acid removes the approximately 2800 Angstroms of silicon nitride while only dissolving approximately 60 Angstroms of silicon dioxide on a continuously exposed surface, for instance the n-channel FET. Recalling
10 that the thinnest silicon dioxide layer is the 500 Angstroms over the S/D region of the n-channel FET, it is apparent that the embodying process provides an adequate margin for fabrication. Furthermore, recent advances in dry etching suggest that new materials,
15 exhibiting acceptable preferential etch ratios, may be available in the foreseeable future as substitutes for this wet acid etchant. A preferential etch ratio greater than 20:1 would be sufficient.

The CMOS fabrication steps following from the
20 structure in Fig. 13 are fairly rudimentary for those skilled in the art. Consequently, they will be described by summary. Namely, a thick isolation oxide is deposited, contact holes are formed therethrough, aluminum interconnects are deposited and delineated, and the final
25 passivation layer is deposited and delineated.

Test devices fabricated according to the embodied process have exhibited excellent performance characteristics. For example, inverter chains have demonstrated propagation delay times of 1.5 nanoseconds
30 per gate with a 5 volt drain-to-source voltage and channel width to channel length ratios at the mask of 50/6 and 25/5 for n-channel and p-channel devices, respectively.

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CLAIMS:

1. A process for selectively doping areas in a semiconductor substrate with different impurity type dopants, including the step of defining first and second regions (18, 20) to be subjected to the application of respective first and second impurity type dopants, characterized by the steps of: covering said first and second regions (18, 20) with a layer of a protective material (32) having a thickness substantially permeable to implants of said first and second impurity type dopants; depositing a first implant mask (34) substantially impermeable to an implant of said impurity type dopant, leaving exposed said first region (18); exposing the masked substrate (10) to an implant of said first impurity type dopant; depositing a second implant mask (42) substantially impermeable to an implant of said second impurity type dopant, leaving exposed said second region (20); exposing the masked substrate (10) to an implant of said second impurity type dopant; and removing said first and second implant masks (34, 42) from the substrate with an etchant which etches the first and second implant mask materials at a greater rate than said protective material.

2. A process according to claim 1, wherein said first and second regions (18, 20) have gate structures (1, 2) projecting above said substrate (10), including gate oxides (16) and electrodes (22), characterized by the step of covering the sidewalls (28) of said electrodes (22) with said layer of protective material (32).

3. A process according to claim 2, characterized by the step of providing a gate oxide layer (16) in said first and second regions (18, 20) and removing said gate oxide layer (16) from said first and second

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3. (concluded)

5 regions (18, 20) except in the region of said gate structures (1, 2), prior to said step of covering with said layer of protective material (32).

4. A process according to claim 3, characterized in that said protective material (32) is silicon dioxide and in that said first and second implant masks (34, 42) are formed of silicon nitride.

5. A process according to claim 4, characterized in that said etchant contains phosphoric acid.

6. A process according to claim 5, characterized in that said etchant has a preferential etch ratio exceeding 20:1.

7. A process according to claim 1, characterized by the step of removing the first implant mask material (34) in said second region (20) after said step of depositing said second implant mask (42) and prior

5 to said step of exposing to an implant of said second impurity type dopant.

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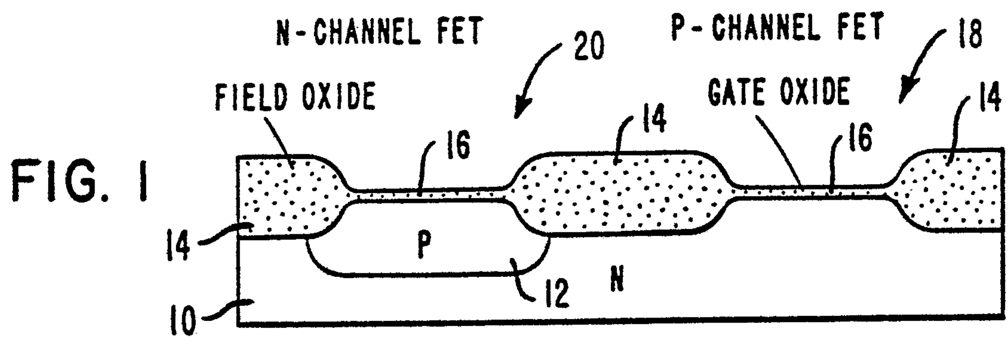

FIG. 1

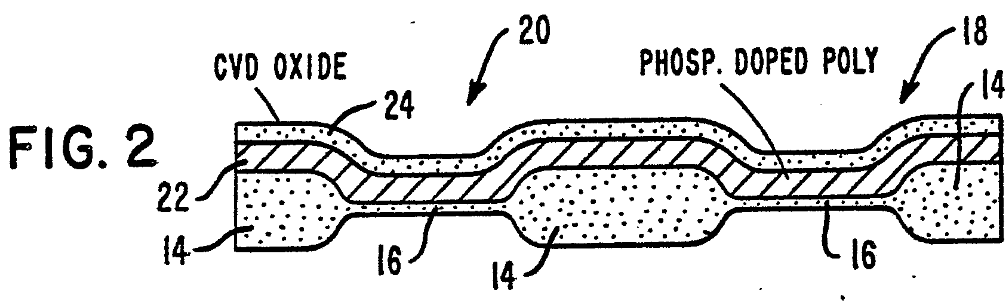

FIG. 2

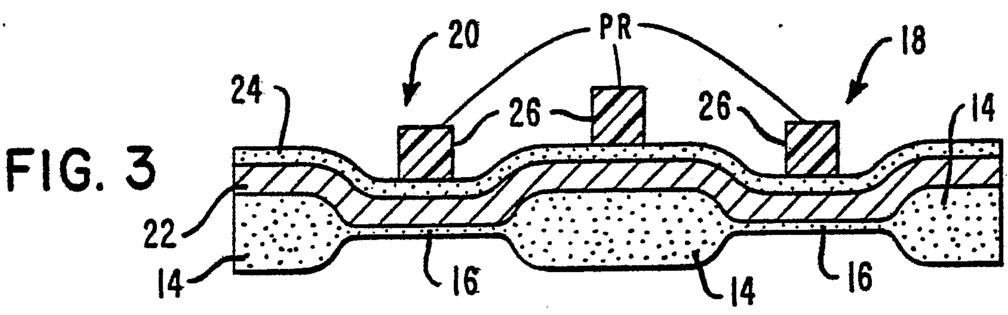

FIG. 3

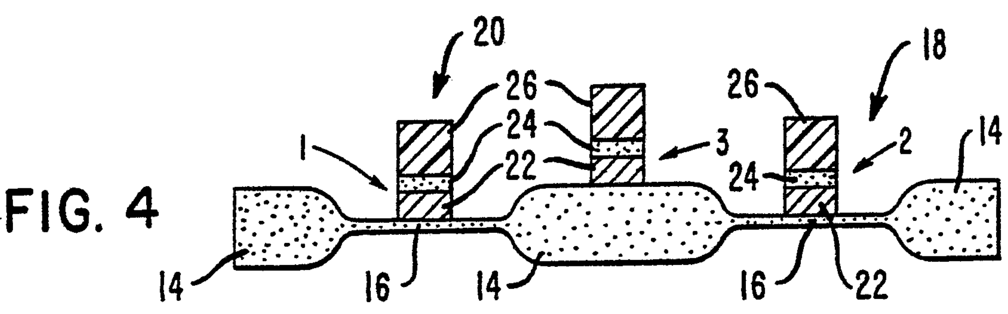

FIG. 4

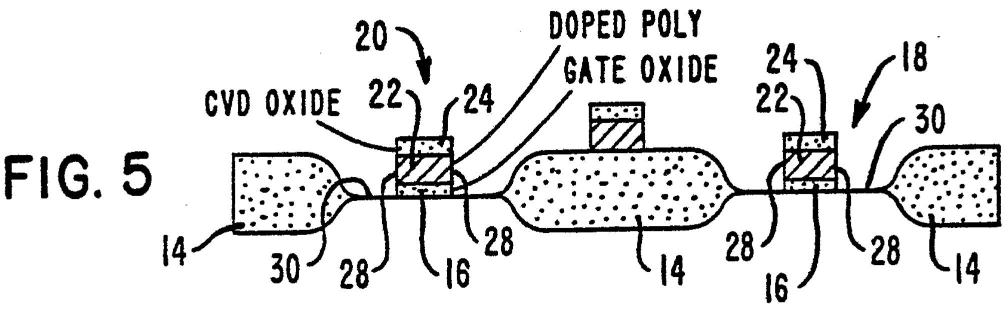

FIG. 5

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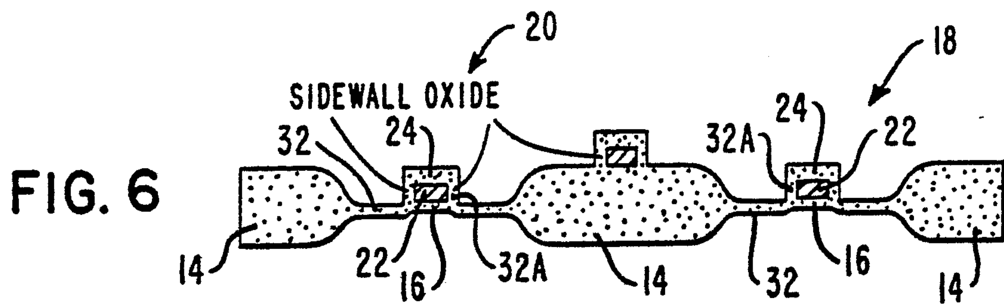

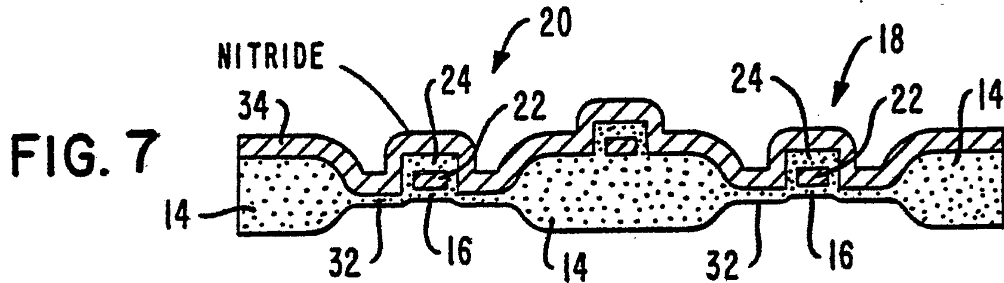

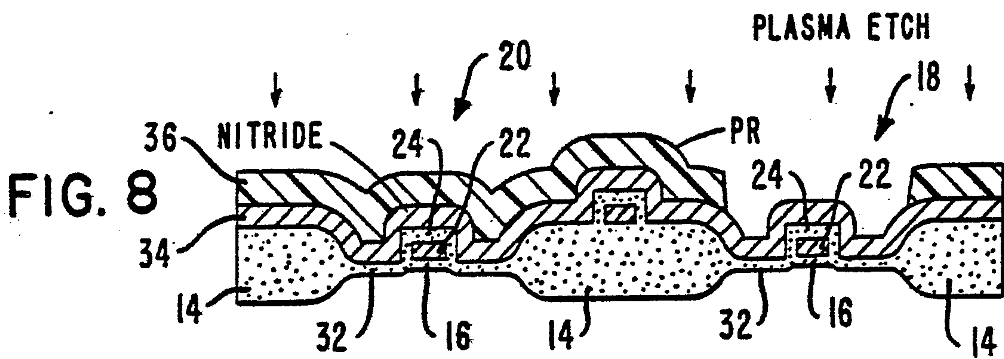

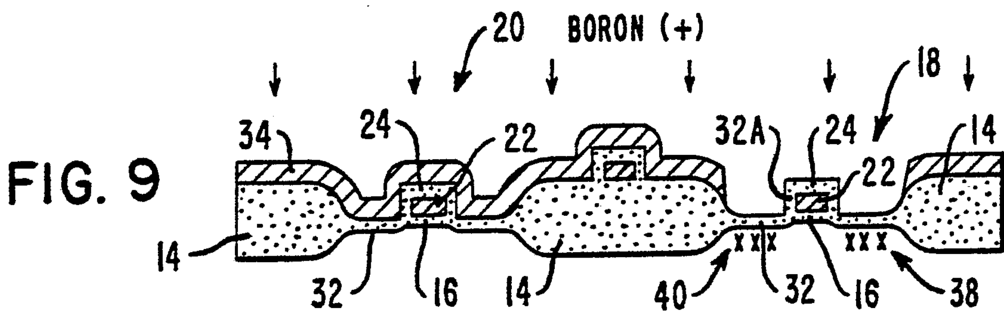

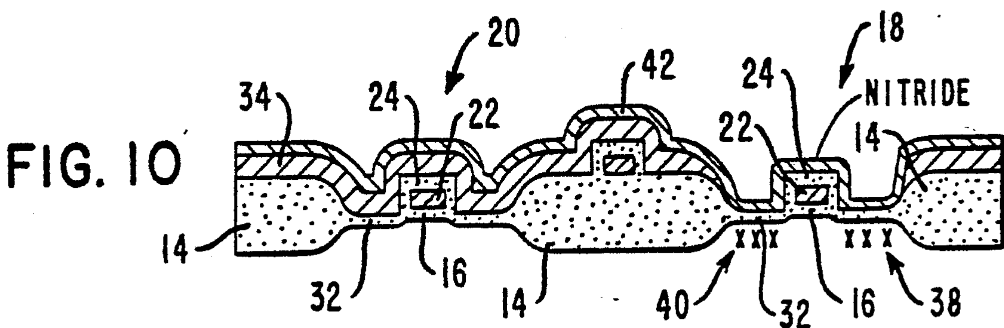

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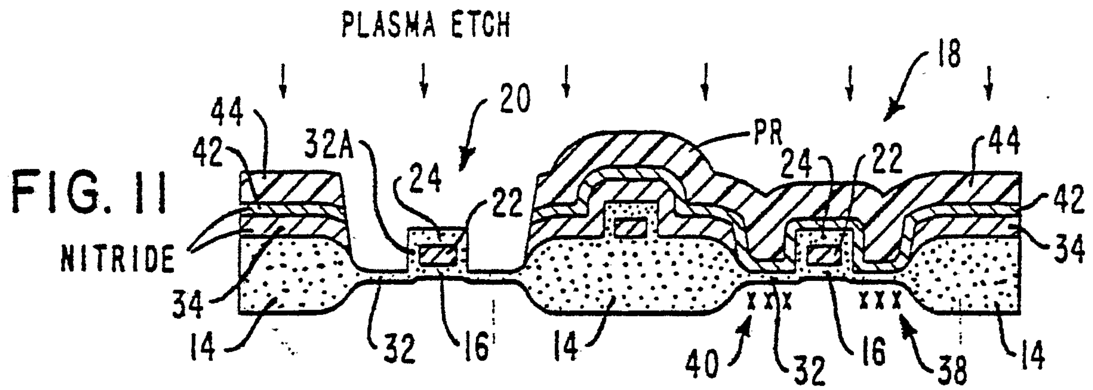

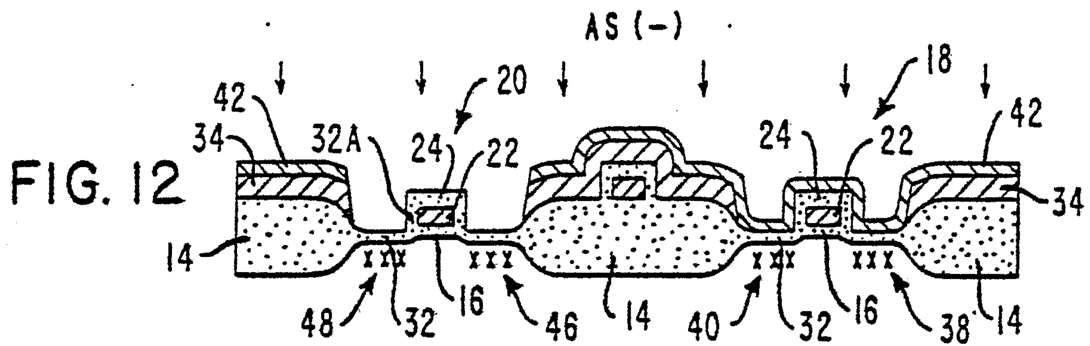

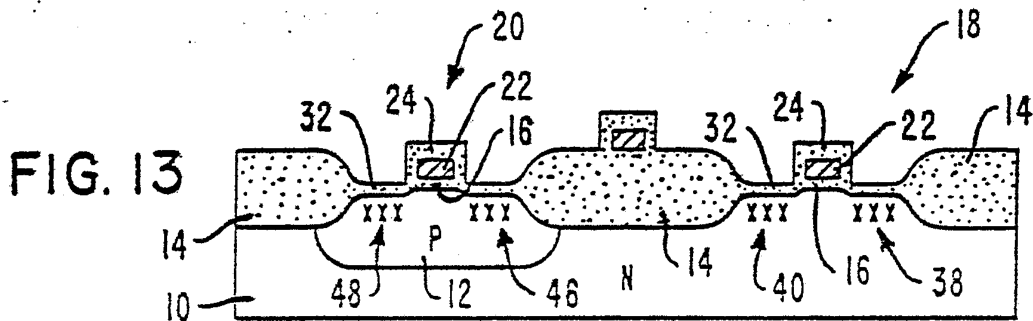

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INTERNATIONAL SEARCH REPORT

International Application No PCT/US 82/00547

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] H01L 21/265, H01L21/54, H01L 21/22
US. CL. 148/1.5, 187; 29/571, 576B; 357/42, 91

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	29/571, 576B 148/1.5, 187 357/42, and 91

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
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X,P	US, A, 4,306,916, Published, 22 December 1981, See fig. 9	1-7
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A,P	US, A, 4,046,606, Published, 06 September 1977	1-7
X,T	US, A, 4,329,186, Published, 11 May 1982	1-7

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
29 JULY 1982	03 AUG 1982
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	UPENDRA ROY Upendra Roy

International Application No. PCT/US 82/00547

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A,P	US, A, 4,306,915, Published, 22 December 1981	1-7

V.☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1.☐ Claim numbers ________, because they relate to subject matter [12] not required to be searched by this Authority, namely:

2.☐ Claim numbers ________, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI.☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1.☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2.☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3.☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4.☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.