(19)日本国特許庁(JP)　(12)公表特許公報(A)　(11)特許出願公表番号
特表2004-507103
(P2004-507103A)
(43)公表日 平成16年3月4日(2004.3.4)

(51)Int.Cl.[7]	FI		テーマコード（参考）
H01L 21/768	H01L 21/90	Q	5F033
H01L 21/31	H01L 21/31	C	5F045
H01L 21/312	H01L 21/312	M	5F058

審査請求 未請求　予備審査請求 未請求　（全 23 頁）

(21)出願番号　特願2002-521330(P2002-521330)
(86)(22)出願日　平成13年8月9日(2001.8.9)
(85)翻訳文提出日　平成14年4月17日(2002.4.17)
(86)国際出願番号　PCT/EP2001/009280
(87)国際公開番号　WO2002/017356
(87)国際公開日　平成14年2月28日(2002.2.28)
(31)優先権主張番号　09/642,074
(32)優先日　平成12年8月18日(2000.8.18)
(33)優先権主張国　米国(US)
(81)指定国　EP(AT,BE,CH,CY,DE,DK,ES,FI,FR,GB,GR,IE,IT,LU,MC,NL,PT,SE,TR),CN,JP

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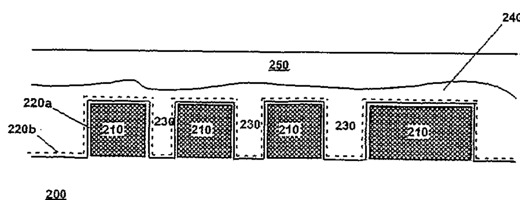
(54)【発明の名称】ライナー酸化物にＭＳＱ材料を結合する方法及び構造

(57)【要約】
【課題】サブミククロンでの半導体製造において低誘電率のスピン・オン材料の結合力を高めるための半導体基板上にライナー誘電体を堆積する方法を提供する。
【解決手段】半導体基板上のアルミニウム合金層上にライナー誘電体を堆積するためのＭＳＱの結合方法である。半導体基板をプラズマ化学気相反応（ＰＥＣＶＤ）環境に晒す。約１：２０乃至１：３０の比率でトリメチルシランとN_2Oの混合ガスをＰＥＣＶＤ環境に導入する。混合ガスが反応して所定厚みのライナー酸化物が堆積される。約５乃至２０秒後にトリメチルシランとN_2Oの比率を約１：３乃至１：７に変えて反応を進展させメチルドープ酸化物を堆積する。



【特許請求の範囲】
【請求項１】
パターン化された金属層、第１のライナー誘電体層、第２のライナー誘電体層そしてスピン・オン誘電体層が積層された半導体装置であって、前記第２のライナー誘電体層は前記金属層とは化学的に親和性が低く、前記第１のライナー誘電体層よりも前記スピン・オン誘電体層と化学的に親和性が高いことを特徴とする半導体装置。
【請求項２】
前記第１のライナー誘電体層はシリコン二酸化物、シリコン含有量の多い酸化物又はSi_xO_y（ｘ＝１，０．４８≦ｙ≦２）のいずれかであり、前記第２のライナー誘電体層はメチルドープ酸化物であることを特徴とする請求項１記載の半導体装置。
【請求項３】
前記第１のライナー誘電体層及び前記第２のライナー誘電体層間に転移層を備え、前記金属層から前記スピン・オン誘電体層の方向に前記第１のライナー誘電体層から前記第２のライナー誘電体層へと変わる成分を前記転移層が有することを特徴とする請求項１又は２記載の半導体装置。
【請求項４】
前記第１のライナー誘電体層及び前記第２のライナー誘電体層の厚みは５乃至１００ｎｍであることを特徴とする請求項１乃至３のいずれかに記載の半導体装置。
【請求項５】
前記転移層の厚みは１０乃至２００ｎｍであることを特徴とする請求項３又は４に記載の半導体装置。
【請求項６】
前記スピン・オン誘電体層は少なくともメチルシルセスクイオキサン（ｍｅｔｈｙｌｓｉｌｓｅｓｑｕｉｏｘａｎｅ）又はハイドロシルセスクイオキサン（ｈｙｄｒｏｇｅｎ　ｓｉｌｓｅｓｑｕｉｏｘａｎｅ）のいずれか一方であることを特徴とする請求項１又は２に記載の半導体装置。
【請求項７】
金属層にスピン・オン誘電体を結合する半導体装置の製造方法であって、
前記金属層上に第１のライナー誘電体層を堆積し、
前記第１のライナー誘電体層上に転移層を形成し、
前記転移層上に第２のライナー誘電体層を堆積し、
前記スピン・オン誘電体を形成し、
前記第２のライナー誘電体層は前記金属層とは化学的に親和性が低く、前記第１のライナー誘電体層よりも前記スピン・オン誘電体と化学的に親和性が高いことを特徴とする半導体装置の製造方法。
【請求項８】
前記第１のライナー誘電体層及び前記第２のライナー誘電体層を、所定の比率で窒素ガス（N_2O）と混合される先駆ガスを用いてプラズマ化学気相反応（ＰＥＣＶＤ）又は化学気相反応（ＣＶＤ）により堆積することを特徴とする請求項７に記載の半導体装置の製造方法。
【請求項９】
前記第１のライナー誘電体層堆積工程における前記所定比率を前記第２のライナー誘電体層堆積工程で変化させて、これに伴い前記転移層を形成することを特徴とする請求項８に記載の半導体装置の製造方法。
【請求項１０】
前記第１のライナー誘電体層を形成する先駆ガスのN_2Oに対する前記比率は１：２０乃至１：３０で、前記第２のライナー誘電体層を形成する先駆ガスのN_2Oに対する前記比率は１：３乃至１：７であることを特徴とする請求項９に記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】

【発明の属する技術分野】
この発明は、半導体装置の製造に関し、特にライナー酸化物に対するメチルシルセスクイオキサン［ｍｅｔｈｙｌ　ｓｉｌｓｅｓｑｕｉｏｘａｎｅ　（ＭＳＱ）］の結合力を高める方法に関する。
【０００２】
【従来の技術】
半導体装置サイズがサブミクロンレベルになると、ミクロンレベルの装置サイズでは無視できうる電気的特性、例えば容量が顕著になる。例えば、サブー０．２０μｍプロセスでは誘電率（ｋ）の低い材料が改めて注目を集めている。
【０００３】
サブミクロンレベル半導体装置の製造においては、ゲート・ソース間容量とゲート・ドレイン間容量を小さくしてゲート容量レベルを維持することが目標となる。酸化物が薄くなるにつれて、ゲート容量は次のような関係を持って増加する。
【０００４】
【数１】

$$C_{ax} = \left(\varepsilon_0 \varepsilon_{sio_2} / t_{ox}\right) \cdot A$$

ここでAはゲート面積、ε_{sio_2}は誘電率（又はSiO_2の誘電率３．９）

そしてt_{ox}は酸化物の厚みである。

ゲート・ドレイン間容量はミラー効果によるスイッチング中に増加するものでトランジスタの性能上特に重要である。例えば、一連の論理回路では、前段の等価容量はゲート・ソース間容量に定数１を掛けてトランジスタゲインを加えたものになる。トランジスタゲインが１００であれば、入力容量はゲート・ドレイン間容量の１０１倍となる。従って、この容量が増加傾向になるパラメータを変更しない方が良い。低誘電率の誘電体材料を用いれば容量も減少する。集積回路設計ではｋの低い材料を用いて寄生容量を小さくすることが望ましい。
【０００５】
サブクオータ・ミクロンの小さい半導体装置用のｋの低い材料の条件により、例えば、メチルシルセスクイオキサン、ハイドロシルセスクイオキサン［ｈｙｄｒｏｇｅｎ　ｓｉｌｓｅｓｑｕｉｏｘａｎｅ　（ＨＳＱ）］等のスピン・オン誘電体が注目を集めている。ＭＳＱの誘電率は２．９程度である。ＭＳＱの実験的な化学式は$CH_3SiO_{1.5}$である。Ｏ－Ｓｉ－Ｏ基に有機物を加えることにより層の耐亀裂抵抗が増加する。この構造は低密度でありSiO_2に比べて誘電率が低い。
【０００６】
【発明が解決しようとする課題】
ｋの低い材料としてＭＳＱを用いるのは困難である。ＭＳＱとＰＥＣＶＤ（プラズマ化学気相反応法）による酸化物は表面のメチル基の存在により結合しずらい。この材料は最大約２５％メチル基を含んでおり、メチル基により層が疎水性になるので、$Si-CH_3$結合を壊してＳｉＯＨ結合を形成するのは困難である。
【０００７】
金属配線１１０を有する基板１００を示す図１において、ＭＳＱ１３０がライナー酸化物１２０より剥がれると装置性能に影響を及ぼす。
【０００８】
このｋの低い材料を用いて剥離しにくいようにＰＥＣＶＤ酸化物にＭＳＱを接着して装置歩留まりと装置性能を高かめることが要求される。
【０００９】
【課題を解決するための手段】
この発明には多くの応用例があり、その一つを示す。ＭＳＱをギャップを埋める誘電体と

して用いる場合、アルミニウム合金にメチルシルセスクイオキサンを完全に結合するのは困難である。結合力を高めるには、アルミニウムに対して高い結合力を示し、さらにＭＳＱに対しても高い結合力を示すライナー誘電体を用いることが有効である。しかし、ライナー誘電体とＭＳＱとの界面に変化が生じるとＭＳＱ層が剥がれる可能性がある。ライナー誘電体内でシリコン酸化物からメチルドープ酸化物へと転移が生じ、各膜がアルミニウム合金とＭＳＱに対し、それぞれ強い結合力を示す。

【００１０】

半導体基板上にライナー誘電体を堆積することにより誘電率の低いスピン・オン材料の結合力を高めることができる。一実施形態としては、半導体基板上の金属層上にスピン・オン誘電体を結合する方法である。第１の厚みのライナー誘電体を金属層上に体積する。このライナー誘電体は金属層と化学的に親和性がある。ライナー誘電体上に第２の厚みの転移層を形成する。転移層は金属層とは化学的にあまり親和性がないが、厚みが増すほどスピン・オン誘電体との化学的親和性が高まる。第３の厚みのライナー誘電体を転移層上に体積する。このライナー誘電体はスピン・オン誘電体と親和性がある。

【００１１】

他の実施形態としては、メチルシルセスクイオキサン化合物を結合する方法で半導体基板上のアルミニウム合金金属層上にライナー誘電体を形成するものである。ＣＶＤ環境に基板を晒し、前駆ガスとN_2Ｏガスの混合ガスをＣＶＤ環境に導入する。前駆ガスとN_2Ｏガスの比率は予め定めた比率である。混合ガスを反応させて所定厚みのライナー誘電体を堆積する。この実施形態のさらなる特徴としては、混合ガス反応中、第１の厚みでシリコン酸化物がアルミニウム合金金属層上に堆積されるように前駆ガスとN_2Ｏガスの比率を再調整することである。前駆ガスとN_2Ｏガスの比率を再調整することにより、メチルがドープされた第２の厚みの酸化物が第１厚みのシリコン酸化物上に堆積される。さらにこの実施例の特徴としては、前駆ガスとN_2Ｏガスの比率を再度調整することにより、ライナー誘電体内においてシリコン酸化物領域からメチル・ドープ酸化物領域への転移が生じることである。

【００１２】

【発明の実施の形態】

この発明は、ライナー酸化物とメチルシルセスクイオキサン（ＭＳＱ）スピン・オン材料との結合をより高めるものである。なお、以下に示す実施例ではＭＯＳ構造を用いているがこの発明はこれらには限定されない。

【００１３】

この発明の一実施形態では、半導体基板上のライナー酸化物の堆積後に転移層を形成する。この転移層がＭＳＱとライナー酸化物間のブリッジとなる。ライナー酸化物と接触する転移層の一側面側では転移層の物理的、化学的特性はライナー酸化物と近い。また、ＭＳＱと接触する転移層の一側面側では転移層の物理的、化学的特性はＭＳＱと近い。この転移層の物理的、化学的特性はＭＳＱと転移層の界面、さらにライナー酸化物と転移層の界面と適合するので、両界面間の特性の不適合により後工程で剥離の原因となる界面の変化が生じることがない。図２Ａ乃至図２Ｄはライナー酸化物へのＭＳＱの結合力を高める一連の工程を示す。

【００１４】

図２Ａにおいて、半導体基板２００は金属配線工程にあり、図示しないトランジスタ、抵抗等の基板下部素子が金属配線２１０により接続される。金属配線２１０は互いに少なくとも、工程上の各設計ルールに基づいた最小限の距離だけ離して形成される。金属配線間のスペース２３０には通常誘電体が埋め込まれる。装置サイズが小さくなるに従い容量を少なくし、ＭＳＱやＨＳＱ等のｋの低い誘電体を用いる必要がある。

【００１５】

この発明の一実施形態では、スピン・オン誘電体を適用する前に半導体基板をプラズマ化学気相反応（ＰＥＣＶＤ）室に入れる。転移ライナー酸化物にトリメチルシラン又はテトラメチルシランを先駆物として用いてメチル・ドープ酸化膜を形成しても良い。酸化物、

メチル・ドープ酸化物のいずれが基板上に形成されるかはトリメチルシランとN_2Oの比率による。N_2Oが多いとシリコン二酸化物層２２０ａがアルミニウム金属配線上に約２５０Åの厚みで堆積される。シリコン二酸化物はアルミニウム金属配線によく結合する。

【００１６】

この堆積工程の化学的特性により、シリコンと酸素の比率が変わり、例えば、この工程でシリコンの多い酸化物ＳｉＯが形成されうる。化学量論での変数を用いてSi_xO_yと表記する。

【００１７】

シリコン二酸化物堆積工程の後、N_2Oを徐々に少なくして、図２Ｂに示すようにライナー中に約２５０Åの厚みのメチルドープ酸化物２２０ｂを形成する。シリコン二酸化物層２２０ａとメチルドープ酸化物２２０ｂ間の転移は徐々に行われる。メチルドープ酸化物堆積後、反応室より基板を取り出す。

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【００１８】

なお、シリコン二酸化物層２２０ａとメチルドープ酸化物２２０ｂは異なる反応室で生成してもよい。酸化物２２０ａによる転移ライナー酸化物とメチルドープ酸化物２２０ｂの堆積後、スピン・オンＭＳＱ又はＨＳＱを用いてもよい。図２Ｃに示すように金属配線２１０間のスペース２３０にＭＳＱ層２４０を埋め込む。ＭＳＱ層２４０の上に、図２Ｄに示すようにキャップ酸化物層２５０を形成する。工程上の条件により、この装置をさらなる工程に移せるようにキャップ酸化物層２５０を平坦化する。他の金属層を用いる場合、前述の工程が繰り返されて金属配線間にｋの低い誘電体が埋め込まれる。

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【００１９】

この発明の工程では、ＰＥＣＶＤ室はＡｐｐｌｉｅｄ　Ｍａｔｅｒｉａｌｓ又はＮｏｖｅｌｌｕｓ等のメーカのものでよい。温度約１５０℃乃至約４００℃で約２乃至１０Ｔｏｒｒの圧力下で約５０至約２５０ＷａｔｔのＲＦ電力を印加すると金属上にSiO_2が堆積される。比率約１：２０乃至１：３０でN_2Oと混合されるトリメチルチラン、$SiH(CH_3)_3$又はテロラメチルチラン、$SiH(CH_3)_4$等の先駆ガスよりSiO_2が形成される。ガス流入量は先駆ガスでは約１０乃至６０ｃｃｍでN_2Oでは約２００乃至１８００ｃｃｍである。約１００乃至１０００Åの厚みのライナー酸化物を堆積後、約３乃至２５秒で混合ガスが変化する。

【００２０】

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混合ガス変化後、メチルドープ酸化物を堆積する。先駆ガスであるトリメチルチラン、$SiH(CH_3)_3$又はテロラメチルチラン、$SiH(CH_3)_4$は比率約１：３乃至１：７でN_2Oと混合される。ガス流入量は先駆ガスでは約１０乃至６０ｃｃｍでN_2Oでは約３０乃至３６０ｃｃｍである。

【００２１】

以上、図面を参照してこの発明の好ましい実施形態を詳細に説明したが、この発明はそれら実施形態に限定されるものではなくこの発明の原理に基づき多くの実施形態や変形が可能であることは明らかである。

【図面の簡単な説明】

【図１】半導体装置においてライナー酸化物よりＭＳＱが剥離される様子を示す断面図である。

40

【図２Ａ】半導体装置においてライナー酸化物が堆積される様子を示す断面図である。

【図２Ｂ】図２Ａにおいてライナー酸化物上にメチルドープ酸化物の転移層が形成された後のこの発明の実施の形態による半導体装置の断面図である。

【図２Ｃ】図２ＢにおいてＭＳＱが堆積された後の半導体装置の断面図である。

【図２Ｄ】図２Ｃにおいてキャップ酸化物が形成された後の半導体装置の断面図である。

【国際公開パンフレット】

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 February 2002 (28.02.2002)

PCT

(10) International Publication Number
WO 02/17356 A2

(51) International Patent Classification[7]: H01L 21/00

(21) International Application Number: PCT/EP01/09280

(22) International Filing Date: 9 August 2001 (09.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/642,074 18 August 2000 (18.08.2000) US

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(81) Designated States *(national)*: CN, JP.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *without international search report and to be republished upon receipt of that report*

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WO 02/17356 A2

(54) Title: METHOD AND STRUCTURE FOR ADHERING MSQ MATERIAL TO LINER OXIDE

(57) Abstract: A method for depositing a liner dielectric on a semiconductor substrate provides for sufficient adhesion of low dielectric constant spin-on materials among metal layers in sub-micron processes. In an example embodiment, a method for adhering MSQ provides for a liner oxide on an aluminum alloy layer on a semiconductor substrate. First, the substrate is placed into a PECVD environment. A gas mixture of trimethylsilane and N_2O is introduced into the PECVD environment at a trimethylsilane-to-N_2O ratio of about 1:20 to 1:30. The gas mixture is reacted to deposit an oxide liner of a predetermined thickness. Adjusting the gas mixture trimethylsilane-to-N_2O ratio to about 1:3 to 1:7 over the course of about 5 to 20 seconds, and sustaining the reaction thereof, deposits a methyl doped oxide.

WO 02/17356 PCT/EP01/09280

Method and structure for adhering MSQ Material to Liner oxide

FIELD OF INVENTION

The present invention is generally directed to the manufacture of a semiconductor device. In particular, the present invention relates to a process that provides for improving the adhesion of methyl silsesquioxane (MSQ) film to a liner oxide.

5

BACKGROUND OF INVENTION

As devices scale down to the sub-micron level, electrical characteristics such as capacitance that were negligible in devices having dimensions in multiples of microns, have become significant. For example, in a sub-0.20 μm process there has been a renewed

10 interest in materials with a low dielectric constant (i.e., "low k").

A goal in processing sub-micron devices is to maintain a level of gate capacitance while minimizing the gate-to-source and gate-to-drain capacitance. As the oxide is made thinner the capacitance increases as shown in the relationship:

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{SiO_2}}{t_{ox}} \bullet A,$$

where

15 A = *area of gate*

ε_{SiO_2} = *dielectric constant (or relative permittivity of* SiO_2 *taken as* 3.9)

t_{ox} = *oxide thickness*

The gate-to-drain capacitance is especially critical for transistor performance as it is amplified during switching due to the Miller effect. For example, in a series of logic stages, the equivalent capacitive loading to the previous logic stage is the gate-to-source

20 capacitance multiplied by a factor of 1 plus the gain of the transistor. If the transistor has a gain of 100, the observed input capacitance would be 101 times the gate-to-drain capacitance. Consequently, it is desirable to not alter the parameters that tend to increase that capacitance. Therefore, using a dielectric material having a lower dielectric constant lowers the

capacitance. It is advantageous to use lower k materials throughout the integrated circuit design where possible to minimize the parasitic capacitance.

The requirement for low k materials for sub-quarter micron and smaller devices has renewed the interest in spin-on dielectrics such as methyl silsesquioxane (MSQ) and hydrogen silsesquioxane (HSQ). MSQ has a dielectric constant of ~2.9. The empirical formula of MSQ is $CH_3SiO_{1.5}$. The addition of organic side groups to the basic O-Si-O backbone results in improved crack resistance of the films. The structure has a lower density and hence a lower dielectric constant than that of SiO_2.

In an example process, it is a challenge to integrate MSQ as a low k dielectric. MSQ and PECVD (plasma enhanced chemical vapor deposition) oxide do not adhere well to one another owing to the presence of methyl groups on the surface. The material has significant methyl content up to about 25%. The presence of methyl groups makes the film hydrophobic, as it is difficult to form SiOH bonds by breaking the Si-CH_3 bonds.

FIG. 1 depicts a substrate 100 having metal lines 110. The de-lamination of MSQ 130 from the liner oxide 120 may degrade performance of the device

There exists a need to provide for the adhesion of MSQ to the PECVD oxide that resists de-lamination enabling the use of this low k dielectric to improve device yield and product performance.

SUMMARY OF INVENTION

The present invention is exemplified in a number of implementations, one of which is summarized below. It is a challenge to obtain sufficient adhesion of methyl silsesquioxane (MSQ) to aluminum alloys when MSQ is used as a gap-filling dielectric. Adhesion may be improved by using a liner dielectric that exhibits good adhesion to the aluminum on one hand, yet good adhesion to MSQ on the other. However, the MSQ layer may de-laminate if there is an abrupt interface between liner dielectric and the MSQ. A transition is made in the liner dielectric between silicon dioxide to a methyl-doped oxide, each film providing sufficient adhesion to aluminum alloy and MSQ, respectively.

A method for depositing a liner dielectric on a semiconductor substrate provides for sufficient adhesion of low dielectric constant spin-on materials. In an example

embodiment, on a semiconductor substrate, there is a method of adhering a spin-on dielectric on a metal layer. A first-predetermined thickness of a liner dielectric is deposited on the metal layer. The liner dielectric has a chemical affinity to the metal layer. A transition layer of a second predetermined thickness is formed on the liner dielectric; the transition layer has less chemical affinity to the metal layer and increasing chemical affinity to the spin-on dielectric as the thickness of the transition layer increases. A third predetermined thickness of liner dielectric is deposited on the transition layer; the liner dielectric has a chemical affinity to the spin-on dielectric.

In another example embodiment, a method for adhering silsesquioxane compounds, provides a liner dielectric on an aluminum alloy metal layer on a semiconductor substrate, the method comprises placing the substrate in a CVD environment. A gas mixture comprising a precursor gas and N_2O is introduced into the CVD environment. The ratio of precursor gas-to-N_2O is predetermined. The gas mixture is reacted to deposit the liner dielectric of a predetermined thickness. An additional feature of this embodiment, is the during the reacting of the gas mixture, the precursor-to-N_2O ratio may be adjusted so that silicon dioxide is deposited on the aluminum alloy metal layer a first predetermined thickness. By re-adjusting the precursor gas-to-N_2O ratio, methyl doped oxide of a second predetermined thickness is deposited on the first predetermined thickness of the silicon dioxide. A further feature of this embodiment is wherein the re-adjusting of the precursor gas-to-N_2O ratio produces a transition in the liner dielectric from a region of silicon dioxide to a region of methyl doped oxide.

The above summary of the present invention is not intended to represent each disclosed embodiment, or every aspect, of the present invention. Other aspects and example embodiments are provided in the figures and the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 is a cross-section of a device structure depicting MSQ delaminating from the liner oxide;

FIG. 2A is a cross-section of a device structure at deposition of liner oxide;

FIG. 2B is FIG. 2A after a transitional layer of methyl doped oxide is formed on the liner oxide in an embodiment according to the present invention;

FIG. 2C depicts FIG. 2B after deposition of MSQ; and

5 FIG. 2D depicts FIG. 2C after cap oxide.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and will herein be described in detail.

10

DETAILED DESCRIPTION

The present invention has been found to be useful and advantageous in connection with providing more reliable adhesion between the liner oxide and methyl silsesquioxane (MSQ) spin-on material. In the discussion that follows, a MOS structure is 15 used to describe an example implementation of the invention. However, the invention is not so limited.

In an example process according to the present invention, after deposition of the liner oxide on a semiconductor substrate, a transition layer is formed thereon. The 20 transition layer provides a bridge between the MSQ and liner oxide. On one side of the transition layer in contact with the liner oxide, its physical and chemical properties are similar to that of the liner oxide. On the other side of the transition layer in contact with MSQ, the transition layer chemical and physical properties are similar to that of MSQ. In that the properties in the transition layer are matched at the MSQ/transition layer interface and the 25 liner oxide/transition layer interface, there is no abrupt interface that may de-laminate during subsequent processing to a mismatch of properties between the interfaces. FIGS. 2A – 2D depict a series of steps involved in improving the adhesion of MSQ to a liner oxide.

Refer to FIG. 2A, a semiconductor substrate 200 is at the metallization stages 30 of fabrication, underlying components such as transistors, resistors (not illustrated) are connected to one another through with metal lines 210. Per design rule requirements of a given process, metal lines 210 are spaced apart at least a minimum distance from each other. The spaces 230 between the metal lines are typically filled with a dielectric. As the device

dimensions decrease there is a need to minimize the capacitance and use a low k dielectric such as MSQ or HSQ.

In an example embodiment according to the present invention, prior to applying the spin-on dielectric, the semiconductor substrate is placed into a plasma-enhanced chemical vapor deposition chamber (PECVD) chamber. The transitional liner oxide may be made using trimethylsilane or tetramethylsilane as precursors for forming the methyl doped oxide film. Whether oxide or a methyl-doped oxide is deposited on the substrate is determined by the trimethylsilane to N_2O ratio. At a high N_2O flow, a silicon dioxide layer 220a forms and deposited onto the aluminum metal at a thickness of about 250Å. Silicon dioxide adheres well to the aluminum metal lines.

Depending upon the chemistry of the deposition process, the ratio of silicon-to-oxygen may vary. For example, the process may form "silicon-rich" oxide, SiO. To include the variations in stoichiometry, t is appropriate to depict the formula as Si_xO_y.

Refer to FIG. 2B. Later in the deposition, the N_2O is gradually decreased to form about 250Å of methyl doped oxide 220b in the liner. The transition between silicon dioxide 220a and the methyl-doped oxide 220b is gradual. After the deposition the substrate is removed from the chamber.

In another example process, the silicon dioxide layer 220a may be formed in a separate chamber and the methyl-doped oxide 220b may be formed in another.

Having deposited a transitional liner oxide of oxide 220a and methyl doped oxide 220b, the spin-on MSQ or HSQ may be applied. Refer to FIG. 2C. The MSQ layer 240 fills in the spaces 230 between metal lines 210. Refer to FIG. 2D. Upon the MSQ layer 240 a cap oxide layer 250 is applied. Depending upon specific process requirements, the cap oxide layer 240 is planarized so that the device may be further processed. If another metal layer is used in the device design, the aforementioned process may be repeated so that low k dielectric may be applied between the metal lines.

In an example process according to the present invention, the PECVD chamber may be of a number of manufacturers such as Applied Materials or Novellus. At a

temperature of about 150°C to about 400°C, at a pressure of about 2 to 10 Torr, with RF power in the range of about 50 Watts to 250 Watts, the SiO_2 is deposited on the metal. The SiO_2 is made from one of the precursor gases, trimethylsilane, $SiH(CH_3)_3$ or tetramethylsilane, $Si(CH_3)_4$ combined with N_2O at a ratio of about 1:20 to about 1:30. The
5 flow rates are about 10 sccm to 60 sccm for precursor gas and about 200 sccm to about 1800 sccm. After about 100Å to about 1000Å of liner oxide is deposited the gas mixtures are transitioned over the course of about 3 to 25 seconds.

After the transition, methyl doped oxide is deposited. The precursor gas,
10 trimethylsilane, $SiH(CH_3)_3$ or tetramethylsilane, $Si(CH_3)_4$ and N_2O are at a ratio of about 1:3 to about 1:7. Flow rates for the precursor gas and N_2O range from about 10 sccm to about 60 sccm and 30 sccm to about 360 sccm, respectively.

While the present invention has been described with reference to several
15 particular example embodiments, those skilled in the art will recognize that many changes may be made thereto without departing from the spirit and scope of the present invention, which is set forth in the following claims.

CLAIMS:

1. A semiconductor device comprises a stack of a patterned metal layer, a layer of a first liner dielectric, a layer of a second liner dielectric and a layer of a spin-on dielectric, which second liner dielectric has less chemical affinity to the metal and more chemical affinity to the spin-on dielectric than the first liner dielectric.

5

2. A semiconductor device according to Claim 1, characterized in that:
the first liner dielectric is chosen from the group of silicon dioxide, silicon-rich oxide and Si_xO_y, in which x=1 and $0.48 \leq y \leq 2$, and
the second liner dielectric is a methyl doped oxide.

10

3. A semiconductor device according to Claim 1 or 2, characterized in that between the layers of the first and the second liner dielectric a transition layer is present with a composition that varies from the first liner dielectric to the second liner dielectric in a direction from the metal layer to the layer of the spin-on dielectric.

15

4. A semiconductor device according to any of the Claims 1 to 3, wherein the layers of the first and the second liner dielectric have each a thickness in the range of 5 to 100 nm.

20 5. A semiconductor device according to Claim 3 or 4, wherein the transition layer has a thickness in the range of 10 to 200 nm.

6. A semiconductor device according to Claim 1 or 2, characterized in that the spin-on dielectric includes at least one of the folowing: methylsilsesquioxane, hydrogen
25 silsesquioxane.

7. A method of manufacturing a semiconductor device, in which method a spin-on dielectric is adhered to a metal layer, characterized in that the method comprises the steps of:

depositing a layer of a first liner dielectric on the metal layer;
forming a transition layer on the first liner dielectric;
depositing a layer of a second liner dielectric on the transition layer,
providing the spin-on dielectric,
5 which second liner dielectric has less chemical affinity to the metal and more chemical affinity to the spin-on dielectric than the first liner dielectric.

8. A method as claimed in Claim 7, characterized in that the layers of the first and the second liner dielectric are deposited by plasma-enhanced chemical vapour deposition
10 (PECVD) or chemical vapour deposition (CVD) using a precursor gas, that is blended with nitrogen oxide (N_2O) in predetermined ratios.

9. A method as claimed in Claim 8, characterized in that the predetermined ratio to yield the first liner dielectric is transitioned to yield the second liner dielectric, therewith
15 forming the transition layer.

10. A method according to Claim 9, wherein the predetermined ratio of precursor gas to N_2O to form the first liner dielectric is in the range of 1:20 to 1:30 and the predetermined ratio to form the second liner dielectric is in the range of 1:3 to 1:7.

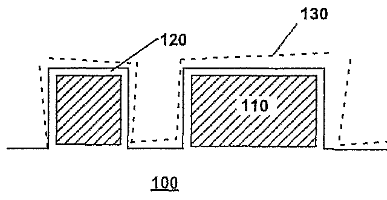

FIG. 1

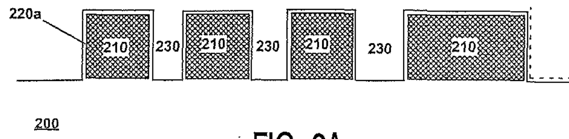

FIG. 2A

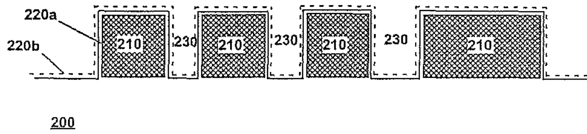

FIG. 2B

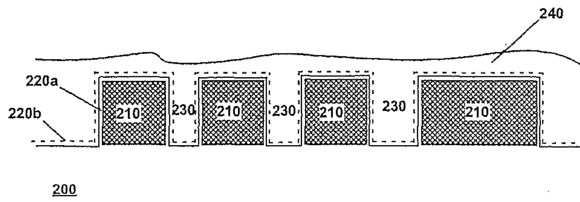

FIG. 2C

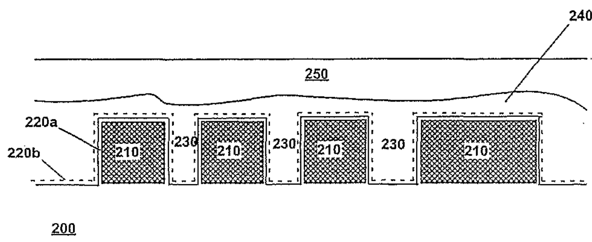

FIG. 2D

【国際公開パンフレット（コレクトバージョン）】

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 February 2002 (28.02.2002)

PCT

(10) International Publication Number
WO 02/017356 A3

(51) International Patent Classification[7]: H01L 21/768, 23/532

(21) International Application Number: PCT/EP01/09280

(22) International Filing Date: 9 August 2001 (09.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/642,074 18 August 2000 (18.08.2000) US

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(81) Designated States *(national)*: CN, JP.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report: 18 July 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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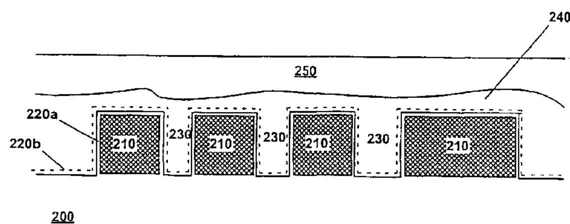

(57) Abstract: A method for depositing a liner dielectric on a semiconductor substrate provides for sufficient adhesion of low dielectric constant spin-on materials among metal layers in sub-micron processes. In an example embodiment, a method for adhering MSQ provides for a liner oxide on an aluminum alloy layer on a semiconductor substrate. First the substrate is placed into a PECVD environment. A gas mixture of trimethylsilane and N_2O is introduced into the PECVD environment at a trimethylsilane-to-N_2O ratio of about 1:20 to 1:30. The gas mixture is reacted to deposit an oxide liner (220a) of a predetermined thickness. Adjusting the gas mixture trimethylsilane-to-N_2O ratio to about 1:3 to 1:7 over the course of about 5 to 20 seconds, and sustaining the reaction thereof, deposits a methyl doped oxide (220b).

WO 02/017356 A3

【国際公開パンフレット（コレクトバージョン）】

(L)60202242576

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 February 2002 (28.02.2002)

PCT

(10) International Publication Number
WO 02/017356 A3

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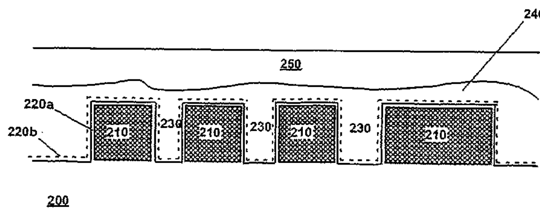

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WO 02/017356 A3

【国際調査報告】

IN RNATIONAL SEARCH REPORT

Inte nal Application No
PCT/EP 01/09280

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 072 227 A (JENG SHIN-PUU ET AL) 6 June 2000 (2000-06-06) column 4, line 63 -column 5, line 44 column 11, line 9 -column 12, line 40 column 13, line 53 -column 14, line 59; figures 6,9,10 ---	1,2,7,8, 10
A	US 6 100 179 A (TRAN KHANH) 8 August 2000 (2000-08-08) the whole document -----	1,4,6,7

☐ Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
10 May 2002	24/05/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Micke, K

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Information on patent family members

Inte nal Application No
PCT/EP 01/09280

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			JP	2002503879	T	05-02-2002
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			US	2001004479	A1	21-06-2001
			US	2001005546	A1	28-06-2001
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			US	2002000670	A1	03-01-2002
US 6100179	A	08-08-2000	US	6034420	A	07-03-2000

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 01/09280

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

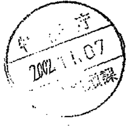
Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 072 227 A (JENG SHIN-PUU ET AL) 6 June 2000 (2000-06-06) column 4, line 63 -column 5, line 44 column 11, line 9 -column 12, line 40 column 13, line 53 -column 14, line 59; figures 6,9,10	1,2,7,8, 10
A	US 6 100 179 A (TRAN KHANH) 8 August 2000 (2000-08-08) the whole document	1,4,6,7



☐ Further documents are listed in the continuation of box C.
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Date of the actual completion of the international search	Date of mailing of the international search report
10 May 2002	24/05/2002

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International Application No
PCT/EP 01/09280

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 6072227	A	06-06-2000	US	6054379	A	25-04-2000
			EP	1055012	A2	29-11-2000
			JP	2002503879	T	05-02-2002
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Ｆターム(参考) 5F033 HH08 RR20 SS03 SS15 SS21 TT01 WW02 WW10 XX14 XX24
5F045 AA08 AB31 AB32 AB39 AC08 AF01 AF08 AF10 BB17
5F058 AC10 AD02 AE01 AF01 AG10